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Title:	A novel high dynamic six phase 120 kW Power Hardware in the Loop Emulation Test Bench for emulating AC/DC Grids and Electrical Machines
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A novel high dynamic six phase 120 kW Power Hardware in the Loop Emulation Test Bench for emulating AC/DC Grids and Electrical Machines

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Keywords

≪Power Hardware-in-the-Loop≫, ≪Cascaded H-Bridge≫,≪Grid emulation≫, ≪Machine emulation≫, ≪Test bench≫, ≪Parallel Hybrid Converter≫

Abstract

This paper presents a highly customizable 120 kVA Power-Hardware-in-the-Loop test bench. The output stage consist of two identical Parallel Hybrid Converters each with a 17-level output voltage and an effective switching frequency of 1 MHz. The Parallel Hybrid Converters can provide 3-phase AC or bipolar DC as output voltage. Thus, one 6-AC, 3-AC or DC system or two systems with 2x3-AC, 1x3-AC and 1xDC or 2xDC can be emulated.

1 Introduction

Modern power electronic systems for grid and drive applications are continuously increasing in complexity, while their development time and costs have to be reduced as well [1]. Therefore, the power electronic hardware, the control unit and the closed loop control of inverters must be tested rapidly, efficiently and most of all reproducible under realistic test conditions early in the development phase. Power-Hardware-in-the-Loop (PHIL) test benches achieve this objective since they can emulate the terminal behavior of an electrical machine, a battery or an electrical grid based on parameterized models, reproducible and rapidly reconfigurable at full power throughput.
Thus, a drive inverter, its controller and especially their behavior in case of failure can be evaluated before the real motor exists and without the need for a rotating test bench. Hereto the drive inverter to be

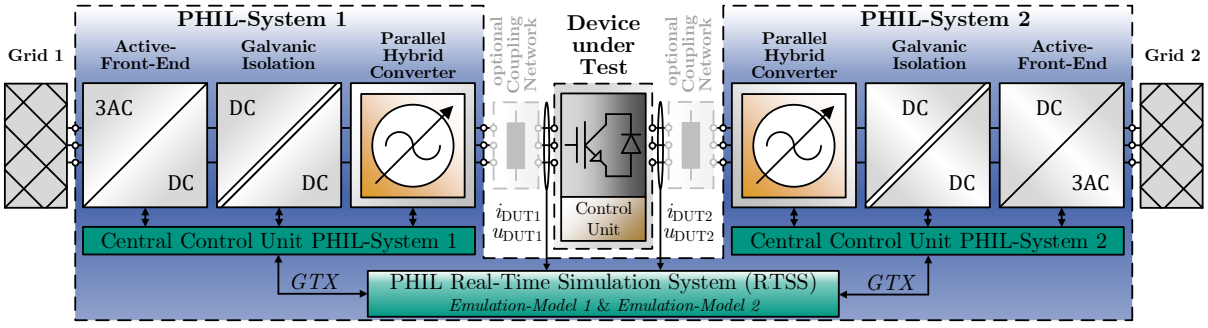

Fig. 1: PHIL emulation test bench for simultaneous emulation of two systems connected to one DUT in the center

tested or Device under Test (DUT) is connected to the PHIL converter via an inductive coupling network. The Real-Time Simulation System (RTSS) of the PHIL test bench measures the output voltages of the DUT, computes the reaction of the emulated machine based on a model and the reference voltage for the PHIL converter to emulate the correct response at its terminals. State-of-the-art PHIL systems are even capable of correctly emulating the current ripple of a machine [2–4]. To further improve the comparability to actual applications later on, in some cases the DC or AC source supplying the DUT (e.g. a battery or a 6-pulse rectifier) is also emulated model-based [5]. Fig. 1 depicts such a PHIL emulation test bench with one DUT between two PHIL converters which are controlled by one RTSS. The optional coupling network between the DUT and the PHIL systems is not needed if the terminals of the DUT have an inductive behavior. Therefore, grid inverters are connected directly to the PHIL converter via their output filter, since the filter is part of the DUT. With a PHIL test bench, the behavior of a grid inverter can be analyzed for various grid impedances, but also for different grid faults in a reproducible and safe manner [6].

In order to achieve a high level of emulation quality, PHIL converters must be able to control their output voltage highly dynamic but also highly precise to realize the voltage-time area required by the model [7]. Therefore, state-of-the-art PHIL Emulation test benches utilize conventional full-power multilevel converters or less efficient high power linear amplifiers as output stage for machine [2–5, 8, 9] or grid [6, 10, 11] emulation. Even though these multilevel converters have a higher efficiency than linear amplifiers, they still have a large footprint and high costs.

To overcome these disadvantages, the concept of a Cascaded H-Bridge based Parallel Hybid Converter (PHC) is introduced in [12]. And in [13], it is shown that this new converter topology inherently has a higher power density and lower costs compared to full-power multilevel converters with the same output voltage characteristics.

2 The Parallel Hybrid Converter

Fig. 2 depicts the equivalent circuit diagram of the Cascaded H-Bridge based Parallel Hybrid Converter topology. It combines the high output voltage quality and dynamics of a low power Cascaded H-Bridge (CHB) converter in star configuration with the high efficiency and high power density of a 2-level voltage source converter as Main Power Source (MPS). The MPS is connected in parallel to the CHB via an inductive coupling network with the line resistance R_m and the coupling inductance L_m. In the following, the operating principle of the PHC is illustrated with the assistance of the simulation results depicted in Fig. 3. Therefor, the MPS, CHB and PHC output voltages ($u_{\mathrm{m},1}$, $u_{\mathrm{c},1}$, $u_{\mathrm{o},1}$) and currents ($i_{\mathrm{m},1}$, $i_{\mathrm{c},1}$, $i_{\mathrm{o},1}$) at a passive RL load at a PHC output voltage frequency of $f_\mathrm{o}^* = 1000\,\mathrm{Hz}$ are shown in Fig. 3.

The high dynamic low-power 17-level CHB converter with a high effective switching frequency $f_{\mathrm{c,SW}} = 1\,\mathrm{MHz}$ acts as a quasi-ideal voltage source on the output terminals of the PHC. Thus it defines the output voltage $u_{\mathrm{o},x}$ and controls the output current $i_{\mathrm{o},x}$ ($x \in \{1,2,3\}$). The MPS and the inductive coupling

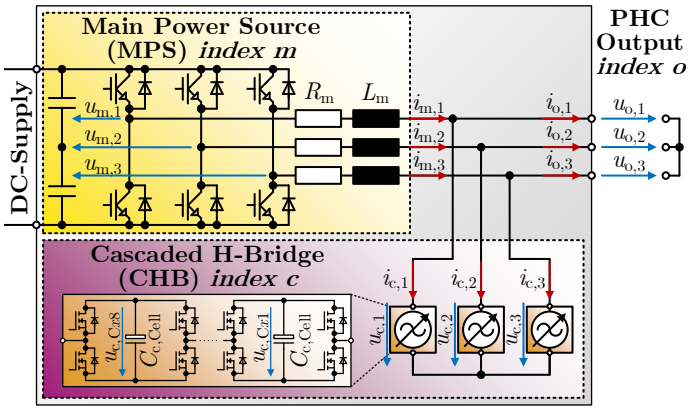

Fig. 2: Equivalent circuit of the novel Cascaded H-Bridge based Parallel Hybrid Converter (PHC)

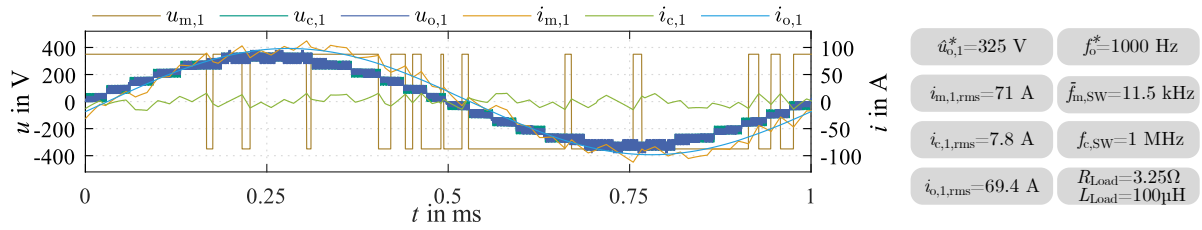

Fig. 3: Left: Simulation results of the PHCs first phase with a passive RL-load; Right: RMS values of the MPS, CHB and PHC currents as well as the switching frequencies of the MPS and the CHB

network thereby act as a current source, which delivers the bulk of the output current (1a).

$$i_{m,x} \approx i_{o,x} \tag{1a}$$

The MPS is implemented as a high-power 2-level converter with a low, operating point dependent average switching frequency $\bar{f}_{m,SW} \approx 5.4\,\text{kHz} - 14.5\,\text{kHz} \ll f_{c,SW}$ [13]. As a result due to Kirchhoff's current law, the CHB only has to compensate for the differences (2a) between the output currents $i_{o,x}$ and the MPS currents $i_{m,x}$. With a proper control of the MPS limiting the CHB currents $i_{c,x}$, these differences are reduced load independent to the current ripple of the 2-level MPS. Thus, the CHB only has to supply distortion reactive power, neglecting losses within the CHB.

$$i_{c,x} = i_{m,x} - i_{o,x} \tag{2a}$$

This reactive power is significantly lower than the output power of the PHC, which is supplied entirely by the MPS connected to a DC-supply. Thus, the eight H-bridge cells depicted in the orange box in Fig. 2 of each CHB phase do not require an additional power supply and have a significant lower rated current compared to the MPS ($\frac{i_{c,1,rms}}{i_{m,1,rms}} \approx 11\%$). However, a decoupled control concept is needed for an energy controller to pre-charge the cells and balance the total stored energy (3a) in each phase of the CHB during operation.

$$w_{c,x} = \frac{1}{2} C_{c,x} \cdot u^2_{c,Cx} = \frac{1}{2} \frac{C_{c,Cell}}{8} \cdot \left(\sum_{y=1}^{8} u_{c,Cxy} \right)^2 \tag{3a}$$

Control Scheme

In [12], a power analysis of the PHC is performed and a decoupled control scheme for the energy controller is derived to balance the voltages $u_{c,Cx1-8}$ of the CHB cell capacitors. Also a modified Predictive Current Controller (PCC) based on [14] is presented and used as limit controller (also known as bang bang controller) to keep the CHB current within a specified boundary circle in the αβ-plane ($|\underline{i}_{c,\alpha\beta}| < i_{c,max}$). Fig. 4 depicts a schematic illustration of the implemented energy controller, the PCC as well as the CHB cell modulation. The energy controller has the following input signals:

- The set-point values of the CHB cell capacitor voltage $u^*_{c,C123}$ for each phase, set by the user with the human machine interface (HMI) via the ARM-Core 1 of the PHIL Central Control Unit (CCU) (Fig. 6 a))
- The cell capacitor voltages $u_{c,Cxy}$ of all $3 \cdot 8 = 24$ CHB cells, measured each with ΣΔ-analog digital converters (ADC) on each CHB cell
- The reference values of the PHC output voltages $u^*_{o,123}$ and their fundamental frequency f^*_o sent from the RTSS via GTX to the CCUs of the PHIL systems

For the energy balancing the reference values $w^*_{c,123}$ and measured values $w_{c,123}$ of the CHB phase energies are calculated and transformed into the αβ0-system, whereas the α- and β-component represent the energy imbalance between the three phases and the 0-component represents the total energy stored in the CHB [15]. Three PI-controllers than determine the power reference values $p^*_{\alpha\beta0}$ to balance the energy

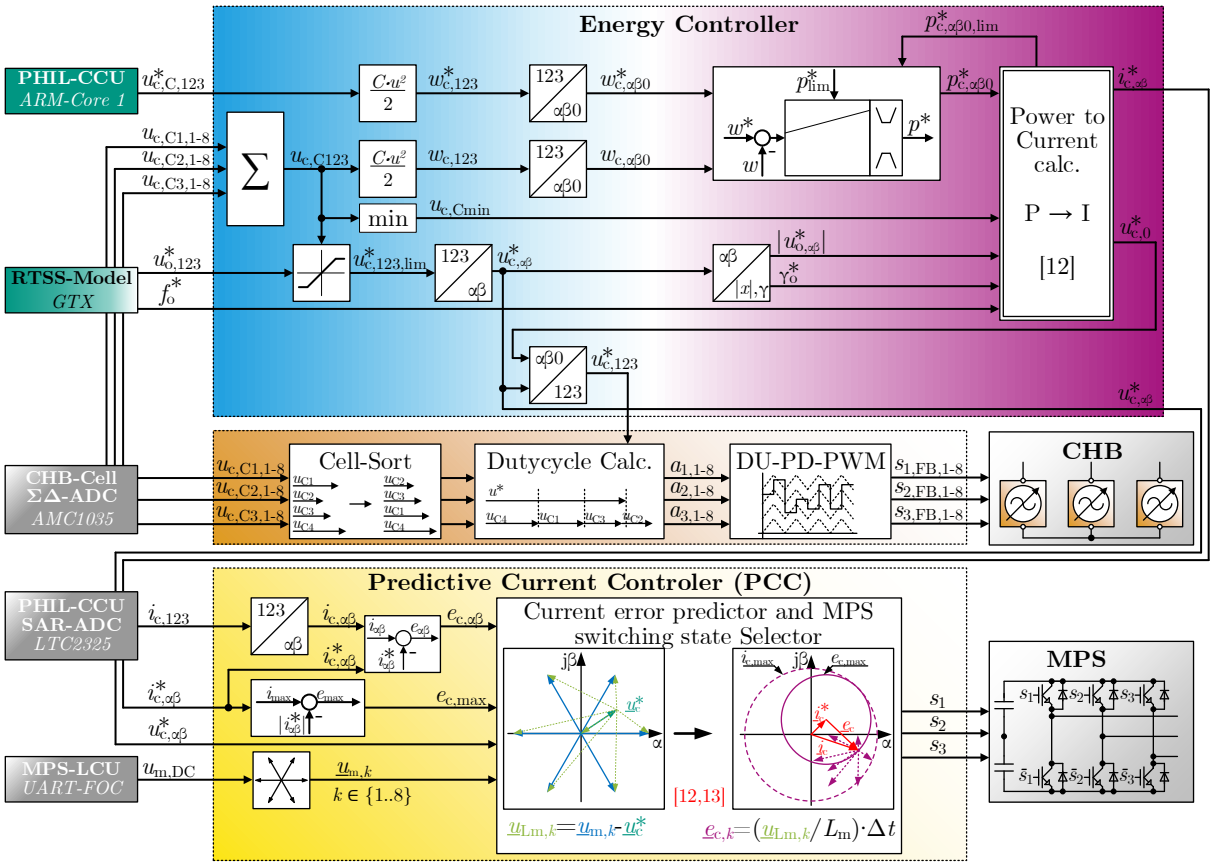

Fig. 4: Control scheme of the energy controller, the CHB cell modulation and the current limiting predictive current controller

differences between the CHB phases and to adjust the total energy within the CHB. On the basis of the power analysis carried out in detail in [12], the power reference values are calculated in the 'P → I' block into CHB reference currents $i^*_{c,\alpha\beta}$ (4b). The reference current values are composed of a positive current sequence $i^*_{c,P,\alpha\beta}$ for the total energy and a negative current sequence $i^*_{c,N,\alpha\beta}$ for the energy difference. For operating points with $|f^*_o| \leq 20\,\text{Hz}$, a high-frequency ($f^*_{c,0} = 500\,\text{Hz}$) common mode voltage component (4a) is added to the CHB reference voltage and a corresponding positive current sequence $i^*_{c,P0,\alpha\beta}$ is also added to the CHB reference current instead of the negative current sequence component $i^*_{c,N,\alpha\beta}$.

$$u^*_{c,0} = \begin{cases} 0 & \text{if } |f^*_o| > 20\,\text{Hz} \\ (u^*_{c,\text{Cmin}} - |u^*_{o,\alpha\beta}|)\sin(\gamma^*_{c,0}) \quad \text{with } \gamma^*_{c,0} = 2\pi f^*_{c,0} t & \text{if } |f^*_o| \leq 20\,\text{Hz} \end{cases} \tag{4a}$$

$$i^*_{c,\alpha\beta} = \underbrace{i^*_{c,P,\alpha\beta}}_{f(p^*_0,|u^*_{o,\alpha\beta}|,\gamma^*_o)} + \underbrace{i^*_{c,N,\alpha\beta}}_{f(f^*_o,p^*_{\alpha\beta},|u^*_{o,\alpha\beta}|,\gamma^*_o)} + \underbrace{i^*_{c,P0,\alpha\beta}}_{f(f^*_o,p^*_{\alpha\beta},u^*_{c,0},\gamma^*_{c,0})} \tag{4b}$$

The CHB reference current $i^*_{c,\alpha\beta}$ and reference voltage $u^*_{c,\alpha\beta}$ are fed in αβ-representation to the PCC, which is depicted in the yellow box in Fig. 4. The PCC has the tasks to limit the CHB current $\underline{i}_c$ to a given maximum $i_{c,\text{max}}$, to ensure, that $\underline{i}_c$ corresponds to $\underline{i}^*_c$ on average, and to achieve this with a minimum number of switching operations, to keep the average switching frequency $\bar{f}_{m,SW}$ of the MPS low. The error predictor calculates whether the CHB current space vector $\underline{i}_c$, whose trajectory is predicted ahead by the system dead time (measurement, controller and execution dead time), would violate the error current boundary circle around $\underline{i}^*_c$ with the radius $e_{c,\text{max}}$. If so, the predictor selects the MPS switching state k which leads $\underline{i}_c$ back into the error boundary circle and keeps it there the longest, with respect to the number of commutations required for this new switching state.

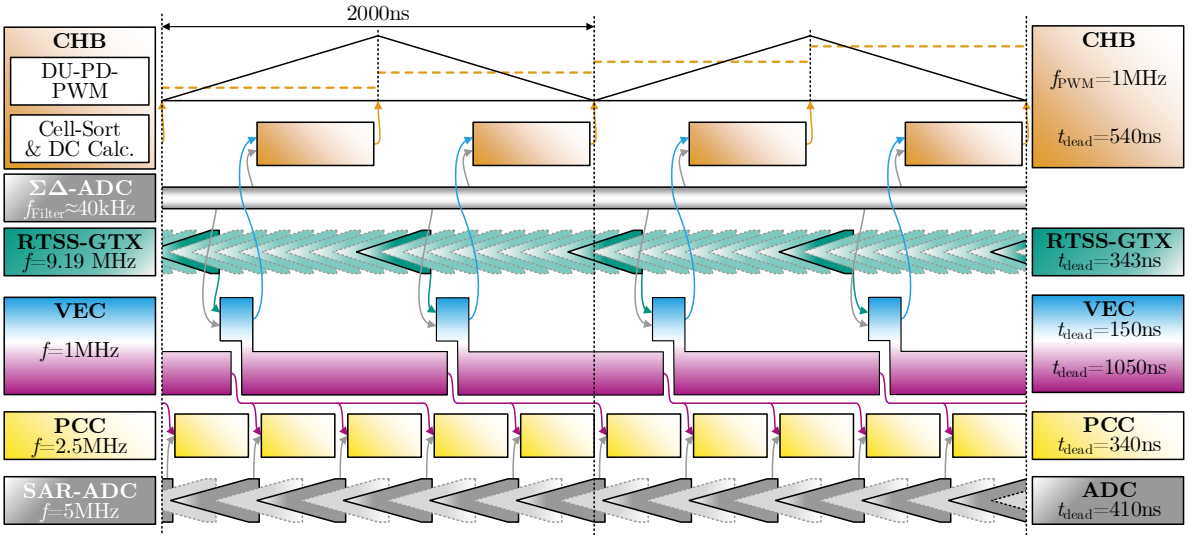

Fig. 5: Timing diagram of the PHC control scheme

As depicted in Fig. 5 the sampling frequency of the ADC is 5 MHz and the calculation dead time of the PCC is 340 ns allowing for an execution frequency of the PCC of 2.5 MHz using every second ADC value. Also as depicted in Fig. 5 the reference input values of the PCC are updated only every second or third PCC cycle since the energy controller has an execution frequency of 1 MHz and is synchronized with the CHB modulation, whereas the PCC is synchronized with the ADC, which measures the CHB currents.

The energy controller limits the PHC output voltages reference values $u^*_{o,123}$ to the available cell capacitor voltage sum $u_{c,C123}$ of each CHB phase, adds operating point dependent ($|f^*_o| \leq 20\,\text{Hz}$) an common mode voltage component $u^*_{c,0}$ to it for the energy balancing between the CHB phases [12] and hands the now limited reference voltage $u^*_{c,123}$ over to the CHB modulation (orange box in Fig. 4). As depicted in Fig. 5 the CHB cells are modulated using the Phase Disposition Pulse Width Modulation [16] with double update (DU-PD-PWM) with a up-down-counter frequency of 500 kHz leading to PWM and a reference value update frequency of 1 MHz. The theoretical effective switching frequency of each CHB MOSFET is than $\frac{f_{c,SW}}{2 \cdot n_{Cells}} = \frac{1\,\text{MHz}}{2 \cdot 8} = 62.5\,\text{kHz}$, with the real effective switching frequency being operating point dependent between this value and $\approx 67.5\,\text{kHz}$ due to additional switching events caused by the cell sorting algorithm.

Implementation

In [12], the performance of the controllers, which uses floating point representation and operations, is shown by simulation in *Matlab/Simulink*.

However for use of the PHC as output stage of a PHIL, a very low system dead time ($< 1\,\mu\text{s} - 10\,\mu\text{s}$) of the overall system is crucial [9, 17]. Therefore, the interrupt frequency of the controllers must be as high as possible, which requires implementing the control algorithms in fixed-point representation on an Field Programmable Gate Array (FPGA). To be able to use the automated Hardware Description Language (HDL) code generation capabilities of *Matlab/Simulink*, the control algorithms had to be transformed to only use *HDL coder* compatible *Simulink* blocks as well as only using fixed-point representation of all signals. As a consequence, the use of division operations (high space and clock cycle count demand) had to be reduced to a minimum and all trigonometric operations had to be performed by Coordinate Rotation Digital Computer (CORDIC)-based functions provided by *Simulink* and the use of look-up tables (LUT). To have full control of the timing, the necessary pipeline stages are placed manually after each mathematical operation. Synchronization between the signals within the respective controllers is also done manually via "data valid" input and output signals for all sub-function running in parallel. This allows to increase the interrupt frequency of the energy controller to 1 MHz and the PCC to 2.5 MHz as

depicted in timing diagram in Fig. 5 with the FPGA it self running at 100 MHz. For data transmission between the RTSS and the CCU using GTX, a custom transmission protocol has been developed. This transfers 16 x 32 bit-data-words and one 32 bit-comma for transmission separation in b8b10 encoding with 6.25 Gbit s^{-1}. After receiving the last data word, the 16 data words are output synchronously. This leads to a data transmission refresh rate of 9.19 MHz with a transmission dead time of 343 ns as shown in Fig. 5.

3 Laboratory Prototype and Measurement Results

As shown in the schematic diagram in Fig. 1, the laboratory prototype shown in Fig. 6 b) of the PHIL test bench consists of one RTSS and two identical PHIL systems. Each PHIL system in turn has its own Central Control Unit (CCU), which controls the Active-Front-End (AFE) for power exchange with the feeding grid, the Dual-Active-Bridges (DAB) using resonant LLC transformers for galvanic isolation and the PHC as the PHIL output stage. Each PHC can provide 3-phase AC or bipolar DC as output voltage [12] and has a power rating of 60 kVA. This leads to a PHIL test bench which can emulate one 6-AC, 3-AC or bipolar DC system with a power rating of 120 kVA or two systems with 2x3-AC, 1x3-AC and 1xbipolar-DC or 2xbipolar-DC with a respective power rating of 60 kVA.
To facilitate the engineering overhead and the maintenance, identical 30 kVA single-board converters (Fig. 6 e)) are used in parallel to form the AFE, the DAB primary side, the DAB secondary side and the MPS of the PHC as depicted in Fig. 6 a) and Fig. 6 b). The eight converters of each PHIL system are equipped with the Silicon Carbide (SiC) MOSFET B6-bridge module *CCS050M12CM2* from *Wolfspeed*.

Signal Processing System

A modular signal processing system based on the *ZYNQ7030* System on Chip (SoC) from *Xilinx* was developed for use as a CCU [13] and is also used as the RTSS. As shown in Fig. 6 c), the system has eight slots for Expansion Cards (EC). Custom ECs have been designed as digital interface to the power electronics hardware, for fast analog signal sampling (5 MS s^{-1}) with low latency ($\approx$ 450 ns) and as interface to peripheral components (contractors, fans, emergency stop, etc.). For high speed measurement of high voltages signals e.g. the output voltage of a DUT, an EC with a measurement range of $\pm$1000 V and a digital galvanic isolation was designed. It has also 5 MS s^{-1} and a latency of $\approx$ 500 ns. The data

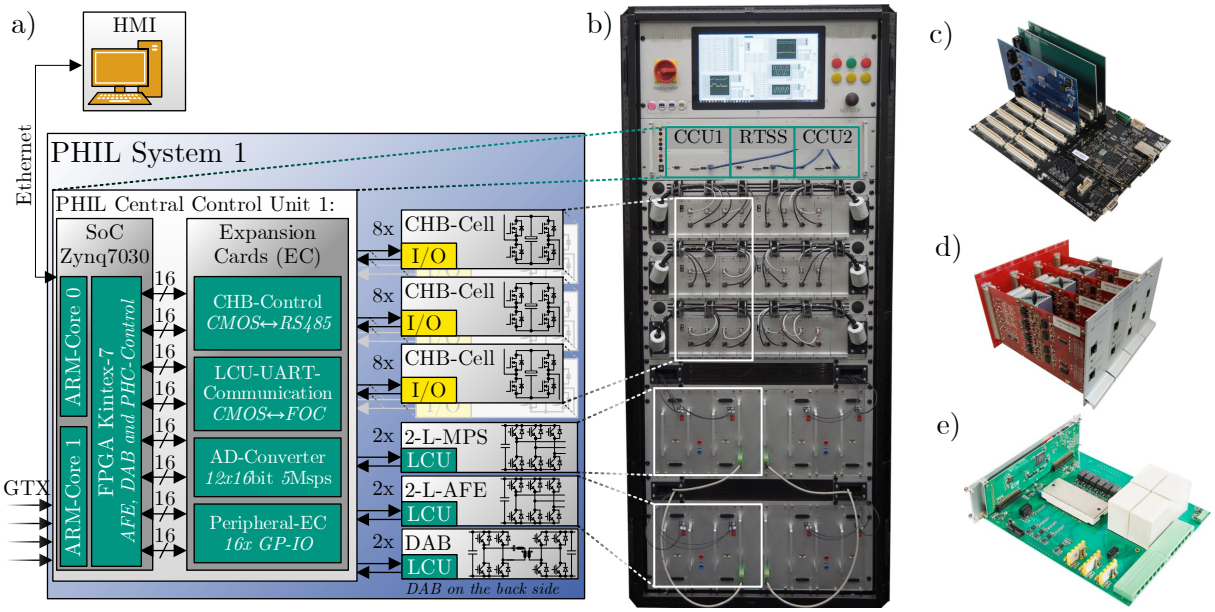

Fig. 6: a) Control structure of PHIL-System 1; b) laboratory prototype with PHIL-System 1 on the left; c) Signal processing system; d) CHB phase with four double H-bridge cells; e) 30 kVA single-board converter with SiC-B6-bridge

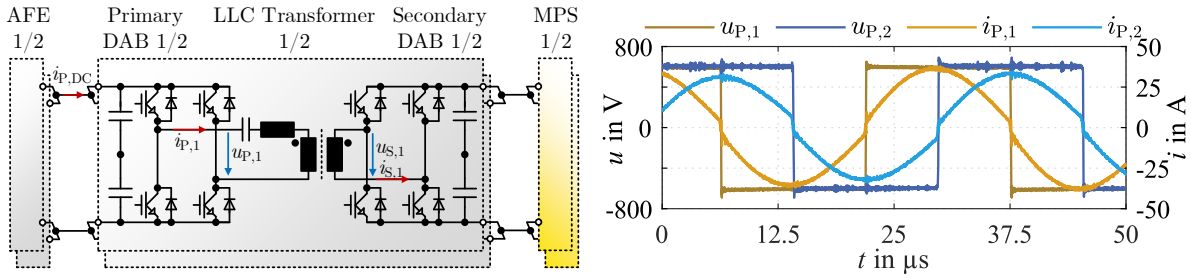

Fig. 7: Equivalent circuit of the galvanic isolation and measurement results of the primary DABs output voltages $u_{P,1/2}$ and currents $i_{P,1/2}$

between the CCUs and the RTSS FPGAs is transferred via high-speed 6.25 Gbit s^{-1} GTX transceivers and the communication with the user computer is done via Ethernet and a *Labview* based Monitor Control Tool (MCT).

Active-Front-End

The cascaded control scheme of the AFE has an interrupt frequency of 50 kHz and is separated into one DC-link voltage controller on CCU FPGA of the PHIL-Systems and one current controller on each of the Local Control Unite (LCU) FPGAs of the 30 kVA single-board converters. The high switching frequency of 50 kHz of the AFE converters and their 1 mH three-legged grid choke with an additional common-mode choke lead to very low grid perturbations.

Galvanic isolation

The galvanic isolation is necessary to separate the output stages of the two PHIL systems from the potential reference of the feeding grid and from each other. Thus the DUT is enabled to define the potential reference and furthermore undesired common mode currents between the PHIL test bench and DUT are avoided. Two parallel Dual-Active-Bridges (DAB) each with their own resonant LLC transformer provide galvanic isolation between the AFE and the PHC. The resonance frequency of both resonant tanks are tuned to be very close to each other and the DABs have a fixed duty cycle of 50 % with a 90° phase shift between each other as depicted in the measurements shown in Fig. 7.

Parallel Hybrid Converter

Fig. 6 d) depicts one phase of the CHB with eight H-bridge cells connected in series via a power back-plane, with two H-bridge cells on each PCB. To ensure a very low dead time, which is required for PHIL applications, the CHB cell's gate drivers and ADCs are directly controlled by the CCU. *RS-485* and twisted *Cat6e* cables are used for the signal transmission to the CHB cells.
Similar to the AFE, two of the 30 kVA single board converters are used in parallel each with their own coupling inductors as MPS. Since the dead time of the MPS is less crucial, the two MPS converter receive the same reference switching states determined by the PCC from the CCU by serial communication protocol via fiber optic cables (FOC). For the coupling inductors iron powder core inductors with a linear relationship between current and inductance [18] are used. At their rated current value of $i_m = 45$ A, their inductance value is $L_m = 160$ mH. The maximum fundamental frequency at rated current of the inductor is 2 kHz, above that the current amplitude must be decreased.

4 Measurement Results

Active pre-charge of the CHB

Fig. 8 depicts the active pre-charging of the CHB cell capacitors of PHIL-System 1. On the left side measured voltages of the CHB arm voltage $u_{c1,C,1}$ of phase 1 and the line to line voltage of phase 1 and phase 2 of the MPS and CHB output voltages $u_{m1,12}$ and $u_{c1,12}$ are depicted. Also depicted on the left side is the CHB output voltage $\bar{u}_{c1,12}$, filtered in post-processing with a symmetric moving average

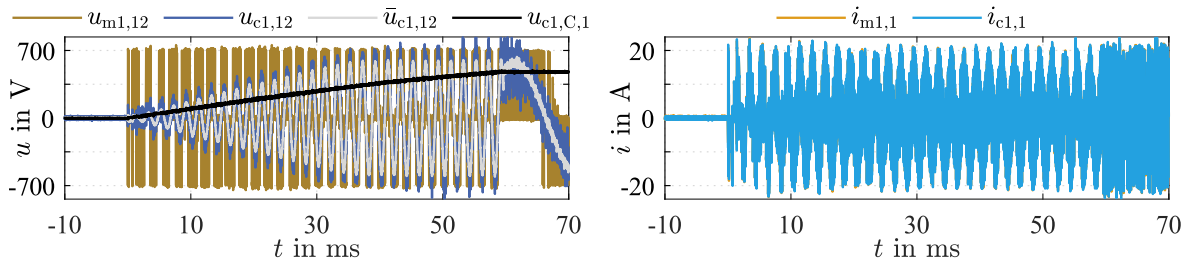

Fig. 8: Active pre-charge of the CHB cell capacitors to an arm voltage of $u^*_{c,C,x} = 480\,\mathrm{V}$ with a $f^*_o = 500\,\mathrm{Hz}$ and $\hat{u}^*_{c,x} = 325\,\mathrm{V}$

filter with a window width of 1 µs to suppress the 1 MHz PWM of the CHB. On the right side the MPS and the CHB currents $i_{m1,1}$ and $i_{c1,1}$ of phase 1 are depicted, which are identical since the PHC output contractors are left open during the pre-charging process. To charge the CHB cell capacitors, the PHC control regulates a positive active power flow into the CHB. Therefore the PHC reference output voltage is set to $u^*_{c,x} = 325\,\mathrm{V}$ and the reference frequency is set to $f^*_o = 500\,\mathrm{Hz}$. During process, the reference current space vector $\underline{i}^*_c$ has its maximum length of 10 A ($i_{c,max} = 20\,\mathrm{A}$), which reduces the error boundary circle radius $e_{c,max}$ to 10 A (cf. PCC in Fig. 4). Thus, the 500 Hz component for active power generation is clearly visible in the CHB current in Fig. 8. Once the reference CHB arm voltage (480 V in Fig. 8) is reached, the system switches automatically to the reference values transmitted by the RTSS ($u^*_{c,x} = 325\,\mathrm{V}$, $f^*_o = 50\,\mathrm{Hz}$ in in Fig. 8).
The measurement also shows that the PHC control is dynamic enough to limit the CHB currents during precharging (even at $u_{c,x} = 0\,\mathrm{V}$) to the set maximum value $i_{c,max} = 20\,\mathrm{A}$, which makes a passive precharging circuit obsolete. Due to the dynamic control of the PHC, the CHB arm voltage can also be adjusted flexibly to other set values within ms while in operation. This allows the multilevel voltage step height to be adjusted for each application to maximize the use of the CHB's 17 voltage levels without the need to adjust the supplying DC link voltage of the PHC. This capability is a unique feature compared to state-of-the-art multilevel converters used for PHIL applications.

Grid emulation for testing a solid-state transformer

In the following, a 30 kVA solid-state transformer (SST) is connected to the two PHIL systems as a DUT, as shown in Fig. 9. The measurement results are shown in Fig. 10. The SST uses the same 30 kVA single board converter depicted in Fig. 6 e) as hardware and the same software for its AFE1, AFE2 and galvanic isolation as the previously presented PHIL system. The objective of the SST is to couple two different grids and control the power flow between them. For this purpose AFE2 controls the DC link voltage of the SST and AFE1 controls the current flow between the two grids. For the measurement the two grids were emulated as ideal 50 Hz three-phase 400 V grids by the two PHIL systems. AFE1 and AFE2 of the SST have a control and switching frequency of 50 kHz and a 1 mH grid inductor leading to a very low current ripple (Fig. 10 c) & Fig. 10 d)). To increase the utilization of the 17 voltage levels, the arm voltage of the two CHBs are reduced to $u_{c1/2,C,x} = 400\,\mathrm{V}$ leaving a voltage margin of 75 V.
As depicted in Fig. 10 c) at $t = -1.2\,\mathrm{ms}$ the current controller of AFE1 was given a setpoint step change

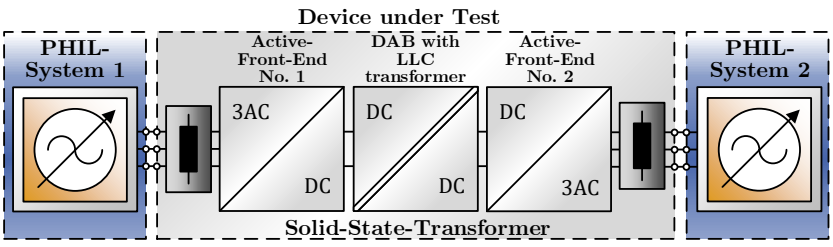

Fig. 9: Test setup with the solid state transformer as DUT between PHIL-System 1 and PHIL-System 2

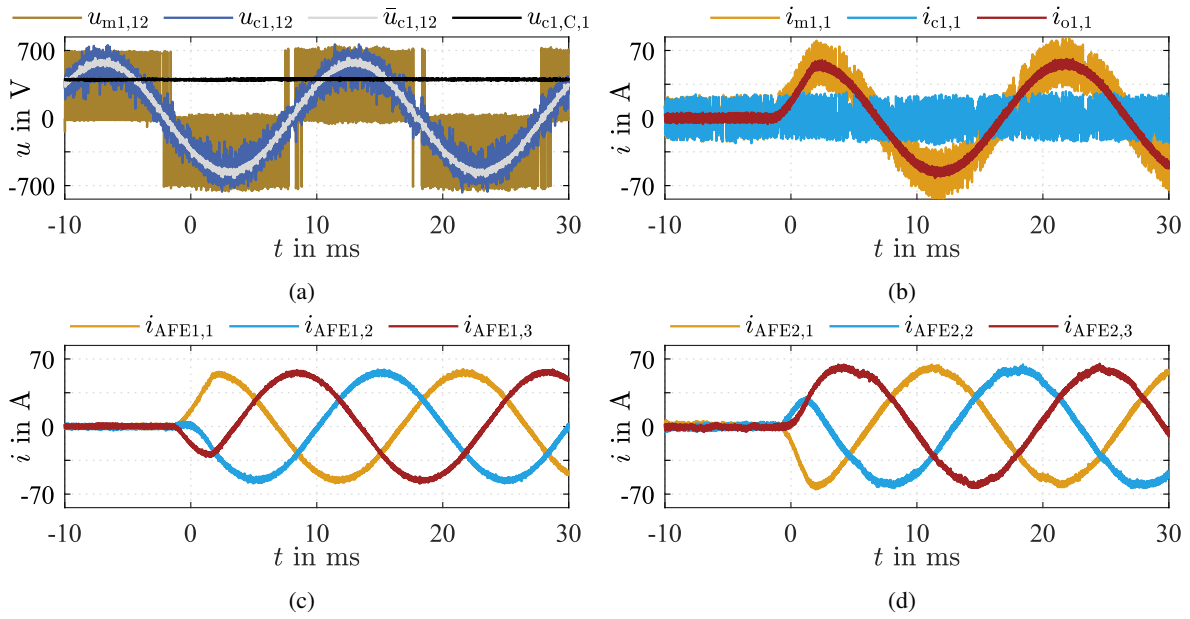

Fig. 10: Measurement results of the two PHIL systems emulating ideal grids connected to a 30 kVA SST

from $i_d = 0\,A$ to $i_d = 60\,A$, whereby the current change is limited by a setpoint ramp within the AFE1 current controller. This 0 kW to 29.3 kW load step does not effect the arm voltage $u_{c1,C,1}$ of the PHIL-System 1 CHB or the CHB output voltage $u_{c1,12}$ as depicted in Fig. 10 a) nor is it visible in the CHB current $i_{c1,1}$ shown in Fig. 10 b). Instead the fundamental current is fully supplied by the MPS regardless of the operating point, thereby limiting the CHB output current to the MPS current ripple. The measured CHB line to line output voltage $u_{c1,12}$ and the in post-processing moving average filtered CHB voltage $\bar{u}_{c1,12}$ (window width of 1 µs) depicted in Fig. 10 a) clearly show that the PHC has the same output voltage characteristics as a full-power multilevel converter. But compared to full-power multilevel converter only the low power CHB has to have the high effective switching frequency of 1 MHz ($\bar{f}_{c,SW,MOSFET} = 63.8\,kHz$) and the high-power 2-level MPS has a low average switching frequency of $\bar{f}_{m,SW} = 6.2\,kHz$. The output voltage and current of the PHC/PHIL are not affected by the switching 2-level voltage of the MPS and the current ripple of the PHC/PHIL output current is only caused by the AFE1 and AFE2 switching with 50 kHz.

5 Conclusion

This paper shows the concept of a six phase Power-Hardware-in-the-Loop (PHIL) Test Bench on basis of the novel Cascaded H-Bridge (CHB) based Parallel Hybrid Converter (PHC) for the emulation of AC and/or DC grids or an electrical machine with three or six phases. The presented 120 kVA laboratory prototype is able to emulate a 6-AC, 3-AC or bipolar DC system with a power rating of 120 kVA or two systems with 2x3-AC, 1x3-AC and 1xbipolar-DC or 2xbipolar-DC with a respective power rating of 60 kVA. Due to advantageous converter configuration, the PHC has the same output voltage characteristics as full-power multilevel converters previously used as PHIL output stage, but has inherently higher power density and lower costs compared to them. The low power CHB only has to carry the current ripple of the 2L-VSC used as Main Power Source (MPS), however it defines the output voltage of the PHC. The laboratory prototype, the signal processing system, the power electronics hardware, the control algorithms and their implementation on the Central Control Unite's FPGA are shown in detail. Measurement results showing the active pre-charging of the CHB and thus demonstrating the high dynamic of the PHC current and energy controller are shown. For a further measurement, a 30 kVA grid-coupling solid-state transformer (SST) is connected to the two PHIL systems, each emulating an ideal 50 Hz three-phase 400 V grid. The measurement results show a 29.3 kW load step of the SST and validate the statements that firstly this load step does not affect the current or the arm voltage of the CHB,

secondly the MPS supplies the entire output current of the PHC and thirdly the output voltage is defined by the CHB regardless of the MPS.
In a next step a non ideal gird model as well as the model of model of a non-linear permanent magnet synchronous machine will be implemented on the real-time-simulation-system of the PHIL test bench and used to test an inverter system consisting of a drive inverter and an active front end.

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