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Medium Voltage Power Electronic Building Block for Quasi-two-level Operation of a Flying Capacitor Converter

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Keywords

≪Multi-level converters≫, ≪Flying Capacitor Converter≫, ≪Medium voltage converter≫, ≪Silicon Carbide (SiC)≫, ≪Grid-connected converter≫.

Abstract

Today's standard medium voltage converters are operated at low switching frequencies and contain bulky line filters. One concept to change this is the Quasi-Two-Level operation of multilevel converters with fast switching semiconductors to minimize passive components. This paper presents the hardware of a full-scale medium voltage SiC-based flying capacitor converter for quasi-two-level operation with up to 10 kV DC voltage and 150 A line current. This hardware enables studies on the influence of components, modulation principles and control algorithms on the needed filters and the operation of the converter.

Introduction

The generation of electrical energy is currently changing and is expected to change completely in the next 30 years. The power of inverter-based generation systems for renewable energy is increasing and these can no longer be efficiently implemented in low voltage alone. Thus, the applications for medium voltage converters will become more present in the grid and increase in relevance. Today's standard medium voltage converters are either based on the Modular Multilevel Converter (MMC) technology or use 3/5-Level approaches operated at low switching frequencies and contain bulky line filters. Both concepts still lead to relatively high costs and low efficiencies, which are major reasons for the slow spread of medium voltage power converters in grid applications. One promising concept is the Quasi-Two-Level operation of multilevel converters with fast switching semiconductors.

The requirement for the blocking voltage at medium voltage converters can be achieved by use semiconductors with a high blocking voltage or connect semiconductors with lower blocking voltage in series. Switching high potentials generate a very high voltage gradient during turn on or off. A high voltage gradient leads to high stress on the insulation and results in shorter lifespan and higher failure rates. Additionally, semiconductors blocking 10 kV and more are currently not commercially available and it is hard to predict if they ever will be for high power applications. Direct series connection of low voltage semiconductors to realise a two-level medium voltage converter is risky and difficult. The static and dynamic voltage distribution among the individual semiconductors must be considered. Multilevel converters can overcome these disadvantages. The passive components in multilevel converters divide the voltage across the individual semiconductors. These passive components make the converter more complex and expensive. More complex control algorithms are required than with the two-level converter, as many more variables have to be controlled or balanced with multilevel converters. There are efforts

to find an optimum between them. Often three or five level topologies are used in the medium voltage because often Semiconductors with high enough blocking voltage are not available.

In this paper, the Flying Capacitor Converter is considered as a possible realization of a such medium voltage converter. Various approaches exist for the Flying Capacitor Converter like new semiconductors and control algorithms. New types of power semiconductors such as silicon carbide (SiC) are used [1] and new methods of mechanical design are presented [2]. Additionally, there are also approaches for modulation techniques for conventional multilevel operation [3]. Furthermore, there are concepts for new operation modes: the quasi-3-level operation [4] or the quasi-two-level operation [5], [6]. These are compared in [7].

The sizing of passive components, such as capacitors or filters, is always dependent on switching frequency, switching time or modulation carrier frequency. A modification always influences the whole system and design impacts both the converter sizing and the interaction with the system components. For investigations in this context, hardware is required that is modular and adaptable to enable multiple studies. For the optimization of the parameters, simulations can be carried out, but only effects that are known and can be described mathematically can be taken into account in simulations. Ultimately, novel concepts must be demonstrated and proven with real hardware.

The concept of building the converter from Power Electronic Building Blocks (PEBB) allows to investigate scalability in the number of levels, reconfigurability of individual elements and different but similar topologies. It is possible to equip the same power units with only one different component to investigate its influence. An example for a similar topology and application example for a possible configuration would be the conversion to a five-level cascaded flying capacitor [8].

Fundamentals

The concept of the flying capacitor converter has been known for a long time and was first presented in [9]. The multilevel output-voltage is generated by switching capacitors into the active current flow path. At different capacitor voltages, this leads to different output voltages depending on the combinations of interconnections. Figure 1 (a) depicts the basic structure of a 5-level flying capacitor (FC) topology. An n-level flying capacitor converter ($n \in \mathbb{N}$) is made of $2 \cdot (n-1)$ power semiconductor switches and $(n-2)$ capacitors in addition to the DC link capacitor. Only one switch in each pair of transistors (commutation cell) can be turned on at the same time to prevent short circuits between the capacitors. Each capacitor C_i has a different nominal voltage $v_{\mathrm{c,nom},i}$.

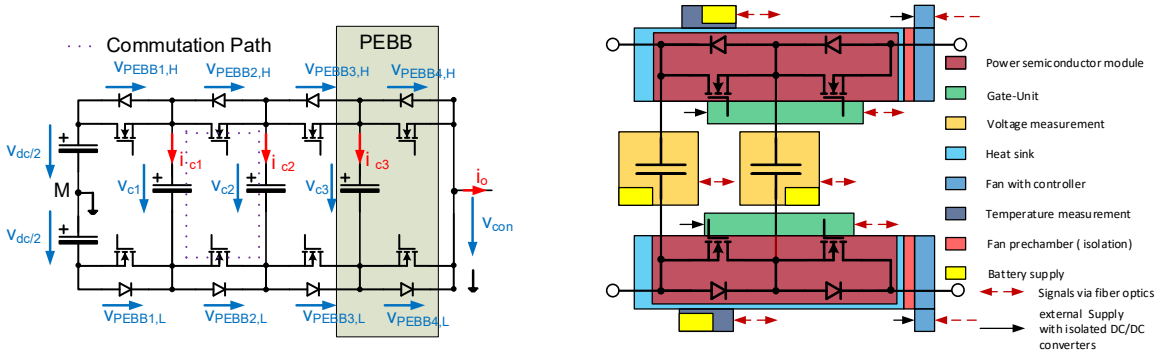
$$v_{\mathrm{c,nom},i} = v_{\mathrm{DC}} \cdot \frac{n-1-i}{n-1} \quad i \in [1...(n-2)] \tag{1}$$

Each commutation cell can connect one of the capacitors into the output path to generate the multilevel output voltage. The commutation path is between the high side and the low side semiconductor of each pair including the adjacent capacitors.

To simplify the construction, the converter is built by using modular components, i.e. Power Electronic Building Blocks (PEBB). In this case, two semiconductor switches and one capacitor are integrated into one PEBB because this is the repeating circuit element of the converter. An n-level converter requires $(n-1)$ PEBBs. The nominal voltage for the semiconductors in a PEBB can be calculated with Equation (2).

$$v_{\mathrm{PEBB,nom}} = \frac{v_{\mathrm{DC}}}{n-1} \tag{2}$$

During operation the applied voltage across the semiconductors always deviates from the nominal voltage, because the capacitor voltages are free-floating and not clamped by external voltages sources. These deviations of the capacitor voltages arise when the output current flows through the capacitors. This happens at all multilevel output voltage levels except for $+\frac{v_{\mathrm{DC}}}{2}$ and $-\frac{v_{\mathrm{DC}}}{2}$. It is necessary to balance the capacitor voltages to keep their deviation in acceptable limits. For the PEBB, it was defined that 10 %



(a) 5-level flying capacitor converter, single phase design

(b) Sketch of dual Power Electronic Building Block with communication and supply

Fig. 1: 5-level flying capacitor converter, circuit diagram and function groups of a PEBB

of $v_{\mathrm{PEBB,nom}}$ is an acceptable deviation for the capacitor voltage. In the same way, it was defined that about 50 % of the semiconductor rated voltage is equivalent to the $v_{\mathrm{PEBB,nom}}$. The remaining voltage is needed for the capacitor voltage deviations and the transient overvoltages by turn on of the MOSFETs. The above limit of capacitor voltage deviation corresponds to about 20 % of the nominal voltage of the semiconductor, because the deviation of two capacitors next to each other can be opposite. This leaves 30 % of the semiconductor nominal voltage for transient overvoltage.

A very important task is therefore to guarantee that the deviations of the capacitor voltages are within the defined limit. There are different ways of achieving this in the various operating modes: Conventional multilevel operation with APOD (Alternative Phase Opposition Disposition) modulation works by exchanging carrier signals symmetrically for the corresponding semiconductor [10]. Alternatively, there are modern solutions with modified space vector modulation [3]. Each of these balancing methods require no measurement of the capacitor voltage during operation. For quasi-two-level operation, there are two types of balancing: passive - without and active - with capacitor voltage measurement. A method with passive balancing in a stationary operating point is presented in [6]. Furthermore, several active balancing algorithms are known in literature, e.g. [5], [6] and [11]. Active balancing is based on the two equal manipulable values: The time that current flows through the same capacitor and the variation of the current direction through the capacitor.

The literature just referred to has shown that in addition to active balancing, passive components can be reduced in this operating mode. Furthermore, it was shown in [12] that the operation mode of quasi-two-level also has a positive influence on other external components like long cables compared to the 2-level operation. A fair comparison of the algorithms is only possible under identical conditions. Such studies will be accomplished in future work by using this full-scale hardware.

Concept of a PEBB

A Power Electronic Building Block is the concept of integrating all functional groups into modular units. A PEBB consists of the power semiconductors, the capacitors and the necessary peripherals. These are gate units, measurement of the capacitor voltage and heat sink temperature and fan control. An overview of the arrangement of a dual PEBB and the supply concept is shown in Figure 1 (b). With the modular design, the presented approach is to build a complete inverter by simply connecting interchangeable units. This means that the insulation of the PEBB must be designed for the highest possible voltage, i.e. DC-Link voltage. This is one of the reasons why this topology is not used for high voltage applications. The PEBB internally isolates the medium voltage from its power supply and higher-level control.

Components of a PEBB

The following requirements were used for the selection of the components and the design. The PEBB should allow a maximum DC operating voltage of 10 kV across the flying capacitors and the DC-Link capacitor. The DC-Link voltage is selected for operation depending on the module type and stage configuration. It should have an RMS line current capability of 150 A. The power semiconductors should have the shortest possible rise and falling time. This is fundamental for the quasi-two-level operation. With the thermal design, operation at switching frequencies from 10 kHz to 20 kHz are possible. The use of either 1200 V or a 1700 V modules is possible. Each capacitor pack for each voltage level has a capacitance of approximately 1 µF. The capacity was calculated according to [5]. In standard multilevel operation, the required capacitance at a switching frequency of 10 kHz would be about 0.2 mF, i.e. 200 times as much compared to the quasi-two-level operation. At a switching frequency of 20 kHz, the required capacitance would be about 0.1 mF. From a mechanical design point of view, it was not a goal to realise such large capacities, therefore it was designed for quasi-two-level operation.

Power Modules

For the quasi-two-level operation mode it is essential that a power semiconductor is turned on and off as fast as possible. Therefore, SiC-MOSFETs were selected as the technology. Most commercially available packages are half bridges or three-phase bridges, single semiconductors are very rare. Therefore, a half bridge module was selected. This is also the reason why the assembly as shown in Figure 1 (b) consists of two PEBBs. An important deciding factor for the packaging was also the placement of the gate connections and power connections in the module housing. It should be possible that the gate connections are on the outside of the commutation cell.

The first prototype is built with CAS300M12BM2 1200 V, 300 A modules. There are 1700 V variants available in the same package with the same nominal current. When selecting the modules, the conduction losses and switching losses were also calculated on the basis of data sheet values. At 150 A phase current and 10 kHz, there is a ratio of 1:1 between conduction losses and switching losses. In this case, the total losses of one half-bridge module are 385 W. At 150 A phase current and 20 kHz, there is a ratio of 1:2 between conduction losses and switching losses. In this case, the total losses of a half-bridge module are 582 W, which is the maximum that can be thermally dissipated at 150 °C MOSFET junction temperature.

Flying Capacitors

The next important components are the capacitors of the PEBB. The capacitance is implemented with two different types of capacitors connected in parallel. One part are ceramic capacitors, which are connected to the modules with a minimized stray inductance to minimize overvoltage at the semiconductors. The larger part consists of film capacitors which are adapted to the voltage of the corresponding flying capacitor. Although the capacitors of different PEBBs differ in voltage rating they always provide the same total capacitance. The different capacitors also differ in their physical size.

The capacitance ratio of ceramic to film was chosen as 1:10 as an usual ratio. The ceramic capacitors with 10 kV nominal voltage are the same for all voltage levels of the flying capacitor. Ceramic capacitors with rated voltage above 2 kV are custom made, each configuration introduces extra costs, so a configuration was chosen that can be used for any capacitor voltage. For industrial use, the ceramic capacitors would be selected accordingly, as with the film capacitors.

Auxiliary Function Groups

In addition to the components in the power section itself, peripheral circuitry is also required for operation. The two important components are the gate unit and the capacitor voltage measurement. There is also a temperature measurement of each heatsink and a control of the heatsink fans. These peripherals are not described further.

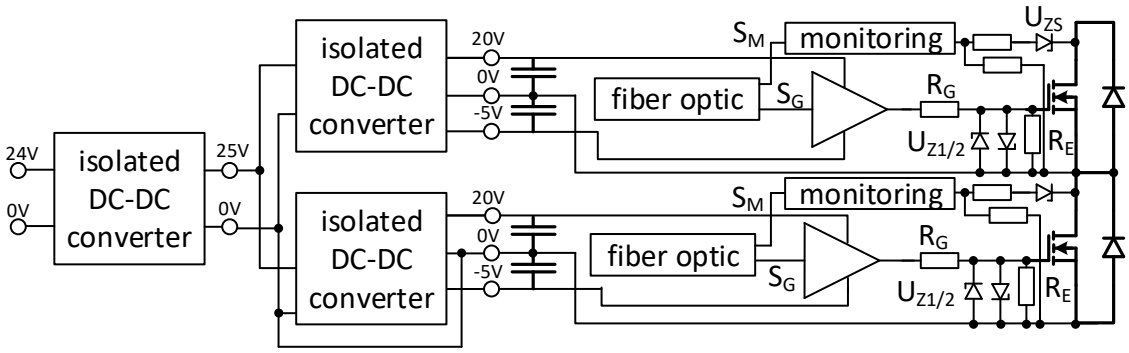


Fig. 2: The gate circuit with supply and monitoring

Gate-Unit

Compared to other topologies, the gate unit is more complex, since it cannot be supplied from a local energy storage (capacitor of the power section as in the modular multilevel converter) or with a constant reference potential (as in the two-level converter). The gate unit is not supplied from the capacitors, because the capacitor voltages vary significantly during operation. The developing of a wide range medium-to-extra-low-voltage DC/DC converter was deemed to be beyond the scope of this project. Therefore, the actual gate driver supply is built from galvanically isolated DC/DC converters with an external supply. The first stage separates the transient voltage jumps of the source connection of the module and the second stage separates the potential of the high and low side MOSFETs. The first stage is equipped with an isolated DC/DC converter with a high isolation voltage ($> 10\,\mathrm{kV}$). It is located outside the PCB of the Gate-Unit. The second stage is equipped with another DC/DC converter with a DC isolation voltage corresponding to the semiconductor. Additionally, a monitoring of the switching state of the MOSFETs was built in. A resistor divider and diodes in series determine the voltage drop across the MOSFETs. The measured voltage is compared with a reference voltage using a comparator, which generates a digital switching state signal. Otherwise, the gate circuitry is the usual state of the art. Gate signals and monitoring signals are transmitted via fiber optic cables. The gate circuit with supply and monitoring is shown in fig. 2.

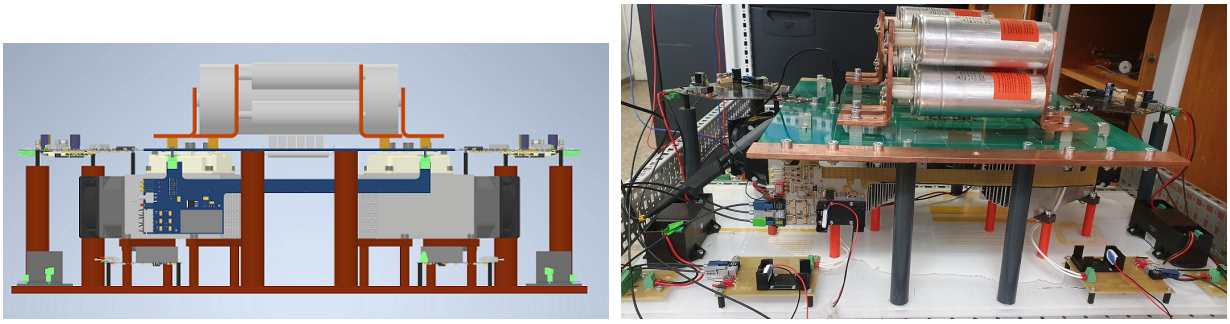
Capacitor Voltage Measurement

By active balancing, measurement of the individual capacitor voltages with sufficient precision and dynamic is necessary. An ohmic/capacitive voltage divider is used for the voltage measurement. The base of the divider is at the potential of the respective capacitor. The alternative idea was to realize a differential voltage measurement, which measures the voltage of the plus or minus pole of the capacitors in relation to ground (marked in Figure 1 (a) with point M). The voltage of both ends of the capacitors with reference to ground changes rapidly with the switching. These would interfere with the measurement path and would require an unfeasible damping or bandwidth limitation to the measurement setup. This is the most usual measurement method for voltages in converters, so it was also analysed.

To avoid difficulties in designing a power supply capable of withstanding the switching interference, the voltage measurement circuitry is instead supplied by batteries. This is feasible since as a lab prototype the setup will only be used for short research experiments - like with the gate unit, a separate high-insulation dc/dc converter would also be possible. The measured voltages are digitized with an ADC integrated into the PCB. The digital AD values are transmitted via fiber optic cables to the central signal processing unit.

Design of a PEBB

The design of a PEBB is divided up into two major areas: the main PCB, containing the power electronic components and the mechanical arrangement of the additional components. The biggest challenge is to



(a) 3D model of a double PEBB

(b) First hardware setup of a double PEBB

Fig. 3: Mechanical construction and realization of a double PEBB

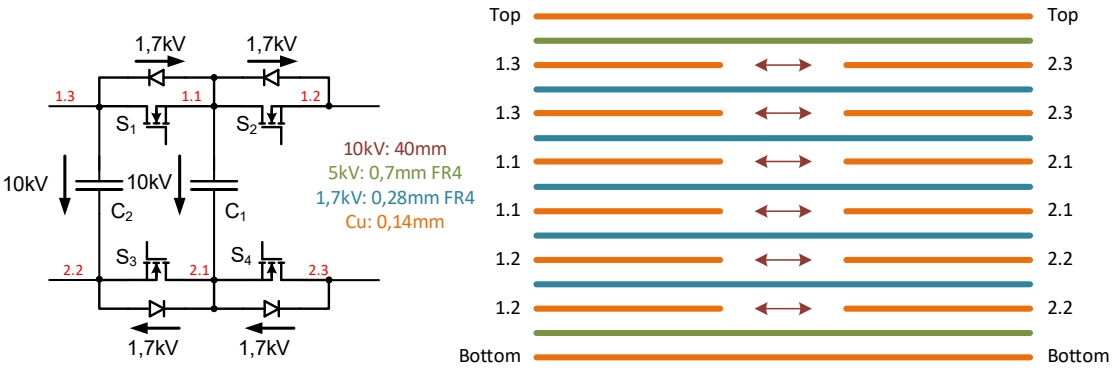


Fig. 4: The stack-up of the main PCB layout with required isolation voltages

create a compact low-inductance design while keeping the spacing for the medium voltage insulation distances. A front view from the 3D model is shown in Figure 3 (a) and a photo of the first prototype is shown in Figure 3 (b).

Main PCB Layout

The main task of the PCB is to realize the electrical connections. To connect the power electronic components a PCB with 8 layers of 120 µm thick copper was used. This allows a RMS current of 150 A which is fully contained on the inside layers since the outer layers only contain the terminals for the components.

The thickness of the PCB between the layers and the creepage distances were selected according to the relevant standards (DIN-EN 61800-5-1). Important aspects in the design of the PCB and thus the performance of the power section were the position of the components and the layer structure. For each of the following connections two layers are used in parallel: Power terminals of PEBB to module, module to capacitors and module to Power terminals of PEBB on the other side. There is a layout separation of the upper half bridge and the lower half bridge, which can be seen in fig. 4. The structure is symmetrical and the high and low sides can be connected in the identically assigned inner layer. The 10 kV isolation is realized with this layout separation in the PCB and the corresponding creepage distances. Except for the power connections from the PEBB, there is no copper on the outer layers to avoid unnecessarily increasing creepage distances and clearances outside the PCB to periphery components such as the fans or voltage measurement.

Mechanical Construction

After designing the Main PCB, it must be integrated with the supporting peripheral components into a stand-alone module. The mechanical construction is shown in fig. 5. Particular attention must be paid

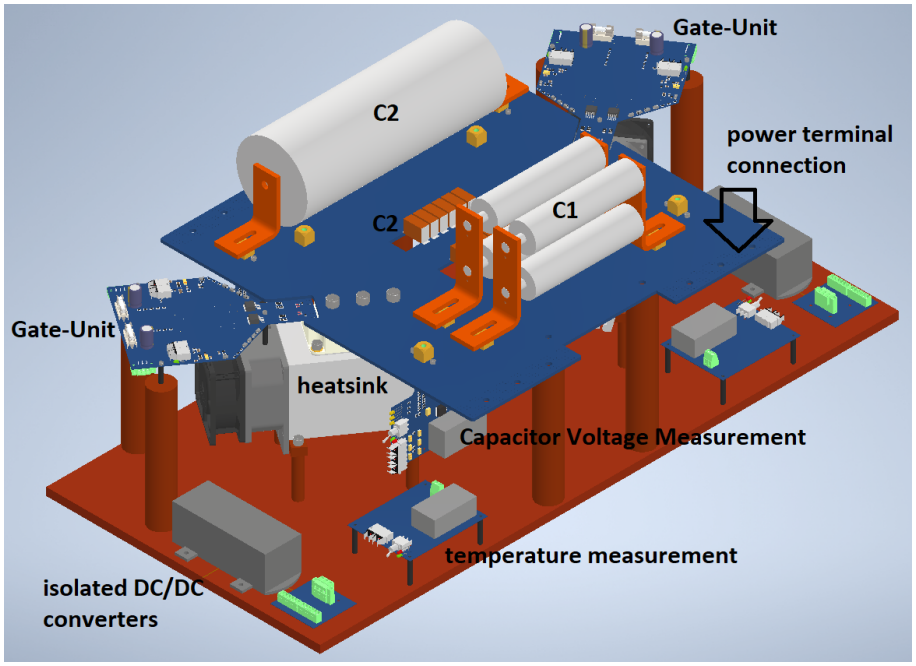


Fig. 5: 3D model of a double PEBB with labeling

to the clearance and creepage distances and the air flow through the heatsink. To make the PEBB stand-alone, all parts are mounted on an isolating polycarbonate board. The power PCB is placed such that the capacitors are on top to give maximum distance of the high voltage parts to the other parts mounted to the board. It also enables easy installation of the film capacitors, which vary in size. This results in the heatsinks being located between the mounting board and the PCB. Additional supports are used to raise the heatsinks from the board and thereby simplify the airflow. The power modules, and consequently also the heatsinks, are mounted at an angle of 35° relative to the vertical axis of the long side of the PCB. This allows airflow from the outside towards the center with a defined total flow direction. The connection terminals are on two opposite edges of the PCB. They extend over the edges of the mounting plate so that they can be mounted directly on top of the other contact surface. The difference in height is compensated with an underlayer, which enables easy chaining of several PEBBs. The peripheral components are designed to fit into the volume defined by the mounting board and the height of the power PCB.

Simulations

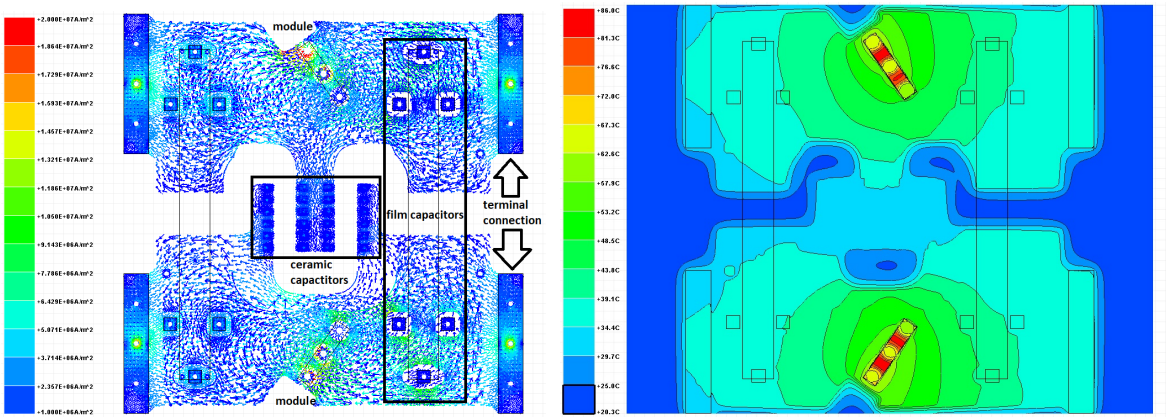
In order to validate the ideas of the PEBB before the main PCB and the mechanical construction were finished, electrical and thermal simulations were executed.

Electrical

First, a SI-Wave simulation was used to determine the current density in the main PCB. It was observed that the rotated module positions reduce the average current density. It also led to an even distribution of the current between the parallel capacitors and to the screw terminals connecting to other PEBBs. The current distribution of the final design can be seen in Figure 6 (a).

Thermal

Another simulation target was to validate that the PCB would provide sufficient cooling at nominal current. With the calculated current density, it was possible to calculate the ohmic losses in the circuit board. The losses of the individual components in the power section were calculated using data sheet values. Losses of the peripheral circuitry were not included. The geometry and the power loss were integrated into a 3D coupled electrical and thermal FEM to determine the thermal conditions at peak power. The results for the PCB can be seen in Figure 6 (b). It is visible that there is a hot spot at the modules, where the highest losses occur. The temperature at the capacitor terminals is significantly



(a) Current distribution in the main PCB

(b) Temperature distribution on the main board

Fig. 6: Simulation of the electrical and thermal design

lower than at the module connections, because in the Quasi-2-Level-mode the capacitors carry current only during the switching instants. This results in very little losses inside the capacitors. In contrast, the power modules themselves transfer a part of their heat into the board through the electrical contacts, which leads to a higher temperature there. The simulations show that the area between the module contacts is hotter than its surroundings. The reason for this is that the module is in direct contact with the PCB in those areas leading to worse cooling.

Measurements

During the initial testing of the PEBB, several measurements have been made. In the following, the thermal design is validated and measurements of the switching behavior during commutation of the power cells on the PEBB are shown.

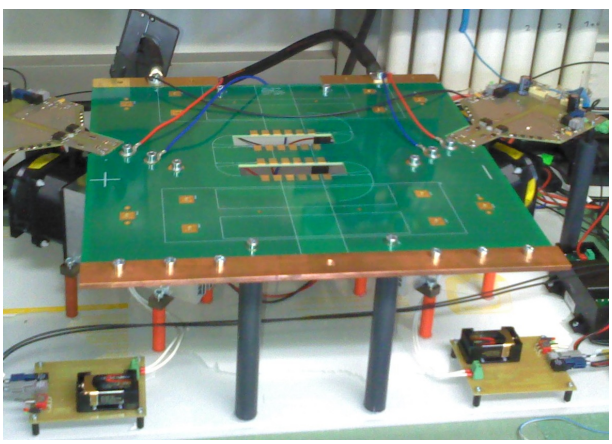
Thermal

A dedicated thermal set-up was built to validate the thermal design and the simulation results. The prototype of the PEBB was assembled except for the capacitors and the capacitor voltage measurement. A bus bar to terminate a phase between point 1.2 and 2.3 and a high-current power supply between point 1.3 and 2.2 were also connected (see fig. 4). The high current power supply injected an adjustable current via the turned on MOSFETs and parallel diodes. The power was measured at the modules and set in such a way that it corresponded to the switching losses and forward losses calculated from data sheet values. The set direct current is greater than the effective value considered in the design for the later application. Thus, in later operation, the board itself will remain colder. The calculated power loss of around 500 W per module was achieved with a DC current of approximately 190 A. The test was run until a thermal steady state was reached. A heat sink temperature of 75 °C was measured with a external Ntc-based temperature measurement. A surface temperature of 55 °C was measured with the thermal imaging camera at the Main PCB, the distribution is shown in fig. 7 (b). The temperature distribution and the measured heat sink temperature confirms the results of the thermal simulation.

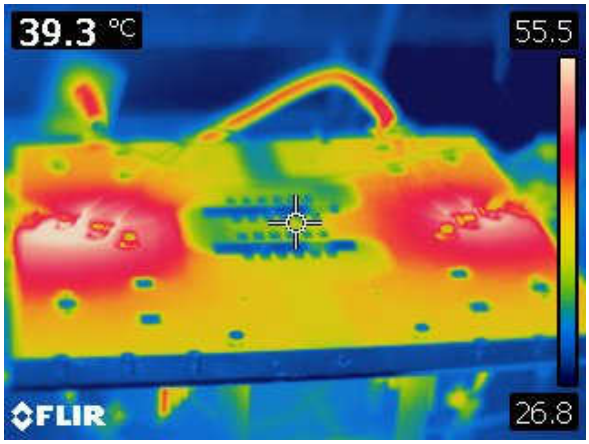
Electrical

The electrical function of the PEBB was tested as a buck converter. A bus bar to terminate a phase between point 1.2 and 2.3 and a choke was also connected to it (see fig. 4). The choke had 1 µH and the voltage at the capacitor behind the choke was also regulated with a DC power supply. The nominal value of the output voltage was 100 V depending on the DC power supply used. Between points 1.3 and 2.2 is also an second DC power supply connected. This DC power supply were supplied the flying capacitors. Only one semiconductor pair was switched and the output current is controlled.

The voltage trajectory at the semiconductors involved and the choke current were measured, which can be seen in fig. 8. In the following, the left cell of the corresponding commutation path is between point



(a) Test setup to validate the current capacity



(b) Measurement of the surface of the Main PCB temperature with a thermal camera

Fig. 7: Results of the validation of the thermal simulation

1.3,1.1, 2.1 and 2.2 - the right cell is between point 1.1,1.2, 2.3 and 2.1 (see fig. 4). In fig. 8 (a) the right cell is clocked (S_2 and S_4) and in the left cell both MOSFETs are permanently turned on. The input voltage was selected as 600 V and the choke current was 33 A. In fig. 8 (b) the left cell is clocked (S_1 and S_3) and in the right cell both MOSFETs are permanently turned on. The input voltage was selected as 300 V and the coke current was 30 A.

The commutation overvoltage is about 350 V in each case, and it can be seen that when the right cell is clocked there is an oscillation between the two capacitors involved. In case (a), the flying capacitor on the right is connected with the left flying capacitor from the left cell by the permanently switched-on MOSFETs. In the transient commutation case, a compensating current still flows through them, which explains the oscillation, which is not similar to real operation. In later operation, no capacities are turned in parallel. This was only done for easier measurements of the overvoltage.

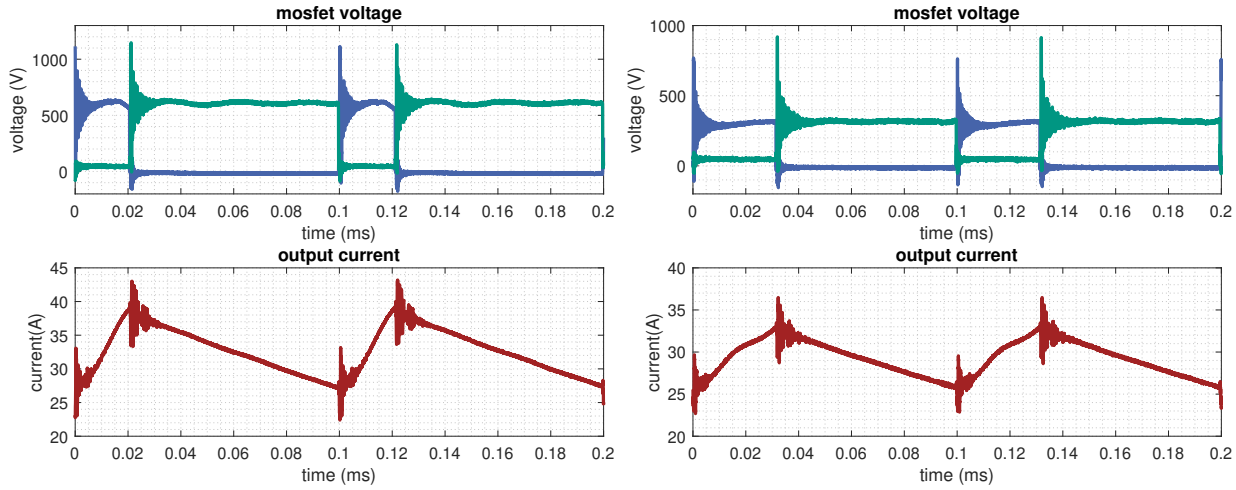
In case (b), the flying capacitor on the right is short-circuited from the right cell by the permanently turned-on MOSFETs and the bus bar. A lower capacitor voltage was selected in order to use a slightly higher modulation ratio.

The measurement was shown primarily to validate how large the overvoltage and thus whether fast switching would be possible. The overvoltage for this set-up is about 350 V, which can be explained by the high switching speed and the physically large commutation path. However, this overvoltage is within the limit of the voltage capabilities of the 1200 V semiconductors presented when using the capacitor voltages as described in the earlier chapter Fundamentals. If even faster switching is desired, then nominal voltage for the PEBB ($v_{\mathrm{PEBB,nom}}$) must be selected even lower. Alternatively, it would also be possible to select a smaller capacitor voltage deviation, but this would lead to larger flying capacitors or to a lower allowed phase current.

Conclusion

A PEBB module designed for quasi-two-level operation of a Flying Capacitor Converter was presented. The idea, the concept and the design of the hardware have been explained. This demonstrated that the modular concept can be implemented in a Flying Capacitor Converter. The electrical and thermal simulations were validated with measurements on the realized setup of the PEBB. It also showed the limitations in voltage distribution resulting from the switching overvoltage at such fast switching and the large commutation cells from medium voltage applications.

The presented PEBB enables easy realization of studies on different components, modulation principles and control algorithms for the medium voltage applications with the Flying Capacitor Converter.



(a) Measurement of the MOSFET voltage at the right commutation cell by buck converter operation

(b) Measurement of the MOSFET voltage at the left commutation cell by buck converter operation

Fig. 8: Results of the commutation as single operation - green is the voltage of the high side MOSFET and blue the voltage of the low side MOSFET of the commutation cell pair

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