Fast SiC-MOSFET Switch with Gate Boosting Technology

Martin Sack, Martin Hochberg, Dennis Herzog, Georg Mueller

Karlsruhe Institute of Technology, Institute for Pulsed Power and Microwave Technology, Germany

Corresponding author: Martin Sack, martin.sack@kit.edu

Abstract

Gate boosting enables a considerable increase in switching speed for commercially available MOSFETs. In the present work, a switch comprising three SiC-MOSFETs in parallel configuration has been combined with a gate drive circuit employing a gate boosting technology based on a series capacitance and increased driver voltage. The gate driver uses GaN-HEMTs in a half-bridge topology. The MOSFET switch has been tested in pulsed operation with a resistive load up to 1 kV and 90 A at the load. Thereby, the capacitance and supply voltage of the gate driver have been varied. A rise time of 3.3 ns at the load has been achieved.

1 Introduction

For microbial decontamination of liquids by means of pulsed electric fields semiconductor-based pulse generators capable of delivering rectangular pulses with fast rise time at a pulsed power level in the range of several megawatt are required. A realized design for such a generator is based on IGBT switches and gate boosting technology [1].

Modern power MOSFETs based on Silicon Carbide or Gallium Nitride combine a high rated voltage in the order of 1 kV with a low drain-source resistance and the capability of fast switching. Hence, they can be considered as interesting alternative to IGBTs, especially if fast switching is of interest for the intended application. Fast switching allows for an operation with less switching losses especially under hard-switching conditions, and enables a more compact design, as an operation at higher switching frequencies involves the use of smaller capacitors and inductors.

However, the inductance of the gate circuit and the voltage drop across the source inductance during switching both have an impact on the switching speed of a MOSFET. The limitations caused by the source inductance can be reduced drastically by selecting a transistor having a second source pin for the ground-side connection to the gate circuit [2]. For RF applications, there are power MOSFETs available, which have even four source pins arranged in such a way, that they form in combination with the ground layer coplanar waveguides for both the gate circuit and the load circuit [3]. For a stacked MOSFET switch equipped with these transistors and connected to a 50 Ohm transmission line in Blumlein configuration, repetitive switching of a voltage of up to 9.5 kV with a signal rise time of not more than 8 ns has been achieved [4].

However, although the inductance of the gate circuit can be kept rather small by the implementation of a proper circuit layout, there is still a considerable contribution to the circuit inductance due to the packaging of the devices.

The switching speed of commercially available MOSFETs can be increased by the use of a gate boosting technology. For a capacitively coupled gate-drive circuit, an additional capacitor is connected in series to the transistor’s gate terminal to reduce the total capacitance of the gate circuit resulting in an increased resonance frequency of the circuit and, hence, faster switching [5].

Figure 1 shows a simplified equivalent circuit of a capacitively coupled gate-drive circuit. The additional capacitor C_C is connected in series to the damping resistor R_D and the parasitic inductance L_P of the connecting leads to the effective gate capacitance C_G on the die inside the

device's package. The transfer function for this circuit is given in eq. 1. It describes a RLC series resonant circuit. According to eq. 2 its undamped resonance frequency ω_0 rises, if the value of the coupling capacitor C_C is decreased, resulting in faster charging of the gate capacitance C_G. However, the capacitors C_C and C_G form a capacitive voltage divider. To compensate for its effect on the gate voltage V_G and to obtain the nominal gate voltage $V_{G,nom}$ at the gate, the gate drive voltage V_{GD} needs to be selected according to eq. 3.

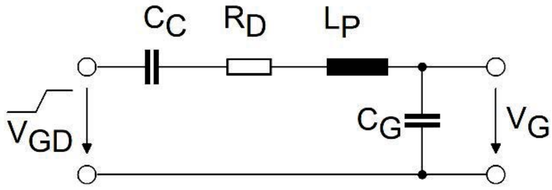

Fig. 1: Simplified equivalent circuit of a capacitively-coupled gate-drive circuit.

$$\frac{V_G}{V_{GD}} = \frac{\frac{1}{C_G \cdot s}}{R_D + \frac{1}{C_C \cdot s} + L_P + \frac{1}{C_G \cdot s}} \quad (1)$$

$$\omega_0 = \frac{1}{\sqrt{L_p \cdot \left(\frac{1}{C_G} + \frac{1}{C_C}\right)^{-1}}} \quad (2)$$

$$V_{GD} = \left(\frac{C_G}{C_C} + 1\right) \cdot V_{G,nom} \quad (3)$$

It should be noted that the gate charge and the related gate capacitance C_G are not constant but depend on the operating point of the MOSFET. An adaptation of the gate drive voltage might be desirable to compensate for this effect. Moreover, the effective coupling capacitance could be varied for fine-tuning of the switching time and to adapt the switching behavior to specific requirements.

In order to investigate the effect of gate-boosting on the switching speed of SiC-MOSFETs connected to a resistive load via an electrically short transmission line a test-setup has been designed and operated at selected operating points.

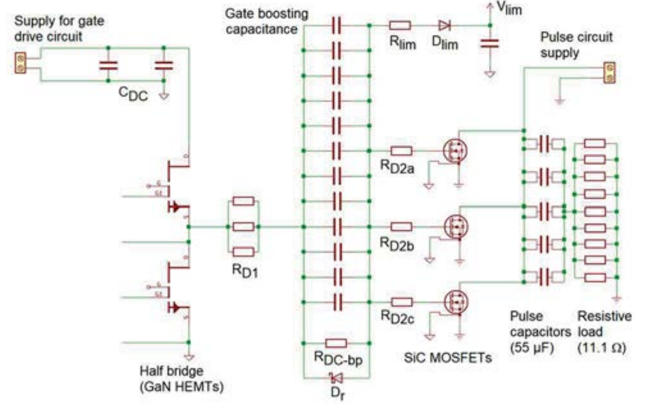

Fig. 2: Simplified circuit diagram.

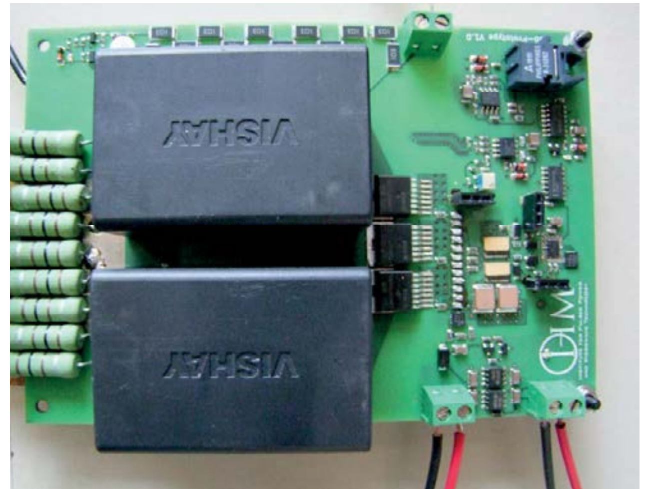

Fig. 3: Photo of the test setup.

2 Circuit Design

2.1 Load Circuit

Figure 2 shows a simplified diagram of the circuit and figure 3 a photo of the test setup.

The load circuit comprises three SiC MOSFETs of type C3M0075120J [2], which have a rated drain-source voltage of 1.2 kV and a rated drain current of 30 A each. Their package features a Kelvin source, i.e. a separate source terminal for connection to the gate circuit. A capacitor bank serves as energy storage for pulsed operation of the circuit. Its five separate capacitors have a total capacitance of 55 µF. The load impedance

consists of a parallel connection of nine resistors with a value of 100 Ohm each, resulting in a resistance of 11.1 Ohm. The ohmic load impedance has been selected such that the current through the load is limited to 90 A at an applied voltage of 1 kV. This selection has been made based on the rated current of 30 A per transistor. During operation, the capacitor bank is charged via a supply terminal by means of a capacitor charger.

As it is the goal of the experiments to demonstrate the effect of gate boosting on the switching performance of the device, for the test setup a low inductance of the pulse circuit is crucial. The components of the pulse circuit are placed onto a printed circuit board. The transistors' drain terminals and the ground-side terminals of the load resistor both are connected to a ground plane. The capacitor bank is placed between the transistors and the load. Hence, their length limits the minimum distance between transistors and load impedance. The terminals of the capacitors are connected to the transistors and to the load via two short microstrip lines, each having a length of approximately 15 mm. For the capacitor bank metallized polypropylene film capacitors have been used. The capacitor bank has been set up using two capacitors each with a capacitance of 20 μF placed onto the top side of the printed circuit board and additionally three smaller capacitors each having a capacitance of 5 μF, which are placed onto the opposite site of the printed circuit board. The stray inductance of the capacitors scales with their size and can be derived from the data sheet [6]. Each of the 20μF-capacitors has a stray inductance of 22.7 nH, and each 5μF-capacitors one of 15.9 nH. This results in a total inductance of 3.6 nH for the capacitors connected in parallel.

The distance between the transistors and the load is approximately 10 cm. In order to verify the assumption of an electrically short arrangement, the propagation delay of a signal along a microstrip line bridging this distance has been calculated. For a microstrip line with a length of 10 cm, a width of 4 cm, a distance between the conductors of 1.5 mm, and a relative permittivity of the board of 4.6, the propagation delay is 0.7 ns. Hence, for pulses with a rise time in the order of a few nanoseconds, wave propagation need not be considered. For the calculation of the inductance of the electrical connection between the components of the pulse circuit via the two microstrip lines and the ground plane beneath the pulse capacitors, this connection again has been considered as a microstrip line. For the above given geometry its inductance has been estimated to be 3.9 nH. In combination with the stray inductance of the capacitor bank and the resistive load the time constant of the load circuit $\tau = L/R$ can be estimated to be approximately 0.7 ns.

2.2 Gate-drive Circuit

The current required for driving the SiC MOSFETs has been estimated based on the total gate charge of approximately 48 nC required for switching under typical conditions according to the data sheet (V_{DS} = 800 V, I_D = 20 A, V_{GS} = -4V / 15V). To provide this charge for the three MOSFETs within approximately 5 ns a total driving current of approximately 30 A is required. So the peak current required for driving the gates during the fast switching process is in the same order as the load current per MOSFET. In order to source this current within the required short time, for the gate driver GaN enhancement mode HEMT power switches have been employed.

The gate driver comprises two GaN enhancement mode HEMT power switches of type GS66508T in a half-bridge configuration, each capable of switching 30 A at a rise time in the order of 4 ns [7]. They are driven by means of an integrated half-bridge driver (LMG1210, [8]), which has been implemented according to the manufacturers' application notes [9]. The half-bridge is powered by an external DC power supply connected to the supply terminal for the gate drive circuit. The supply voltage is buffered by means of two capacitors (C_{DC}) which are placed next to the half-bridge. The gate-boosting capacitance consists of a parallel connection of twelve separate SMD capacitors in order to keep the stray inductance of this arrangement low. Its value is selected in combination with the driving voltage such that the gate voltage of the SiC-MOSFETs does not exceed the rated voltage according to the data sheet.

For the experiments the values of the gate-boosting capacitance and the driving voltage will be varied to study the effect on the switching speed of the device and the signal rise-time at the load.

For the existing design, the maximum operating voltage of the integrated half bridge driver LMG1210 limits the supply voltage for the driver to 200 V [8]. For the experiments three different combinations of gate-boosting capacitance and driver voltage have been selected. In order to benchmark the performance of the circuit without gate-boosting, first, the driver will be operated at a voltage of 15 V with the gate-boosting capacitor shorted. For this experiment, 0-Ohm bridge elements have been soldered to the pads instead of capacitors. To demonstrate mild gate boosting, a gate-boosting capacitance of 6 nF has been selected, and for stronger gate-boosting a capacitance of 816 pF. For each gate boosting capacitance the driving voltage will be adjusted in the course of the experiment such, that a gate-voltage of around 15 V is achieved. The voltage is measured at the gate terminal of one SiC-MOSFET as soon as the signal has settled after the transient process of switching.

The resistor $R_{DC\text{-}bp}$ provides a DC bypass to compensate for a loss of gate charge due to leakage currents. This is especially important, if the transistors need to be kept switched on for a longer period. In this case, the series connection of R_{lim} and D_{lim} limits the DC voltage at the gate to a voltage of approximately 15 V. Thereby, the resistor R_{lim} allows for a larger transient voltage at the gate terminals of the transistors to compensate for the inductive voltage drop along the leads inside the package to the die. The Schottky diode D_r guarantees a low-impedant return path via the half-bridge to ground to keep the gate voltage of the blocking transistor safely near zero volts.

3 Measurement Results

3.1 Measurement System

For the measurements, the switch has been operated in single pulse mode. The gate voltage and the drain-source voltage at the SiC-MOSFETs together with the voltage at the load have been acquired using an oscilloscope with an analog bandwidth of 2 GHz. In order to be able to perform voltage measurements up to a voltage level of 1 kV, probes for a rated voltage of 4 kV have been employed. However, these probes have a bandwidth of 150 MHz only and, hence, limit the rise time of the measurement system. The rise time of a measurement system or device $t_{r,system}$ can be estimated based on the system's bandwidth B according to eq. 4 [10].

$$t_{r,system} = \frac{0.35}{\mathrm{B}} \tag{4}$$

The total rise time of a measurement system consisting of an oscilloscope and a probe can be estimated based on the rise times of its components according to eq. 5 [10].

$$t_{r,total} = \sqrt{{t_{r,1}}^2 + {t_{r,2}}^2 + \cdots} \tag{5}$$

The rise time of the employed measurement system has been estimated to be 2.34 ns.

As one goal of applying gate-boosting is fast switching, the rise times of the voltage across the load obtained for different configurations is of interest. The rise time of the pulses has been measured between 10% and 90% of the pulse amplitude.

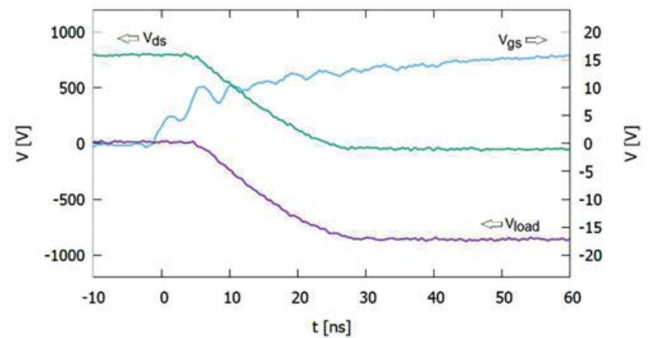

Fig. 4: V_{gs}, V_{ds}, and V_{load} while switching a voltage of 800 V without gate boosting.

3.2 Operation without Gate-boosting

Figure 4 shows the measurement results when operating the circuit with a driving voltage of 15 V and the gate-boosting capacitance shorted. The pulse capacitors have been charged to a voltage of 800 V resulting in a current of 72 A through a resistive load of 11.1 Ohm or 24 A per device

under the assumption of equal current distribution among the three SiC-MOSFETs. A rise time of 14.7 ns has been achieved. This result corresponds well to the rise time of 15 ns according to the data sheet obtained for one MOSFET under similar conditions. The operating point referred to in the data sheet is characterized by a gate-source voltage of 800 V and a drain current of 20 A with a voltage step rising fast from -4 V to 15 V applied to the transistor's gate without any additional external gate resistance. Thereby, only the transistor's internal gate resistance of 9 Ohm was effective.

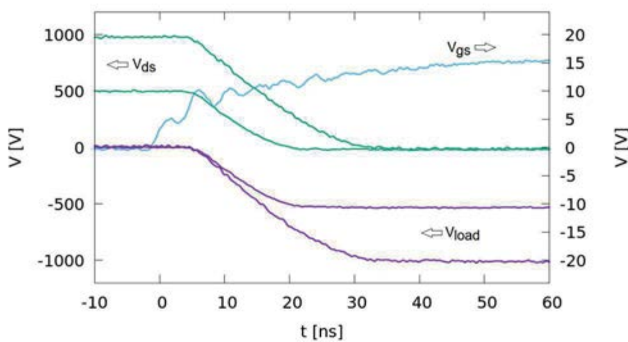

Fig. 5: V_{gs}, V_{ds}, and V_{load} without gate boosting, measured at 500 V and 1000 V charging voltage.

Fig. 5 shows a comparison of two sets of measurements acquired at charging voltages of the pulse capacitors of 500 V and 1000 V. For the voltage across the load rise times of 11.1 ns and 18.5 ns have been obtained, respectively.

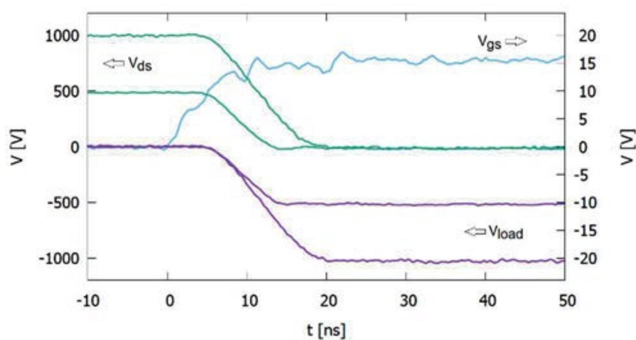

Fig. 6: V_{gs}, V_{ds}, and V_{load} with gate boosting (gate-boosting capacitance: 6 nF, driving voltage: 31.5 V).

3.3 Operation with Gate-boosting

For the measurements according figure 6 the gate driving voltage has been approximately doubled. For a gate-boosting capacitance of 6 nF a driving voltage of 31.5 V has been adjusted to obtain a gate-source voltage of 15 V. At 500 V and 1000 V charging voltage, the voltage across the load rises within 5.6 ns and 9.5 ns, respectively, which is approximately half the time obtained under usual gate drive conditions for both charging voltages.

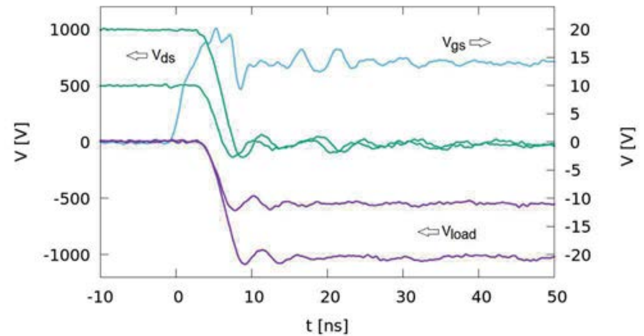

Fig. 7: V_{gs}, V_{ds}, and V_{load} with gate boosting (gate-boosting capacitance: 816 pF, driving voltage: 132 V).

Figure 7 shows the measurement results for a gate-boosting capacitance of 816 pF combined with a driving voltage of 132 V to obtain a voltage of approximately 15 V at the gate. This results in a further rise time reduction for the voltage across the load. From the measurements a rise time of 2.5 ns has been derived in the case of 500 V charging voltage and 3.5 ns for a charging voltage of 1000 V. However, these rise times are in the order of the rise time of the measurement system and, hence, represent an upper limit for the actual signal's rise time only.

Based on eq. 5 the signal rise time can be estimated to be 2.6 ns in the case of 1000 V charging voltage.

3.4 Comparison of Gate Signals

Fig. 8 shows a superposition of the gate signals acquired for the case of mild gate boosting with a gate-boosting capacitance of 6 nF and a driving voltage of 31.5 V for charging voltages of the capacitor bank between 100 V and 1000 V. The gate signals exhibit an overdamped approach towards their end value of around 15 V. During the switching process, some ringing is superimposed to the measurement. Fig. 9 shows the curves magnified after having settled to their end value. Fig. 10 shows the same, but for the case of stronger gate-boosting with a gate boosting

capacitance of 816 pF combined with a driving voltage of 132 V.

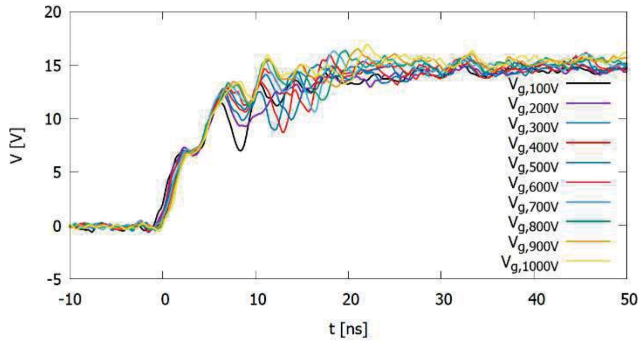

Fig. 8: V_{gs}, with gate boosting at different charging voltages ranging from 100 V to 1000 V (gate-boosting capacitance: 6 nF, driving voltage: 31.5 V).

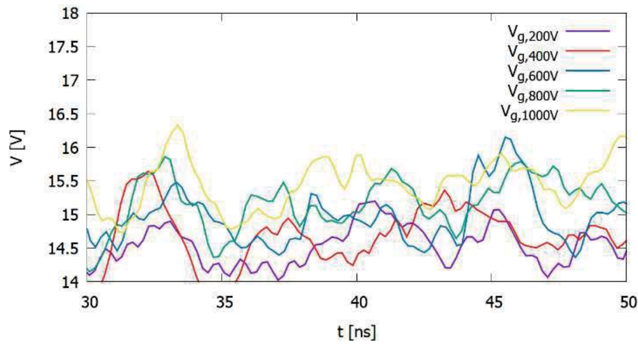

Fig. 9: V_{gs}, with gate boosting at different charging voltages ranging from 100 V to 1 kV after settling (gate-boosting capacitance: 6 nF, driving voltage: 31.5 V).

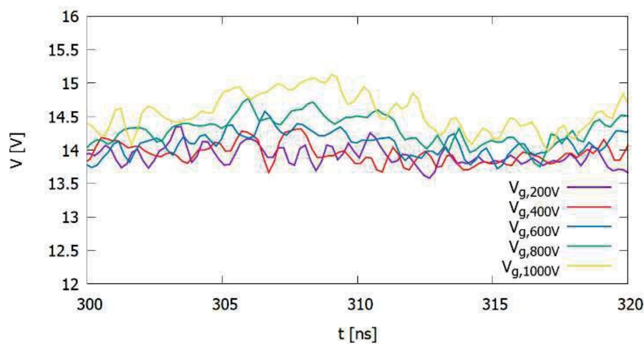

Fig. 10: V_{gs}, with gate boosting at different charging voltages ranging from 100 V to 1000 V after settling (gate-boosting capacitance: 816 pF, driving voltage: 132 V).

The measurements show, that after settling the gate signals vary for both cases by not more than 1 V. Hence, an adaptation of the driving voltage to the drain-source voltage of the MOSFET is for this setup not necessary. It should be noted, that in the latter case more ringing requiring a longer settling time disturbed the measurements of the gate voltage at higher charging voltage.

To demonstrate the effect of varying the driving voltage, the test setup has been operated at a driving voltage of 150 V, while the capacitance of the gate boosting capacitor has been kept at 816 pF. Fig. 11 shows two sets of measurements for charging voltages of the capacitor bank of 500 V and 1000 V.

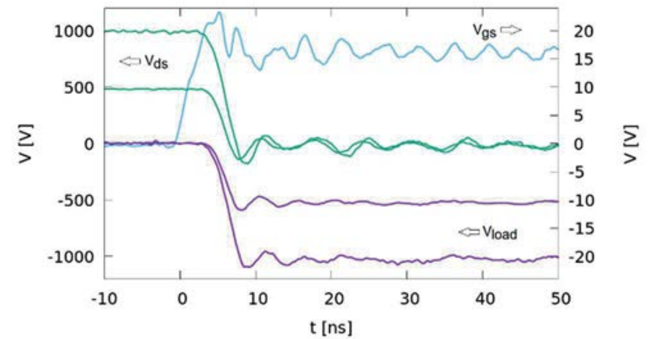

Fig. 11: V_{gs}, V_{ds}, and V_{load} with gate boosting (gate-boosting capacitance: 816 pF, driving voltage: 150 V).

The voltage across the load rises slightly faster than during the experiment with a driving voltage of 132 V. The measurements show for the voltage across the load rise times of 2.4 ns and 3.3 ns for 500 V and 1000 V charging voltage, respectively. The estimated signal rise time according to eq. 5 in the latter case is 2.3 ns.

The gate signal has a rise time of 3.3 ns according to the measurement. It exhibits an overshoot with a peak voltage of around 24 V and settles at a voltage of approximately 16 V.

4 Conclusion

A MOSFET switch comprising three SiC MOSFETs in parallel connection has been combined with a capacitively coupled gate-drive circuit capable of performing gate boosting operation. In order to source the required current to charge the gate capacitance within the required short time the gate driver features a half bridge

equipped with GaN enhancement mode HEMT power switches.

The switch has been operated in combination with a capacitor bank serving as voltage source and a resistive load impedance of 11.1 Ohm up to a voltage of 1000 V. With gate boosting at a driving voltage of 150 V and after charging the capacitor bank to a voltage of 1000 V the voltage across the load rises within 3.3 ns according to the measurement. For a charging voltage of 500 V a rise time of 2.4 ns has been measured. Thereby, an adaptation of the driving voltage to a varying operating voltage of the switch was not required.

5 References

[1] M. Sack, D. Herzog, M. Hochberg, W. Frey, G. Mueller: 8-Stage Pulse Generator for Bipolar Ground-Symmetric Operation, Proceedings of PCIM 2019, Nuremberg, Germany, 07.-09. May 2019.

[2] Cree: Datasheet C3M0075120J, Rev.B, 07-2019, online available at www.wolfspeed.com, retrieved 10/14/2020.

[3] IXYS RF: Datasheet for MOSFET 475-102N21A-00, Doc #9200-0247, Rev 6, 2009, online available at http://www.ixyscolorado.com/index.php/product-support/doc_download/77-475-102n21a-00-datasheet, retrieved 10/18/2012.

[4] M. Sack, M. Hochberg, G. Mueller: Setup and Testing of a Fast Stacked-MOSFET Switch, Proc. PPC 2013, San Francisco, USA, June 16-21, 2013, on DVD-ROM

[5] M. Hochberg, M. Sack, and G. Mueller: Simple Gate-boosting Circuit for Reduced Switching Losses in Single IGBT Devices, Proceedings of PCIM 2016, Nuremberg, Germany, 10.-12. May 2016.

[6] Vishay: Datasheet MKP1848C DC-Link, Metallized Polypropylene Film Capacitor DC-Link Capacitor, Document Number: 26015, Revision: 29-Sep-14, online available at www.vishay.com, retrieved 10/14/2020.

[7] GaN Systems: Datasheet GS66508T, Rev 180424, 2018, online available at gansystems.com, retrieved 10/14/2020.

[8] Texas Instruments: Datasheet LMG1210, online available at www.ti.com, retrieved 10/14/2020.

[9] GaN Systems: GN001 Application Guide, updated on FEB 28, 2018, online available at gansystems.com, retrieved 10/14/2020.

[10] A. Schwab: Hochspannungsmesstechnik, zweite Auflage, Springer Verlag Berlin Heidelberg New York, 1981.

Karlsruher Institut für Technologie

OPEN ACCESS

Repository KITopen

Dies ist ein Postprint/begutachtetes Manuskript.

Empfohlene Zitierung:

Sack, M.; Hochberg, M.; Herzog, D.; Mueller, G.
Fast sic-mosfet switch with gate boosting technology.
2021. PCIM Europe digital days 2021 : International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management Proceedings, 3 - 7 May 2021, VDE Verlag
doi: 10.5445/IR/1000139891

Zitierung der Originalveröffentlichung:

Sack, M.; Hochberg, M.; Herzog, D.; Mueller, G.
Fast sic-mosfet switch with gate boosting technology.
2021. PCIM Europe digital days 2021 : International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management Proceedings, 3 - 7 May 2021, 40–46, VDE Verlag

Lizenzinformationen: KITopen-Lizenz