Enhanced Current-Type P-HIL Interface Algorithm for Smart Transformers Testing

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***Abstract*—The energy systems are evolving towards the wide integration of power electronics-based technologies, such as electric vehicles. A promising solution to increase the grid controllability is represented by grid-forming converters, such as smart transformers (STs). Being a new technology, the ST experimental testing is a fundamental step before commercialization. Instead of performing time consuming and not flexible on-field tests, the Power Hardware In the Loop (P-HIL) offers a flexible testing environment for experimentally validating new technologies. The real time simulation of the electrical grid offers the possibility to vary quickly the testing environment, while the power amplification stage offers the validation of the real hardware. Despite the clear testing advantages, the P-HIL stability and testing accuracy is still a matter of study. This paper introduces a new P-HIL interface approach for ST application, that can guarantee high testing accuracy in a large frequency spectrum. The proposed approach combines the tracking capability of the existing controlled Current-Type P-HIL interface algorithm, with the well-known partial circuit duplication approach. The accuracy and stability analysis has been performed analytically and validated by means of extensive experimental P-HIL testing.**

***Index Terms*—Power hardware in the loop simulation, real-time simulation, P-HIL accuracy, P-HIL stability, smart transformer.**

I. Introduction

THE smart transformer (ST) is a power electronics-based medium voltage (MV) to low voltage (LV) transformer [1]. In addition to the voltage transformation and galvanic isolation services offered by conventional power transformers, the ST offers advanced services to the electrical distribution grid, such as MV and LV dc-connection, multi-frequency power transfer [2], on-line load control [3]–[5] and grid impedance estimation [1].

The smart transformer is an emerging technology, and thus its features are yet to be validated in a realistic environment. However, its implementation in the field may be risky in the first testing stages. Being the grid-forming unit for the downstream grid, any hardware fault can lead to a black-out for the connected loads.

For this reason, the Power Hardware In the Loop (P-HIL) evaluation [6], [7] offers an interesting approach to validate under realistic grid conditions energy technologies, such as energy storage systems [8], renewables, and new energy solutions, such as grid-forming converters like the ST.

In a generic P-HIL simulation like in Fig. 1, the device under test (DUT) is connected to a digital real-time simulator (DRTS) through a power interface, e.g. power amplifier (PA). This power interface "translate" a digital signal coming from the DRTS (e.g., a voltage or a current) in a power signal at the DUT hardware side. The type of signals and the way in which they are processed, is part of the so called interface algorithm (IA) [9]. As mentioned in the literature [10], the choice of the interface algorithm is fundamental in the accuracy and stability of the P-HIL experiments. In [11], [12] a controlled Current-Type (C-CT) P-HIL interface algorithm is proposed for ST applications, due to the grid-forming characteristics of the ST at the LV dc/ac stage. In those studies, although a first accuracy and stability assessment has been provided, the analysis is based on empirical evaluation, without any comprehensive accuracy and stability investigation.

In this paper, a systematic definition of the accuracy based on the concept of emulated real-time impedance at the point of common coupling (PCC), is given. The dichotomy between stability and accuracy in C-CT P-HIL simulations is mathematically proven and the limits of the different P-HIL algorithms in terms of accuracy are analyzed in the overall frequency spectrum. The C-CT and the partial circuit duplication (PCD) interface algorithm are analyzed in details, and an enhanced combination of both the approaches, namely C-CT with PCD, is proposed to increase the P-HIL accuracy in a wider range of frequencies. The emulated real-time impedance

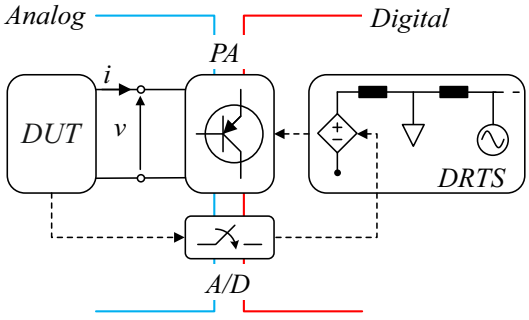

Fig. 1. Generic Power Hardware in the Loop scheme.

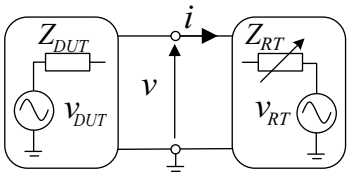

Fig. 2. Equivalent impedance model of P-HIL simulation.

approach is a powerful tool which can be used also to assess the stability of the P-HIL. In fact, the stability analysis of the ST connected to a P-HIL simulation has been carried out by using the impedance-based stability criteria [13], for the aforementioned interface algorithms.

The rest of the paper is organized as following: in Section II the definition of the accuracy in P-HIL simulations for power electronics is given, while in Section III the control structure and the output impedance of the ST are presented. In Section IV the three different interface algorithms for ST application are analyzed, and in Section V the stability analysis of P-HIL simulations with the impedance-based criteria is conduced in ST application. In Section VI, the analytical findings about the P-HIL accuracy are experimentally validated. Finally, Section VII concludes the paper.

II. Definition of Accuracy in P-HIL Simulations

A generic impedance model based representation of the P-HIL simulation can be derived as in Fig. 2. Z_{RT}represents the emulated real-time grid impedance, and it is defined as the transfer function between the voltage and the current at the simulated PCC, that includes the simulated grid, the interface algorithm, and the power amplifier contributions. In Fig. 2, Z_{RT} is represented as a variable impedance since it can change during normal operations, and its model depends on the chosen P-HIL interface algorithm, while the DUT is modeled as a voltage source v_{DUT} with in series an impedance Z_{DUT}.

$$Z^* = \frac{v^*}{i^*}, Z_{RT} = \frac{v}{i} \tag{1}$$

The accuracy of a P-HIL simulation in power electronics/system applications can be defined in terms of an error transfer function calculated as the ratio between the emulated Z_{RT} and the ideal impedance of the plant, Z^*.

$$err_{acc}(j\omega) = \frac{|Z_{RT}(j\omega)|}{|Z^*(j\omega)|} \frac{e^{\angle(Z_{RT}(j\omega))}}{e^{\angle(Z^*(j\omega))}} \tag{2}$$

An ideal P-HIL generates an equivalent impedance model which behaves like the naturally-coupled plant all over the relevant range of frequencies.

In the ST testing, the required P-HIL accuracy depends on the frequency range of the investigated power system phenomena. As an example, if the analysis is carried on at steady-state conditions, the P-HIL shall reproduce perfectly the naturally-coupled plant only at the grid frequency. In case

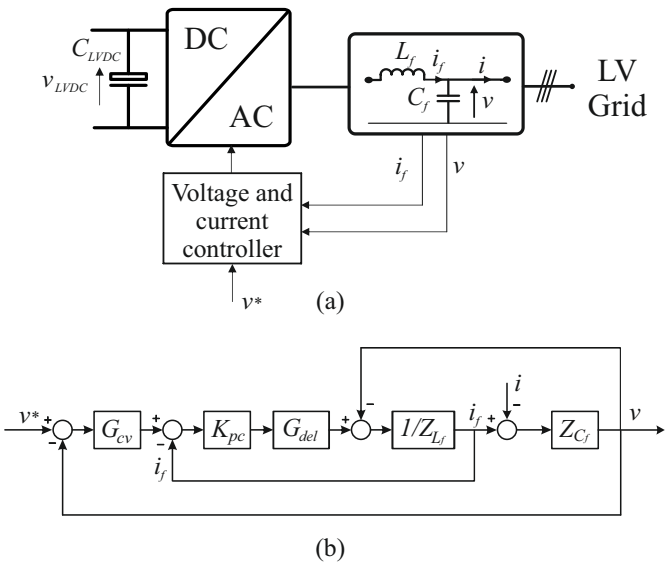

Fig. 3. ST control structure: (a) control scheme of LV converter, (b) block diagram of LV converter using double-loop control scheme.

of reverse power flow or voltage/frequency control in ST-fed distribution grid [4] the dynamics involved are in the low frequency range, accordingly a perfect accuracy of the P-HIL emulate grid is required in the range of $0 - 200Hz$. Another case is the impact of distributed generations (DGs) and nonlinear loads on the power quality of the voltage when comparing various ST voltage controllers [14]. In this case a perfect accuracy of the model at specific frequencies, typically from the 5^{th} until the 13^{th} harmonic $(650Hz)$, is required. The same considerations can be done when testing the ST for multi-frequency power transfer [2]. In stability analysis of ST connected to a LV-distribution grid, the frequency of interest are typically near the resonance frequency of the LC filter and a correct stability assessment requires accuracy until $3-4kHz$. For ST short circuit analysis, the frequencies below $1kHz$ must be accurately represented.

III. Output Impedance of the Smart Transformer LV dc/ac Converter

In this work, the DUT is represented by the ST LV dc/ac converter. Its main control objective is to provide three-phase sinusoidal waveform with constant amplitude and frequency to the LV grid regardless the load dynamics. To achieve this target, double-loop voltage control strategy as shown in Fig. 3(a) can be used since it is easy to implement and presents good steady-state as well as dynamic performance. The detailed control scheme of the LV control is shown in Fig. 3(b), where a voltage outer loop and an inner current loop are used. $\alpha\,\beta$ or abc-frame could be implemented in the control system of the LV converter. In both the cases, Proportional-Resonant (PR) controllers can be used for controlling sinusoidal signals in the outer loop. For the inner loop, a proportional controller is usually used to minimize the current error.

In its general definition the ST can be seen as a grid forming converter controlled to work as an ideal voltage source with a given amplitude and frequency, and with in series an impedance. In a micro-grid the ac voltage generated by grid-forming converter is used as reference for the grid-feeding converters. Based on the previous definition and with reference to the classical double-loop control structure in 3(b), the ST can be modeled in an equivalent Thevenin form:

$$v = \underbrace{H_v(s)\, v^*}_{v_{DUT}} + Z_{DUT}\, i \tag{3}$$

$H_v(s)$ is the closed-loop transfer function of the outer voltage loop, while Z_{DUT} is the ST output impedance:

$$H_v(s) = \frac{Z_{C_f} G_{cv} K_{pc} G_{del}}{Z_{L_f} + (K_{pc} G_{del}) + Z_{C_f}[1 + G_{cv} K_{pc} G_{del}]} \tag{4}$$

$$Z_{DUT} = \frac{Z_{C_f}[Z_{L_f} + K_{pc} G_{del}]}{Z_{L_f} + K_{pc} G_{del} + Z_{C_f}[1 + G_{cv} K_{pc} G_{del}]} \tag{5}$$

where Z_{L_f} and Z_{C_f} are the inductance and capacitance impedance of the LC filter, K_{pc} is the inner loop gain, G_{del} is the equivalent computational/PWM delay and G_{cv} is the voltage outer loop controller, implemented in $\alpha\,\beta$ or abc-frame with a PR integrator. The ST output impedance has an important role in the stability assessment of P-HIL interconnected systems as further analyzed in Section V.

IV. Interface Algorithms for ST Testing

In this section the controlled Current-Type, the PCD and the controlled Current-Type with PCD interface algorithms are schematically presented with block diagram representation, while their equivalent real-time impedance are analytically derived. Only single-phase systems are analyzed in this section for simplicity of representation without losing of generality. The overall interface algorithms and the derived analysis are also valid and can be extended to a three-phase system.

A. Controlled Current-Type Interface Algorithm

A graphical representation of the controlled Current-Type interface algorithm is given in Fig. 4. The DUT, represented as a controlled voltage source v_{DUT} with in series an impedance Z_{DUT}, regulates the voltage on the LV ac side of the converter. The voltage v measured at the PCC is sent to the DRTS, and here it is applied at the input of a simulated grid by means of an ideal voltage source, indicated with v_S. The current i_S demanded by the simulated grid is sampled in the DRTS and sent to the interface controller $G_{cc}(s)$. PR controllers are used for controlling sinusoidal signals in the current loop. Here the hardware current i_{CT} over the coupling inductor L_{PA} is controlled through the power amplifier voltage v_{PA}, closing the power loop. To derive the emulated real-time impedance in the controlled Current-Type scheme, the block diagram of the power loop interface from the DRTS side is represented in Fig. 5. The emulated real-time grid admittance in controlled Current-Type P-HIL simulation can be derived as following:

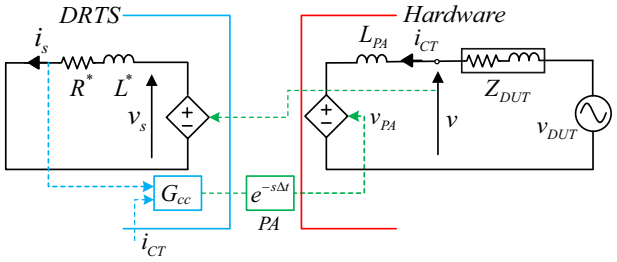

Fig. 4. Controlled Current-Type interface algorithm.

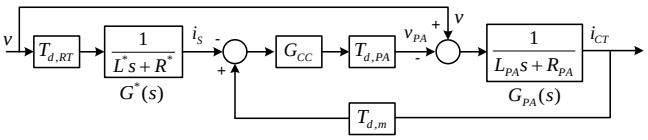

Fig. 5. Controlled Current-Type interface algorithm in the RTDS side.

$$i_{CT} = \frac{(G_{cc} T_{d,PA} G_{PA})\; i_s + G_{PA}\; v}{1 + G_{cc} T_{d,PA} G_{PA} T_{d,m}} \tag{6}$$

$$i_s = T_{d,RT} G^*\; v \tag{7}$$

where $T_{d,RT}$, $T_{d,PA}$, $T_{d,m}$ are the delays due to the DRTS sampling, the PA actuation and the current measurement respectively. Each delay has been represented with a first order Padé approximating transfer function as $T_{d,x}(s)$:

$$T_{d,x}(s) = \frac{2 - T_x s}{2 + T_x s} \tag{8}$$

where T_x is the generic x time delay, with $x \in [RT; PA; m]$. The current controller $G_{cc}(s)$ is a PR integrator expressed as:

$$G_{cc}(s) = K_{p,cc} + \frac{K_{r,cc} s}{s^2 + \omega_0^2} \tag{9}$$

where $K_{p,cc}$ and $K_{r,cc}$ are the proportional and resonant gain of the current controller respectively, while ω_0 is the nominal grid angular frequency. $G_{PA}(s)$ is the transfer function of an ac-filter used at the coupling point between the DUT and the power amplifier and it is expressed as:

$$G_{PA}(s) = \frac{1}{L_{PA} s + R_{PA}} \tag{10}$$

where L_{PA} and R_{PA} are the inductive and resistive part of the ac-filter respectively. The grid reference $G^*(s)$ is represented by a passive load expressed as:

$$G^*(s) = \frac{1}{L^* s + R^*} = \frac{1}{Z^*} \tag{11}$$

where L^* and R^* are the inductive and resistive part of the grid impedance respectively. Finally, the real-time grid model:

$$Y_{CT} = \frac{i_{CT}}{v} = \frac{G_{PA}(1 + G_{cc} T_{d,PA} G^* T_{d,RT})}{1 + G_{cc} T_{d,PA} G_{PA} T_{d,m}} \tag{12}$$

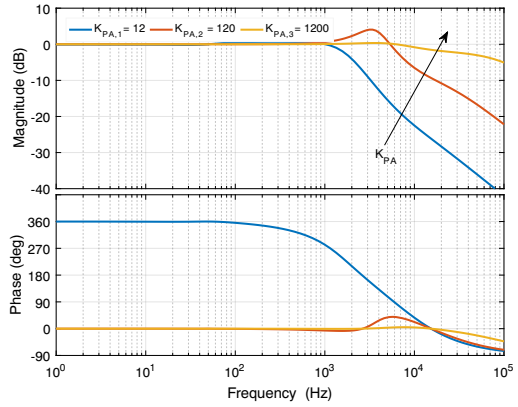

Fig. 6. Bode diagrams of the current closed-loop transfer function $H_{PA}(s)$ for different K_{PA} values.

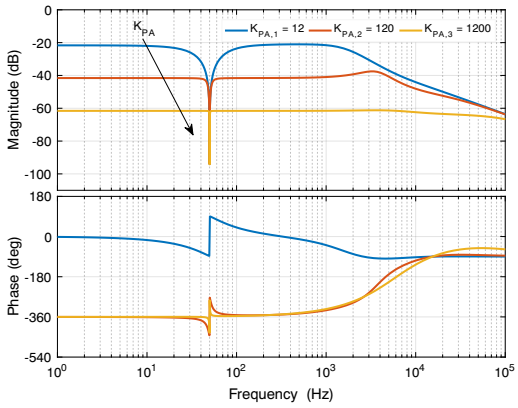

Fig. 7. Bode diagram of the Current-Type sensitivity function $S_{PA,v}(s)$ for different K_{PA} values.

From (12), two important considerations can be derived about the accuracy. Firstly, assuming that the DRTS sampling $T_{d,RT}(s)$ and the current measurement $T_{d,m}(s)$ are small and close each other, there is a condition for which the emulated real time impedance (admittance) is equal to the impedance (admittance) of the reference plan. This condition is a trivial solution and can be satisfied if $G_{PA}(s)$ is equal to $G^*(s)$. This solution is trivial because it would mean that the real plant can be simply in hardware implemented with the filter $G_{PA}(s)$ and all the benefit of the P-HIL concept are lost. Secondly, (12) can be decomposed into two parts:

$$Y_{CT} = \underbrace{\frac{G_{cc}T_{d,PA}G_{PA}T_{d,RT}}{1+G_{cc}T_{d,PA}G_{PA}T_{d,m}}}_{H_{PA}(s)} G^* + \underbrace{\frac{G_{PA}}{1+G_{cc}T_{d,PA}G_{PA}T_{d,m}}}_{S_{PA,v}(s)} \tag{13}$$

In (13), the first part is the closed-loop transfer function of the power amplifier current control $H_{PA}(s)$, which multiplies the ideal model of the plant $G^*(s)$, while the second part is the sensitivity transfer function $S_{PA,v}(s)$ which represents the capability of the loop to reject external disturbances on the actuation. The disturbance in this case is the voltage v at the PCC, while the actuating signal is the PA output voltage, v_{PA}. From (13) it is evident the interconnection between the emulated admittance (or impedance) and the closed-loop current control. Ideally, for the system to be accurate, the $H_{PA}(s)$ must have unitary magnitude gain and null phase across the overall spectrum, while $S_{PA,v}(s)$ must provide both null magnitude and phase contribution. Increasing the gain K_{PA}, the bandwidth of the current loop increases (Fig. 6) as well as the disturbance rejection capability (Fig. 7). As a consequence, while the error between Z^* and Z_{CT} is nullified, the stability of the current loop is not guaranteed for high values of K_{PA}.

Fig. 8 shows the emulated impedance in C-CT for different K_{PA} values. Only $Z_{CT,1}$ satisfies the stability requirements, with the consequence of a degraded accuracy in all the frequency range, except for the fundamental frequency, where the

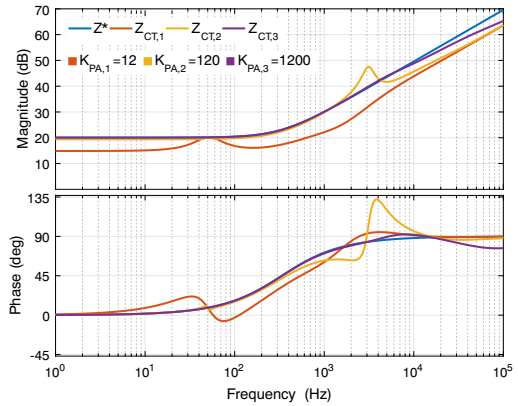

Fig. 8. Emulated controlled Current-Type impedance Z_{CT} for different K_{PA} values.

effect of the resonant controller can guarantee both a perfect tracking capability and a disturbance rejection at $50Hz$. The Current-Type impedance cannot emulate even at low frequency the reference impedance Z^*, with the drawback of an error in magnitude and phase of the corresponding current. In particular the impedance estimated is lower than the reference, this means that the P-HIL simulation current is higher than the current required by the naturally coupled system.

B. Partial Circuit Duplication

The partial circuit duplication takes its name from the partial replication of the hardware plant into the real-time simulation. Essentially, this algorithm aims to control the voltage at the terminal of the common filter L_{PA}, to ensure the same current flowing at both hardware and software sides. The PCD scheme requires a voltage controlled PA, as shown in Fig. 9.

In [10] the PCD is assessed to be stable while not accurate, but any accuracy index is given to support such statement and the evaluation is based on steady-state analysis at few frequencies. With the proposed definition of accuracy, based on the equivalent real-time impedance, it is possible to analysis how accurate is a simulation in the overall spectrum. To derive

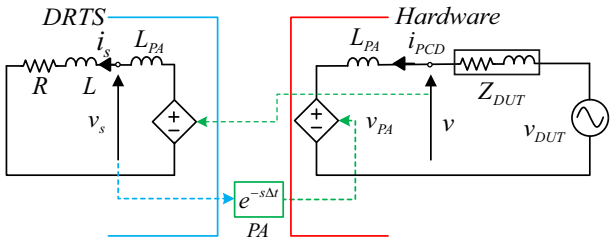

Fig. 9. Partial Circuit Duplication interface algorithm.

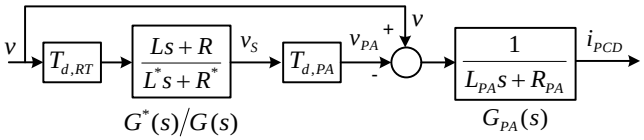

Fig. 10. Partial Circuit Duplication equivalent block diagram in the DRTS side.

the emulated real-time impedance in the PCD scheme, the block diagram of the power loop interface from the DRTS side is carried out as shown in Fig. 10. The emulated real-time grid admittance in PCD simulation is:

$$Y_{PCD} = \frac{i_{PCD}}{v} = G_{PA}\left(1 - \frac{T_{d,RT}T_{d,PA}}{G}G^*\right) \tag{14}$$

where $G^*(s)$ is the grid model, and it is assumed to be expressed as a generic $R-L$ plant, namely $G(s)$, with in series the power amplifier filter $G_{PA}(s)$, as follows:

$$G^*(s) = \frac{1}{L^*s+R^*} = \frac{1}{(L_{PA}+L)s+(R_{PA}+R)} \tag{15}$$

From this assumption is evident that $G_{PA}(s)$ is the hardware component which is partial replicated in the real-time simulation. The system presents a condition which satisfy the highest accuracy possible, when ideally $G_{PA}(s)$ is equal to $G^*(s)$. In all the other cases, the algorithm lacks of accuracy in the overall frequency spectrum, which makes the PCD not suitable even for steady-state analysis at the grid frequency, typical of power system studies (Fig. 11).

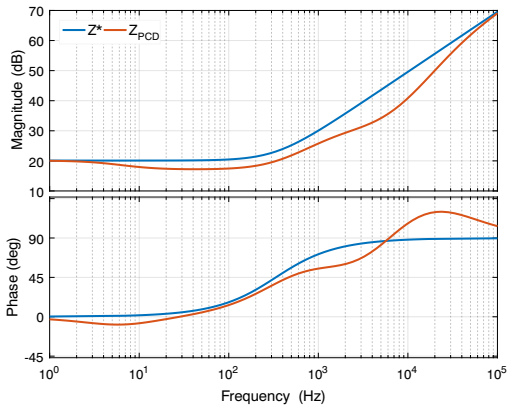

Fig. 11. Emulated Partial Circuit Duplication impedance Z_{PCD}.

C. Proposed Enhanced Current-Type Interface Algorithm

Both the analyzed P-HIL algorithms share two common elements: 1) the voltage measurement at the PCC, 2) they both require a voltage controlled PA to close the loop. In the C-CT the power amplifier voltage reference is the output of the current controller, while in the PCD it is voltage simulated across the terminal of the common filter. Combining the two approaches in a hybrid solution as shown in Fig. 12, the advantages of both the approaches can be obtained. The equivalent block diagram in the DRTS side is carried out as shown in Fig. 13, while the emulated real-time grid admittance in C-CT with PCD simulation is:

$$Y_{CT+PCD} = \frac{i_{CT+PCD}}{v} = \underbrace{\frac{G_{cc}T_{d,PA}G_{PA}T_{d,RT}}{1+G_{cc}T_{d,PA}G_{PA}T_{d,m}}}_{H_{PA}(s)}G^* + \\ + \underbrace{\frac{G_{PA}}{1+G_{cc}T_{d,PA}G_{PA}T_{d,m}}}_{S_{PA,v}(s)}\left(1 - \frac{T_{d,RT}T_{d,PA}}{G}G^*\right) \tag{16}$$

By analyzing (16), the output impedance is composed of the same closed-loop transfer function $H_{PA,v}(s)$ as in (13), while the sensitivity $S_{PA,v}(s)$ is down-scaled in the frequency by a multiplicative factor, represented by the PCD contribution. The PCD contribution can be interpreted as a feed-forward action which reshapes only the sensitivity component of the C-CT admittance in (13). In Fig. 14, by comparing the sensitivity of the C-CT $S_{CT}(s)$ with the proposed one $S_{CT+PCD}(s)$, it can be noticed that the feed-forward action of the PCD strongly reduces the sensitivity magnitude in the

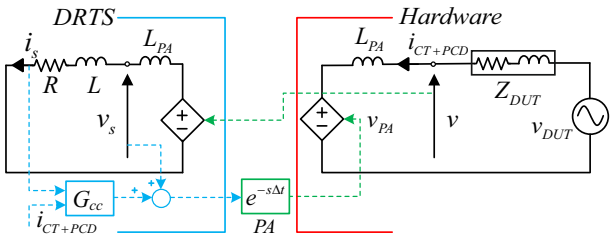

Fig. 12. Current-Type with Partial Circuit Duplication algorithm.

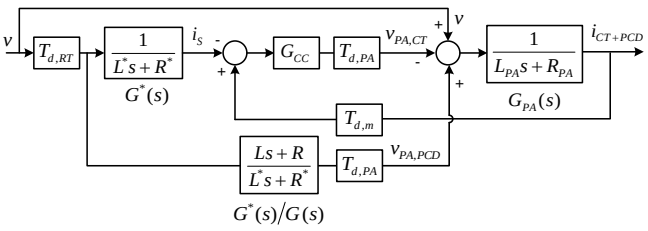

Fig. 13. Current-Type with PCD equivalent block diagram in the DRTS side.

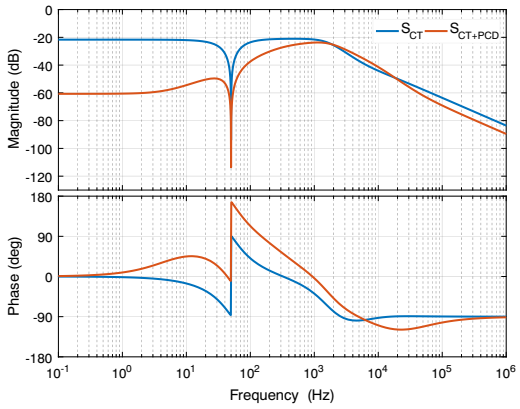

Fig. 14. Bode diagram of the Current-Type with PCD sensitivity function.

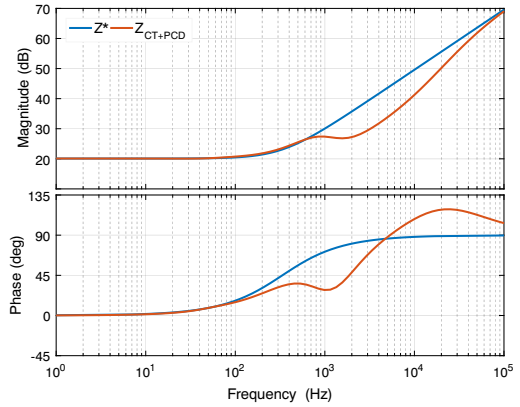

Fig. 15. Emulated Current-Type with PCD impedance Z_{CT+PCD}.

low frequency range from $[0Hz - 1kHz]$. The sensitivity at high frequencies remains instead unchanged. The proposed algorithm can provide at the same time high accuracy at low frequencies and perfect tracking at the fundamental frequency, if compared with the other approaches. The overall output impedance is shown in Fig. 15, where the emulated Current-Type with PCD impedance Z_{CT+PCD} is compared with the ideal Z^*. The proposed methods can track the magnitude of the reference model in the range of $[0Hz - 1kHz]$, making P-HIL real-simulations suitable for power quality and harmonic propagation analysis in ST-fed distribution grid [14].

V. Stability Analysis of P-HIL Simulation with Impedance-Based Criteria

With the DUT impedance, Z_{DUT}, as in (5) and with the equivalent grid impedance for each P-HIL interface algorithm as in (13)-(16), generically here indicated with Z_{RT}, the stability of such interconnected system can be studied by using the impedance-based stability criteria. Considering the linear model in Fig. 2, with $v_{RT} = 0$, the load current i flowing from the source to the load is:

$$i = \frac{v_{DUT}}{Z_{RT}} \cdot \frac{1}{(1 + Z_{DUT}/Z_{RT})} \tag{17}$$

For the stability analysis, it can be assumed that the voltage source v_{DUT} is stable when unloaded, i.e. $H_v(s)$ in (4) has no unstable poles, and the load is stable when powered from an ideal voltage source, i.e. Z_{RT} has no right-half plane zeros. Those assumptions are usually satisfied in grid connected applications, since the voltage source is always tuned to be internally stable and Z_{RT} is an equivalent impedance representation of a stable grid with P-HIL interface algorithms and delays. In our case, all the three equivalent analyzed impedance Z_{RT} are stable load with no right-half plane zeros.

If both the v_{DUT} and $1/Z_{RT}$ are stable, the stability of the current depends on the stability of the second term on the right-hand side of (17). The impedance-based stability criterion is based on the assertion that the stability of the interconnected system requires the ratio of the source impedance to the load impedance Z_{DUT}/Z_{RT} meet the Nyquist stability criterion [13]. Equivalently, the stability analysis can be conduced

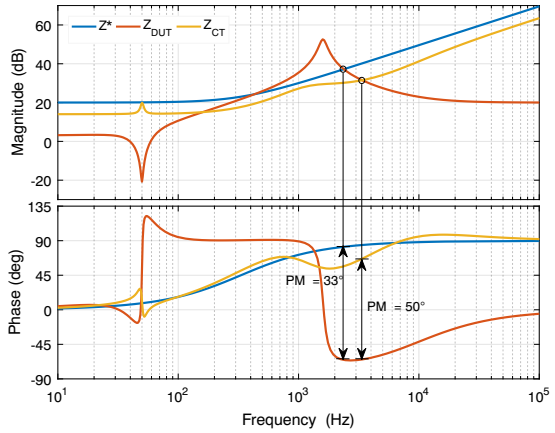

Fig. 16. C-CT impedance based-stability analysis: phase margin comparison between the ideal Z^* case (with Z^* the $PM^* = 33°$) versus the real Current-Type Z_{CT} impedance (with Z_{CT} the $PM = 50°$).

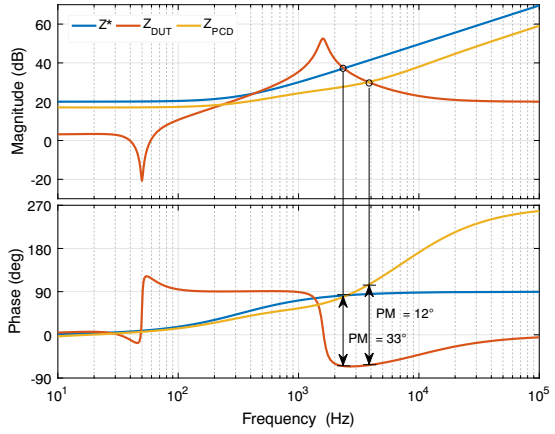

Fig. 17. PCD impedance based-stability analysis: phase margin comparison between the ideal Z^* case (with Z^* the $PM^* = 33°$) versus the real Partial Circuit Duplication Z_{PCD} impedance (with Z_{PCD} the $PM = 12°$).

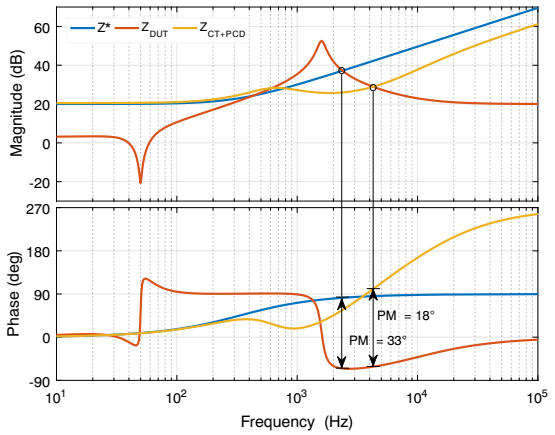

Fig. 18. C-CT with PCD impedance based-stability analysis: phase margin comparison between the ideal Z^* case (with Z^* the $PM^* = 33°$) versus the real Z_{CT+PCD} impedance (with Z_{CT+PCD} the $PM = 18°$).

by using the Bode diagrams of both the source and grid impedance. When the Z_{DUT} impedance intersects with the equivalent grid (load) impedance, the quantity calculated as $[180° - (\angle Z_{RT} - \angle Z_{DUT})]$ indicates the phase margin (PM) of the system. Figs. 16-18 indicate sufficient PM to guarantee the system stability in all the three analyzed cases. Each PM has been also compared with the ideal case of $PM^* = 33°$. From this comparison, the Partial Circuit Duplication underestimates the ideal PM, making the system prone to instability, while the Controlled Current-Type overestimates it. Controlled Current-Type with PCD is a good compromise.

VI. Experimental Results

Experimental tests in a laboratory environment have been performed in order to validate the results of the performed analysis. A picture of the P-HIL facility at the CAU in Kiel is shown in Fig. 19. A Danfoss Series FC-302 converter, with 4 kVA rated power, operating with a switching frequency of 10 kHz and equipped with an LC output filter is used as ST LV dc/ac converter. The converter is connected to a 4-quadrant linear power amplifier PAS 15000 from Spitzenberger-Spies (single phase rated power 15 kVA, total three phase rated power 45 kVA). The control algorithm of the ST is implemented in a dSPACE control Desk DS1202 MicroLabBox, whereas the grid model is simulated in real-time by means of a real-time digital simulator (RTDS). The overall system parameters specifications are given in Table I.

To assess the P-HIL accuracy, the equivalent impedance of the emulated grid needs to be derived. A measurement routine for P-HIL impedance estimation is implemented in the ST control scheme. A mono-frequency perturbing voltage with adjustable amplitude and frequency is generated at the ST output voltage in a range, from $50Hz$ to $3kHz$. The magnitude and phase of the 3-phase grid AC voltages and currents at the PCC are measured for each frequency, and the grid impedance is simply derived from its definition as voltage over current ratio. The frequency resolution of the

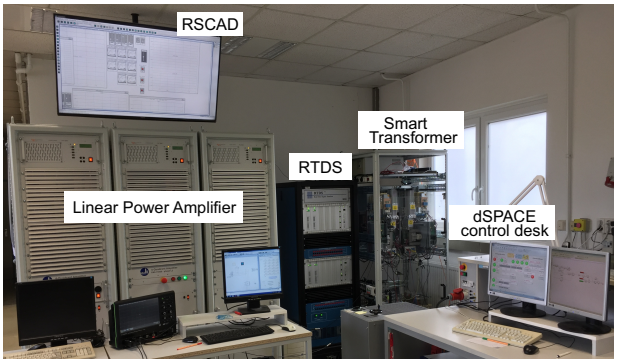

Fig. 19. P-HIL facility at the CAU Kiel.

TABLE I
Overall System Parameters

Parameters	Value
Converter Rated Power (P_{rated})	4 kW
DC-Link Voltage (v_{LVDC})	700 V
Nominal ac Voltage (v_n)	230 V_{rms}
Switching and Sampling Frequency (f_{sw})	10 kHz
Inductive Filter (R_f, L_f)	(0.016Ω, 5 mH)
Capacitive Filter (R_d, C_f)	(8Ω, 1.5 μF)
PA Inductive Filter (L_{PA})	2.4 mH
RTDS step time ($T_{d,RT}$)	50 μs
Grid Impedance (R^*, L^*)	(10Ω, 4.8 mH)

implemented method is equal to $50Hz$. The results of the grid impedance measurements are shown in Fig. 20. The PCD cannot accurately represent the plant at low frequencies and even at the fundamental frequency where the impedance mismatch results in an hardware current higher then the simulated one. The C-CT instead can accurately represents the plant at the fundamental frequency, while the proposed C-CT with PCD combines the accuracy at the fundamental frequency with a small impedance mismatch at low frequencies. The above findings are confirmed by comparing the hardware and the real-time simulation currents for each interface algorithms at $50Hz$ (Fig. 21) and at $350Hz$ (Fig, 22), with a grid $R^* = 10\Omega, L^* = 4.8mH$, and $v^* = 23V_{rms}$.

VII. Conclusions

The smart transformer is an emerging technology, and thus its features are yet to be validated in a realistic environment, however, its implementation in the field may be risky in the first testing stages. The P-HIL is a powerful tool for testing energy technologies, such as the ST, allowing realistic results and a flexible testing environment. Despite the advantages, the stability and accuracy of the validation is still object of study. This work proposed a new approach to estimate the accuracy of P-HIL experiments based on the concept of the equivalent grid impedance model. This modeling approach helps to characterize and to compare different P-HIL interface algorithms in the frequency domain. In particular, this paper

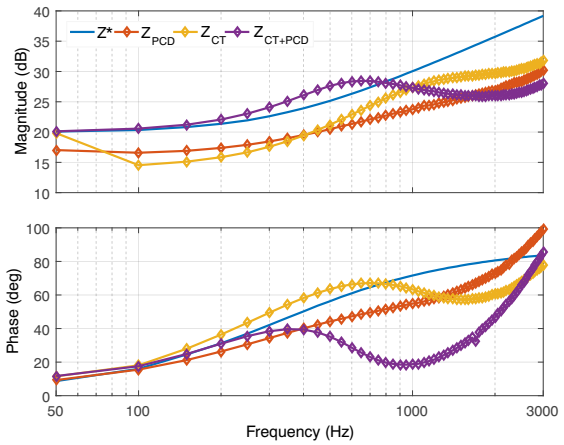

Fig. 20. Experimental P-HIL grid impedance measurements for C-CT, PCD and proposed C-CT with PCD interface algorithms.

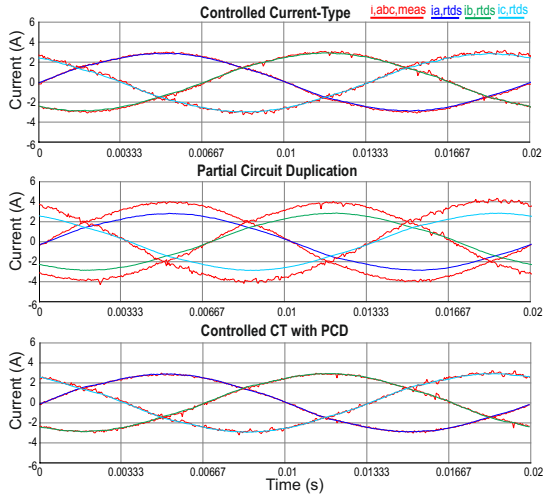

Fig. 21. Accuracy at 50Hz: measured vs simulated currents for all the three analyzed P-HIL interface algorithms.

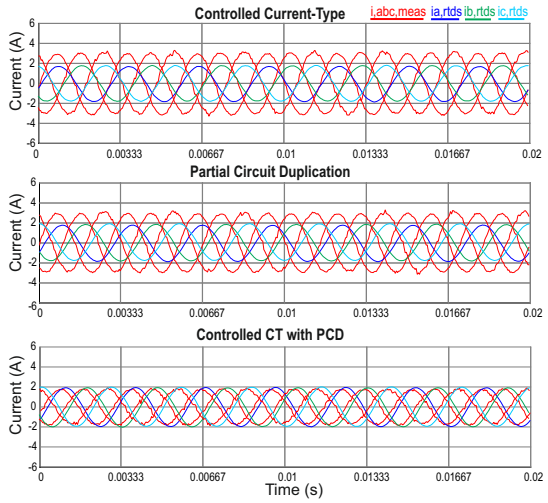

Fig. 22. Accuracy at 350Hz: measured vs simulated currents for all the three analyzed P-HIL interface algorithms..

introduces a new interface algorithm, the C-CT with PCD interface, that increases considerable the experimental accuracy in a wide range of frequencies, $[0Hz - 1kHz]$, if compared to the existing common PCD and current-controlled interfaces approaches. Furthermore, the effects of the different interface algorithms on the stability of the P-HIL simulations have been investigated by using the impedance-based stability criteria.

ACKNOWLEDGEMENT

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