Components and Systems Based on Printed Metal Oxide Electronics and Silicon Devices

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DISSERTATION

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M.Sc. Alexander Scholz
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Hauptreferentin:	Prof. Dr. rer. nat. Jasmin Aghassi-Hagmann
Korreferent:	Prof. Dr. Mehdi Baradaran Tahoori

Kurzfassung

Gedruckte Elektronik ermöglicht die Anfertigung elektrischer Bauteile und Systeme auf großflächigen, flexiblen Trägersubstraten. Des Weiteren wird durch berührungsfreie Druckverfahren, wie dem Tintenstrahldruck, eine flexible, dezentrale Fertigung elektronischer Bauteile und Systeme ermöglicht. Dies erlaubt unter anderem das Split-Manufacturing sicherheitskritischer elektronischer Komponenten, sowie eine größtmögliche Designfreiheit im Sinne von freien Formfaktoren und nicht standardisierter Strukturen mit unterschiedlichsten Abmessungen im Bereich von wenigen Mikrometern bis hin zu mehreren Millimetern.

Durch die genannten technologischen Aspekte bildet die gedruckte Elektronik einen interessanten Gegenpol zur klassischen hochintegrierbaren, miniaturisierten Silizium-Elektronik. Durch eine komplementäre Nutzung der Vorteile beider Technologien entstehen neuartige Synergien und Applikationen in Form von hybriden Systemen. Während hybride Lösungen, basierend auf passiven gedruckten Bauteilen und elektrisch leitfähigen Komponenten bereits kommerziell erhältlich sind, bleiben komplexe Systeme, die sowohl passive, als auch aktive, gedruckte elektronische Bauteile nutzen, noch selten. Um ganzheitliche, gedruckte sowie hybride elektronische Systeme zu ermöglichen, sind diverse Bausteine erforderlich. Hierzu zählen leichtgewichtige Möglichkeiten zur Datenspeicherung sowie Komponenten, die sich selbst mit Energie versorgende Systeme ermöglichen und insbesondere Schaltungen zur sicheren, eindeutigen Identifizierbarkeit ganzheitlicher, gedruckter Systeme für das Internet der Dinge.

Die hier vorliegende Arbeit befasst sich mit, durch Tintenstrahldruck hergestellten, elektronischen Bauteilen, Schaltkreisen, sowie hybriden Systemen. Es wurden Lösungen zu aktuellen wissenschaftlichen Fragestellungen in den Bereichen

effizienter gedruckter Speicherbausteine, nachhaltiger elektronischer Systeme, sowie der hardwarebasierten Sicherheit, auf Basis gedruckter Elektronik, erforscht und entwickelt.

Zur Datenspeicherung für gedruckte Systeme wurde ein, mittels Tintenstrahldruck hergestellter, Memristor entwickelt. Das Bauteil wurde vollumfänglich im Hinblick auf die Speicherung digitaler Information, charakterisiert. Die erzielten Ergebnisse zeigen, dass der Memristor als nichtflüchtiges Speicherelement genutzt werden kann.

Um ganzheitliche, nachhaltige elektronische Systeme zu ermöglichen wurde ein gedruckter Vollweggleichrichter entwickelt. Durch die Verwendung von Electrolyte-Gated Transistoren mit einer Schwellspannung von nahe-null Volt, ist die Schaltung in der Lage kleine Wechselspannungen, wie sie von piezoelektrischen Energy Harvestern erzeugt werden, gleichzurichten. Der, mittels Tintenstrahldruck hergestellte, Vollweggleichrichter wurde elektrisch vollumfänglich charakterisiert.

Zur Erzeugung einzigartiger Identifikationsmerkmale wurden zwei Implementierungenmöglichkeiten physikalisch unklonbarer Funktionen entwickelt. Dieser Ansatz nutzt die unvorhersehbare, intrinsische Variation gedruckter Bauteile als hardwarebasiertes Sicherheitsfeature. Eine untersuchte Implementierung basiert auf einer Crossbar-Anordnung integrierbarer Electrolyte-Gated Transistoren. Die zweite Implementierungsvariante nutzt Inverterstrukturen, ebenfalls auf Basis von Electrolyte-Gated Transistoren, zur Erzeugung der einzigartigen Systemantworten. Beide Varianten wurden sowohl mit Hilfe von elektrischen Simulationen, als auch experimentell untersucht. Die Inverter-basierte, intrinsische Variationsquelle wurde des Weiteren vollständig in ein Silizium-basiertes Gesamtsystem integriert und hinsichtlich ihrer Sicherheitsmetriken untersucht. Das Gesamtsystem bildet ein hybrides System, bestehend aus gedruckten Bauteilen sowie klassischer Silizium-Elektronik, zur Erzeugung einzigartiger Systemantworten.

Abstract

Printed electronics, due to its manufacturability using printing technology, allows for fabrication on large areas and the usage of flexible substrates and thus enables novel applications. Non-impact printing technology, such as inkjet-printing, permits for flexible, decentralized manufacturing of electronic devices and systems. This further facilitates split-manufacturing in security-critical electrical components, as well as a maximum in design flexibility in terms of free form factors and non-standardized structures with different geometrical sizes, reaching from a few micrometers up to several millimeters.

Based on the technological benefits printed electronics offers, it provides an interesting counterpart to classical silicon-based electronics, which is usually densely integrated on miniaturized, rigid areas. By utilizing both technologies in a complementary manner, novel systems in the form of hybrid systems can be enabled. Whilst hybrid systems, incorporating passive printed components and electrically conductive wiring concepts, are already commercialized, complex printed systems, which also utilize active components remain rare. To enable more complex (hybrid) systems, various building blocks are required. This includes possibilities for lightweight, printed data storage, the capability to provide sustainable, self-powered printed components and especially circuits for secure, unique identification for holistic printed systems, deployed in the internet of things.

The presented thesis focuses on inkjet-printed electronic devices, circuits and hybrid systems. It investigates solutions for current scientific questions in the area of efficient data storage, sustainable electronics and hardware-based security in printed electronics.

For data storage, an inkjet-printed memristor is developed. The device is fully electrically evaluated with a focus on its data storage capabilities. Furthermore, the printed device is of special interest due to its easy manufacturability and integration capabilities. The experimental analysis reveals that the developed memristor is highly suitable as lightweight non-volatile memory device.

In order to enable sustainable electronic systems, an inkjet-printed full-wave rectifier based on near-zero threshold voltage electrolyte-gated transistors is developed and fully electrically characterized. The circuit is capable for small alternating voltage rectification of low-frequency vibration energy harvesters in the sub-volt region. This provides an important building block in enabling sustainable, self-powered electronic systems. The inkjet-printed full-wave rectifier is evaluated by electrical simulation and experimentally.

To tackle hardware-based security for printed electronics, two implementations for inkjet-printed physically unclonable functions are developed and presented. For unique identification, intrinsic variation in active printed devices are exploited. One implementation is based on a crossbar architecture, incorporating integrable electrolyte-gated transistor cells. The second implementation, the so-called differential circuit physically unclonable function, is based on inverter structures, which provide the basis for unique response generation. Both physically unclonable functions are evaluated using an electrical simulation-based approach and experimentally. The differential circuit approach is furthermore fully integrated within a silicon-based electronic platform environment and serves as intrinsic variation source in a hybrid system. The hybrid system physically unclonable function is fully verified regarding performance metrics and is capable to generate highly unique responses for secure identification.

Preface

First, I would like to thank Prof. Jasmin Aghassi-Hagmann, as my main supervisor, for providing me the opportunity in pursuing this thesis. This includes numerous scientific discussions, encouragement in presenting the obtained results, up to funding acquisition and in improving my overall scientific skill set. Also, thanks to Prof. Mehdi Tahoori for all scientific discussions and valuable feedback, which helped in improving my scientific skill set as well and for being the second examiner of this thesis. I would also like to thank Prof. Uli Lemmer and Prof. Axel Sikora for valuable scientific feedback.
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Contents

Abbreviations

AC	Alternating Current
ADC	Analog-to-Digital Converter
Ag	Silver
Au	Gold
BA	Bit Aliasing
BE	Bit Error
BU	Buffer Amplifier
CC	Compliance Current
CMOS	Complementary Metal-Oxide-Semiconductor
CNT	Carbon Nanotube
CPU	Central Processing Unit
CR	Chromium
CRP	Challenge-Response Pair
CSPE	Composite Solid Polymer Electrolyte
DAC	Digital-to-Analog Converter
DC	Direct Current
DEMUX	Demultiplexer

DiffC	Differential Circuit
DoD	Drop-on-Demand
DPI	Dots Per Inch
ECM	Electrochemical Metallization Memory
EDL	Electrical Double Layer
EGFET	Electrolyte-Gated Field-Effect Transistor
EGT	Electrolyte-Gated Transistor
EKV	Enz-Krummenacher-Vittoz
FF	Form Factor
FHD	Fractional Hamming Distance
FHE	Flexible Hybrid Electronics
FIB	Focused Ion Beam
$\mathbf{H_2InN_3O_{10}}$	Indium (III) Nitrate Hydrate
HD	Hamming Distance
HRS	High-Resistance State
I/O	Input-/Output
$\mathbf{I-V}$	Current-Voltage
IC	Integrated Circuit
$\mathbf{In_2O_3}$	Indium Oxide
IoT	Internet-of-Things
ITO	Indium Tin Oxide

LAE Large-Area Electronics

LP Low-Pass

LRS Low-Resistance State

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor

MUX Multiplexer

NL Noise Level

OE Organic Electronics

OFET Organic Field-Effect Transistor

OLED Organic Light-Emitting Diode

OTFT Organic Thin-Film Transistor

PC Personal Computer

PCB Printed Circuit Board

PCE Power Conversion Efficiency

PE Printed Electronics

PEDOT : PSS
Poly(3,4ethylenedioxythiophene):Poly(styrenesulfonate)

PEN Polyethylene Naphthalate

PET Polyethylene Terephthalate

PUF Physically Unclonable Function

PVA Polyvinyl Alcohol

RFID Radio Frequency Identification

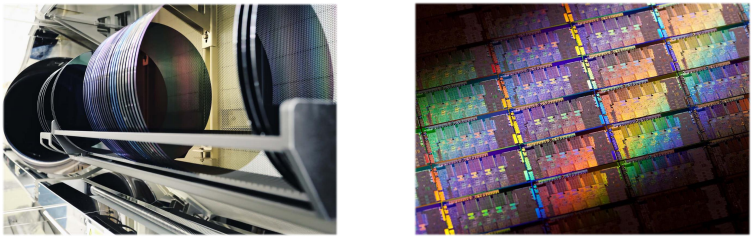
RH Relative Humidity

RMS	Root Mean Square
RS	Resistive Switching
RtR	Roll-to-Roll
SCLC	Space-Charge Limited Current
SCPI	Standard Commands for Programmable Instruments
SEI	Semiconductor Electrolyte Interface
SEM	Scanning Electron Microscopy
Si	Silicon
TFT	Thin-Film Transistor
TGEI	Top-Gate Electrolyte Interface
VCM	Valence Change Memory
VCR	Voltage Conversion Ratio
$\mathbf{Zn(NO_3)_2 \cdot 6H_2O}$	Zinc Nitrate Hexahydrate
ZnO	Zinc Oxide
µC	Microcontroller

1 Introduction

The rapid development in densely integrated semiconductor devices forms the backbone of a modern, digitized society. Integrated circuits (ICs), based on monocrystalline silicon (Si), provide the basis for communication, data processing and digital information exchange in general. With state of the art central processing units (CPUs) exhibiting several billions of transistors on square millimeter sized areas. Production of ICs is done in globally distributed foundries. However, foundries supporting current technology nodes, are scarce. This is mainly reasoned by the intense cost in establishing a modern foundry, exhibiting several billions of dollars, in combination with the required infrastructure for energy, water, gas and waste management.
While IC integration densities on miniaturized areas are unmatched, combined with production in large quantities, initial costs in IC designs, customization and redesigns are expensive. This leads to centralized production, in combination with low customization possibilities due to the enormous cost barriers faced in production. Figure 1.1 shows examples for Si-based electronics, from wafer to IC, in the form of a microprocessor architecture.

In 1977, scientists report on electrical conductivity in polymers by doping of polyacetylene [1]. On the long term, this discovery enabled novel research and business areas based on organic electronics (OE). Reasons for the increased interest in OE is in reduction of processing complexity, compared to conventional manufacturing methods, as well the possibility for fabrication on large areas and flexible substrates at low processing temperatures. Furthermore, OE allows for so-called "green" electronics utilizing bio-compatible materials [2]. Popular examples for organic electronics are organic light-emitting diodes (OLEDs), which



(a) **(b)**

Figure 1.1: Exemplary images for Si-based electronics from wafer to IC. **(a)** Multiple bare silicon wafers. Source: Infineon Technologies. **(b)** ICs in the form of an Intel "Sandy Bridge" microprocessor architecture, based on 32 nm technology node, on processed wafer. Source: Intel Free Press, reproduced under CC BY-SA 2.0 license, https://creativecommons.org/licenses/by-sa/2.0/.

are successfully commercialized in display technology mainly using evaporation techniques, currently still at high temperatures and rigid substrates [3, 4]. However, transparent, flexible large-area OLED displays are already successfully demonstrated [5].

To further enable large-area electronics (LAE) on flexible substrates for low-cost electronics, the idea of using printing technology to process organic and inorganic materials to build electronic devices from a liquid phase emerged [6–9]. With various printing technologies at disposal, different needs can be addressed. Roll-to-roll (RtR) printing solutions are capable for high-throughput fabrication over large areas, whilst non-impact printing technologies, such as inkjet-printing, offer decentralized manufacturing with highly dynamic design customization of the print product. This makes inkjet-printing an interesting and disruptive manufacturing technology in the era of the internet-of-things (IoT) and fourth industrial revolution.

Due to the immense application potential of PE and persistent shortcomings in realizing complex, fully printed systems, such as reduced performance in active devices and performance reliability in general, interest in flexible hybrid electronics (FHE) increased [14–17]. By merging both technologies benefits, classical

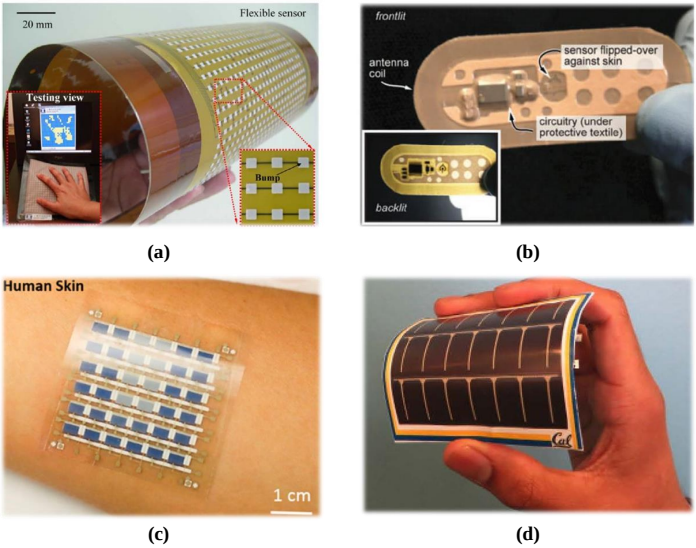


Figure 1.2: Examples for PE-based electronics and hybrid systems. **(a)** Screen-printed sensor array for large-area sensing on flexible substrates [10], © 2009 IEEE. **(b)** Flexible, adhesive RFID patch for sweat electrolyte detection. The patch also incorporates Si-based electronics for signal processing and communication [11], © 2014 IEEE. **(c)** Screen-printed active matrix electrochromic display on flexible substrate. Reprinted with permission from [12], © 2016 American Chemical Society. **(d)** Flexible solar cell combined with battery. The battery electrodes are printed [13]. Reproduced under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

Si-based electronics, as well as PE, novel systems in the form of hybrid systems can be designed. With the already mentioned unmatched integration capabilities and device speed, Si-based electronics provides the backbone for high-speed, wireless communication and control, whilst PE enables for additive, large-area manufacturing on flexible substrates [15–20]. Possible application scenarios are in large-area sensing, healthcare, smart packaging and logistics. Examples for PE-based electronics and hybrid systems can be seen in Figure 1.2. In order to realize high-performance flexible hybrid systems, thinned Si-based ICs can be incorporated into the flexible substrate [21, 22].

Initially, the term LAE was used and enabled by hydrogenated amorphous silicon (*a*-Si:H)-based thin-film-transistor (TFT) technology [23–25], which allows fabrication on large areas. The need for LAE arise from emerging display technology, where TFTs were - and still are - used as control elements in active matrix configurations [26–28]. With increasing demand in higher performance TFTs for active matrix displays utilizing the aforementioned OLEDs, semiconducting metal oxides, such as zinc oxide and indium-gallium-zinc oxide, gained attention [29–32].
Conventional fabrication of LAE, utilizing TFTs on both, rigid [33,34] and flexible substrates [31,35–38] is possible using evaporation, sputtering and various deposition methods, such as plasma-enhanced chemical vapor deposition [39]. Due to reduced device performance of TFTs, hybrid systems are proposed [37,40,41]. A combination of Si-based electronics as signal conditioning backend and a LAE TFT-based frontend offers a hybrid approach, harvesting both technologies benefits in a complementary manner. Besides the large-area manufacturability, cost per transistor is massively increased in conventionally manufactured TFT technology, in comparison to the densely integrated transistors in ICs [28], due to the increased feature size of a TFT.

Solution processing and printing of inorganic semiconductors in the form of silicon [42, 43], as well as oxide semiconducting materials over a wide variety is possible [44–47]. However, TFT-based LAE with solution-processed, or printed devices, in combination with Si-based electronics, to enable holistic hybrid systems, remain scarce. Nonetheless, LAE in the form of printed structures (strain, force, temperature), without active devices, are broadly reported [48–51].

PE-based electronics, may it be organic, inorganic, (semi)-conducting materials, passive or active devices, fabricated on small or large areas, utilizing rigid and flexible substrates, offers a broad field of novel applications. This highlights the importance of a holistic development approach for promising PE-based devices, circuits and hybrid systems in order to shape and enable the future of electronics, which will increasingly impact our everyday life.
In this work, inkjet-printed electronic devices, circuits and hybrid systems are investigated.

1.1 Structure of the Thesis

In the following, the structure of the thesis, which incorporates inkjet-printed electronic devices, circuits and hybrid systems, is listed.

- Chapter 2 introduces fabrication and structuring methods for thin-film devices. This includes printing technologies for printed electronics with a focus on drop-on-demand piezo-inkjet printing. The general working principle of laser ablation, for solid material structuring, is discussed.
  In the following, an introduction to printed transistors is given. A focus is on inkjet-printed electrolyte-gated transistors (EGTs). The chapter concludes with the description of state of the art printed circuits.

- Chapter 3 presents new design and hardware concepts in printed electronics. This includes sustainable energy, new paradigms in computing and hardware-based security. For sustainable energy, a focus is on processing of low-voltage, low-frequency systems harvesting environmental energy. Furthermore, novel paradigms in computing are introduced with a focus on memristors, which have shown great potential as memory devices and as general building blocks in Beyond-von-Neumann computing and neural networks. Hardware-based security introduces the concepts of physically unclonable functions, which can be used for the creation of a device specific fingerprint.

- Chapter 4 shows the fabrication routine for inkjet-printed, top-gate bottom-contact EGTs on lasered substrates, which are used for all further investigated circuits and hybrid systems.
  Furthermore, inkjet-printed memristors, which show great potential as (non-volatile) memory devices are investigated. The devices are fully electrically characterized and switching characteristics are reported. Furthermore, statistical analysis regarding cycle-to-cycle and device-to-device variability is presented and an investigation regarding the device's conduction mechanism is made.

- Chapter 5 presents the results for novel inkjet-printed circuits, based on EGTs. This incorporates an inkjet-printed full-wave rectifier for low alternating voltage rectification and a full electrical characterization of the circuit.
  Furthermore, two inkjet-printed physically unclonable functions are designed and investigated, using electrical simulation. A focus is on the printed PUF core intrinsic and systematic variation. Moreover, emulated Si-based control logic systematic variation is incorporated for holistic PUF metric investigation of the proposed printed PUFs. For both PUF implementation, the printed PUF cores are fabricated and electrically evaluated.

- Chapter 6 shows the obtained experimental results for the embedded differential circuit (DiffC)-PUF as hybrid system platform, incorporating a printed DiffC-PUF core and a Si-based control logic. For reference design in a first step, a Si-based DiffC-PUF core is fully evaluated for commissioning of the platform. It shows that the Si-based PUF core allows for extremely reliable, unique key generation, which can be utilized for integration of PUF schemes in software-communication layers.
  Finally, a PE-based DiffC-PUF core is integrated within the system and fully investigated, with respect to voltage levels and PUF performance metrics. The PE-based PUF is capable to generate unique responses and is highly suitable for fingerprinting.

- Chapter 7 summarizes the results obtained in this thesis and highlights possible future investigation scenarios.

2 Background & State of the Art

In this chapter, methods for TFT fabrication and device structuring, as they are used for this work, are discussed. An overview of popular printing technologies for PE is given. The main focus regarding printing technologies is on drop-on-demand piezo-inkjet printing. Also, solid material structuring via laser ablation is introduced. Thin-film transistors based on printable organic and inorganic semiconducting materials are shown, with special focus on low-voltage electrolyte-gated transistors. A brief overview about state of the art, advanced printed circuits with emphasis on digital and analog circuit building blocks are given.

2.1 Fabrication Processes & Structuring of Thin-Film Devices

2.1.1 Conventional Printing Technologies for Printed Electronics

Printing techniques, requiring a printing form, are labeled as conventional printing processes. The printing form, which holds the desired design, is used to transfer the print material onto the carrier substrate [7, 52]. Changes in the design require a change in the print form. Popular conventional printing technologies for PE are gravure-, flexo-, screen- as well as offset- printing [7, 53]. The mentioned printing technologies offer roll-to-roll compatibility and allow for high throughput printing. Primary differences are in various processing parameters, including

Figure 2.1: Pilot printing line "Gallus RCS 330", using conventional printing methods for PE. Source: Innovationlab GmbH.

printing resolution, throughput, mechanical complexity as well as requirements regarding processable fluids, to name but a few.

Due to possible multi-modal requirements for PE-based applications, printing technologies can be used either standalone or as combined systems. Figure 2.1 shows partially a pilot printing line utilized for PE, based on conventional, RtR printing technology. Next to the printing elements, modules for substrate and fluid treatment, such as heating elements or systems for removal of electrostatic charge [54] need to be deployed.

In Table 2.1, several core performance parameters of above mentioned conventional printing methods for PE are compared.

Table 2.1: Comparison between several conventional printing technologies for PE, adapted from [7]. The absence of a parameter is denoted by (/).

Printing technology	**Print resolution** (µm)	**Print speed** ($m \cdot min^{-1}$)	**Fluid surface tension** ($mN \cdot m^{-1}$)	**Fluid viscosity** (Pa·s)
Gravure	50 - 200	8 - 100	41 - 44	0.01 - 1.1
Flexographic	30 - 80	5 - 180	13.9 - 23	0.01 - 0.5
Screen	30 - 100	0.6 - 100	38 - 47	0.5 - 5
Offset	20 - 50	0.6 - 15	/	2 - 5

2.1.2 Drop-on-Demand Piezo-Inkjet Printing for Printed Electronics

Drop-on-demand (DoD) piezo-inkjet is a non-impact printing technology. To realize a print-design, no physical print form is required. Layouts can be fully adapted in software and transferred from a personal computer (PC) to the machine in form of a digital picture matrix.

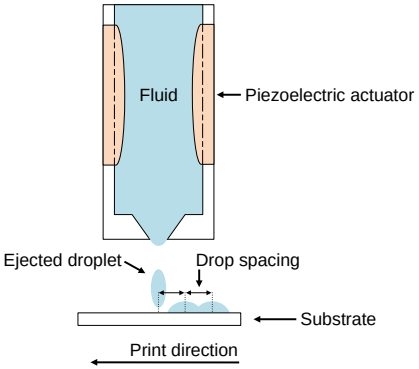


Figure 2.2: Schematic for a DoD piezo-inkjet printhead ejecting a droplet on a carrier substrate within a defined drop spacing.

In piezo-inkjet printing, the fluid is ejected from the printer nozzle, due to a volume change in the fluid reservoir of the printhead, onto the desired substrate area [52], as visualized in Figure 2.2. This is enabled through to a voltage-controlled, mechanical actuation of a piezoelectric transducer [55], within the printhead. Typical jetting frequencies are in the range of $1\,\mathrm{kHz} - 20\,\mathrm{kHz}$ [55, 56]. With droplet volumes in the picoliter range, in combination with precise, on-demand droplet ejection, DoD piezo-inkjet printing allows for fabrication at a minimum material usage and thus reduced material waste.

Requirements for inkjet-printable fluids are high. Viscosity, surface tension, density, size of polymers, molecular weight and particle size in general, to name

but a few, impact inkjet-printing behavior [57–60]. Inkjet-printability and droplet formation of fluids can be estimated with the dimensionless, inverse Ohnesorge number *Z*, as shown in Equation 2.1. With *Re* being the Reynolds and *We* the Weber number [55].

$$Z = \frac{Re}{\sqrt{We}} \tag{2.1}$$

Values for *Z* between $1 < Z < 10$ show proper inkjet-printing behavior of fluids, according to Reis and Derby [56]. Jang et al. [60] report on *Z* values ranging from $4 \leq Z \leq 14$, for optimal inkjet-printing behavior of certain fluids, processed with piezo-inkjet printers.

Drop-on-demand piezo-inkjet printer offer various options for printhead parameter configuration, which allows to adapt for different fluids. This includes jetting frequency, dedicated pulse waveform settings, applied voltage level on the piezoelectric actuator, static pressure level and fluid reservoir temperature. Usually, a heatable vacuum plate for substrate placement is employed. This is required to control pinning of the fluid on substrate surface impact. Surface impact effects, based on ejected droplet speed, in combination with pinning of the fluid on the substrate, are further important points in DoD piezo-inkjet printing, when high resolution print results are required. The print resolution, for digital printing technologies, is given as dots per inch (DPI). Commercially available inkjet-printers, for research and development, such as the Fujifilm Dimatix DMP series provide print resolutions up to 5080 DPI. This allows for $5\,\mu\mathrm{m}$-spaced droplet ejection, also referred to as drop spacing.

2.1.3 Laser Ablation

Laser ablation enables non-contact structuring of solid materials. This is achieved by high optical irradiation intensities with a strongly focused laser beam on a solid material, which leads to material removal [61–63]. The ablation process is achieved above a threshold fluence, which is heavily influenced by a material's

absorption characteristics, laser pulse duration and laser wavelength [61–63]. For high quality machining of solid materials with high thermal diffusivity, fast laser pulses (ps to fs) are required [64]. Simplified, when the laser pulse duration is longer then the material's heat diffusion time, the material is vaporized due to predominantly thermal interaction [65, 66], which can result in ejected blobs of melted material and surface shock, which also can lead to damage of material in the heated zone [66]. However, the fluence heavily influences the pre-dominantly laser-/material interaction [62, 63].

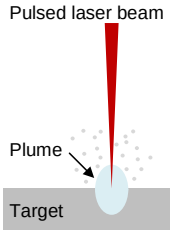


Figure 2.3: Conceptual, simplified schematic of a laser ablation process.

With laser pulses exceeding the material's thermal diffusivity, the material is directly exposed to high amounts of energy, which can lead to non-thermal, photochemical ablation mechanisms. The material is forced in a state of plasma due to the occurring direct ionization and expands in the form of a energetic dense, visible vapor plume [62, 66], as schematically visualized in Figure 2.3. This form of ablation is called cold ablation and allows for precise micro-machining of solid material. However, the dense vapor plume may contain liquid or solid material, which may lead to debris on the material surface [63]. Furthermore, due to the expansion of the vapor plume, surface shock effects can occur.

2.2 Printed Thin-Film Transistors & Circuits

2.2.1 Printed Thin-Film Transistors

Material and substrate possibilities are broad and allow for manifold options in printed TFT realization. Organic TFTs (OTFTs), also labeled organic field-effect transistors (OFETs), mainly incorporate semiconducting materials, based on conjugated polymers and conjugated small-molecules [67]. Organic semiconducting materials are of interest due to their low processing temperature compatibility, which allows for fabrication on low-cost, flexible substrates [68] such as polyethylene terephthalate (PET) and polyethylene naphthalate (PEN). Reported field effect mobilities for OTFTs are in the range of $0.1\,\mathrm{cm^2V^{-1}s^{-1}}$ up to $10\,\mathrm{cm^2V^{-1}s^{-1}}$, whereas *p*-type semiconductors usually show improved performance and reliability in contrast to their *n*-type counterparts [68].

Printed, inorganic TFTs incorporate semiconductors such as metal oxides and silicon. Printed *n*-type metal oxide semiconductors, formed from precursor salts, enable TFTs with high field effect mobilities, exceeding $100\,\mathrm{cm^2V^{-1}s^{-1}}$ [69]. However, a drawback is the high processing temperature of $200\,^\circ\mathrm{C} - 500\,^\circ\mathrm{C}$ [69]. To reduce processing temperature for precursor-based metal oxide semiconductor fabrication, chemical [70] or photonic curing [71] methods are required, which however also impact field effect mobility. Nanoparticle-based inorganic semiconductors can be sintered at lower temperatures, which allow for fabrication on PET and PEN substrates. For inorganic TFTs, *n*-type semiconductors show increased performance in comparison to *p*-type semiconducting materials [72]. However, printed TFTs generally require operating voltages exceeding $3\,\mathrm{V}$, even when employing high mobility semiconductors.

In inkjet-printing, fabrication of the gate insulator material often yields a bottleneck. Inkjet-printed dielectrics usually require relatively thick layers to prevent leakage currents and shortages between the gate and source-/drain electrodes as well as the gate and semiconductor channel of the TFT. This often leads to small gate capacitance per unit area, which impacts drain current as technology related

parameter. To tackle these issues, at the cost of maximum device operating speed, electrolytes can be deployed as insulating material. Electrolyte-gated transistors are capable to reduce operating voltage requirements drastically and enable sub-voltage operation [73–76].

2.2.1.1 Inkjet-Printed Electrolyte-Gated Transistors

The basis for device and material composition of inkjet-printed electrolyte-gated transistors, also labeled as electrolyte-gated field-effect transistors (EGFETs), were demonstrated by Garlapati et al. using in-plane device structures [73]. Later, Marques et al. presented classical top-gate bottom-contact stack TFT-architecture fabricated EGTs, using lithographically-structured electrodes and interconnects, which show better dynamic device performance including inverter output swing and device switching speed [77, 78].

The EGT device material stack consists of an indium tin oxide (ITO) signal routing layer, which forms the drain and source electrodes. Furthermore, indium oxide $(\mathrm{In_2O_3})$, as high mobility, inorganic *n*-type semiconductor is deployed. As insulating layer a composite solid polymer electrolyte (CSPE), which is capable to follow the rough semiconductor surface, is used [73]. The increased surface roughness of the indium oxide thin-film is assumed to be influenced by the slow evaporation of water, which is the main solvent of the inkjet-printable precursor fluid [73]. The top-gate consists of the conductive polymer poly(3,4ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS).

Electrolyte-gated transistors operate in accumulation of charges at the semiconductor/electrolyte interface (SEI) within the semiconductor surface, by applying a positive voltage at the gate-electrode terminal [75]. Due to the occurring migration of ions in the electrolyte, electrical double layers (EDLs) at the top-gate/electrolyte interface (TGEI) and the SEI are formed. Whereas anions, within the electrolyte, migrate towards the positively charged TGEI interface and cations towards the SEI interface, which leads to the aforementioned accumulation of charges in the

semiconductor, which enables a current to flow between the drain and source electrodes [79]. The nanometer-sized distances of the resulting capacitor plates, at both EDLs, result in a large gate capacitance per unit area [74]. The combination of a large gate-capacitance per unit area due to the CSPE, and a high field-effect mobility of the semiconductor allow EGTs to generate drain currents (I_{D}) ranging from hundreds of $\mu\mathrm{A}$ to mA at low operating voltages ($\leq 1.5\,\mathrm{V}$) [80].

Inkjet-printed EGTs typically operate at several tens of Hz up to kHz [77, 78]. Advances in materials can further increase device switching speed. Currently, the limiting factor in device switching speed is the cutoff-frequency, which arises from the electrolyte-gating approach and is heavily influenced by the top-gate and bulk-electrolyte resistance [81]. Lately, research advancing and highlighting the capabilities of EGTs, due to device modeling with respect to direct-current (DC) characteristics and transistor variability [82, 83], EGT capacitance modeling [84], noise characteristics [85] and circuit designs [80, 86], have been shown.

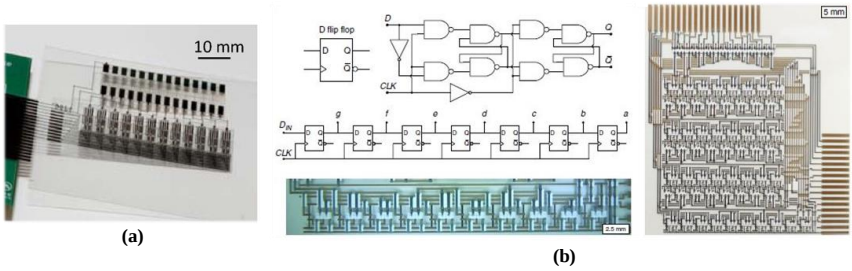
2.2.2 Printed Circuits

Advanced printed digital circuits, such as D-flip flops [87] and address decoders [88] (see Figure 2.4a), using OTFTs are reported. Furthermore, analog building blocks for small signal amplification such as operational [89–91] and transimpedance amplifiers [91], were successfully presented.

Of special interest are tags for radio frequency identification (RFID), which are one of the many application scenarios where printed TFTs can be employed. Passive RFID designs operating at the $13.56\,\mathrm{MHz}$ frequency band, incorporating printed inorganic TFTs, are successfully demonstrated [92]. These presented results are fabricated with devices, employing dielectrics as insulating material. Operating voltages range from $5\,\mathrm{V} - 20\,\mathrm{V}$.

Low-voltage circuits based on printed electrolyte-gated transistors are increasingly gaining interest. Reported results are mainly on digital circuits such as logic gates, ring oscillators and storage elements [76, 86]. Furthermore, complex systems

incorporating digital logic circuitry with monolithically integrated electrochromic displays [93] are reported and shown in Figure 2.4b. Operating voltages are $\leq 2\,\mathrm{V}$, at operation frequencies reaching from several up to hundreds of Hz.



(a) **(b)**

Figure 2.4: Advanced circuits based on printed TFTs. **(a)** Printed OTFT-based address decoder and ferroelectric memory on flexible substrate, connected with rigid printed circuit board (PCB) [88]. Reproduced under CC BY-NC-ND 3.0 license, https://creativecommons.org/licenses/by-nc-nd/3.0/. **(b)** Electrochemically-gated transistors deployed in addressing circuitry for an integrated electrochromic display [93]. Reproduced under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

3 New Concepts in Printed Electronics

In this chapter, new concepts for PE are introduced, with a focus on current trends and requirements for future PE-based applications. Therefore, PE-based solutions for sustainable energy are suggested with a focus on small alternating voltage rectification. In order to enable novel paradigms in computing, current trends are introduced, which are empowered using memristors. Furthermore, printed physically unclonable functions as hardware-based security primitive are discussed.

3.1 Sustainable Energy with Printed Rectifiers

With an ever increasing amount of electronic devices joining the IoT worldwide, an increase in environmentally harmful electronic waste is expected [94, 95]. Therefore, ecologically sustainable solutions for electronic devices are required. Autonomous operating systems could be partially equipped with micro energy harvesting devices, which are capable to generate energy from natural resources. This increases lifetime of batteries, which are required for complex, wireless information exchanging, systems [96].

Printed-electronics based solutions for energy harvesting could be equipped on various non-conformal surfaces over large areas and be attached on systems in motion. For self-powered micro systems, vibration energy harvesters, operating at frequencies from tens of Hz to kHz, have proven an interesting option [97–100]. However, micro energy harvesters, such as vibration energy harvesters, output low

alternating voltages, which makes efficient rectification for micro power systems a challenging task [101]. This is often tackled using sophisticated, active Si-based ICs [102, 103]. Comparable rectifier solutions using printed electronics for alternating sub-voltage rectification have not been presented, yet.

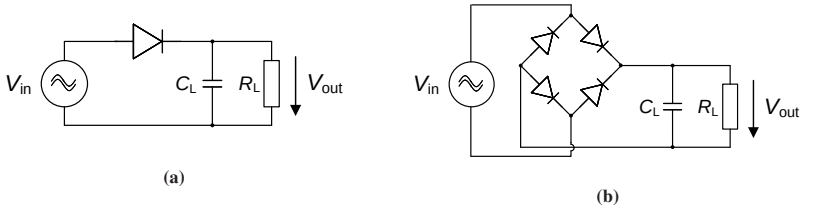


Figure 3.1: Basic passive rectifier circuit schematics, including a capacitor for rectified voltage smoothing and a resistive load. **(a)** Schematic for a half-wave rectifier, incorporating a single diode. **(b)** Schematic for a full-wave rectifier, incorporating four diodes.

Rectifiers are fundamental electronic building blocks for signal and power conversion [80]. For PE, mainly rectifier circuits with a focus on frequencies in the MHz range for radio frequency identification are researched to enable smart tags on flexible substrates [80]. Reported, printed solutions often require high voltages in the range of 20 V peak-to-peak (V_{pp}). This is attributed to large forward voltage drops in printed diodes and high threshold voltages in printed transistors. As mainly high frequency responses are reported, the voltage-loss due to damping of the input radio frequency signal, over the printed devices at higher frequencies further influences the required input voltages. Nonetheless, the reported high-speed devices aren't capable to rectify low alternating voltages generated from e.g. micro energy harvesting devices. Also, most reported printed rectifiers are realized as passive half-wave rectifier circuits (see Figure 3.1a), with only a few passive full-wave rectifiers (see Figure 3.1b) reported [104], despite their better power conversion efficiency (PCE) [80].

With passive RFID tags as target application, many printed rectifiers are based on multistage voltage multiplier topologies, such as modified Dickson charge pumps, which are commonly used for RFID input signal rectification, in order to provide high DC output voltage levels for the following circuit stages [105–107].

Rectifiers, fabricated using printing technology, are shown in Table 3.1, which includes the rectifier type, rectifying element, printing technology, input voltage, targeted frequency and year of publication. Direct comparison of different works and performance metrics, which are heavily dependent on the targeted application and utilized load, is not straightforward. Furthermore, as mainly RFID capable rectifier solutions for PE are targeted, also printed voltage multiplier topologies are included in the table.

Table 3.1: Reported printed rectifiers and voltage multipliers.

Type	Rectifying element	Printing technology	Input voltage (V_{pp})	Target frequency (Hz)	Year	Ref.
Half-wave rectifier & voltage multiplier	Diode (Schottky)	Gravure & Inkjet	20	13.56 M	2010	[92]
Voltage multiplier	TFT (diode-connected)	Screen	40	13.56 M	2012	[108]
Half- & full-wave rectifier	Diode (Schottky)	Gravure	20	100 k - 13.56 M	2013	[104]
Voltage multiplier	Diode (Schottky)	Gravure	20	13.56 M	2014	[109]
Voltage multiplier	TFT (V_{th}-cancelling)	Screen	60	13.56 M	2015	[110]
Half-wave rectifier & voltage multiplier	Diode (Schottky)	Inkjet	20	13.56 M	2020	[111]

3.2 New Paradigms in Computing using Memristors

With the trend of Si-based integrated device scaling reaching its physical limits and amounts of data are increasing, new paradigms for future computing systems emerged. This includes Beyond-von-Neumann data processing and neural networks. Furthermore, NAND-flash as non-volatile storage element is reaching its physical limitations, with respect to integration density, speed and reliability [112].

To tackle the aforementioned problems, memristors have shown a promising option [113]. Memristors offer the capability for emulating synaptic plasticity, programmable (multi)-bit information storage and large-scale integration using crossbar architectures. Current trends in research and fabrication is mostly based

on high-density integration of nanometer devices using advanced manufacturing. Furthermore, usability of PE-based neuromorphic computing primitives are shown feasible [114] as well as the need for PE-based, lightweight non-volatile memory. Printed memristors can be utilized to enable Beyond-von-Neumann-, neuromorphic- as well as memory applications in printed electronics.

The theoretical framework and foundations of the memristor, a combination of the words memory and resistor, was formulated by Chua in the form of a dynamical system [115–117]. In 2008 researchers report on a physically realized memristor, which exhibits resistive switching behavior in titanium dioxide crosspoint structures, linking Chua's theory to a practical implementation [118]. Resistive switching behavior in metal oxides has been reported before and was proposed to be utilized in memory applications [119–121]. Non-volatile memory, based on resistive switching devices, is also referred to as (non-volatile) resistance random access memory [122]. However, the systematical link to the memristor, as introduced by Chua was missing. In a retrospective the previously reported devices can also be labeled as memristors or memristive devices [123]. The discovery of the memristor by Strukov et al. boosted research in resistive switching devices heavily, due to the massive potential highlighted by Chua's initial theoretical works.

Resistive switching mechanisms can occur due to various effects, such as amorphous-crystalline phase change, magnetoresistive effects and nanoionic redox phenomena [124]. In the following, focus is on resistive switching caused by nanoionic redox phenomena.

A memristor is usually built in a stacked material architecture. In its most basic form, only two metal electrodes and a single storage material layer are required for device formation, as shown in Figure 3.2a. The storage layer is based on insulating or semiconducting material, whereas the electrodes are mostly metals [122]. The device is capable to obtain at least two distinctive resistive states, a low-resistance state (LRS) and high-resistance state (HRS), based on applied voltage. The resistive state remains programmed within the device until the next programming phase, which enables non-volatile information storage. The device junction area is based on the top and bottom electrode crossing junction, in which

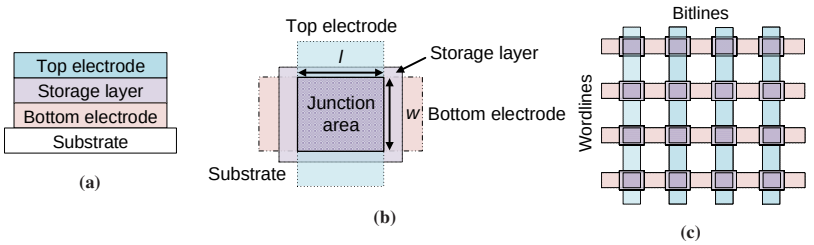


Figure 3.2: Conceptual memristor schematics. **(a)** Cross section of a memristor material stack. **(b)** Top-view of a basic resistive switching device stack including the junction area in which resistive switching occurs, based on the overlap in bottom electrode (w) and top electrode (l). **(c)** Memristors arranged in a crossbar architecture.

the storage layer is sandwiched in, as shown in Figure 3.2b. In this area, interfacial effects can occur, which enables area-based switching, or stochastic filament formation within a fraction of the area is possible. Furthermore, it describes the minimal fabrication possibilities of certain manufacturing technologies. Area-based switching usually occurs close to one electrode and is referred to as interface-type switching, whereas current is proportional to the effective active area. If the switching mechanism is based on formation and dissolution of a conducting filament it's referred to as filamentary switching [124]. High density integration of devices can be achieved using crossbar architectures, as shown in Figure 3.2c. Filamentary-type switching in memristors is possible mainly due to migration of ions, which lead to formation of a conducting filament/path within the storage layer, which connects both electrodes (low-resistance state) and can be dissolved again (high-resistance state). These effects are based on a different primary mechanism thus devices are named electrochemical metallization memory (ECM) and valence change memory (VCM) [125]. For ECM, cations drift from an active metal electrode such as silver and copper, which lead to metal nano-filament formation. In VCM devices, often metal oxides with high ion mobility, oxygen ion or metal cation migration within the metal oxide leads to redox reaction along with a change in electric conductivity, due to valance change in the cation sublattice [126].

Many ECM-based memristors require an initial forming voltage, which leads to the formation of the conductive filament. This forming voltage usually exceeds the set voltage, which is applied to switch the devices from HRS to LRS. Furthermore, a reset voltage is used to switch the devices from LRS to HRS again. The most common switching-type behavior can be distinguished between unipolar- and bipolar switching and is observable in current-voltage ($I - V$) device characteristics. Unipolar switching behavior is given, when the applied voltage polarity is identical for set and reset processes, as visualized in Figure 3.3a. In bipolar switching, opposite voltage polarities are required to enable device switching. Figure. 3.3b, shows a bipolar switching process, where a positive voltage is required for the set and a negative voltage is required for the reset process. Usually, a compliance current (CC) is required to limit the current over the device and prevent breakdown or device degradation when the memristor switches from HRS to LRS.

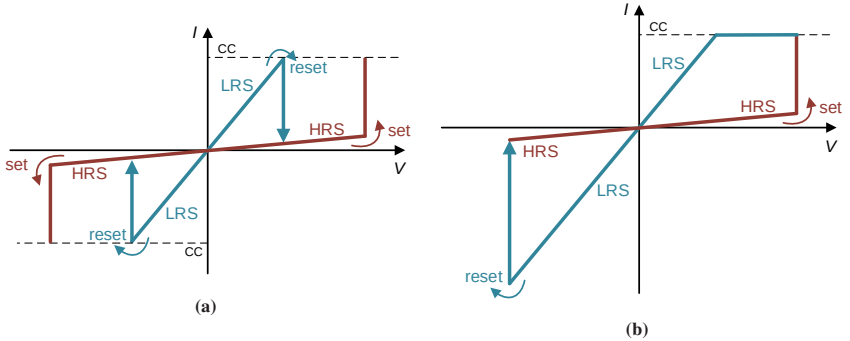


Figure 3.3: Typical switching behavior of memristors, including compliance current for current limiting, when the device switches from HRS to LRS. **(a)** Unipolar device switching. Set and reset voltages have the same polarities. **(b)** Bipolar device switching. Set and reset voltages require opposite polarities.

3.3 Hardware-Based Security with Physically Unclonable Functions

Hardware-based security builds the basis for security in electronic devices in general. With software-sided security being extremely effective at low computational overhead, hardware-based security receives less attention. This is due to the possibly increased overhead in hard- and software, cost and at high performance electronic systems, such as CPUs, also reduced speed. The popular, non-invasive, cache-based side-channel attacks Meltdown and Spectre [127, 128] impressively demonstrated how sensitive information, at the very fundamental levels of data processing within modern, assumable secure, CPU architectures can be exploited due to leaky hardware. This highlights the need for hardware-based security.

With PE-enabled devices joining the IoT, hardware-based security primitives for these devices have to be investigated at the very beginning of their product lifecycle.

Physically unclonable functions are hardware-security primitives, which enable secure identification, authentication and can be utilized for cryptographic purposes [129–136]. A PUF generates a random sequence of bits, namely response (R), in dependency of an input challenge (C) and based on the intrinsic variations within a stimulated system. The one-way functionality of a PUF can be described as $R = f(C)$ [129, 137, 138] and is unique for each physical instance of the PUF [130], as visualized in Figure 3.4.

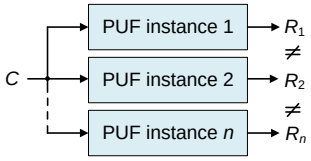


Figure 3.4: Schematic for response R generation over different PUF instances of the same type, stimulated with an identical challenge C. Due to intrinsic, unpredictable PUF instance behavior, the output response differs for each PUF instance.

The challenge-response generation and correlation is also referred to as challenge-response pair (CRP). The volatility of the PUF CRP generation procedure offers an advantage against invasive attacks in comparison to non-volatile electrically erasable read-only-memories, which are commonly used for secret key storage [130].

PUFs can be further classified as either weak or strong PUFs. In weak PUFs the CRPs scale polynomially, based on the exploited variation footprint, whereas strong PUFs show an exponential increase in CRPs dependent on exploited variation footprint. Therefore, for weak PUFs, only a small amount of CRPs can be generated from a PUF instance. Weak PUFs are primarily employed for identification and cryptographic purposes. To obfuscate the resulting challenge-response generation procedure, hashing can be utilized. This operating mode is called controlled PUF [139]. Strong PUFs allow to utilize different challenges, within one PUF instance, in order to generate different and independent responses, thus resulting in a large CRP space [137, 140]. For strong PUFs, the CRP generation does not utilize hashing, as each challenge is capable to deliver a different response. Strong PUFs are mainly used for authentication purposes.

As possible variation sources for PUFs, various surfaces and materials can be stimulated via optical methods, which act as the challenge C and being digitized, to generate a response R. PUFs of this type can be categorized as optical PUFs. Pappu et al. proposed one of the first PUF-related concepts, exploiting randomized speckle patterns for key generation, using optical methods [141]. Optical PUFs are capable to derive large responses at small areas, however often sophisticated external instrumentation is required to achieve high quality, reproducible responses [142]. This can result in high equipment requirements and precise mechanical alignment of the stimulation source and the exploited imperfect surface. Recently, novel material optical PUFs exploiting variation in random, inkjet-printed patterns incorporating fluorescent quantum dots, are presented by Liu et al. [143]. Many novel materials provide surfaces and properties in general that can be exploited using optical methods [144–149].

Another broadly researched field for PUFs are Si-based PUFs [131]. These type of PUFs exploit the explicit intrinsic variations in ICs to generate a response. Physical sources for manufacturing induced variation in Si-based PUFs can be numerous. For metal-oxide-semiconductor field-effect transistors (MOSFETs), the mainly utilized transistor technology within ICs, this includes threshold voltage (V_{th}) variation due to random dopant placement [150–152], oxide-thickness [153], channel-area dependent errors [150, 154] and line edge roughness [155–157]. These variations impact device switching speed and drain current. Further down-scaling in MOSFET gate length, besides increasing gate-leakage currents and short-channel effects, impact transistor variability even further. Passive components in ICs, such as poly-resistors and metal-oxide-semiconductor capacitors as well as interconnects, are subject to variation [158–162]. The idea in exploiting IC intrinsic variation for key generation was proposed by Lofstrom et al. [163].

The first systematic concept for PUFs in silicon was presented by Gassend et al. [131, 135, 164], exploiting variations in digital circuitry. Silicon-based PUFs can be categorized in analog-PUFs, which often employ amplifying and device biasing techniques to exploit V_{th} -impact on transistor drain current in the form of analog circuit design [165–169]. Delay-based PUFs [170, 171] exploit variation in device switching speeds and are more oriented in digital circuits, such as ring oscillator [172–174] and arbiter structures [175, 176]. Furthermore, bistable PUFs often employ cross-coupled inverter configurations, which are commonly used for memory implementations, such as static random-access memory (SRAM) [177–179], in order to generate a response.

Recently, novel material PUFs, utilizing variations with respect to novel materials and devices in the form of Si-based PUFs are emerging. Therefore, variations in electrical characteristics of these devices and circuits are exploited. This includes carbon nanotube (CNT) transistor variation [180, 181], switching type and connection yield in CNTs [182], CNT resistive variation [183], memristors [184–187] and OTFTs [188–191].

For holistic PUF implementation, two main building blocks are required to enable reliable CRP generation. One building block is the so-called PUF core. It

contains a PUF's internal intrinsic variation source. The second PUF building block consists of a control logic for PUF core addressing and readout, which enables CRP generation. However, the control logic is usually also effected by variation, which introduces systematic errors within the PUF. This dilutes PUF core intrinsic variation and negatively impacts PUF metrics. Furthermore, fabricated PUF implementations require error correction strategies for PUF metric optimization [192].

3.3.1 Printed Physically Unclonable Functions

Printed electronics often suffers from increased device variation, in comparison to Si-based electronics. The reason is the nature of the manufacturing process, which is based on material processing from a liquid phase. Therefore, registration accuracy of PE-based manufacturing is in general poorer than lithographic processes. Exemplary, variation in active devices, such as printed thin-film transistors, is related to rheology of the printed fluid, quality of interfaces between printed layers such as increased surface roughness, scaling errors in the channel width-to-length ratio and physical layout of a design, to name but a few [89, 90, 193–196]. These factors increase the fabrication-induced as well as intrinsic variation, of printed in comparison to Si-based devices.

Furthermore, PE offers a broad bandwidth of usable substrates, fluids and printing techniques and provides an interesting basis for hardware-based security. However, as variation impacts device and circuit yield, feasible designs for PUF implementations, which extract variation on the electrical signal level (such as Si-based PUF implementations), need to be considered. Thus PUFs utilizing printing technology remain scarce. Especially with a focus on PUF metric evaluation. Mostly single-bit functionalities of these type of PUFs are experimentally verified. Physically unclonable functions, fabricated using printing technology are listed and compared in Table 3.2, with a focus on the printing technology, the PUF type, response generation, corresponding response bit width, experimentally reported PUF metrics and year of publication.

Table 3.2: Comparison of printed PUFs including reported performance parameters. The absence of a parameter is denoted by (/).

PUF	Printing technology	PUF type	Response generation	Response bit width	PUF metrics (experimental)	Year	Ref.
SRAM-PUF	Screen	Weak	Electrical	4	/	2012	[108]
Memory-PUF	Inkjet	Weak	Electrical	1	/	2018	[197]
Resistive CNT-PUF	Inkjet	Weak	Electrical	/	/	2019	[198]
Quantum Dot-PUF	Inkjet	Strong	Optical	/	/	2019	[143]

3.3.2 Evaluation of Physically Unclonable Functions

To evaluate and compare PUF implementations, performance metrics were proposed by Hori et al. and Maiti et al. [175, 199]. In the following discussion and regarding the results obtained for this thesis, the focus is on PUF metrics introduced by Maiti et al. [199]. This includes the uniqueness, reliability, bit aliasing and uniformity metrics. The hamming distance (HD) is shortly discussed as it provides a fundamental element in PUF metric calculation. Also the bit error metric is shown.

Hamming distance
The Hamming distance is used to evaluate the amount of different bits between two bit strings of equal length L. Therefore, each l-th bit position between both bit strings is compared by an exclusive or operation and summed up, according to Equation 3.1.

$$\mathrm{HD}(x, y) = \sum_{l=0}^{L-1} (x_l \oplus y_l) \tag{3.1}$$

Uniqueness
To measure the correlation of responses stimulated with the same challenge from different PUF instances, the uniqueness metric is used. The uniqueness is a measure of the PUFs inter-Hamming distance. A uniqueness value of 50% is

optimal, as all PUF responses should differ due to the random intrinsic variations. The uniqueness for N PUFs, incorporating two different PUF instances i and j, each with L-bit responses R_i and R_j, is defined as [138, 200]:

$$\mu_{\text{inter}} = \frac{2}{N(N-1)} \sum_{i=1}^{N-1} \sum_{j=i+1}^{N} \frac{\text{HD}(R_i, R_j)}{L} \cdot 100\% \tag{3.2}$$

Reliability

The reliability metric is a measure of the intra-Hamming distance of a PUF and describes the stability of PUF responses under varying operating conditions, such as temperature, noise, humidity and supply voltage, when applying the same challenge. The ideal value is $100\,\%$. The reliability REL_n for PUF instance n is calculated by using the L-bit reference response $R_{\text{ref},n}$ measured at nominal conditions and the L-bit test response $R'_{n,t}$ for T different operating conditions [138, 200]:

$$\text{REL}_n = 100\% - \frac{1}{T} \sum_{t=1}^{T} \frac{\text{HD}(R_{\text{ref},n}, R'_{n,t})}{L} \cdot 100\% \tag{3.3}$$

Bit aliasing

To evaluate the logic 0's and 1's distribution across different PUF entities of the same type, the bit aliasing metric is used. In an ideal case, both binary values occur with the same probability of 50%. If the l-th bit of the tested PUF responses has the same bit value across all PUF entities, the inter-Hamming distance of this bit will be zero. As a result various PUFs may produce the same responses, which degrades the uniqueness and leads to false positives in device authentication. The bit aliasing for N PUF entities at the l-th bit position is calculated as [138, 200]:

$$\mathrm{BA}_l = \frac{1}{N} \sum_{n=1}^{N} R_{n,l} \cdot 100\% \tag{3.4}$$

Uniformity

To evaluate the occurrence of logic 0's and 1's in the PUF responses, the uniformity metric is used. Preferably, both binary values should occur equally often (50%) in a PUF response. For PUF instance n, having an L-bit long response $R_{n,l}$ at bit position l, the uniformity is defined as [138]:

$$\mathrm{Uni}_n = \frac{1}{L} \sum_{l=0}^{L-1} R_{n,l} \cdot 100\%. \tag{3.5}$$

Bit errors

When generating a PUF response multiple times, bit errors due to flipped bits may occur over time. Reasons are in changing operating conditions over time. Due to possible bit errors, the regenerated CRPs might differ. This degrades both, the uniqueness and the reliability scores. In an ideal case, no bits should flip over time, therefore the optimal value is 0%. Bit errors (BE_n) are calculated for PUF instance n by using the L-bit reference response $R_{\mathrm{ref},n}$ at nominal conditions and the L-bit response $R'_{n,w}$ regenerated W-times [138, 200]:

$$\mathrm{BE}_n = \frac{1}{W} \sum_{w=1}^{W} \frac{\mathrm{HD}(R_{\mathrm{ref},n}, R'_{n,w})}{L} \cdot 100\% \tag{3.6}$$

4 Inkjet-Printed Devices

In this chapter the fabrication routine for inkjet-printed EGTs on laser-ablated ITO substrates, which are used for all obtained results incorporating EGTs during this work, is provided. Furthermore, an inkjet-printed memristor, which provides an important building block for future PE-based circuit and system development, is presented including its fabrication routine and performance evaluation.

4.1 Inkjet-Printed Electrolyte-Gated Transistors

A schematic cross section of a top-gate bottom-contact EGT material stack can be seen in Figure 4.1a, including voltage biasing scheme. In Figure 4.1b, a corresponding cross section image of an EGT, acquired by focused ion beam scanning electron microscopy (FIB-SEM) is shown. The top-gate layer can not be seen in the image due to the CSPE thickness, which exceeds the visualizable area of the machine. Shadowing effects in the top area of the CSPE as well as hole formation within the CSPE, due to electron beam damage can be observed. Furthermore, the structure of the semiconductor channel is visible. Parts of the inkjet-printed semiconductor also cover the ITO surface partially. The laser-ablated ITO layer shows a gradual increase in thickness. The layer thicknesses for the EGT material stack shown in Figure 4.1b are $100\,\mathrm{nm}$ for the ITO and $\approx 50\,\mathrm{nm}$ for the $\mathrm{In_2O_3}$ thin-film.

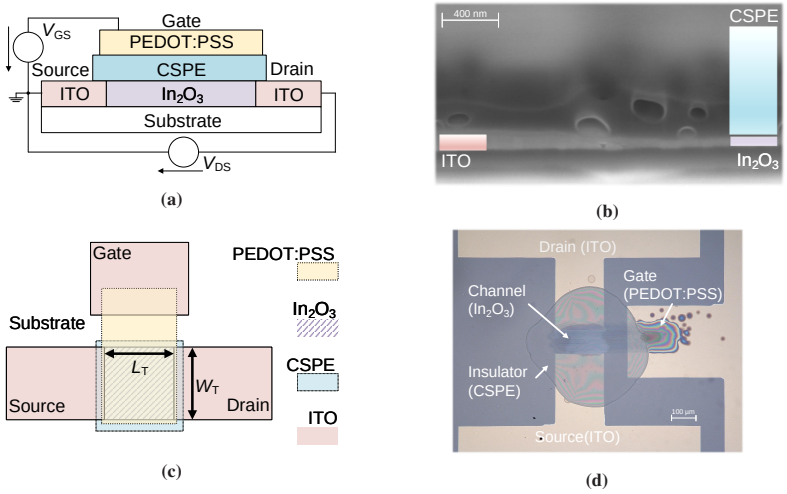
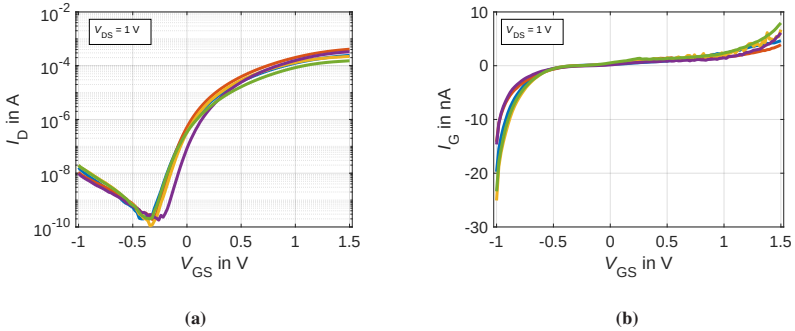


Figure 4.1: EGT cross section and top-view. **(a)** Schematic cross section of the top-gate bottom-contact EGT material stack, including voltage biasing scheme. **(b)** Cross section of the EGT material stack, obtained by FIB-SEM. The top-gate is not visible in the picture, due to the limited viewable area of the machine. **(c)** Schematic top-view of the EGT material stack. Top layers are displayed slightly transparent to visualize the underlying layers and the corresponding geometric channel proportion with respect to channel width W_T and channel length L_T. **(d)** Microscopic top-view image of a fabricated EGT at $10\times$ optical magnification.

Electrolyte-gated transistors show a dependency in their functionality with respect to humidity [201]. Therefore, electrical measurements are made at controlled relative humidity (RH). For EGTs, the channel width (W_T) is defined by the width of the source and drain electrodes, which are in contact with the semiconductor channel. The distance between the source and drain electrodes, which are separated by the semiconductor channel, define the devices' length (L_T). This has proven a good trade off in active channel area approximation. The geometrical structure for an EGT, from a top view, is schematically shown in Figure 4.1c. Figure 4.1d shows a microscopic image, of a fabricated EGT at $10\times$ optical magnification, from a top view. Furthermore, in Figure 4.2 transfer curves and corresponding gate leakage currents (I_G) of five EGTs, in dependency of the gate-source (V_GS) voltage, at $1\,\mathrm{V}$ drain-source voltage (V_DS) at $50\,\%$ RH are visualized. The drain



(a) **(b)**

Figure 4.2: Measured transfer curves and corresponding gate leakage of five EGTS with a channel width $W_T = 200\,\mu m$ and length $L_T = 60\,\mu m$ at V_{DS} = 1 V and RH = 50 %. **(a)** Transfer curves of the measured EGTs, with I_D plotted in logarithmic scale. **(b)** The corresponding gate leakage currents.

current is plotted in logarithmic scale. The channel width for the shown EGTs is $200\,\mu m$ and the channel length is $60\,\mu m$, respectively. The presented current-voltage ($I - V$) curve measurements, incorporating EGTs, were performed with an Agilent 4156C semiconductor parameter analyzer.

In the following, the fabrication workflow for EGTs is described.
Initially, a commercially available ITO-covered glass substrate is structured using laser ablation with a Trumpf TruMicro Series 5000 picosecond-laser with a $1030\,nm$ wavelength at $800\,kHz$ repetition rate. The ITO layer is used for patterning of interconnects, resistive structures as well as EGT drain- and source-electrodes. Usually, an additional area for gate-electrode contacting is also structured with ITO. This eases device probing and external contacting of the gate-electrode. For laser ablation of the used ITO thin-film, the laser was operated at an average power of $2.5\,W$. Prior to printing, the structured substrate is cleaned using a mixture of acetone and isopropanol (1:1) in an ultrasonic bath for one hour. Subsequently, an indium (III) nitrate hydrate $(H_2InN_3O_{10})$-based precursor is inkjet-printed between the source and drain electrodes of the EGT. In order to increase device yield, small amounts of the semiconductor material, next to the source and drain electrodes, are printed on the ITO film. This optical feedback

during fabrication helps to exclude device malfunction due to bad or non-existing contact of the semiconductor channel with the ITO signal layer. To form the poly-crystalline indium oxide semiconductor, the substrate is heated in a furnace at $400\,°\mathrm{C}$ [73], with a two hour ramp-up time and held at this temperature for another two hours. For cooling, the device is kept in the furnace over an extended time period, until the furnace temperature decreased to room temperature. This annealing step, which is in air, influences the sputtered ITO resistivity of the samples and increases its sheet resistance. This effect could be explained by interaction of free oxygen in the air with the ITO thin-films, which decreases its oxygen vacancies and therefore the carrier concentration [202]. After the $\mathrm{In_2O_3}$ thin-film is formed, the CSPE is inkjet-printed onto the semiconductor. In a last fabrication step, the PEDOT:PSS top-gate is inkjet-printed on the CSPE, covering the geometrical area of the semiconductor. The conductive PEDOT:PSS layer is also connected with the probing-/contacting ITO gate-terminal. To reduce the impact of parasitic capacitances, the geometric overlap between the top-gate area with the source and drain electrodes is kept as small as possible. Variability due to the printing process, fluid dispersion on the substrate, during material solidification and batch-to-batch variability of fluids can lead to differences in inkjet-printed layer thickness and differing overall electrical performance. Furthermore, the print settings, such as drop-spacing and multi-layer printing of materials influence the observed, solidified material's layer thickness, which can be adjusted as required. Typical layer thicknesses for EGT materials, how they were fabricated during this thesis, are: ITO = $100\,\mathrm{nm}$ (commercial product), $\mathrm{In_2O_3}$ = $50\,\mathrm{nm} - 100\,\mathrm{nm}$, CSPE = $2.5\,\mu\mathrm{m} - 5\,\mu\mathrm{m}$ and PEDOT:PSS = $150\,\mathrm{nm} - 250\,\mathrm{nm}$. The fluid formulation and settings for the inkjet-printer and the laser are shown in the Appendix. All inkjet-printing processes for EGT fabrication were performed on the Fujifilm Dimatix DMP-2831 and DMP-2850, using print heads of the type Dimatix DMC-11610 with an average droplet volume of $10\,\mathrm{pL}$.

4.2 Inkjet-Printed Memristor

Parts of the results in this section were reported in [203].

The developed inkjet-printed memristor utilizes a three-material stack, which consists of a gold (Au) bottom electrode, a zinc oxide (ZnO) storage layer and a silver (Ag) top electrode, as shown in Figure 4.3. The devices are fabricated on a glass substrate, which is covered by a thermally evaporated, $5\,\mathrm{nm}$ thick chromium (Cr) layer for increased adhesion of the gold bottom electrode. The gold electrode was also thermally evaporated on the Cr-covered glass substrate, with a thickness of $45\,\mathrm{nm}$ and structured using laser ablation at an average laser power of $1.5\,\mathrm{W}$.

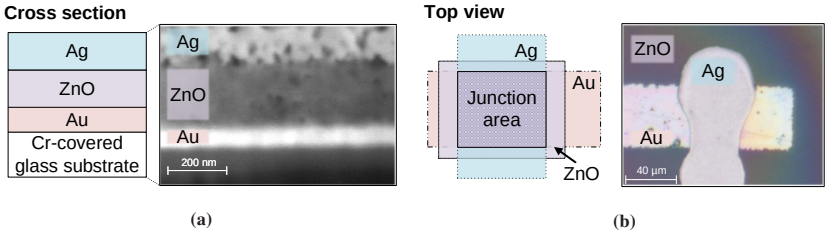


Figure 4.3: Schematic and optical images of the inkjet-printed memristor stack. **(a)** Cross section of the memristor material stack. The optical image was obtained via FIB-SEM. **(b)** Top view of the device, visualizing the crossing junction. The optical image clearly shows the different material layers from a top view. The ZnO is covering an extended surface area. Adapted from [203], © 2021 AIP Publishing.

The ZnO storage layer is inkjet-printed on the gold electrode, using a zinc nitrate hexahydrate $(\mathrm{Zn(NO_3)_2 \cdot 6H_2O})$-based precursor salt. The corresponding fluid formulation is shown in the Appendix. After printing of the storage layer, a $2\,\mathrm{h}$ heating interval at $400\,^{\circ}\mathrm{C}$ is required to form a poly-crystalline ZnO thin-film.

For the top electrode, a commercially available silver nanoparticle-based fluid is inkjet printed vertically to the bottom electrode onto the ZnO layer. Subsequently, the device is annealed in air at $150\,^{\circ}\mathrm{C}$ over $1\,\mathrm{h}$. The overlapping electrode crossing junction forms the effective memristor area. Figure 4.3a shows a schematic of

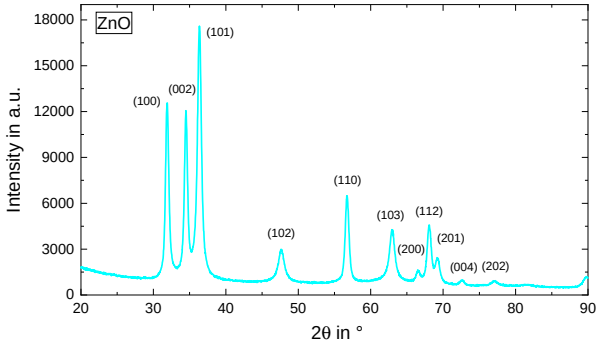


Figure 4.4: X-ray powder diffraction results of the poly-crystalline ZnO film, formed from the inkjet-printed zinc-nitrate precursor salt. Adapted from [203], © 2021 AIP Publishing.

the used material stack and an optical cross section image, which was obtained by FIB-SEM. The approximate thickness of the investigated material stack was determined with Ag $\approx 80\,\mathrm{nm}$, ZnO $\approx 200\,\mathrm{nm}$ and Au = $45\,\mathrm{nm}$, as shown in the image. The Cr layer is not highlighted in the image, as it is not directly part of the material stack and doesn't impact device performance. A visual top view of the memristor is shown in Figure 4.3b, which highlights the crossing junction. As shown in the microscopic image, on the right hand side, the crossing junction for the inkjet-printed device is $\approx 50\,\mu\mathrm{m} \times 50\,\mu\mathrm{m}$. In order to investigate the quality of the formed ZnO, x-ray powder diffraction analysis is performed. As shown in Figure 4.4 no peaks, other than ZnO are visible. The storage layer is formed in a poly-crystalline hexagonal wurtzite ZnO structure, according to the Joint Committee on Powder Diffraction Standards card number 36-1451. Due to the processing from a liquid phase and required material solidification process, thicknesses in fabricated devices vary at a higher degree than classical thin-film fabrication methods.

In the following, electrical characterization of the inkjet-printed devices is performed at room temperature in air. To investigate the resistive switching (RS) behavior of the device, its $I - V$ characteristics are measured using a Keithley 4200A SCS semiconductor parameter analyzer. A compliance current (CC) of $0.8\,\mathrm{mA}$ is set to prevent breakdown of the device and reduce negative impact

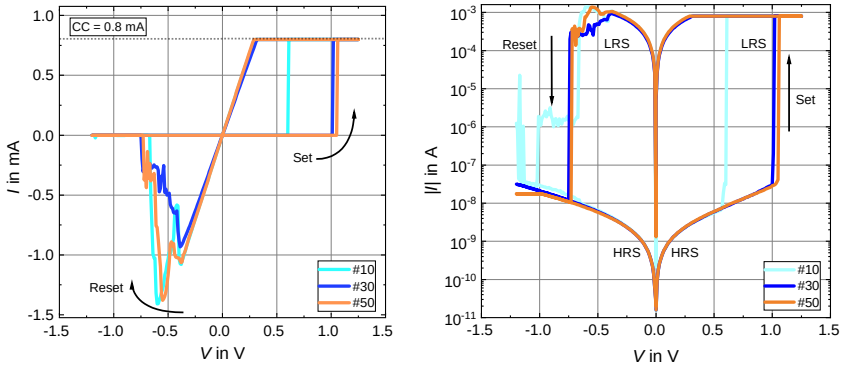
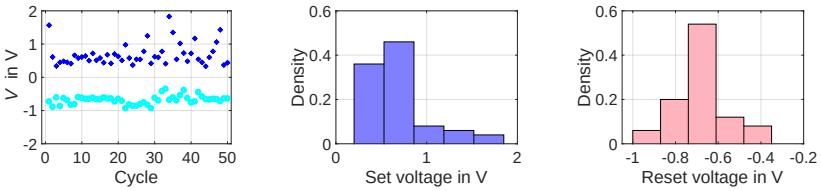


Figure 4.5: $I - V$ curves of the inkjet-printed memristor, which shows a bipolar-switching behavior. For the set process, a compliance current of $0.8\,\mathrm{mA}$ is used. Furthermore, ECM-cell type switching behavior is observable. **(a)** $I - V$ curves on a linear scale, showing cycle number ten, 30 and 50. **(b)** $I - V$ curves on a semi-logarithmic scale, showing cycle number ten, 30 and 50. Adapted from [203], © 2021 AIP Publishing.

of increased current on its general performance [204, 205]. The $I - V$ curve investigations further reveal information about the forming, set and reset voltages of the device.

Figure 4.5 shows $I - V$ curves, obtained with a DC voltage sweep at a step size of $0.01\,\mathrm{V}$, plotted on linear and semi-logarithmic scale. For all obtained measurements, the bias voltage is applied to the top electrode and the bottom electrode is grounded. For set voltage investigation, the voltage is swept from $0\,\mathrm{V}$ to $1.5\,\mathrm{V}$ and back to $0\,\mathrm{V}$. To reset the device state, the voltage is swept from $0\,\mathrm{V}$ to $-1.3\,\mathrm{V}$ and back to $0\,\mathrm{V}$. The $I - V$ curves show bipolar resistive switching behavior, since the set and reset processes were completed at opposite voltage polarities. Furthermore ECM cell-type behavior can be observed from the $I - V$ characteristics, such as steep, abrupt switching at the set and reset voltages [206]. The initial forming voltage of the device of which the curves were obtained, in Figure 4.5 was $\approx 5\,\mathrm{V}$.

As shown in Figure 4.5, the set voltage is $0.5\,\mathrm{V}$ for the tenth DC voltage sweep and therefore lower than for sweep loop number 30 and 50 where the set voltage



(a) **(b)** **(c)**

Figure 4.6: Cycle-to-cycle variability for a single device over 50 repetitions. The initial forming voltage was $5.17\,\mathrm{V}$. **(a)** Set and reset voltage variation over 50 cycles. **(b)** Set voltage variation visualized as histogram. **(c)** Reset voltage visualized as histogram. Adapted from [203], © 2021 AIP Publishing.

increases up to $1\,\mathrm{V}$. The reduced set voltage at the tenth DC sweep can be explained due to residual amounts of conductive filament (CF) from the forming process. The peaking in the reset process $I - V$ curves (see Figure 4.5) indicate possible subfilamentary networks, which aren't ruptured at once.

Furthermore, the switch in set voltage over cycles resembles device specific cycle-to-cycle variability. Cycle-to-cycle variability is a common effect in redox-based memristors. These effects can be attributed to competing subfilamentary networks [207, 208]. To visualize cycle-to-cycle variability more detailed, continuous cycling over 50 repetitions over one device and corresponding distributions for set and reset voltage variation is shown in Figure 4.6. From the histograms a mean value for the set voltage is $0.68\,\mathrm{V}$ and a standard deviation of $0.34\,\mathrm{V}$. The reset voltage is on average $-0.68\,\mathrm{V}$ with a standard deviation of $0.13\,\mathrm{V}$.

To investigate the device-to-device variability of the inkjet-printed memristors, the forming, set and reset voltages of 40 devices were measured and visualized as histogram in Figure 4.7. Due to the printing process, which provides another factor in variability, compared to classical thin-film manufacturing, increased device variability can be expected. This is due to the increased feature sizes, which already provide a larger effective area for filamentary and subfilamentary forming, which increases sources for variability. On the other hand, stochastic filament forming which manifests in memristor cycle-to-cycle and device-to-device variation can be exploited for hardware-based security [209].

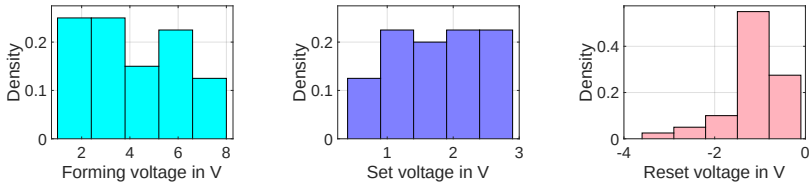


Figure 4.7: Device-to-device variability for the forming, set and reset voltages, plotted as histogram over 40 devices. **(a)** Forming voltage. **(b)** Set voltage. **(c)** Reset voltage. Adapted from [203], © 2021 AIP Publishing.

While the forming voltage varies over a broad voltage spectrum, the set and reset voltages present higher consistency, once the CFs are established in the ZnO layer. The mean value of the forming voltage is $4.05\,\mathrm{V}$ with a standard deviation of $2.05\,\mathrm{V}$. The mean value for set voltages is $1.76\,\mathrm{V}$ with a standard deviation of $0.65\,\mathrm{V}$, whilst the mean value of the reset voltages is $-1.07\,\mathrm{V}$ with a standard deviation of $0.61\,\mathrm{V}$, respectively.

For investigation of the device endurance, over DC sweep voltage and pulsed voltage, 50 cycles with both resistive states after each cycle are plotted in Figure 4.8a and 4.8b. For readout of the memristor resistive state, a readout voltage of $0.01\,\mathrm{V}$ was used after each RS operation. Under DC sweep voltage cycling, the resistive state of an arbitrary device can be successfully switched between a HRS of $10^8\,\Omega$ and LRS of $10^4\,\Omega$, which results in a on-/off ratio of 10^4. During cycling the HRS increases further, whilst the LRS decreases as shown in Figure 4.8a.

For the pulse voltage, a set pulse of $2\,\mathrm{V}$ and a reset pulse voltage of $-1\,\mathrm{V}$ are applied sequentially over a duration of $200\,\mathrm{ms}$, each. After each set and reset voltage stimulus, the resistive state is read out at $0.01\,\mathrm{V}$. The device endurance under pulse voltage is shown in Figure 4.8b. The device shows, in comparison to the DC sweep cycled device, a lower success rate in RS. However, for both devices under both testing modes after 50 switching cycles, no further degradation is visible. This highlights a high reliability of the inkjet-printed device. Also, both

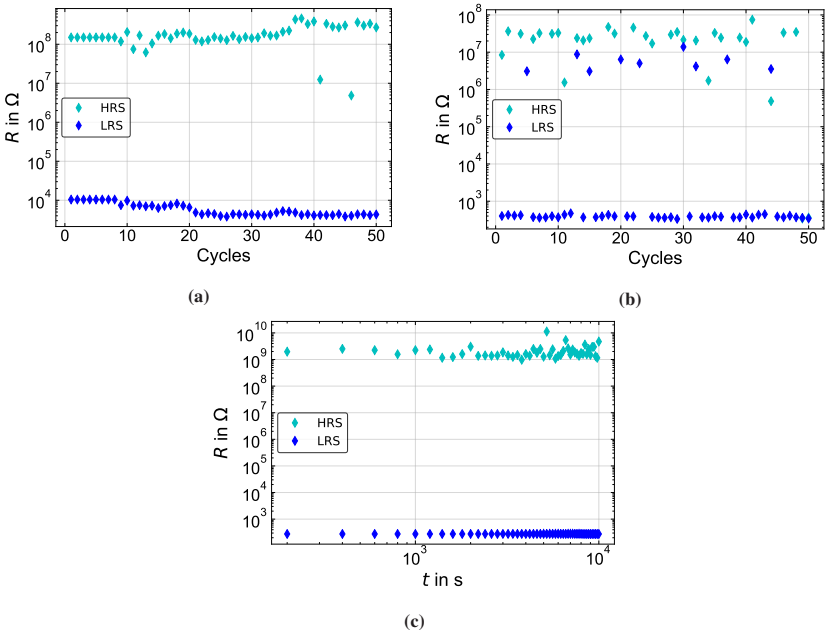


Figure 4.8: Endurance and retention test results of the printed device. **(a)** Endurance test using DC sweep cycling over 50 cycles. **(b)** Endurance test using pulse voltage cycling over 50 cycles. **(c)** Retention test over 10^4 s time period over the HRS and LRS, respectively. Adapted from [203], © 2021 AIP Publishing.

measurement modes show fluctuation in HRS value, whilst the LRS resistance is showing less fluctuation in resistance value, compared to the HRS value.

To obtain the retention of the device, time dependent analysis is performed. Therefore, a device is put into HRS and LRS and kept at the state for 10^4 s. The resistive state is read out during that time period each 200 s at 0.01 V. Figure 4.8 shows the results for the device in HRS and LRS, respectively. No degradation of the resistive state can be observed for HRS and LRS, which renders the developed memristor an interesting candidate for PE-based memory applications. Furthermore, a very high device on-/off ratio of 10^7 is observed in the device used for retention testing, with a HRS of 10^9 Ω and LRS of 10^2 Ω. These obtained values

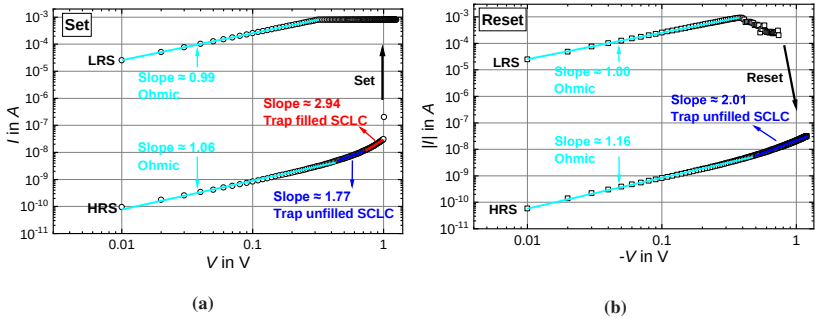


Figure 4.9: Double-logarithmic $I - V$ plot for conduction mechanism investigation. **(a)** Set process investigation including the linear fitted curves and corresponding slopes over different voltage regions. **(b)** Reset process investigation, including the linear fitted curves and corresponding slopes, over different voltage regions. Adapted from [203], © 2021 AIP Publishing.

are comparable to memristors fabricated with advanced manufacturing processes, such as enhanced atomic layer deposition [210].

For investigation of the conducting mechanism, during an applied voltage to the device, the $I - V$ curves of the set and reset process over its absolute values are plotted on a double-logarithmic scale in Figure 4.9. To obtain the conduction mechanism, linear fitting over different resistive states and voltage regions of the $I - V$ curves is performed. The obtained slopes of ≈ 1 in both, set and reset processes at LRS, are in agreement with Ohmic conduction [211]. The high current at LRS is contributed to high conductivity, which indicates formation of conducting silver filaments in the ZnO layer.

In contrast to the LRS, which is governed by a single mechanism, the fitting results of HRS, incorporating multiple slope values, can be linked to trap-controlled space-charge limited conduction (SCLC) [212]. The conduction behavior of HRS is investigated for different voltage regions. In the lower voltage region, in the set process, the fitted curve reveals a slope of ≈ 1.06 and the $I - V$ curves fit Ohm's law. In this low electric field regime, the current can be attributed to the minuscule amount of thermally excited charge carriers in the active layer [213]. As a consequence, only a small magnitude of current, compared with that of

LRS, can be observed. As the applied voltage increases, the electrons from the metallic electrode can be injected into the ZnO layer and partially fill the traps, which leads to a slight growth in conductance, at increased fitted line slope of ≈ 1.77. This behavior in the $I - V$ curve can be attributed to trap-unfilled space-charge limited conduction, with $I \propto V^2$ and is within the triangle region, as discussed by Lampert [214]. With increasing external electrical field, the electrons originating from the electrode fill up the traps in the active layer, which results in an exponential increase of current that leads to a fitted curve slope of 2.94. This indicates a transition of trap-unfilled to trap-filled SCLC. The observed $I - V$ relationships of the HRS relate to the three stages of SCLC, which is summarized in [214, 215]. For the HRS in the reset process an absence of trap-filled SCLC attributes to the abrupt rupture of the CFs, which does not provide enough time for electrons to fill up the traps completely. The different conduction mechanisms of HRS and LRS support the formation and rupture of CF in ZnO to achieve the resistive switching of the inkjet-printed memristor studied in this work.

4.3 Conclusion

In this chapter, the fabrication routine for inkjet-printed top-gate bottom-contact stack EGTs on laser-structured substrates is shown. All further circuits and systems developed in this thesis, incorporating EGTs, are based on the shown manufacturing workflow. Current-voltage measurements show that printed EGTs on laser-ablated substrates perform similar to lithographically structured ITO substrates.

Furthermore, an inkjet-printed memristor consisting of a Ag/ZnO/Au material stack, is presented. The device is highly suitable for memory applications due to its low operation voltage, high resistance on/off ratio of 10^7, its high retention time, exceeding 10^4 seconds and shows reliable resistive switching over 50 cycles. From the obtained $I - V$ curves, the device shows ECM-cell type and bipolar switching behavior, which suggests filament forming due to silver ion migration within the poly-crystalline zinc oxide storage layer. The conduction mechanisms

of the device were studied. Variations in inkjet-printed memristors furthermore provide a basis for novel hardware-based security applications.

5 Inkjet-Printed Circuits

The investigated inkjet-printed circuits in this chapter focus on PE-enabled solutions regarding sustainable energy and hardware-based security using EGTs, which were shown in Section 4.1. Low alternating voltage rectification can be achieved by employing near-zero threshold voltage diode-connected EGTs in a bridge-configured full-wave rectifier. The circuit shows a minimal forward voltage loss and allows to process low alternating voltages, produced by vibration energy harvesters. In order to provide comparability of the obtained printed rectifier results, several performance metrics are investigated to provide a benchmark for printed low-voltage rectification circuits.

To enable hardware-based security, the focus is on physically unclonable function circuit architectures, which deploy a PE-based core circuit as intrinsic variation source. The proposed designs are verified using electrical simulation. First, a printed crossbar PUF is proposed and evaluated with respect to PE-based design constraints. As proof of concept, a printed crossbar PUF core is fabricated and experimentally verified.

As second PUF implementation, the differential circuit (DiffC)-PUF is developed and investigated. The DiffC-PUF utilizes inverter structures to generate the response and is further used as intrinsic variation source for holistic hybrid PUF deployment. In a first step the PE-based DiffC-PUF core is fabricated and investigated as a proof of concept.

5.1 Inkjet-Printed Low-Voltage Rectifier

The results in this section were reported in [80].

To provide inkjet-printed low-voltage rectification, diode-connected EGTs with near-zero threshold voltage are used in a full-wave bridge rectifier. Diode-connected transistors are realized by connecting the drain (D) and gate (G) terminals, which results in a two-terminal device with a diode-like behavior (see Figure 5.1), however at a reduced steepness in the $I - V$ characteristics in comparison to diodes.

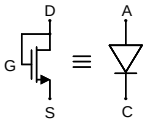
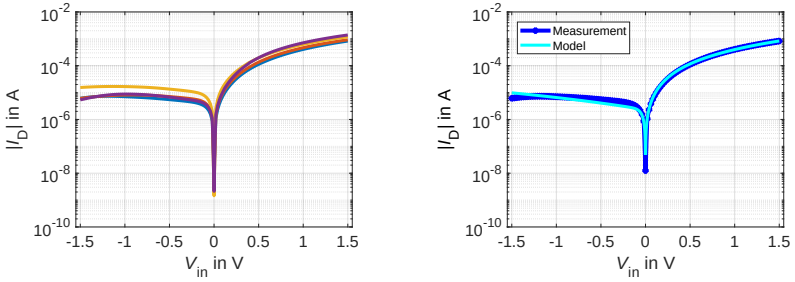


Figure 5.1: Schematic for a diode-connected EGT in comparison to a diode. Drain (D), gate (G) and source (S) terminals of the EGT are labeled. The corresponding diode anode (A) and cathode (C) terminals are labeled.

Figure 5.2a shows four measured $I - V$ curves of near-zero threshold voltage, diode-connected EGTs with a channel width $W_\mathrm{T} = 200\,\mu\mathrm{m}$ and length $L_\mathrm{T} = 90\,\mu\mathrm{m}$, at RH = 60 %. The device with the highest on-current reaches $1.39\,\mathrm{mA}$ at $1.5\,\mathrm{V}$ input voltage and $-6\,\mu\mathrm{A}$ at $-1.5\,\mathrm{V}$, resulting in a current on-/off ratio of $> 10^3$.

To provide a simulation model for diode-connected EGTs with near-zero V_th, a curve is fit with an extended Enz-Krummenacher-Vittoz (EKV) model for EGTs, developed by Rasheed et al. [82]. The extracted threshold voltage for the fitted device is $-50\,\mathrm{mV}$, whereas the current on-/off ratio is 10^2 at $\pm 1.5\,\mathrm{V}$. The schematic and a stitched microscopic image at 5× optical magnification of the fabricated full-wave bridge rectifier is shown in Figure 5.3. In the schematic, the highlighted blue area shows the inkjet-printed part.



(a) **(b)**

Figure 5.2: Near-zero threshold voltage, diode-connected EGT $I - V$ curves plotted on semi-logarithmic scale over the absolute drain current and EKV model fit. **(a)** Four measured diode-connected near-zero V_{th} EGT $I - V$ curves with a channel width $W_T = 200\,\mu m$ and length $L_T = 90\,\mu m$ at RH = 60 %. **(b)** Fitted EKV model curve over one of the measured diode-connected EGT. Adapted from [80], © 2020 IEEE.

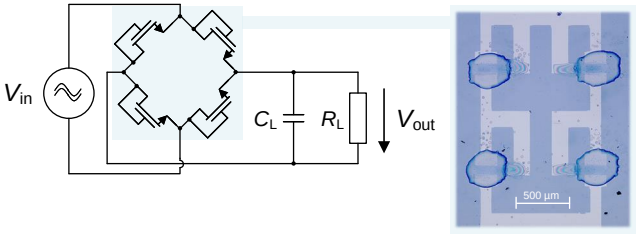


Figure 5.3: Schematic for the diode-connected EGT full-wave rectifier, including the externally connected capacitor and resistive load. The light blue shaded area marks the inkjet-printed part. A microscopic image of the inkjet-printed full-wave rectifier is shown. Adapted from [80], © 2020 IEEE.

For measurements, a sinusoidal input voltage with an amplitude of $V_{in} = 1\,V$ is generated by a Keithley 3390 function generator. The output waveform of the full-wave rectifier is measured with a Yokogawa DL6104 oscilloscope. To measure the frequency dependent performance of the rectifier, frequencies from 10 Hz to 20 kHz are used. To evaluate the rectifier performance metrics over different load conditions, external discrete resistors and capacitors are attached. Therefore, load resistors R_L, ranging from 5 kΩ to 1 MΩ, are used. These values comply with

other rectifier works in the field of energy harvesting [216]. As load capacitors C_{L}, $20\,\mathrm{pF}$ and $10\,\mu\mathrm{F}$ are utilized to observe both, ripple and smoothed, output voltages (V_{out} and $V_{\mathrm{out,smooth}}$), respectively.

In Figure 5.4 the ripple and smoothed output voltages of the rectifier, with R_{L} = $1\,\mathrm{M\Omega}$ at $10\,\mathrm{Hz}$, $1\,\mathrm{kHz}$ and $10\,\mathrm{kHz}$ are visualized. Optimal rectification can be observed at $10\,\mathrm{Hz}$, with a forward-voltage loss over the full-wave rectifier of $\approx 140\,\mathrm{mV}$. To further visualize simulation capabilities of the capacitive modeling approach by Feng et al. [84], the simulated transient rectifier output voltage at $10\,\mathrm{Hz}$ is also visualized.

With increasing frequency, the rectification process is degrading. At $1\,\mathrm{kHz}$ input frequency, the output of the rectifier is skewed and negative amplitude parts start to appear, as the transistors start to work in the non-quasi-static state. The transition of the channel fails to follow the applied gate voltage at increased frequencies, due to the finite ionic mobility of the electrolyte, leading to a decline of the channel conductivity and consequently higher signal loss [81]. The skewed amplitude parts are further contributed to the difference of AC characteristics between devices, which is affected by the thickness variation of the electrolyte insulator introduced in the printing process. The negative amplitude parts can be attributed to capacitive shunting caused by the EDL, which also reduces the DC output voltage. At a frequency of $10\,\mathrm{kHz}$, as shown in Figure 5.4c, the capacitive shunting through the insulator dominates the operation of the device and no rectification can be seen at the output [80].

A comprehensive investigation of the rectifier frequency response is shown in Figure 5.5a, with respect to the DC output voltage, which was calculated according to Equation 5.1.

$$V_{\mathrm{DC}} = \frac{1}{T} \int_0^T v_{\mathrm{out}}(t)\, dt \tag{5.1}$$

At frequencies below $300\,\mathrm{Hz}$, the rectifier generates almost a constant DC output voltage over various load resistances. As the frequency increases, a drop in

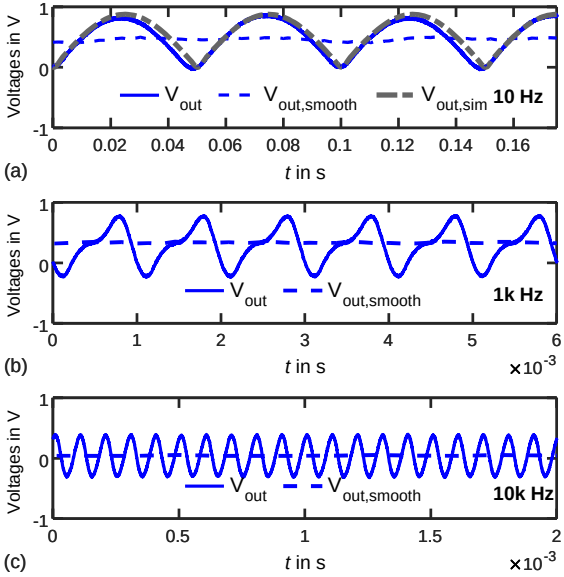


Figure 5.4: Frequency dependency of the full-wave rectifier. **(a)** Rectifier output voltages V_{out}, $V_{\text{out,smooth}}$ and $V_{\text{out,sim}}$. **(b)** Rectifier output voltage at 1 kHz. **(c)** Rectifier output voltage at 10 kHz. Adapted from [80], © 2020 IEEE.

the output voltage can be seen. The cutoff frequency of the rectifier can be determined at $\approx 300\,\text{Hz}$. The frequency dependent behavior is mainly limited by the charge speed of the gate resistance and terminal capacitance, while the operation of the device has not reached its transition frequency. However, in this region, especially vibration energy harvesters are functional [97]. Furthermore, Figure 5.5a shows the relationship between V_{DC} and the load resistance. In particular, with a load resistance of $1\,\text{M}\Omega$, the measured value of the DC output is very close to the theoretical maximum produced by an ideal, lossless rectifier, which is $V_{\text{DC,max}} = 2V_{\text{AC}}/\pi = 0.637\,\text{V}$ with $V_{\text{AC}} = 1\,\text{V}$ [217]. This is due to the near-zero V_{th} diode-connected EGTs. The remaining voltage loss is mainly contributed to the on-resistance of conducting devices. With a smaller load resistance, the voltage drop over the on-resistance of the channel is increased due

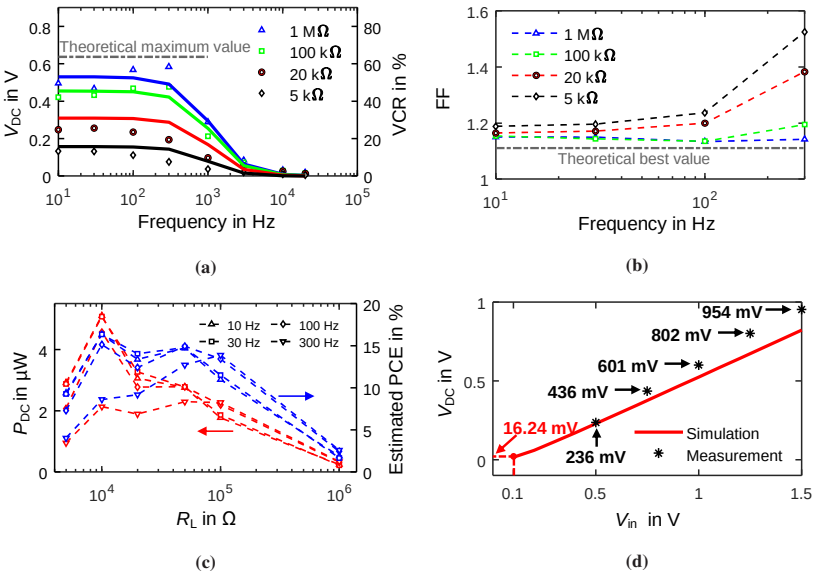


Figure 5.5: Rectifier performance metrics. **(a)** Output voltage V_{DC} and corresponding voltage conversion ratio, as a function of the input frequency, measured with various load resistors R_L. Solid lines represent simulation results whereas the dots are measurement results. **(b)** Form factor of the inkjet-printed full-wave rectifier below its cut-off frequency. **(c)** Rectifier output power and estimated PCE. **(d)** Output voltage V_{DC} with respect to input voltage amplitude, incorporating measurements and simulation results, at $R_L = 1\,\mathrm{M\Omega}$ at 10 Hz. Adapted from [80], © 2020 IEEE.

to increased on-current. Hence, a decrease in the output voltage can be seen [80]. Additionally, the dotted parts show measurement results, whereas the solid lines are simulation results. The voltage conversion ratio (VCR) is shown on the right hand side of the plot.

To address the efficiency of the rectification process, the form factor (FF) is calculated, whereas a lower FF indicates a better result [217, 218]. The FF of the

rectifier is given as the ratio of the root mean square (RMS) and DC voltage, as shown in Equation 5.2.

$$\mathrm{FF} = \frac{V_{\mathrm{RMS}}}{V_{\mathrm{DC}}} \tag{5.2}$$

with

$$V_{\mathrm{RMS}} = \sqrt{\int_0^T \frac{1}{T} v_{\mathrm{out}}^2(t)\, dt} \tag{5.3}$$

The FF is calculated for measurements below the cut-off frequency and visualized in Figure 5.5b, whereas the theoretical best value for an ideal full-wave rectifier with 1 V input amplitude can be determined as FF $\approx$ 1.11. In general, a lower form factor can be achieved at low frequency with large load resistance, which indicates a better efficiency in that region. Besides, the form factor achieved by all tested load resistances at low frequencies is well below 1.2, close to the theoretical best value of $\approx$ 1.11 based on the assumption of an ideal full-wave rectifier [217].

The output power and power conversion efficiency are also verified over frequency and load resistances, as visualized in Figure 5.5c. The output power is calculated according to Equation 5.4 and the PCE evaluated using Equation 5.5. The PCE gives a ratio of the converted, utilizable power at the circuit output, with respect to the power applied at the rectifier input. The higher the PCE, the lower the losses induced by the circuit.

$$P_{\mathrm{DC}} = \frac{V_{\mathrm{DC}}^2}{R_{\mathrm{L}}} \tag{5.4}$$

$$\mathrm{PCE} = \frac{P_{\mathrm{out}}}{P_{\mathrm{in}}} = \frac{V_{\mathrm{DC}}^2/R_{\mathrm{L}}}{\frac{1}{T}\int_0^T v_{\mathrm{AC}}(t) i_{\mathrm{AC}}(t)\, dt} \tag{5.5}$$

During the measurements $i_{\mathrm{AC}}(t)$ was not available, thus it is estimated as, $i_{\mathrm{AC}} = i_{\mathrm{load}} + i_{\mathrm{leak}}$, where i_{load} is the current through the load resistance and i_{leak} is the

summation of the two reverse biased EGTs during operation. From Figure 5.2, the leakage current can be assumed as $i_{\text{leak}} = 20\,\mu\text{A}$ under worst-case consideration. As shown in Figure 5.5c (red dashed line) more power is obtained using smaller load resistances. The rectifier can generate DC output power of more than $2.8\,\mu\text{W}$ using load resistances ranging from $5\,\text{k}\Omega$ to $20\,\text{k}\Omega$. For larger load resistances of $1\,\text{M}\Omega$, the output power is $< 1\,\mu\text{W}$. The overall estimated PCE (dashed blue line) is below $20\,\%$. This is influenced by the reverse leakage current. Near-zero V_{th} devices usually suffer from increased reverse leakage currents, which reduces power PCE in rectifier structures. In particular, at the load resistance of $10\,\text{k}\Omega$, the DC output power reaches the maximum of $5\,\mu\text{W}$, where the load resistance is close to the internal resistance of the rectifier. This value can be interpreted as the effective load resistance of the rectifier circuit, which is an important metric to estimate the circuit performance in various applications. In a last step the minimum input voltage amplitude rectification possibility of the circuit with $R_{\text{L}} = 1\,\text{M}\Omega$ and at $10\,\text{Hz}$ operating frequency, is verified. The rectifier was verified experimentally down to $V_{\text{in}} = 500\,\text{mV}$. Using the simulation, the minimum input voltage amplitude, where the rectifier is capable to deliver a rectified output voltage, is at $V_{\text{in}} = 100\,\text{mV}$, as visualized in Figure 5.5d.

5.2 Inkjet-Printed Low-Voltage Security Circuits

In the following, two inkjet-printed PUF implementations are proposed and discussed. Both PUF implementations follow the concept of analog Si-based PUFs, exploiting sensed differences in $I - V$ characteristics of inkjet-printed EGTs. Inkjet-printed EGTs offer an interesting source for intrinsic variation, due to their low operating voltage capabilities. Threshold voltage variation is visible in differing drain current of devices [83].

Both printed PUF core implementations are based on single stage circuits. This helps to increase PUF core yield. For sequential circuits variation increases the chance of circuit malfunction and are avoided. The functionality for bit generation

is similar for both PUF implementations. The control logic can be implemented in silicon, which allows to minimize the systematic error of the control logic. Furthermore, this hybrid system approach allows for split-manufacturing, whereas the printed PUF core can be attached on a the physical entity, which hosts the control logic, such as a PCB or an IC before PUF commission in a decentralized environment.

The first investigated PUF implementation is based on a crossbar architecture, incorporating positive V_{th} diode-connected EGTs. The printed crossbar PUF is first verified by PUF metric evaluation via electrical simulation. As a proof of concept, the printed crossbar PUF core is fabricated and measured. The second PUF implementation is based on a differential circuit architecture incorporating inverter structures. The DiffC-PUF is evaluated by electrical simulation and proof of concept implementation of the PE-based PUF core.

5.2.1 Printed Crossbar PUF Architecture

Parts of the results in this section were reported in [219].

Crossbar architectures offer straightforward high density device integration, which comes in handy in constrained PE-based environments. In the following, a crossbar architecture utilizing diode-connected EGTs is used as PUF core to enable high response bit width PUFs. In this work, primary intrinsic variation of the printed crossbar PUF core is evaluated.

The layout of the crossbar integrated diode-connected EGT is shown in Figure 5.6a. The material stack for fabrication is identical to EGT fabrication, as shown in Section 4.1. In order to enable crossbar architectures, crossovers for bit- and wordlines are required. Therefore, an inkjet-printable polyvinyl alcohol (PVA)-based insulator is used [220]. The insulator fluid formulation is given in the Appendix.

The crossbar addressing and readout is based on a floating biasing scheme, as visualized in Figure 5.6b. Biasing is achieved by grounding the bitline and

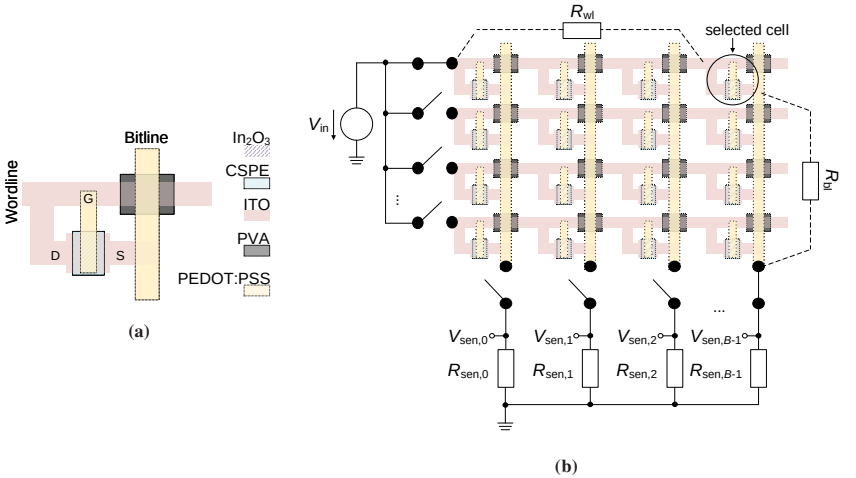


Figure 5.6: Printed crossbar layout. **(a)** Layout for crossbar integrated, diode-connected, EGT cell. The drain (D), gate (G) and source (S) terminals are labeled. **(b)** Diode-connected EGT crossbar single cell biasing scheme. Adapted from [219], © 2021 IEEE.

applying an input voltage V_{in} at the corresponding wordline [221]. All other nodes are kept floating, using switches. Each bitline is terminated with a sense resistor R_{sen}. For EGTs with positive threshold voltages, the devices in diode-connection are working in active region, as $V_{\text{DS}} = V_{\text{GS}}$, with $V_{\text{ov}} = V_{\text{GS}} - V_{\text{th}} \leq V_{\text{DS}}$, where V_{ov} is the transistor overdrive voltage. In Figure 5.6b, the $(0, B-1)$-th device is selected and grounded for reference. The PEDOT:PSS-based, inkjet-printed bitlines, in combination with the sense resistors lead to line resistances and cause source-degeneration in the EGT, which decreases its square law drain current relation. Especially in the upper wordline devices, which are subject to long bitlines and thus increased line resistance, this effect is increased. Voltages over unselected wordline devices, which share the same bitline to the selected cell can lead to a current, which contributes to the overall sensed current. The corresponding sensable output voltage is $V_{\text{sen}} = (I_{\text{cell}} + I_{\text{res}}) \cdot R_{\text{sen}}$. Where I_{res} describes the sum of parasitic currents from residual EGT cells within the crossbar.

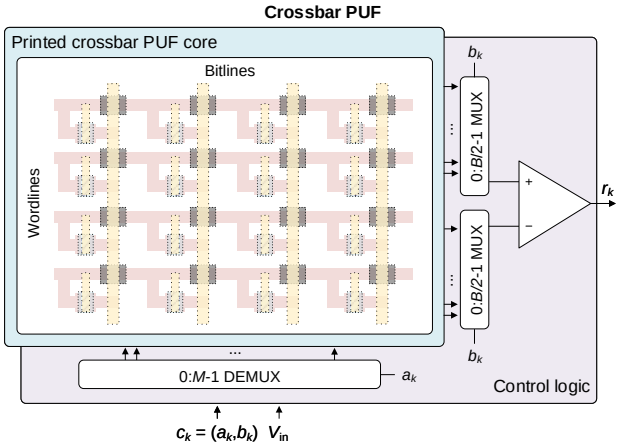


Figure 5.7: Printed crossbar PUF including addressing and readout schematic and PUF core. The diode-connected EGT crossbar builds the PUF core, whilst the external circuitry is the PUF control logic, which is required for CRP generation. Adapted from [219], © 2021 IEEE.

To verify the intrinsic variation capabilities in diode-connected EGTs in a crossbar architecture, the switches and sense resistors are close-to-ideal devices. The on-resistance of the switches is $R_{\mathrm{sw,on}} = 10\,\Omega$ and the off-resistance is $R_{\mathrm{sw,off}} = 1\,\mathrm{G}\Omega$. For the sense resistors, values of $R_{\mathrm{sen}} = 10\,\mathrm{k}\Omega$ are chosen.

The printed crossbar PUF implementation is investigated by simulation. Therefore, a 8×8-cells crossbar testbench, including 64 EGT cells, is set up in Cadence Virtuoso. For EGT simulation, the extended EKV and variation model, developed and implemented in Verilog-A by Rasheed et al. [82, 83], is utilized. To enable converging transient simulation, a $1\,\mathrm{pF}$ capacitor is added at the gate-source terminal of the EGT. The later utilized voltages for the printed crossbar PUF are settled constant voltages. Furthermore, the EGT drain current temperature coefficient approach for temperature dependability simulation by Erozan et al. [197] is used. For simulation, the geometrical settings for the EGT are $W_{\mathrm{T}} = 200\,\mu\mathrm{m}$ and $L_{\mathrm{T}} = 40\,\mu\mathrm{m}$. The chosen input voltage is $V_{\mathrm{in}} = 1\,\mathrm{V}$. For thin-film resistance of the bit- and wordlines three dimensional thin-film resistive behavior, according

to Equation 5.6, is given. With L_{tf} is the length, W_{tf} the width, t_{tf} the thickness, and ρ_{tf} the specific electrical resistance of the thin-film.

$$R_{\mathrm{tf}} = \rho_{\mathrm{tf}} \frac{L_{\mathrm{tf}}}{W_{\mathrm{tf}} \cdot t_{\mathrm{tf}}} \tag{5.6}$$

For PEDOT:PSS bitline resistance ($R_{\mathrm{bl,cell}}$), each resistive strip adds up a resistive value of $4.5\,\mathrm{k}\Omega$ per cell. The ITO wordline resistance ($R_{\mathrm{wl,cell}}$) is $700\,\Omega$ and also adds up with length per cell. The line resistances are labeled as R_{wl} for the wordline resistance and R_{bl} for the bitline resistance. The values increase with increasing line length and at increasing crossbar size. The system implementation schematic can be seen in Figure 5.7, where the k-th sub-challenge c_k includes the cell address tuple (a_k, b_k), representing an addressed wordline and the bitline block with $a_k = \{0, 1, 2, ..., M-1\}$ and $b_k = \{0, 1, 2, ..., B/2-1\}$. Therefore, one demultiplexer (DEMUX) for wordline addressing and two multiplexer (MUX) for bitline addressing are deployed. Each pair of neighboring bitlines is compared and forwarded into the corresponding MUX. Whereas one MUX contains all odd-numbered bitlines and the other MUX all even-numbered bitlines. By addressing a block of two neighboring bitlines simultaneously, two V_{sen} voltages can be sensed at each bitline. Both V_{sen} voltages are forwarded to a comparator. Based on the voltage difference between the sensed voltages (ΔV_{sen}), a corresponding k-th sub-response r_k is generated at the comparator output. This process is sequentially iterated over all bitline blocks and wordlines for each printed crossbar PUF instance, in order to generate R. With this addressing and readout scheme, a $L_{\mathrm{max}} = \frac{M \cdot B}{2}$ bit wide PUF response can be generated, where M is the amount of wordlines and B the amount of bitlines. With the 8×8-cells crossbar arrangement, a single 32-bit wide PUF response can be generated.

5.2.2 Simulation-Based Printed Crossbar PUF Metric Evaluation

PUF metrics are calculated from Monte Carlo (MC) simulation results of sensed voltages. Therefore, 1,000 printed crossbar PUF cores, each containing a single 32-bit wide response, are generated (see Figure 5.8). The EGT variation model parameters can be seen in [83]. Next to the EGT variation, Gaussian variation for the ITO and PEDOT:PSS resistances for each cell are added, with three sigma variation at $\pm 10\,\%$, respectively. Variation in PEDOT:PSS is caused by the printing process and material solidification, ITO resistance and variation is also due to the laser ablation and subsequent heating process.

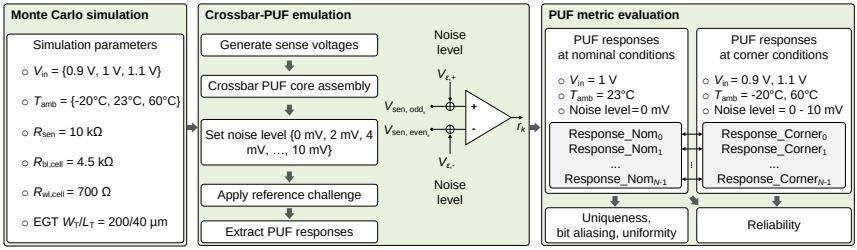


Figure 5.8: Printed crossbar PUF simulation methodology including noise level allocation and simulation parameter. Adapted from [129], ©2019 IEEE.

In a first step, the expected average voltage differences ΔV_{sen} and the standard deviation are investigated, as they provide the basis for response bit generation, which is shown in Figure 5.9. Using this implementation method, the optimal average voltage difference should be $0\,\text{V}$ for large enough sample sizes. A mean value $\neq 0\,\text{V}$ can indicate a systematical bias. The upper wordline devices show the smallest average voltage difference and standard deviation, whilst both values are increasing in the lower wordlines and are highest in the bottom wordline. This can be explained as upper wordline devices as well as currents from residual, unselected cells, are largely source-degenerated. Therefore, impact of V_{th} induced variation is also reduced as drain current is more linear. The sensed voltage

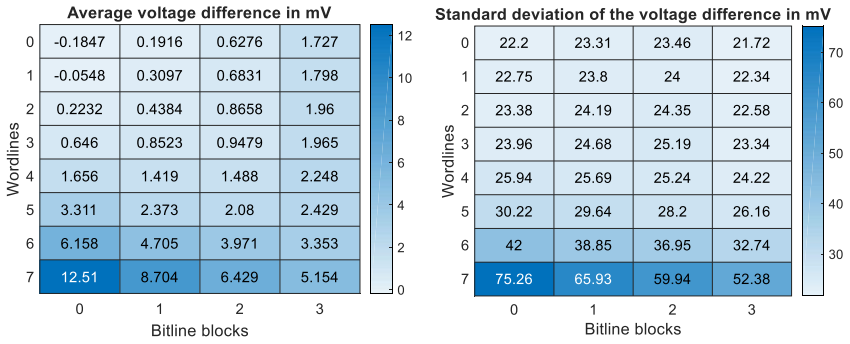
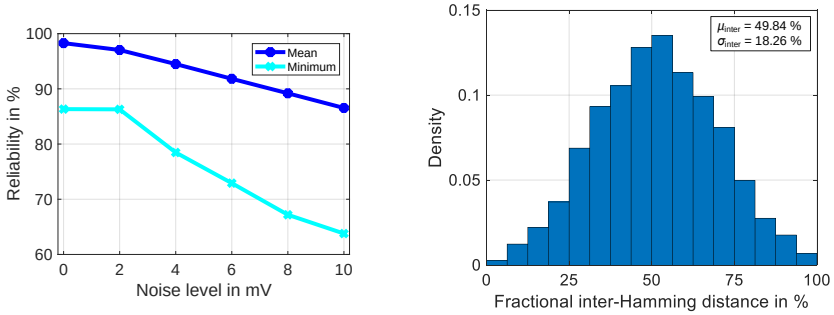


Figure 5.9: Voltage difference (ΔV_{sen}) investigations. **(a)** Average voltage difference of each bitline block. **(b)** Standard deviation of the voltage difference.

variation is more heavily affected by bitline resistance variation and residual currents. Whilst lowest wordline devices are more heavily affected by addressed transistor square law drain current behavior. At the same time, due to the increased wordline resistance and occurring IR drop, the applied voltage of the second addressed device is slightly reduced than the first device. However, at the same time, standard deviation of voltage differences are also increasing largely, which allows for lower constraints regarding safe detection of ΔV_{sen}.

To emulate the influence of systematic errors of the control logic on PUF metrics arbitrary error voltages, namely $V_{\varepsilon,+}$ and $V_{\varepsilon,-}$, are used in adaption to [129]. These voltages are placed at the positive (+) and negative (-) comparator input terminals, which allows to add or subtract static offset voltages from the sensed output voltages V_{sen}. The corresponding voltage levels at the comparator input are $V_{\text{comp},+} = V_{\text{sen,MUX1}_k} + V_{\varepsilon,+}$ and $V_{\text{comp},-} = V_{\text{sen,MUX2}_k} + V_{\varepsilon,-}$. For the following PUF metric investigation, values for $V_{\varepsilon,+}$ and $V_{\varepsilon,-}$, ranging from $0\,\text{mV}$ up to $10\,\text{mV}$ in $2\,\text{mV}$ steps, are chosen. The maximum error induced voltage difference $\Delta V_{\varepsilon} = V_{\varepsilon,+} - V_{\varepsilon,-}$ is $\pm 10\,\text{mV}$. The nominal operating conditions for the printed crossbar PUF are $V_{\text{in}} = 1\,\text{V}$ and $T_{\text{amb}} = 23\,^{\circ}\text{C}$. The reference response R_{ref} of the reference challenge C_{ref} is therefore extracted using these parameters.



(a) **(b)**

Figure 5.10: Printed crossbar PUF reliability and uniqueness evaluation. **(a)** Mean and minimum reliability including noise levels, ranging from $0\,\mathrm{mV}$ to $10\,\mathrm{mV}$. **(b)** The printed crossbar PUF uniqueness is $\mu_{\text{inter}} = 49.84\,\%$ with a standard deviation of $\sigma_{\text{inter}} = 18.26\,\%$. Adapted from [219], © 2021 IEEE

For reliability evaluation $\pm 10\,\%$ V_{in} variation and EGT temperature variation in the range of $T_{\text{amb}} = \{-20\,^{\circ}\mathrm{C}, 23\,^{\circ}\mathrm{C}, 60\,^{\circ}\mathrm{C}\}$ is used. Furthermore, the voltages $V_{\varepsilon,+}$ and $V_{\varepsilon,-}$ are used as noise level (NL) on both comparator inputs. The noise levels are utilized to emulate RMS noise voltage effects on the PUF reliability with both polarities as well as static offset voltages. Figure 5.10a shows the PUF mean and minimum reliability, over the noise levels. For a noise level in the range of $2\,\mathrm{mV}$, the reliability shows good results with a mean reliability of $97.03\,\%$ and a minimum reliability of $86.28\,\%$, which is almost identical without NL. The reliability decreases as noise levels increase.

For uniqueness investigation no NL is added to evaluate the internal obtainable uniqueness, excluding control logic impact. The corresponding uniqueness is shown in Figure 5.10b over the fractional inter-Hamming distance (inter-FHD). For the given printed crossbar PUF implementation, highly unique responses can be generated with a uniqueness $\mu_{\text{inter}} = 49.84\,\%$ and a standard deviation of $\sigma_{\text{inter}} = 18.26\,\%$, which is close to an optimal uniqueness of $50\,\%$. However, additional variation in the switches and sense resistors as well as full control logic, could further impact uniqueness.

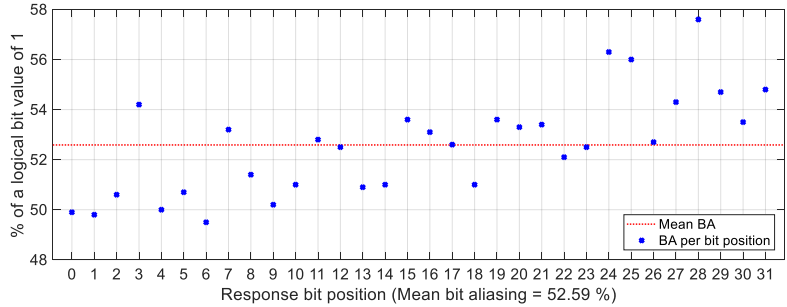


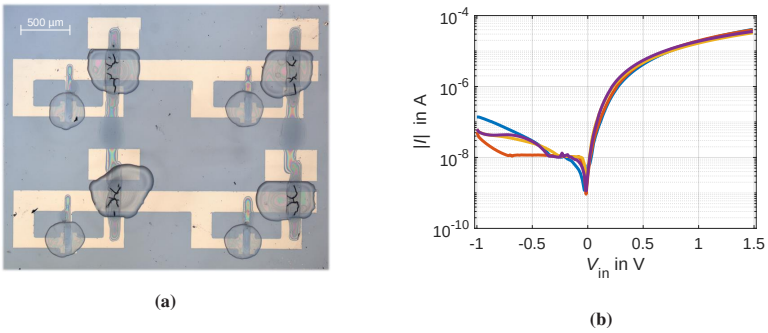
Figure 5.11: Printed crossbar PUF bit aliasing plotted over each response bit position, including the mean bit aliasing.

The printed crossbar PUF shows an mean bit aliasing of $52.59\,\%$ with a maximum BA of $57.60\,\%$ and minimum BA of $49.50\,\%$, as visualized in Figure 5.11. The mean uniformity is $52.59\,\%$ with a maximum at $100\,\%$ and a minimum of $0\,\%$. For bit aliasing and uniformity calculation no systematic error of the control logic is added. It shows that the printed crossbar PUF core responses are slightly systematically biased towards logic 1, which lowers the effective response bit width due to reduced entropy of the response. This effect can be explained by the impact of line resistances of the wordlines, which systematically decreases the generated drain current of the second bitline devices, which are routed to the negative comparator input terminal. The increased BA matches with the investigated average ΔV_{sen} values, as discussed before. This error can be minimized by reducing the wordline resistance. Furthermore, the bitline resistance can be reduced to enable larger scale crossbar implementations and reduce source-degeneration within the EGT cells.

Holistic investigation of novel material PUF implementations is important, as novel devices are often subject so specific fabrication related constraints. In this case, PEDOT:PSS-based bitline resistance is high, which leads to source-degeneration in the EGT cells and reduced drain-current. Also, wordline resistance generates a systematic bias within the crossbar, which leads to bit aliasing of the printed crossbar PUF. To improve bit aliasing in a crossbar configuration, lower resistance wiring concepts can be deployed.

5.2.3 Proof of Concept Printed Crossbar PUF Evaluation

To experimentally verify the printed PUF crossbar design, a 2×2-cells diode-connected EGT-based crossbar is fabricated. A stitched, microscopical image of the fabricated crossbar with $5\times$ optical magnification is shown in Figure 5.12a. The fabricated EGT has a channel width of $W_\mathrm{T} = 200\,\mu\mathrm{m}$ and a length of $L_\mathrm{T} = 60\,\mu\mathrm{m}$. By printing the PEDOT:PSS-based bitlines piecewise, new resistive strips per each bitline cell can be fabricated. The insulating PVA layer shows slight non-uniform surfaces, due to thick printed layers and corresponding material solidification dynamics, as the solvent evaporated. However, no negative impact on electrical performance regarding the resistive bitlines could be observed.



(a) **(b)**

Figure 5.12: Fabricated PUF crossbar and measured device characteristics. **(a)** Stitched microscopic image of a fabricated 2×2-cells, diode-connected EGT-based printed crossbar PUF at $5\times$ optical magnification. **(b)** Addressed crossbar cells $I - V$ curves, measured at RH $= 50\,\%$ on semi-logarithmic scale. Adapted from [219], © 2021 IEEE.

For electrical characterization $I - V$ curves of the corresponding addressed cells within the crossbar were read out using manual probes at RH = $50\,\%$. The measured $I - V$ curves include all possible currents from residual devices within the crossbar and as no sense resistor is attached, the effect of source-degeneration is slightly reduced. However, the obtained results highlight the capability for

diode-connected EGTs in a crossbar architecture for hardware-based security. The corresponding $I - V$ curves are shown in Figure 5.12b as semi-logarithmic plot. The average sensable current of the four integrated diode-connected EGT cells is $18\,\mu\mathrm{A}$ at $V_{\mathrm{in}} = 1\,\mathrm{V}$. The average reverse leakage current is $-78\,\mathrm{nA}$ at $-1\,\mathrm{V}$ reverse bias voltage.

For bit generation, as an example, for the shown $I - V$ curves in Figure 5.12b, the equivalent response is $R = (r_0, r_1) = (0, 0)$, as both right side devices show a higher drain current, than the left side devices at $V_{\mathrm{in}} = 1\,\mathrm{V}$ and would generate a higher V_{sense} voltage at the negative comparator input terminal. However, at $V_{\mathrm{in}} = 1.5\,\mathrm{V}$, the corresponding response would change to $R = (1, 0)$, as the curves cross, due to different slopes. It should be noted that this drain current behavior could be further exploited by adapting the CRP scheme, without changing the hardware.

5.2.4 Printed Differential Circuit PUF Architecture

The results in this section were reported in [129, 222].

Inverter structures offer straightforward I_{D} mismatch sensing, as the corresponding inverter output voltage is $V_{\mathrm{out}} = \mathrm{V}_{\mathrm{DD}} - I_{\mathrm{D}} \cdot R_{\mathrm{D}}$. This leads to different V_{out} per inverter, due to variation in both, I_{D} and R_{D}. Due to the additional supply voltage, amplification of V_{th} induced variations on I_{D} is possible, by biasing the inverter at high DC gain, where small V_{ov} differences can lead to increased differences in output voltages. However, this requires proper biasing strategies to ensure operating point stability.

As variation in PE is already increased, in comparison to Si-based electronics, no high gain inverter structures need to be deployed and variation can be detected at lower design constraints. This allows to utilize similar inverter biasing conditions over different substrates without requiring additional regulating mechanisms. Single inverter structures provide a good basis to enable high yield, inkjet-printed PUF cores.

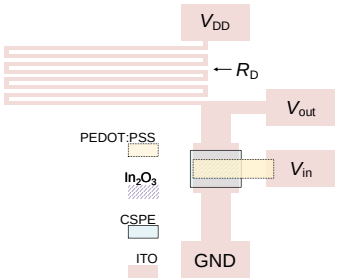


Figure 5.13: Inverter incorporating resistive ITO strip and EGT, including probing pad labels.

In the following, the differential circuit, or DiffC-PUF, based on a printed inverter array incorporating M inverters, as PUF core is investigated. Differential circuits are commonly used in communication technology to allow for small differential signal amplification for robust signal processing. In this work, common-mode input voltage biasing of the inverters is utilized, to generate a small, unpredictable differential output voltage.

The DiffC-PUF is capable to generate a high response bit width, whilst requiring a low amount of printed devices in the PE-based DiffC-PUF core. The control logic remains Si-based but can also be printed once printing technology matures. A single inverter is realized with an inkjet-printed EGT and a ITO-based resistive load R_D, utilizing both elements as a source of variability. Furthermore, complementary design remains challenging due to the largely reduced performance of inkjet-printed p-type metal oxide semiconductors. An arbitrary, standalone EGT-based inverter layout with labeled probe terminals and employed materials is shown in Figure 5.13.

The DiffC-PUF hybrid system architecture is shown in Figure 5.14. The input voltage V_in is used to bias two inverters at their input terminals simultaneously. The voltage difference between two addressed inverters ΔV_out of the DiffC-PUF core provides the basis for the generated response. For input signal routing, both DEMUXs identical output channels are tied together and routed to one

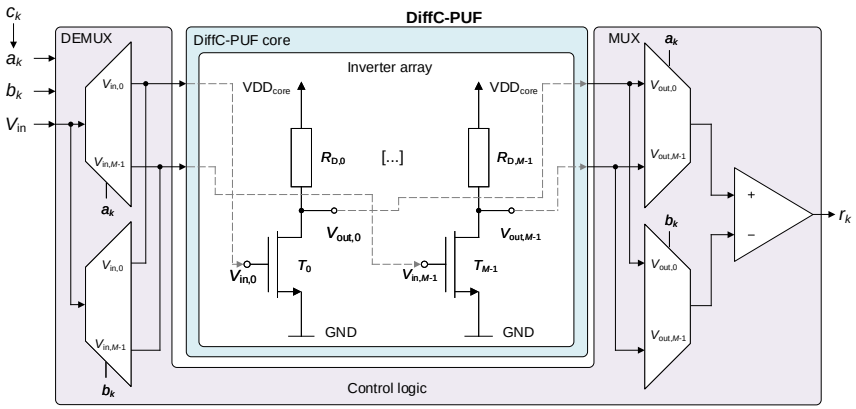


Figure 5.14: System architecture of the DiffC-PUF, including the inverter-based PUF core and the Si-based control logic. Adapted from [138] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

corresponding inverter input terminal. For output signal routing, each inverter output voltage is routed at both MUXs input terminals, as visualized in Figure 5.14.

The DiffC-PUF CRP generation is controlled by dynamic selection of the DEMUXs and MUXs. The sub-challenge c_k contains the DEMUXs and MUXs addresses a_k and b_k for inverter input and output voltage routing and can be expressed as $c_k = (a_k, b_k)$, with $(a_k, b_k) = \{0, 1, 2, ..., M-1\}$, as displayed in Figure 5.14. For each sub-challenge c_k, V_{in} is applied at the corresponding inverter inputs via the DEMUXs. Simultaneously, the MUXs are used to forward the corresponding inverter output voltages to the comparator input terminals. The comparator output equals the sub-response r_k. The differential sensing provides robustness against fluctuation in DiffC-PUF core supply voltage VDD_{core} and keeps ΔV_{out} stable over time [138]. Furthermore, self-comparison of V_{out} values increases the PE-based DiffC-PUF yield, due to probability for different mean output voltages per PUF core substrate, which would need to be evaluated before adding an external reference voltage on a comparator input terminal.

It is possible to reverse the challenge schedule from (a_k, b_k) to (b_k, a_k), which inverts the sub-response to $\overline{r}_k$. This can be used as system check at DiffC-PUF

core commissioning. Nonetheless, for DiffC-PUF CRP generation, lexicographic addressing of the inverters is used, excluding repetitions and reversed addressing. To increase the probability to obtain reliable responses, ΔV_{out} should be, on average, larger than the residual systematic error $\Delta V_{\varepsilon} = V_{\varepsilon,+} - V_{\varepsilon,-}$ of the control logic [129]. The full CRP per DiffC-PUF instance can be generated by sequentially applying all sub-challenges and reading out the sub-responses bitwise. For DiffC-PUF CRP generation a re-addressing mechanism is used, which allows to generate a maximum L_{max}-wide response, according to Equation 5.7.

$$L_{\text{max}} = \frac{M \cdot (M-1)}{2} \tag{5.7}$$

5.2.5 Simulation-Based DiffC-PUF Metric Evaluation

To determine the optimal input voltage for DiffC-PUF biasing, MC simulation is performed using the aforementioned, extended EKV and variation model for EGTs developed by Rasheed et al. [82, 83]. For EGT temperature variation, the drain current coefficient approach proposed by Erozan et al. [197] is used, as introduced before.

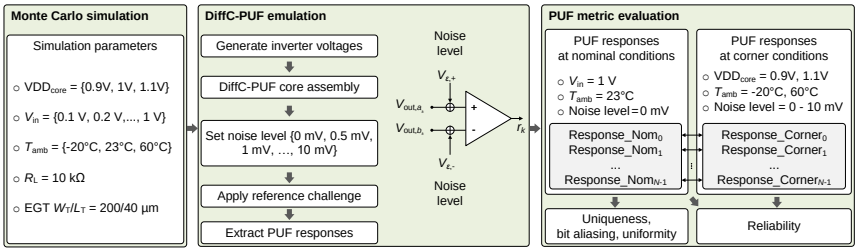


Figure 5.15: DiffC-PUF simulation methodology including noise level allocation and simulation parameter. Adapted from [129], ©2019 IEEE.

In the case of the DiffC-PUF, the PUF core inverters should provide the highest probability for variation in their output voltage V_{out}. This is achieved by investigation of proper inverter input voltage V_{in} biasing, as $V_{\text{out}} = f(V_{\text{in}})$. This increases

the probability that sensed voltage differences are high enough to reduce impact of systematic errors on PUF response generation. The input voltage ranging from $V_{\text{in}} = \{0\,\text{V}, 0.1\,\text{V}, ..., 1\,\text{V}\}$, and the relating output voltage behavior is systematically investigated. The general DiffC-PUF simulation methodology is shown in Figure 5.15. The geometrical design parameters for EGTs used in the simulation are $W_{\text{T}} = 200\,\mu\text{m}$ and $L_{\text{T}} = 40\,\mu\text{m}$. For the inverter load resistor, a value of $R_{\text{D}} = 10\,\text{k}\Omega$ is chosen. The DiffC-PUF core supply voltage is $\text{VDD}_{\text{core}} = 1\,\text{V}$. For simulation, the noise levels $V_{\varepsilon,+}$ and $V_{\varepsilon,-}$ are used, similar as introduced before, in order to emulate the control logic's systematic errors and RMS noise voltage. This leads to the equivalent input voltage at the comparator input terminal, according to $V_{\text{comp},+} = V_{\text{out},a_k} \pm V_{\varepsilon,+}$ and $V_{\text{comp},-} = V_{\text{out},b_k} \pm V_{\varepsilon,-}$. The noise levels used for systematic error evaluation range from $0\,\text{mV}$ up to $10\,\text{mV}$ with a step size of $500\,\mu\text{V}$, in a permutation-based order. The maximum error induced voltage difference using this strategy is ΔV_{ε} is $\pm 20\,\text{mV}$. For each simulation step, $Y = 1,200$ inverter output voltages are generated. This enables the construction of 150 DiffC-PUF cores including $M = 8$ inverters, which are capable to generate a 28-bit wide DiffC-PUF response, according to Equation 5.7.

Initially, the simulated DiffC-PUF core inverter output voltage is investigated regarding its variation, according to the sample standard deviation s, where $\overline{x}$ is the sample mean, as shown in Equation 5.8.

$$s = \sqrt{\frac{1}{Y-1}\sum_{i=1}^{Y}(x_i - \bar{x})^2} \tag{5.8}$$

Figure 5.16 shows V_{out} variation over V_{in} and VDD_{core} as surface plot, for each temperature level $T_{\text{amb}} = \{-20\,°\text{C}, 23\,°\text{C}, 60\,°\text{C}\}$. The largest s can be obtained at $V_{\text{in}} = 0.4\,\text{V}$, with $s = 253.94\,\text{mV}$ at ambient conditions.

To link standalone voltage investigations with PUF related performance metrics, further optimal input biasing voltage investigation is made by evaluating the reliability metric over the full V_{in} range. Figure 5.17 shows the mean reliability at increasing V_{in} and NLs split over each investigated temperature of

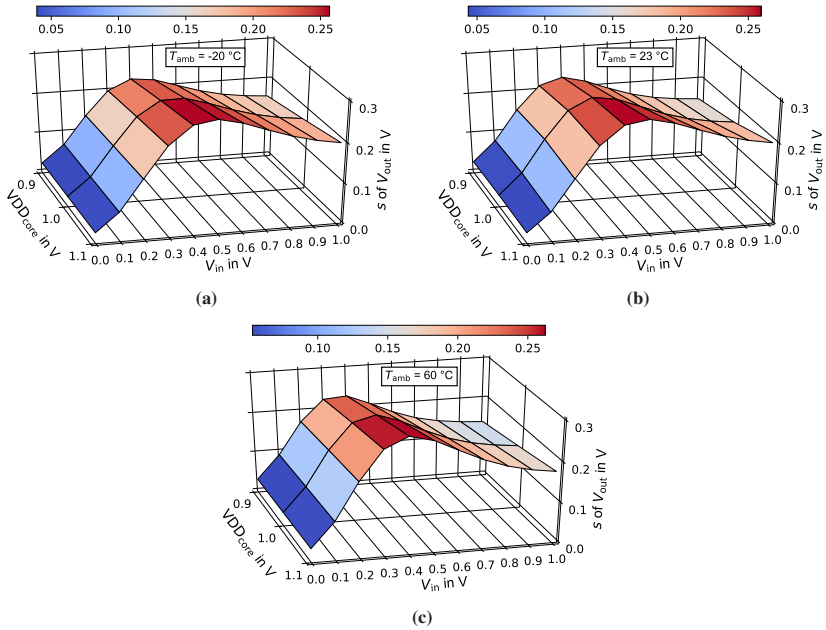


Figure 5.16: Standard deviation s of V_{out} over $T_{\text{amb}} = \{-20\,°\text{C}, 23\,°\text{C}, 60\,°\text{C}\}$, V_{in} and VDD_{core}, visualized as surface plot. **(a)** Surface plot at $-20\,°\text{C}$. **(b)** Surface plot at $23\,°\text{C}$. **(c)** Surface plot at $60\,°\text{C}$. Adapted from [129], © 2019 IEEE.

$T_{\text{amb}} = \{-20\,°\text{C}, 23\,°\text{C}, 60\,°\text{C}\}$ as surface plots. The plot starts at $V_{\text{in}} = 0.2\,\text{V}$, as mean reliability below this value is impracticable. With an increase in NL, the mean reliability decreases over all V_{in}. The surface plots indicate a peak in reliability for $V_{\text{in}} = 0.4\,\text{V}$ over all three temperature levels, which highlights the resilience of VDD_{core} and NL corner conditions of the investigated PUF. This cross check between the analog signal levels and the reliability metric further highlights that biasing of the DiffC-PUF at $V_{\text{in}} = 0.4\,\text{V}$ is beneficial. However, as temperature impacts drain current behavior, which heavily impacts especially high DC gain biased inverters, the DiffC-PUF reliability over all corners, including temperature is investigated. The mean and minimum reliability for each V_{in}, including temperature corner conditions, are shown in Figure 5.18. In Figure 5.18a the mean reliabilities over NL and V_{in} are visualized. The best mean reliability

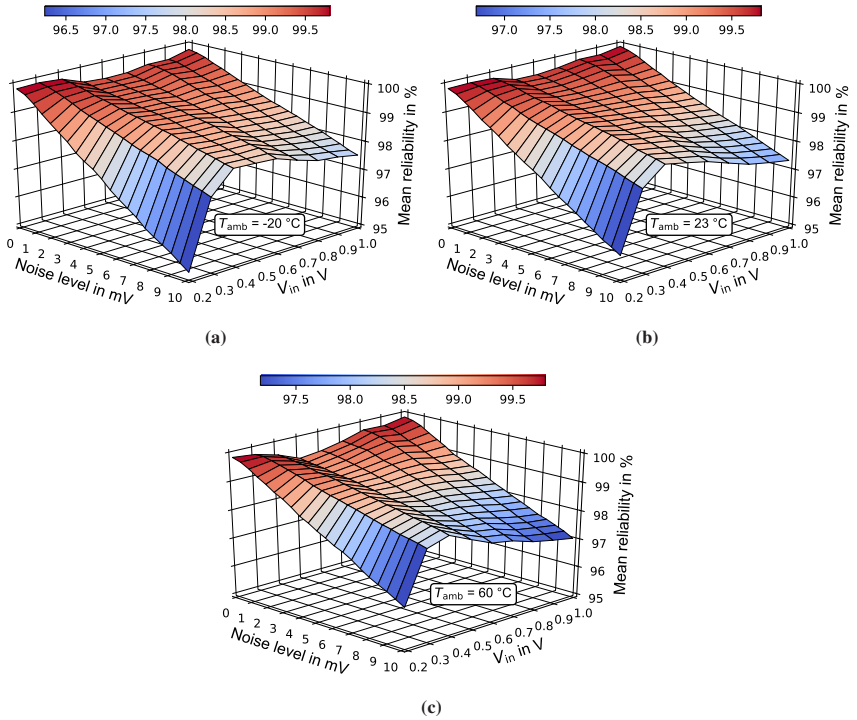
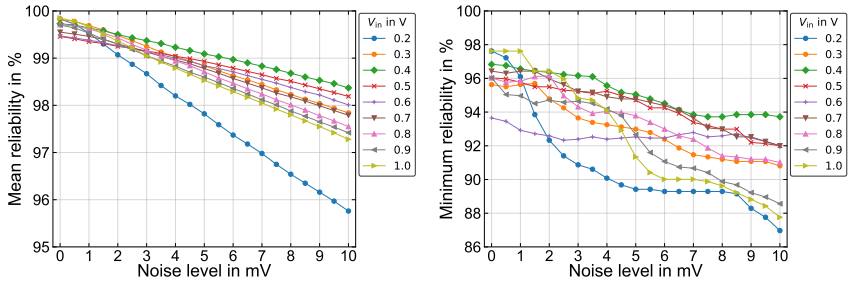


Figure 5.17: DiffC-PUF reliability over noise levels and temperature, visualized as surface plot. **(a)** Reliability surface plot at $-20\,°\mathrm{C}$. **(b)** Reliability surface plot at $23\,°\mathrm{C}$. **(c)** Reliability surface plot at $60\,°\mathrm{C}$. Adapted from [129], © 2019 IEEE.

performance can be achieved at $V_{\mathrm{in}} = 0.4\,\mathrm{V}$ over the full NL range, which also shows the highest resilience against high NL, due to the high probability that $\Delta V_{\mathrm{out}} \gg \Delta V_{\varepsilon}$, also at incorporated temperature variations. A similar behavior can be seen in Figure 5.18b for the minimum reliability, which shows the overall best performance, at $V_{\mathrm{in}} = 0.4\,\mathrm{V}$, especially at $\mathrm{NL} \geq 2\,\mathrm{mV}$. A comprehensive comparison between the obtained PUF metrics over all investigated biasing points is shown in Table 5.1 including the reliability, uniqueness and bit aliasing.



(a) **(b)**

Figure 5.18: DiffC-PUF reliability over V_{in} and NL. **(a)** Mean reliability. **(b)** Minimum reliability. Adapted from [129], © 2019 IEEE.

Table 5.1: DiffC-PUF security metrics over $V_{\text{in}} = \{0.2\,\text{V}, 0.3\,\text{V}, ..., 1\,\text{V}\}$ (NL for reliability metric: $\pm 10\,\text{mV}$). Adapted from [129], © 2019 IEEE.

V_{in}	Reliability		Uniqueness		Bit aliasing
	Mean	Min.	μ_{inter}	σ_{inter}	Mean
0.2 V	95.76 %	86.97 %	50.01 %	14.28 %	49.55 %
0.3 V	97.84 %	90.81 %	50.08 %	14.31 %	49.38 %
0.4 V	98.37 %	93.72 %	50.02 %	14.37 %	49.81 %
0.5 V	98.19 %	92.00 %	50.03 %	14.36 %	49.40 %
0.6 V	98.01 %	92.00 %	49.98 %	14.42 %	49.64 %
0.7 V	97.79 %	92.00 %	49.97 %	14.40 %	49.83 %
0.8 V	97.55 %	91.01 %	49.97 %	14.42 %	49.60 %
0.9 V	97.42 %	88.56 %	49.99 %	14.42 %	49.71 %
1 V	97.28 %	87.76 %	49.92 %	14.44 %	49.69 %

Figure 5.19 shows DiffC-PUF metrics evaluated at the obtained best input voltage biasing of $V_{\text{in}} = 0.4\,\text{V}$. The reliability (see Figure 5.19a) is plotted over the fractional intra-Hamming distance (intra-FHD) including all NL , the uniqueness (see Figure 5.19b) over the inter-FHD without NL and the corresponding bit aliasing (see Figure 5.19c) over each response bit position, also without NL. The mean reliability is at $98.37\,\%$ with a minimum reliability of $93.72\,\%$ at a worst case NL of $10\,\text{mV}$. With a uniqueness of $\mu_{\text{inter}} = 50.02\,\%$ and a standard deviation of $\sigma_{\text{inter}} = 14.37\,\%$, the DiffC-PUF is capable to generate unique responses, which makes it an ideal candidate for identification purposes. The mean bit aliasing

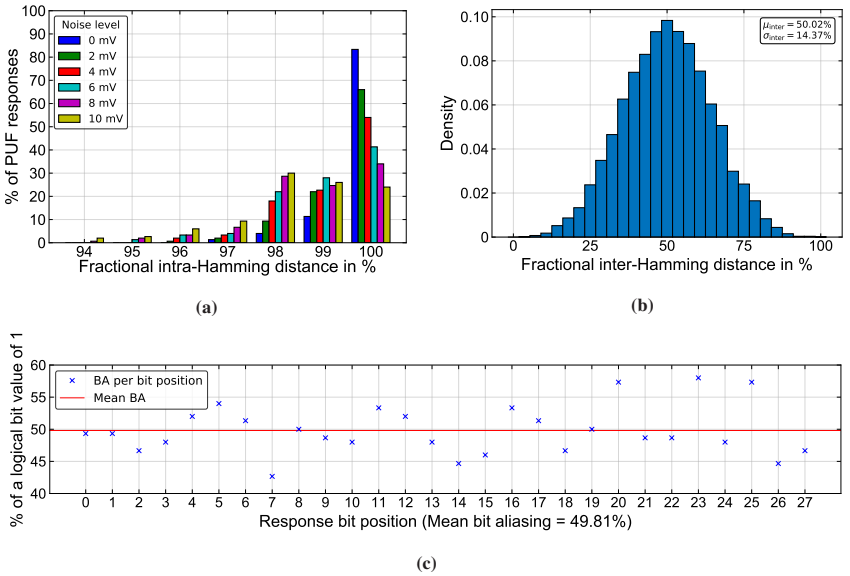


Figure 5.19: DiffC-PUF reliability uniqueness and bit aliasing at $V_{\text{in}} = 0.4\,\text{V}$. **(a)** Reliability plotted over the intra-FHD. **(b)** Uniqueness plotted over the inter-FHD. **(c)** Bit aliasing plotted over each response bit position, including mean bit aliasing. Adapted from [129], © 2019 IEEE.

at $V_{\text{in}} = 0.4\,\text{V}$ is $49.81\,\%$, with a maximum at $58\,\%$ and a minimum value of $42.67\,\%$, which shows that DiffC-PUF responses are not systematically biased and the response bit width can be fully utilized. The calculated uniformity of the DiffC-PUF at $V_{\text{in}} = 0.4\,\text{V}$ is $49.81\,\%$ with a minimum at $7.10\,\%$ and a maximum at $82.10\,\%$. This wide distribution is problematic for cryptographic applications, however the printed DiffC-PUF is intended to be used for identification and uniformity can be improved using post-processing [129, 138].

For further comprehensive best biasing investigation, the DiffC-PUF core biasing at the maximum inverter DC gain is evaluated. The maximum inverter DC gain, with the given inverter setup, is at $V_{\text{in}} \approx 0.48\,\text{V}$. Figure 5.20 shows the reliability over $V_{\text{in}} = \{0.4\,\text{V}, 0.48\,\text{V}, 0.5\,\text{V}\}$ as violin plot for direct comparison in reliability distributions. The mean reliability at $V_{\text{in}} = 0.48\,\text{V}$, with a NL of

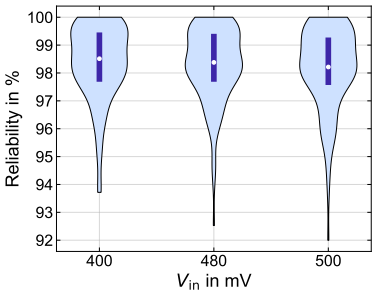
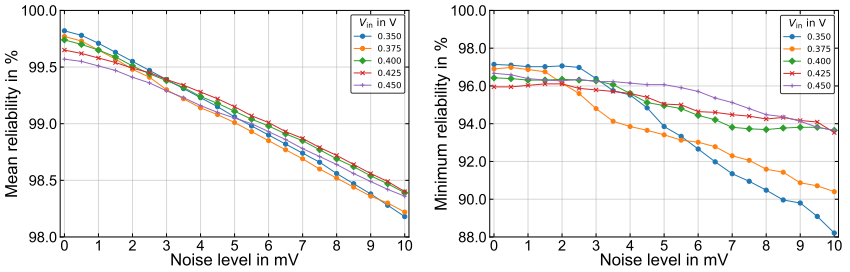


Figure 5.20: DiffC-PUF reliability distribution over $V_{in} = \{0.4\,V, 0.48\,V, 0.5\,V\}$, visualized as violin plot. Adapted from [129], © 2019 IEEE.

$10\,mV$, is $98.31\,\%$ with a minimum reliability of $92.53\,\%$. For both investigated input biasing voltages $V_{in} = (0.48\,V, 0.5\,V)$, the obtained reliability is slightly worse compared to the reliability obtained at $V_{in} = 0.4\,V$. The uniqueness at the maximum inverter DC gain biasing, is at $\mu_{inter} = 50.02\,\%$ with a standard deviation of $\sigma_{inter} = 14.37\,\%$. The mean BA is $49.76\,\%$ with a maximum at $60\,\%$ and a minimum of $44\,\%$. Whilst the uniqueness is identical to the values obtained at $V_{in} = 0.4\,V$, the BA is slightly degraded in comparison.

As $V_{in} = 0.4\,V$ shows the best overall PUF metrics, further fine tuned simulation around $0.4\,V$ is performed to evaluate the impact of V_{in} fluctuations on DiffC-PUF metrics. The reliability over the investigated voltage range of $V_{in} = \{0.35\,V, 0.375\,V, ..., 0.45\,V\}$, is evaluated, incorporating a $25\,mV$ step size.

Figure 5.21 shows the mean and minimum reliabilities over the NL. Reliability values over the investigated input voltage range show a high overall mean reliability exceeding $98\,\%$. At increased NLs $\geq 5\,mV$, input voltages at $V_{in} = (0.35\,V, 0.375\,V)$ perform slightly worse compared to input biasing at $0.425\,V$ and $0.45\,V$. Furthermore, the uniqueness and bit aliasing metrics over the given V_{in} range are evaluated and listed, next to the reliability metrics, in Table 5.2.



(a) **(b)**

Figure 5.21: DiffC-PUF reliability over $V_{\text{in}} = \{0.35\,\text{V}, 0.375\,\text{V}, ..., 0.45\,\text{V}\}$ and NL. **(a)** Mean reliability. **(b)** Minimum reliability. Adapted from [129], © 2019 IEEE.

Table 5.2: DiffC-PUF security metrics around $V_{\text{in}} = 0.4\,\text{V}$ (NL for reliability $10\,\text{mV}$). Adapted from [129].

V_{in}	Reliability		Uniqueness		Bit aliasing
	Mean	Min.	μ_{inter}	σ_{inter}	Mean
0.350 V	98.22 %	88.21 %	50.11 %	14.36 %	49.45 %
0.375 V	98.22 %	90.40 %	50.07 %	14.33 %	49.71 %
0.400 V	98.37 %	93.72 %	50.02 %	14.37 %	49.81 %
0.425 V	98.47 %	93.53 %	50.04 %	14.36 %	49.81 %
0.450 V	98.36 %	93.65 %	50.04 %	14.36 %	49.98 %

5.2.6 Proof of Concept DiffC-PUF Core Evaluation

To provide a proof of concept realization of the DiffC-PUF core, with respect to optimal input voltage biasing, a DiffC-PUF core incorporating eight inverters is fabricated and measured at RH $= 50\,\%$. The fabricated EGT channel width is $W_{\text{T}} = 200\,\mu\text{m}$ and its length $L_{\text{T}} = 100\,\mu\text{m}$, with a R_{D} of $10\,\text{k}\Omega$. The larger L_{T}, in comparison to the simulation, is due to more reliable fabrication at increased feature size.

The physical design of the printed DiffC-PUF core includes eight inverters on a $20\,\text{mm} \times 20\,\text{mm}$ - sized, ITO-covered, glass substrate, as visualized in Figure 5.22a. The equidistant and symmetrical inverter and input - / output (I/O) -

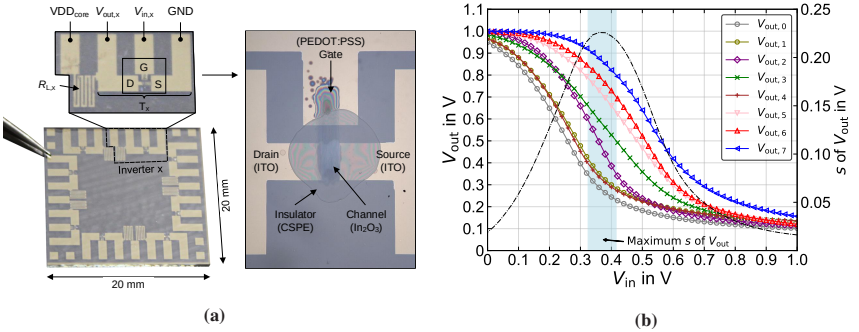


Figure 5.22: PE-based DiffC-PUF core on glass substrate. **(a)** Photograph of the fabricated DiffC-PUF core. **(b)** Measured inverter transfer curves, including the standard deviation of the incorporated inverters V_{out}. Adapted from [129], © 2019 IEEE.

terminal layout is used to minimize systematic variation in the ITO signal routing layer and reduce parasitic line resistance. Each line is provided standalone, which balances out possible voltage drops due to parasitic resistance in the supply voltage. Furthermore, it avoids crossovers during fabrication to maximize printed DiffC-PUF core yield. The design allows for standardized, seamless integration of the DiffC-PUF core into a Si-based environment, which will be discussed later. The maximum standard deviation of the output curves can be obtained at $V_{\text{in}} \approx 0.4\,\text{V}$ with $s = 225.92\,\text{mV}$, as shown in Figure 5.22b. The measured output curves match the simulated inverter behavior. As the printed DiffC-PUF core shows good performance with respect to PUF metrics and allows for minimized systematic variation in the layout, in a next step the printed DiffC-PUF core will be integrated into a Si-based control logic and evaluated on a larger scale.

5.3 Conclusion

In this chapter, circuits, based on low-voltage EGTs, are presented. This includes an inkjet-printed full-wave rectifier, which is capable to rectify small alternating voltages in the sub-volt region. Currently, for PE no possibility exists to rectify

low alternating voltages, due to high voltage drops over existing PE-based devices. The presented inkjet-printed full-wave rectifier benefits from near-zero V_{th} diode-connected EGTs. With the presented circuit, low alternating input voltages at frequencies < $300\,\text{Hz}$ can be rectified. This feature is of special interest for vibration energy harvesters, which operate in this frequency region and generate low alternating output voltages. The presented full-wave rectifier has been fully characterized. Furthermore, simulation results suggest operation of the circuit down to $V_{\text{in}} = 100\,\text{mV}$. Increased reverse leakage currents in the near-zero V_{th} devices reduce PCE. Increasing the PCE can be further obtained with devices offering a higher current on-/off ratio and active rectifier structures, as implemented in Si-based electronics.

Furthermore, two physically unclonable functions, realized with inkjet-printed EGTs, were developed and investigated. For both implementations, a simulation-based PUF metric evaluation approach along with proof of concept fabrication and measurements are made. A holistic PUF implementation approach is used to investigate control logic impact errors on standalone printed PUF core circuits. This enables a comprehensive PUF metric analysis. The obtained results cover the PUF reliability, uniqueness, bit aliasing and uniformity.

The first PUF implementation is based on printed EGT-cells in a crossbar architecture. The crossbar alignment allows for straightforward high density fabrication, which allows for full differential, high entropy response generation. However, the crossbar configuration suffers from increased PUF core bias, due to line resistance and residual currents within the system. Nonetheless, the printed crossbar PUF is capable to generate reliable, unique responses at a NL of $2\,\text{mV}$, with a mean reliability of $97.03\,\%$. The corresponding uniqueness at optimal conditions is $\mu_{\text{inter}} = 49.84\,\%$. A proof of concept implementation of a 2×2-cells crossbar PUF core shows that integrated EGT-cells can be utilized within this configuration for PUF purposes.

The second printed PUF implementation is based on a differential circuit architecture. The so-called DiffC-PUF allows for symmetrical layout and flip-chip integration and uses a re-addressing approach for PUF response generation, which

helps to reduce required printed components and increase overall system yield. First, an optimal inverter input biasing investigation is made, based on the expected inverter output voltages and corresponding DiffC-PUF metrics. It is found that at an input biasing voltage of $V_{\text{in}} = 0.4\,\text{V}$, the DiffC-PUF shows the best corresponding PUF operating conditions. The DiffC-PUF is capable to generate reliable, unbiased and highly unique responses. At $V_{\text{in}} = 0.4\,\text{V}$, the mean reliability at a NL of $10\,\text{mV}$ is $98.37\,\%$ with a nominal, mean uniqueness of $\mu_{\text{inter}} = 50.02\,\%$. The DiffC-PUF core is fabricated and evaluated as a proof of concept. The measured results match the simulation-based investigations.

6 Hybrid Systems

In this chapter, the developed systems are presented. The main focus is on the embedded DiffC-PUF as holistic system platform, which enables the usage of a PE-based DiffC-PUF core. Therefore, the full system setup including the required peripherals are shown. The system is commissioned with a Si-based PUF core and fully investigated with a focus on system design constraints and effects on PUF metrics. Furthermore, the embedded DiffC-PUF is implemented in form of a hybrid PUF, incorporating a PE-based DiffC-PUF core. The hybrid DiffC-PUF is also fully evaluated regarding its PUF security metrics. The shown approach allows for large-scale experimental validation, incorporating novel devices.

The results shown in this chapter were reported in [138, 200].

6.1 Embedded Differential Circuit Physically Unclonable Function Platform

To provide a holistic platform for physical, embedded DiffC-PUF deployment, further peripherals are required. This includes the control logic for signal routing as well as a microcontroller (μC) for CRP generation and communication with a personal computer (PC). An off-the-shelf development board (Silicon Labs EFM32LG-STK3600), which includes an EFM32 Leopard Gecko μC, is deployed. The control logic is a custom, self-built PCB, which is designed to minimize systematic variation impact, to generate unique and reliable DiffC-PUF responses.

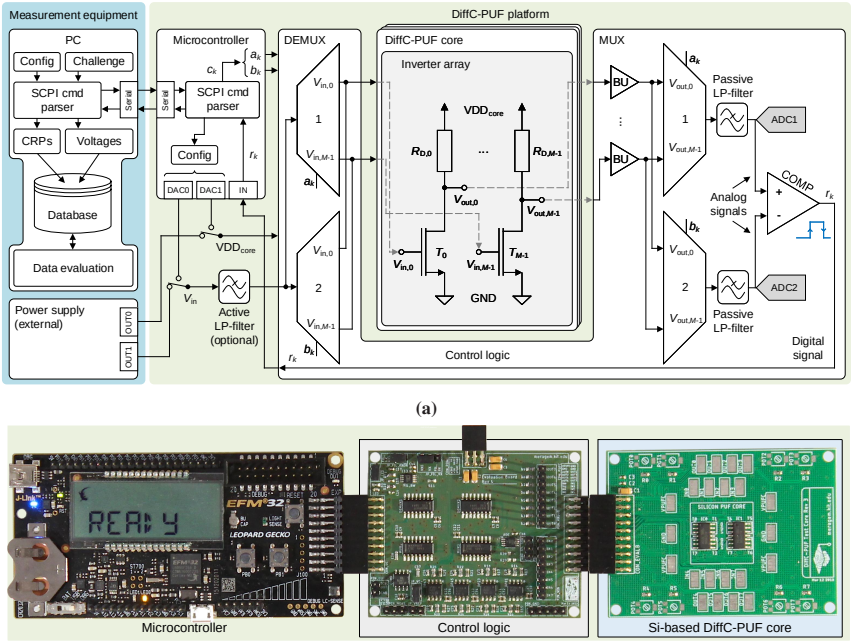


Figure 6.1: DiffC-PUF as a holistic embedded platform in a schematic view and as photograph. **(a)** Schematic for the DiffC-PUF, including the required peripherals for CRP generation. **(b)** Photograph of the DiffC-PUF as platform incorporating the EFM32LG-STK3600 development board, the control logic and Si-based PUF core. Adapted from [138] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

The embedded DiffC-PUF is built as modular platform to allow for an exchange in DiffC-PUF cores, whilst reusing the control logic and the µC. This further enables the usage of different technology nodes for the DiffC-PUF core, such as classical, discrete Si-based as well as low-voltage PE-based devices and reduces hardware manufacturing overhead at low cost. Figure 6.1a shows the overall system architecture of the DiffC-PUF, including the software control layer on the left hand side, which is part of the automated measurement equipment unit as well as control logic components for real system implementation. For PC $\leftrightarrow$ µC communication, Universal Asynchronous Receiver Transmitter as serial communication

interface is used. The Standard Commands for Programmable Instruments (SCPI) protocol is used to send commands to the platform [138]. An image of the full DiffC-PUF with Si-based PUF core attached, is shown in Figure 6.1b. The active components, deployed for the control logic, can be powered by the supply pins of the EFM32LG-STK3600 at $5\,\mathrm{V}$ and $3.3\,\mathrm{V}$. Furthermore, the EFM32LG hosts internal digital-to-analog converters (DAC), which can be used as programmable sources for the PUF core biasing voltage V_{in} and supply voltage $\mathrm{VDD}_{\mathrm{core}}$. External power supplies can also be used, based on preference.

The control logic includes an optional, second order Butterworth active low-pass (LP) filter in a Sallen Key topology [223], which can provide a known input and output impedance of the inverter input biasing voltage source. The active filter output incorporates an additional first-order passive RC-filter to suppress Sallen Key topology filter stopband attenuation. The optional input filter can be selected and bypassed, using jumpers. As the platform is mainly designed for low-speed, low-voltage PE-based devices, the input filter and the two passive low-pass filters, which are included in each readout path of the control logic, are set up with a cutoff-frequency of $f_c \approx 10\,\mathrm{kHz}$ to limit the overall system operating bandwidth. This helps to suppress high frequency thermal noise and high frequency switching regulator ripple from external power supplies, as higher bandwidth is not required for successful DiffC-PUF operation. Furthermore, the defined, limited bandwidth allows to use a ground plane in the PCB for improved DC voltage precision [224]. The DiffC-PUF is mainly biased at a constant input voltage, which should be easily adjustable at an acceptable rate. Nonetheless, each waveform can be applied to the input terminals, if required, to enable flexibility for different CRP generation schemes. For all following investigations, the optional input filter remains activated.

To reduce systematic variation in the control logic, each deployed active component for the control logic offers low leakage currents, high precision and is specified over a temperature range from $-40\,^{\circ}\mathrm{C}$ up to $85\,^{\circ}\mathrm{C}$. The employed thin-film resistors, within the control logic, have a variation of $0.1\,\%$ and a temperature coefficient of $25\ \mathrm{ppm}^{\circ}\mathrm{C}^{-1}$. Four identical analog multiplexers, where each contains eight channels, are used for input and output signal routing. For

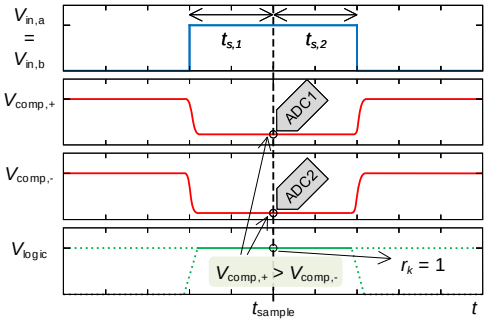


Figure 6.2: Schematical readout timing setup for the voltage levels and the corresponding output bit. Adapted from [138] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

input voltage routing, the device is configured as DEMUX and as MUX for output voltage routing, respectively. The control logic uses low input offset voltage (V_{os}) buffer amplifiers (BUs), which provide a defined, capacitive and resistive load to the DiffC-PUF core inverter outputs and isolate the intrinsic variation source from the control logic. A 12-bit analog-to-digital converter (ADC) allows to track the analog signals at the comparator input terminals, which are used to generate the PUF response bits, at a resolution of $500\,\mu\mathrm{V}$. Two of the ADC channels are used to track both comparator inputs, respectively. For robust measurement, each digitized ADC value is obtained by averaging eight measured samples. Tracking the voltage levels at the comparator input terminals helps to gain insight in applied voltage levels and eases in experimentally obtaining the minimum voltage difference, which can be safely detected to prevent flipping bits in the PUF response. Furthermore, it allows for correlating the applied voltages and obtained (sub)-response. The ADC communicates via an inter-integrated circuit data bus with the EFM32LG μC.

The μC controls the analog multiplexers according to the addresses included in the sub-challenge c_k. The sub-challenges are processed sequentially and the full binary PUF response is generated and sent to the PC by the μC along with the measured analog signal levels [138]. The timing of the DiffC-PUF response generation procedure can be defined through the $t_{s,1}$ and $t_{s,2}$ time delay parameters,

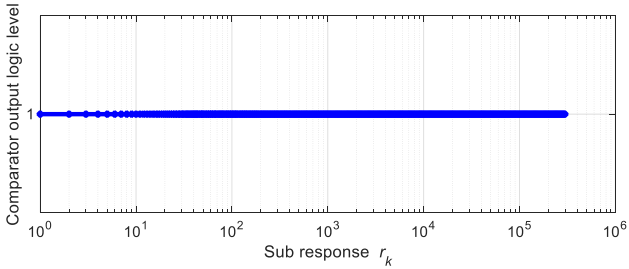


Figure 6.3: Comparator output, over the corresponding $298,200$ sub-responses r_k, during the prolonged continuous cycling test.

which affect ADC sampling time t_{sample}, as shown in Figure 6.2. The figure shows a schematic sampling process for obtaining the analog voltage levels and a response bit. The average measured power consumption of the DiffC-PUF control logic, operated at nominal conditions, over a CRP cycle is $\approx 35\,\mathrm{mW}$. The power consumption was obtained by measuring the current drawn from the supply voltages with two BBC Goerz MA5D multimeter.

For first commissioning of the control logic as standalone system, a prolonged continuous cycling test is performed. Therefore, the PUF core is disconnected and the DEMUX outputs are directly connected to the corresponding buffer amplifier input terminals, respectively. Thus, the input voltage can be directly sensed at the comparator input terminals. For powering of the control logic's active components, the supply pins of the EFM32LG-STK3600 with $5\,\mathrm{V}$ and $3.3\,\mathrm{V}$ are used. For input voltage routing the DAC of the EFM32 is used with a constant input voltage $V_{\text{in}} = 1\,\mathrm{V}$. Continuous CRP generation is performed over 10,650 cycles, in order to emulate standard DiffC-PUF CRP generation, incorporating a response bit width of 28-bit. Over the cycling time the comparator output and the comparator input voltages, which are in this case V_{in} at both terminals, are tracked.

The investigated ADC measurement result, which contains $298,200$ measured values of ΔV_{comp} shows a mean value for ΔV_{comp} of $82.04\,\mu\mathrm{V}$ and a standard deviation of $223.92\,\mu\mathrm{V}$, due to noisy least significant bit (LSB), as the resolution

limit of the ADC is at $500\,\mu\mathrm{V}$. The obtained values suggest that possible systematic bias in the control logic is small between both readout paths. Furthermore, the comparator output is tracked over all $298,200$ occurring sub-responses. The comparator output over the testing cycles is shown in Figure 6.3. As both input voltages at the comparator input terminals are assumed equal, the output is mainly affected by its V_{os}, which is amplified by the open-loop gain of the device. In this case, the comparator output is pulled towards its supply voltage rail, which corresponds to logic 1. The specified V_{os} of the comparator is $\approx 200\,\mu\mathrm{V}$. Correlating the tracked voltages with the comparator output suggests that systematic residual error of the control logic ΔV_{ε} is small ($\leq 500\,\mu\mathrm{V}$).

6.1.1 Platform with Silicon-Based PUF Core

To experimentally verify the DiffC-PUF metrics and investigate the control logic's precision capabilities, in a first step, a Si-based DiffC-PUF core is assembled and attached to the control logic. The Si-based DiffC-PUF core consists of eight inverters, which are set up with two arrays of discrete, analog long-channel n-type enhancement-mode MOSFETs. Each MOSFET array contains four devices. For operation, the source and body bias terminals are tied to ground. The deployed thick-film resistors have a resistance of $R_{\mathrm{D}} = 10\,\mathrm{k}\Omega$ with $1\,\%$ variation and a temperature coefficient of 100 ppm $^{\circ}\mathrm{C}^{-1}$. As the transistor process parameters aren't known, a computational, pre-investigation approach is not directly feasible. However, to utilize the transistors as imperfect DC current source, the overdrive voltage is kept low to increase the possibility for V_{th} induced variation on I_{D}. The Si-based DiffC-PUF core is biased, such as $V_{\mathrm{out}} = \mathrm{VDD}_{\mathrm{core}} - I_{\mathrm{D}} \cdot R_{\mathrm{D}}$, with $V_{\mathrm{out}} = V_{\mathrm{DS}} \geq V_{\mathrm{ov}}$, thus the devices are operating in active region, where $I_{\mathrm{D}} \propto (V_{\mathrm{GS}} - V_{\mathrm{th}})^2$. The transistors are capable to generate drain currents of several tens of $\mu\mathrm{A}$. The inverter output voltage is primarily effected by I_{D} and R_{D} and differs due to variation in both, which will be utilized as variation source for the DiffC-PUF.

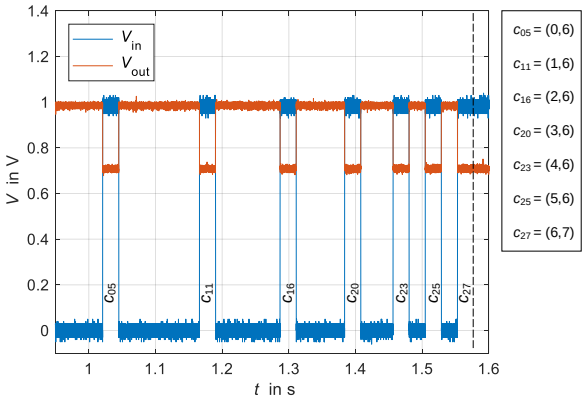


Figure 6.4: Exemplary input and output voltages of inverter number six of an arbitrary Si-based DiffC-PUF core. The corresponding sub-challenge c_k, which is used to address inverter number six is labeled. The end of the CRP cycle is marked with the vertical black dashed line.

Figure 6.4 shows one CRP cycle by measuring the input terminal and the output voltage of inverter number six, on an arbitrary Si-based DiffC-PUF core. The sub-challenges c_k, which utilize inverter number six, are labeled. The blue pulse waveform shows the input voltage applied to the gate terminal with $V_{\text{in}} = 1\,\text{V}$ and the orange curve shows the Si-based DiffC-PUF inverter output voltage. When the input voltage is applied at the inverter input, the corresponding output voltage drops accordingly. The corresponding inverter output voltage, of this specific inverter, is $V_{\text{out}} = 714\,\text{mV}$ over each cycle. The lexicographic sorting mechanism of the applied challenge is visible in the curves, as time distance between addressed inverter number six decreases at increased sub-challenge. The measurements were performed on a Yokogawa DL6104 oscilloscope with a sample rate of 125 kilo samples per second, to visualize a full CRP cycle. For bandwidth limitation and better visibility, due to reduced noise pickup of the oscilloscope probe pins, a digital low-pass filter with a cutoff frequency of 200 MHz is used on the channel of the oscilloscope, which is utilized for inverter output voltage measurement.

For experimental Si-based DiffC-PUF verification, 30 Si-based DiffC-PUF cores are assembled. The DiffC-PUF responses and analog output voltages, under the

impact of changing operating conditions, are investigated and evaluated. All possible test cases P_w, are listed in Table 6.1.

Table 6.1: Test cases for Si-based DiffC-PUF experiments (test cases marked with × denote the configured testing setup, * Ambient room temperature). Adapted from [138].

Test case	**Ambient Temperature**							**$\mathbf{VDD_{core}}$**			**$\mathbf{V_{in}}$**		
P_w	−20 °C	0 °C	20 °C	25 °C *	40 °C	60 °C	80 °C	0.9 V	1 V	1.1 V	0.9 V	1 V	1.1 V
P_1	×								×			×	
P_2		×							×			×	
P_3			×						×			×	
P_4					×				×			×	
P_5						×			×			×	
P_6							×		×			×	
P_7				×				×			×		
P_8				×				×				×	
P_9				×				×					×
P_{10}				×					×		×		
P_{11}				×					×			×	
P_{12}				×					×				×
P_{13}				×						×	×		
P_{14}				×						×		×	
P_{15}				×						×			×

For the experimental setup, the DiffC-PUF is powered by a Hameg HM80403 triple terminal laboratory DC power supply with $5\,\mathrm{V}$ and $3.3\,\mathrm{V}$ for the control logic's active devices and the DiffC-PUF core voltages $\mathrm{VDD_{core}}$ and V_{in}, both using the same terminal at $1\,\mathrm{V}$. The average measured power consumption of a Si-based DiffC-PUF core is $\approx 66\,\mu\mathrm{W}$. For each testing case as shown in Table 6.1, the response is extracted 125 times. All responses are generated by using a reference challenge C_{ref}, which includes all inverter address combinations in a lexicographic sorting order, without repetitions. The, under ambient conditions, with $T_{\mathrm{amb}} = 25\,^{\circ}\mathrm{C}$, $\mathrm{VDD_{core}} = 1\,\mathrm{V}$, $V_{\mathrm{in}} = 1\,\mathrm{V}$, extracted response with the most occurring bit sequence over a set of 125 repetitions is used as reference response R_{ref}. As the deployed components are humidity insensitive, humidity impact is not directly investigated for the Si-based DiffC-PUF. The measurements, over test cases $P_1 - P_6$, are performed in a Weiss WK3 climatic chamber.

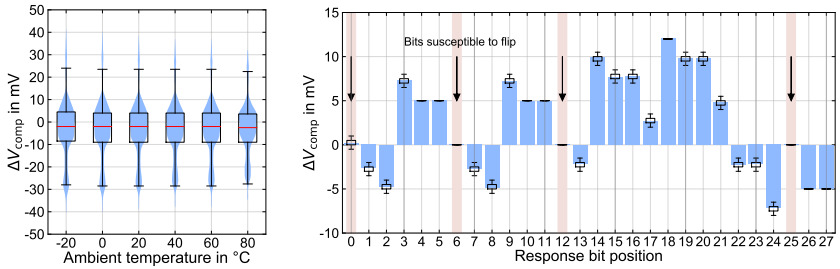


Figure 6.5: Si-based DiffC-PUF comparator input voltage differences ΔV_{comp}. **(a)** ΔV_{comp} of ten PUF cores over temperature. **(b)** ΔV_{comp} per response bit of one selected PUF core (no. 20). Adapted from [138] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

Figure 6.5a shows the tracked voltage differences at the comparator input terminal ΔV_{comp} over the full T_{amb} range at nominal V_{in} and VDD_{core} biasing conditions of 10 DiffC-PUF cores as box- and violin plot. The distribution covers both, the inter as well as intra device variation, thus slightly multimodal distributions are visible in the violin plots. The median value of $\Delta V_{\text{comp}} = -2\,\text{mV}$ is stable over all temperature levels. The interquartile range (IQR) of the voltage differences is $13\,\text{mV}$ over the full temperature range. With the given transistor biasing, an increase in I_{D} at increasing temperature can be observed, due to the low V_{ov}. The devices are operating below the zero-temperature coefficient, at which drain current is mainly effected by decrease in V_{th} at increasing temperature.

To exemplary highlight the minimum voltage levels, which can be safely detected, the ΔV_{comp} of each response bit of PUF core 20 at nominal conditions is shown in Figure 6.5b, including 125 repetitions. At low ΔV_{comp} levels the response bits become unstable because voltage differences can not be safely detected anymore, as highlighted in the image for the response bit positions r_0, r_6, r_{12} and r_{25}. The boxplots in the figure occur due to noisy LSB, which is at $500\,\mu\text{V}$ per ADC channel. To further evaluate the stability of ΔV_{comp}, effects on PUF metrics are investigated.

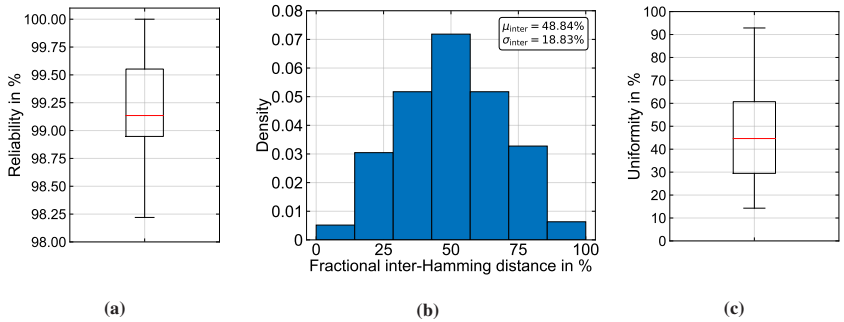


Figure 6.6: Measured Si-based DiffC-PUF metrics. **(a)** Reliability of 10 DiffC-PUF cores, visualized as boxplot. **(b)** Uniqueness plotted over the inter-FHD, including 30 DiffC-PUF cores. **(c)** Uniformity, visualized as boxplot, incorporating 30 Si-based DiffC-PUF cores. Adapted from [138] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

For reliability investigation, test cases $P_1 - P_{15}$ are used. Due to the high amount of possible combinations and extensive measurements 10 DiffC-PUF cores are used for reliability analysis. The reliability analysis shows an almost ideal, mean reliability of $99.20\,\%$ and a minimum reliability of $98.22\,\%$. The reliability of all 10 DiffC-PUF cores is visualized as boxplot in Figure 6.6a. The reliability values show that only minuscule changes in some responses at certain corner conditions occur. Next to the very high reliability of the Si-based DiffC-PUF, this also highlights the control logic's high precision operation capabilities over a broad temperature spectrum.

To obtain the uniqueness, all 30 Si-based DiffC-PUF core responses, under nominal conditions, are extracted over 125 times. For experimental cross check, a second identical control logic board is assembled to investigate the impact of the control logic on Si-based DiffC-PUF uniqueness. The obtained uniqueness is equal for both control logic boards, using the same 30 DiffC-PUF cores, with $\mu_{\text{inter}} = 48.84\,\%$ and standard deviation of $\sigma_{\text{inter}} = 18.83\,\%$, as shown over the inter-FHD in Figure 6.6b. Therefore, the obtained uniqueness depends primarily on the Si-based DiffC-PUF cores, as intended for the overall DiffC-PUF design.

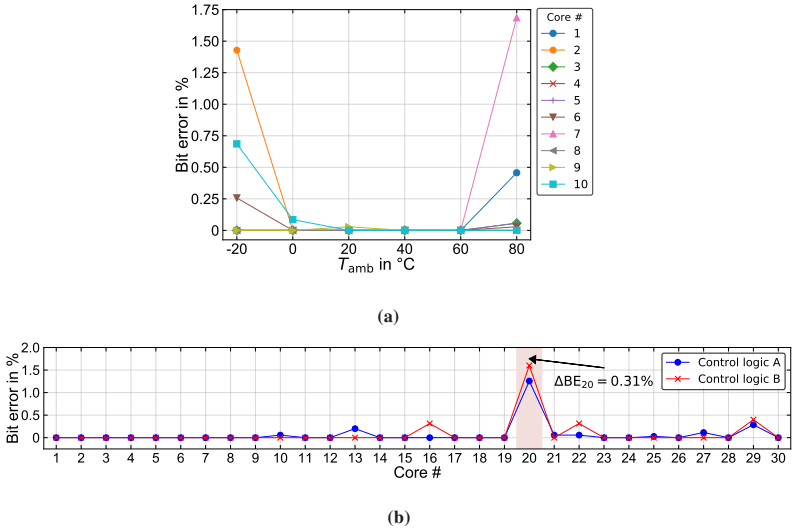


Figure 6.7: Measured Si-based DiffC-PUF bit errors. **(a)** BE of 10 DiffC-PUF cores, visualized over T_{amb}. **(b)** BE of 30 DiffC-PUF cores over two deployed control logic boards (A and B). Adapted from [138] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

The experimentally obtained mean bit aliasing is $45.60\,\%$ with a maximum at $63.30\,\%$ and a minimum of $26.70\,\%$ over the test cases $P_1 - P_6$. The mean bit aliasing shows a slight bias in the response towards logic 0. This effect correlates with the reported ΔV_{comp} median, which is also slightly negative. However, as investigated before in the uniqueness cross check, this minimal error is mainly attributed to the PUF core elements. At increasing sample sizes this bias should be resolved. The obtained mean uniformity is $45.60\,\%$, with a maximum uniformity of $92.86\,\%$ and a minimum at $14.29\,\%$. As the uniformity is broad, the DiffC-PUF without post-processing, isn't directly capable for cryptographic applications. This can be improved by deploying of fuzzy extractors to provide uniform keys [138]. However, with the obtained uniqueness, the Si-based DiffC-PUF is suited for identification purposes.

As PUF responses should be stable over repetitions, the bit errors are investigated, by reproducing the identical response over 125 times. The bit error evaluation extends the reliability metric analysis and helps to visualize temporal errors over a defined operating spectrum for each PUF core. For bit error analysis 10 Si-based DiffC-PUF cores are investigated over temperature (test cases $P_1 - P_6$). The responses over temperature are compared to R_{ref}. The results are visualized in Figure 6.7a. The bit errors are overall very low, especially at temperatures ranging from $0\,^{\circ}\mathrm{C}$ up to $60\,^{\circ}\mathrm{C}$. Bit errors increase at the corner temperature conditions of $-20\,^{\circ}\mathrm{C}$ and $80\,^{\circ}\mathrm{C}$ but remain $< 1.75\,\%$. Furthermore, the bit errors over both control logic boards (A and B) are investigated over 30 PUF cores at nominal operating conditions, as visualized in Figure 6.7b. The difference in bit errors remains very low but temporal effects become more visible, such as noise induced effects, which result in flipping bits. The maximum bit error is given for PUF core 20 for both control logic boards. However, the difference between both remains almost equal with $\Delta\mathrm{BE}_{20} = 0.31\,\%$. The error at PUF core 20 originates from low ΔV_{comp}, as discussed before (see Figure 6.5b).

6.1.2 Platform with Printed Electronics-Based PUF Core

To investigate the DiffC-PUF as hybrid system, incorporating a decentralized manufacturable PE-based PUF core, based on EGT technology, an adapter PCB is designed, which provides a standardized interface for printed DiffC-PUF core integration in a Si-based system environment.

The interchangeability of the adapter PCB enables large-scale evaluation and PE-based PUF metric investigation. The integration of the glass substrate, which contains the printed inverters, follows a flip-chip derived mounting approach [200]. The adapter PCB hosts 36 gold-coated contact pads, of which 28 are electrically connected with the DiffC-PUF core on the glass substrate. The contact pads are $1\,\mathrm{mm}$-spaced and $1\,\mathrm{mm} \times 1\,\mathrm{mm}$-sized. The adapter PCB has a cut out area

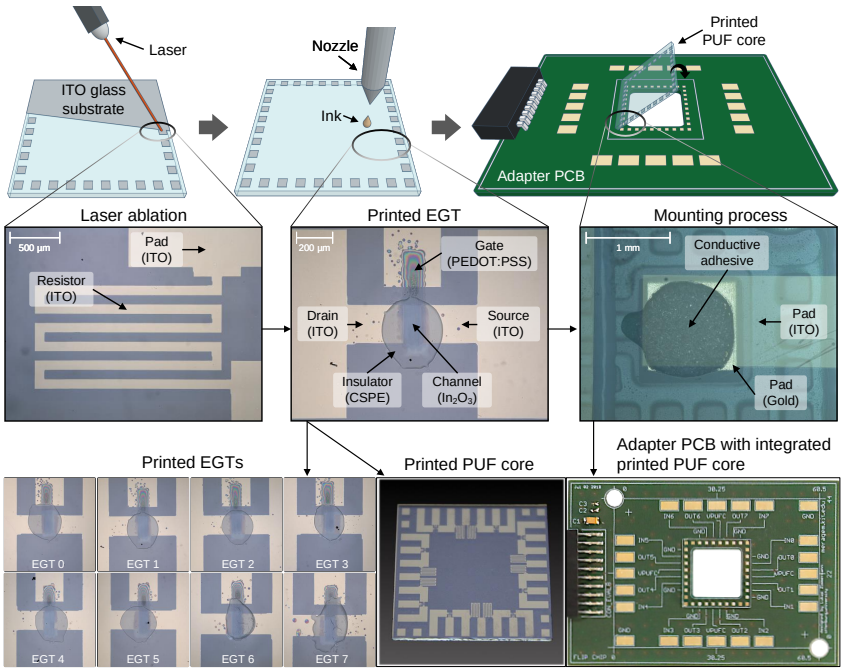


Figure 6.8: Fabrication and integration workflow of the PE-based DiffC-PUF core on the adapter PCB, from left to right. Furthermore, additional images are shown, such as microscopic images of eight EGTs on a printed PUF core, a standalone printed PUF core on glass substrate and the integrated PUF core on the adapter PCB. Adapted from [200] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

underneath the glass substrate, which provides better conditions for humidity dependency testing. Two fiducials on the glass substrate and on the adapter PCB are used to enable a semi-automated integration of the glass substrate on the adapter PCB. The electrical connection between the adapter PCB contact pads and the ITO-based I/O terminals of the glass substrate is realized by a silver-filled, two-component adhesive Panacol Elecolit 325, with a pot time of $\approx$ 90 minutes. The glue allows for drying in ambient conditions, in order to exclude possible negative impact from temperature during heating of the fully fabricated EGTs. A mechanically stable and electrical connection is achieved after $\approx$ 16 hours, when dried at room temperature [200]. The dispensing of the glue on the contact pads

Table 6.2: Test cases for hybrid PUF experiments (test cases marked with × denote the configured test setup P_w).

Test case	**Ambient temperature**			**Rel. humidity**			**$\mathbf{VDD_{core}}$**		
P_w	20 °C	40 °C	60 °C	45 %	50 %	55 %	0.9 V	1 V	1.1 V
P_1	×				×			×	
P_2	×			×				×	
P_3	×					×		×	
P_4	×				×		×		
P_5	×				×				×
P_6		×			×			×	
P_7		×			×		×		
P_8		×			×				×
P_9			×		×			×	
P_{10}			×		×		×		
P_{11}			×		×				×

is an automated process. More information about the full integration process can be found in [200, 225].

The schematic workflow for PE-based DiffC-PUF core fabrication and integration is shown in Figure 6.8, which starts with the laser structuring of the ITO substrate and is followed by inkjet-printing of the materials for EGT realization and finalized by flip-chip mounting of the glass substrate on the adapter PCB. The image includes eight microscopic images at a 10× optical magnification of fabricated EGTs with a $W_{\mathrm{T}} = 200\,\mu\mathrm{m}$ and $L_{\mathrm{T}} = 100\,\mu\mathrm{m}$, utilized for a PE-based DiffC-PUF core. For fabrication of the devices, each device is printed standalone with the same printing parameters to exclude possible systematic impact due to printing fabrication.

For electrical characterization and PE-based DiffC-PUF evaluation, extended measurements are performed. The test cases and used testing conditions are listed in Table 6.2. Each test case and the corresponding response is extracted over 20 repetitions. All measurements were performed in a Weiss WK3 climatic chamber at controlled operating conditions. Each response is extracted from the same

reference challenge C_{ref}. Test case P_1 is the reference test case and provides the reference response R_{ref} under nominal operating conditions. For PE-based DiffC-PUF core input voltage biasing investigations, different voltages are deployed and further described in the corresponding PUF metric evaluation section.

To gain insight into the inverter output voltage behavior and variation, 15 PE-based DiffC-PUF cores, each containing eight inverters, were measured over $V_{\text{in}} = \{0\,\text{V}, 0.2\,\text{V}, ..., 1\,\text{V}\}$, in a $200\,\text{mV}$ step size, at $\text{VDD}_{\text{core}} = 1\,\text{V}$, $\text{RH} = 50\,\%$ and over the temperatures $T_{\text{amb}} = \{20\,°\text{C}, 40\,°\text{C}, 60\,°\text{C}\}$, which equals test cases P_1, P_6 and P_9.

Figures 6.9a,b,c show the respective inverter output voltage transfer curves $V_{\text{out}} = f(V_{\text{in}})$ over all 120 inverters as box- and violin plots. A fourth-degree polynomial is fit over the median V_{out} values. The data contains the inter and intra device variations and is, as expected, relatively broad. At nominal operating conditions of $20\,°\text{C}$ and $V_{\text{in}} = 0.4\,\text{V}$, the largest V_{out} variation is obtainable (see Figure 6.9a), as investigated using the simulation-based approach shown in Subsection 5.2.4. The output voltage decreases on average as temperature increases, which can be attributed to increased I_{D} at the given operating conditions.

Furthermore, the voltage difference at the comparator input terminals ΔV_{comp} is shown in Figure 6.9d,e,f, also as box- and violin plot. The maximum ΔV_{comp} can be obtained at $V_{\text{in}} = 0.4\,\text{V}$ at nominal conditions with a median of $-48\,\text{mV}$ and an IQR of $284.1\,\text{mV}$. From the obtained results a high ΔV_{out}, which exceeds ΔV_{ε}, can be expected. The voltage differences slightly decrease at increasing temperature. The observed voltage difference changes at a decreased rate in the temperature range from $40\,°\text{C}$ up to $60\,°\text{C}$. In the future, more detailed work on the temperature dependency of top-gated EGTs is required.

For PUF reliability investigation, incorporating the PE-based DiffC-PUF core, the corner conditions are compared with the nominal response R_{ref}, which equals the most observed response for test case P_1 over 20 repetitions at $V_{\text{in}} = \{0.3\,\text{V}, 0.4\,\text{V}, 0.5\,\text{V}\}$. For full reliability evaluation, test cases $P_2 - P_{11}$ are performed to incorporate VDD_{core}, RH and T_{amb} impact on reliability. The extracted reliability over these test cases are shown in Figure 6.10a. The highest mean

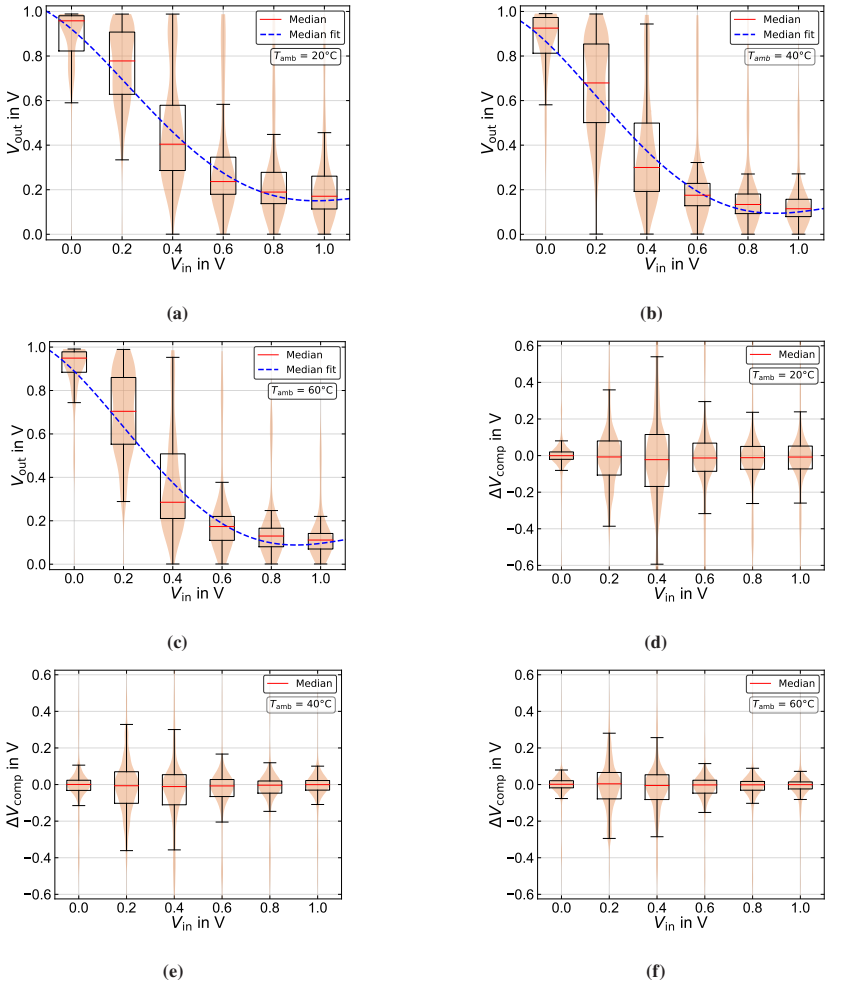


Figure 6.9: Measured PE-based DiffC-PUF inverter $V_{\text{out}} = f(V_{\text{in}})$ and corresponding ΔV_{comp} over temperature at RH $= 50\,\%$ and $\text{VDD}_{\text{core}} = 1\,\text{V}$, visualized as box- and violin plot. **(a)** Output voltage transfer curve at $T_{\text{amb}} = 20\,°\text{C}$. **(b)** Output voltage transfer curve at $T_{\text{amb}} = 40\,°\text{C}$. **(c)** Output voltage transfer curve at $T_{\text{amb}} = 60\,°\text{C}$. **(d)** ΔV_{comp} at $T_{\text{amb}} = 20\,°\text{C}$. **(e)** ΔV_{comp} at $T_{\text{amb}} = 40\,°\text{C}$. **(f)** ΔV_{comp} at $T_{\text{amb}} = 60\,°\text{C}$. Adapted from [200] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

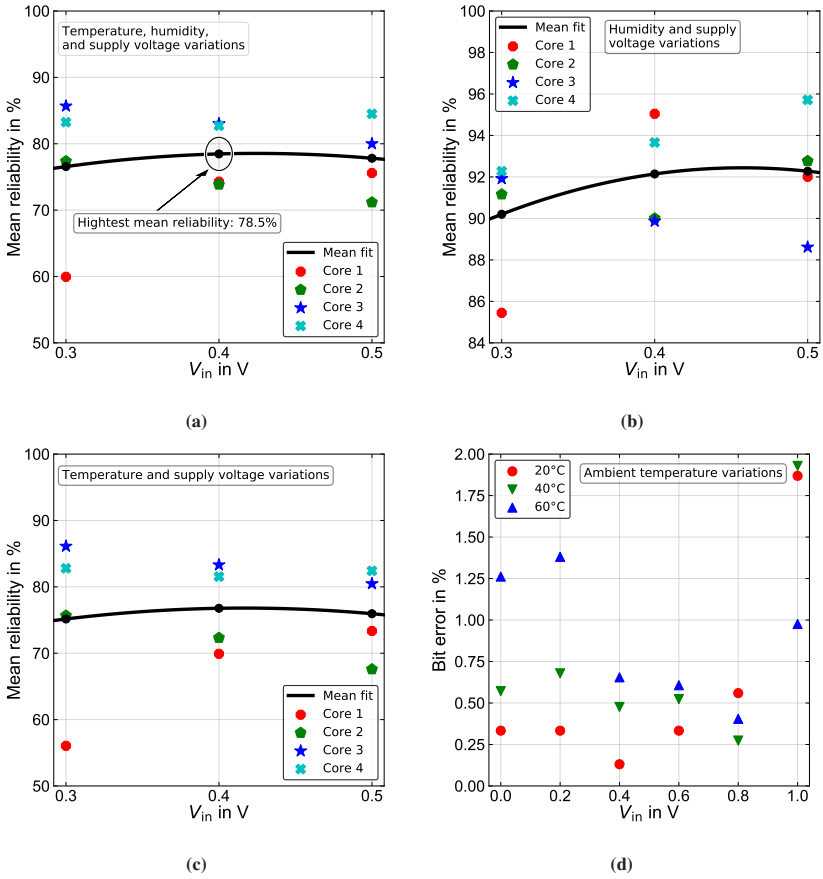
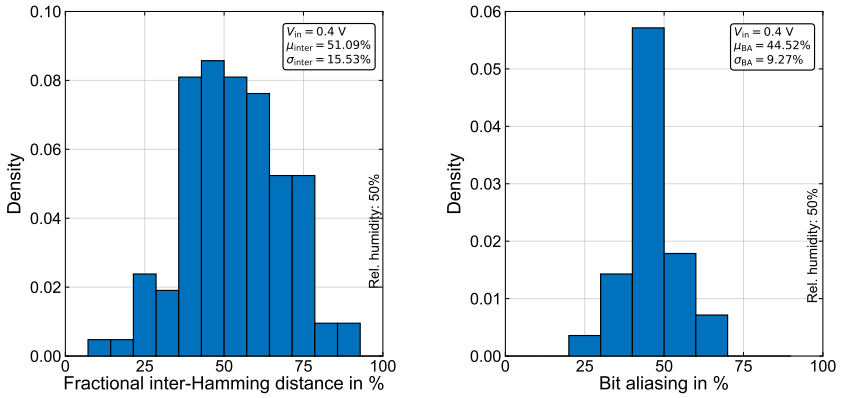


Figure 6.10: PE-based DiffC-PUF reliability over $V_{\text{in}} = \{0.3\,\text{V}, 0.4\,\text{V}, 0.5\,\text{V}\}$ and bit errors over $V_{\text{in}} = \{0\,\text{V}, 0.2\,\text{V}, ..., 1\,\text{V}\}$. **(a)** Reliability including variation in T_{amb}, RH and VDD_{core}. **(b)** Reliability including variation in RH and VDD_{core}. **(c)** Reliability including variation in T_{amb} and VDD_{core}. **(d)** Bit error metric over T_{amb}. Adapted from [200] under CC BY 4.0 license, https://creativecommons.org/licenses/by/4.0/.

reliability can be obtained at $V_{\text{in}} = 0.4\,\text{V}$ with $78.50\,\%$. Furthermore, reliability is calculated over test cases $P_2 - P_5$, excluding temperature variation. The mean



(a) **(b)**

Figure 6.11: PE-based DiffC-PUF uniqueness and bit aliasing. **(a)** PE-based DiffC-PUF uniqueness. **(b)** PE-based DiffC-PUF bit aliasing. Adapted from [200] under CC BY 4.0 license. https://creativecommons.org/licenses/by/4.0/.

reliability over the full investigated V_{in} range exceeds $90\,\%$. As a third investigation, test cases $P_4 - P_{11}$ are evaluated, excluding humidity effects. Here, the reliability is below $80\,\%$. Comparing the reliability results, temperature effects clearly impact reliability in a negative manner to the largest extend. Interestingly, variation in RH effects the hybrid PUF reliability at relatively small amounts.

For further robustness analysis of the PE-based DiffC-PUF, the responses are tracked over time to investigate impact of temporal environmental effects on the hybrid PUF response, such as noise and supply voltage fluctuations, with respect to the occurring bit errors. Investigating possible effects of temporal degradation is especially important for novel devices, where next to environmental effects, also device specific degradation over time, might occur. Therefore, the hybrid PUF is measured using test cases P_1, P_6 and P_9 over $V_{\text{in}} = \{0\,\text{V}, 0.2\,\text{V}, ..., 1\,\text{V}\}$ in $200\,\text{mV}$ steps. As different temperature levels change the responses, bit errors are calculated, based on the nominal response per each temperature level and compared to the most occurring response over 20 repetitions. The highest bit errors are at $V_{\text{in}} = (0.8\,\text{V}, 1\,\text{V})$, as the inverter output voltages are already saturated and

ΔV_{out} is low. The relative bit errors of the 28-bit responses are $< 2\,\%$, which relates to less than one bit flip on average per response, as shown in Figure 6.10d, over the full V_{in} spectrum. The bit error investigations reveal no clear negative impact of possible transistor degradation on DiffC-PUF performance over time and multiple cycles.

For investigation of the PE-based DiffC-PUF uniqueness, 15 PUF cores were read out at nominal conditions (P_1) at an optimal input biasing of $V_{\text{in}} = 0.4\,\text{V}$. The obtained uniqueness is shown over the inter-FHD in Figure 6.11a. With a almost ideal uniqueness of $\mu_{\text{inter}} = 51.09\,\%$ and a corresponding standard deviation of $\sigma_{\text{inter}} = 15.53\,\%$, the hybrid PUF is highly viable for identification purposes and matches the obtained results from the simulation-based analysis, as shown in Subsection 5.2.5.

Finally, the BA is calculated from the same measurement route as for the uniqueness verification. The mean BA is at $44.52\,\%$ with a standard deviation of $9.27\,\%$, as visualized in Figure 6.11b. This shows a slight bias towards logic 0, which correlates with the investigated, also slightly negative median ΔV_{comp} value. The response bias can be explained due to the relative low amount of PUF cores and utilized re-addressing method, where minuscule bias has a relatively high impact.

6.2 Conclusion

In this chapter, the full embedded DiffC-PUF platform implementation is investigated. This includes commissioning of the control logic and performance analysis as well as PE-based DiffC-PUF core implementation. The embedded DiffC-PUF platform was commissioned utilizing a Si-based PUF core. Extensive measurements were performed, which gave insights to the DiffC-PUF response behavior under varying operating conditions. A systematic optimization approach was used to minimize systematic variation in the DiffC-PUF control logic and allow to harvest primarily the intrinsic variation of the DiffC-PUF core element. The embedded DiffC-PUF platform, incorporating a Si-based PUF core, shows high

resilience against temperature effects over a broad temperature range of $-20\,^{\circ}\mathrm{C}$ up to $80\,^{\circ}\mathrm{C}$ and voltage induced errors of $\pm 10\,\%$ for both, V_{in} and $\mathrm{VDD}_{\mathrm{core}}$. Furthermore, PUF metric evaluation shows that the Si-based DiffC-PUF is capable to generate very reliable, bit stable and unique PUF responses, viable for identification with a uniqueness of $\mu_{\mathrm{inter}} = 48.84\,\%$ and a mean reliability of $99.20\,\%$. This allows the Si-based DiffC-PUF to be deployed as a low-cost platform for software-based, application-focused development, such as PUF CRP implementation in communication protocols.

Furthermore, the presented embedded DiffC-PUF platform, incorporating the PE-based DiffC-PUF core within the Si-based system, is fully experimentally verified. Optimal input biasing investigations are performed to visualize and verify the initial, simulation-based investigations. It is shown that at $0.4\,\mathrm{V}$ inverter input voltage, the maximum voltage difference at the comparator could be tracked. Therefore, PE-based DiffC-PUF core inverter biasing at $V_{\mathrm{in}} = 0.4\,\mathrm{V}$ is beneficial. State of the art PE-based DiffC-PUF evaluation was performed and corresponding PUF metrics investigated. It shows that the embedded DiffC-PUF platform with PE-based PUF core is capable to generate, highly unique responses with a uniqueness $\mu_{\mathrm{inter}} = 51.09\,\%$. A high bit stability, incorporating low average bit error of $< 2\,\%$ per temperature level, was obtained. The mean reliability incorporating temperature, supply voltage and humidity variation is at $78.50\,\%$. It shows that temperature instability of printed EGTs lead to a change in inverter operating point and thus change in the PUF response. For further implementations, temperature stability measures have to be taken. This includes possibilities in temperature stable inverter biasing and adaptions in PE-based DiffC-PUF architecture.

7 Summary and Outlook

7.1 Summary

In this thesis, new concepts in printed electronics over a manifold application spectrum were presented. This includes inkjet-printed devices, circuits and hybrid systems, combining printed electronics with classical silicon-based electronics.

Chapter 4 shows the results obtained for inkjet-printed devices. The fabrication workflow for top-gate electrolyte-gated transistors on laser structured substrates, which enables higher throughput circuit fabrication in comparison to electron beam-based structuring, is shown.
Furthermore, to enable lightweight data storage in printed electronics, an inkjet-printed memristor is presented. The device offers a high retention time, which exceeds 10^4 seconds, a large distinguishable difference in high- and low-resistance state of 10^7 and shows stable switching over 50 cycles. Its device-to-device and cycle-to-cycle variability is investigated, along with the memristor's conduction mechanism.

In Chapter 5 the focus is on inkjet-printed circuits. An inkjet-printed full-wave rectifier for low alternating voltage rectification was developed and fully electrically characterized. The full-wave rectifier incorporates diode-connected electrolyte-gated transistors with near-zero threshold voltages. The circuit was experimentally verified over a broad spectrum, incorporating different loading conditions, its frequency dependency and various input voltage levels. At high load resistance, the full-wave rectifier is capable to rectify a $1\,\mathrm{V}$ amplitude with a voltage drop across the utilized devices of merely $\approx 140\,\mathrm{mV}$. The circuit is capable to generate a maximum output power of $\approx 5\,\mu\mathrm{W}$ at a load resistance of $10\,\mathrm{k}\Omega$ at $1\,\mathrm{V}$ input

voltage amplitude. A simulation-based approach suggests that, at high load resistance, the full-wave rectifier is capable to rectify voltages down to $100\,\mathrm{mV}$. The developed circuit can be used as building block to enable sustainable electronic systems, as it is capable to rectify small alternating voltages, as obtained from vibration energy harvesters.

To enable secure hardware-based identification, two printed electronics-based physically unclonable functions are designed and investigated, using electrical simulation. The primary focus is on the intrinsic and systematic variation of the printed physically unclonable function cores. Furthermore, impact of systematic variation of the control logic on the designs and its performance metrics is incorporated. One proposed implementation strategy utilizes electrolyte-gated transistors in a crossbar architecture to enable high density device integration at low manufacturing overhead. Another physically unclonable function utilizes a differential circuit, incorporating inverter structures, also based on electrolyte-gated transistors, to generate a unique response. Both implementations and their performance metrics are evaluated based on electrical simulation and proof of concept fabrication and measurement of the printed physically unclonable function cores. The crossbar-type architecture is capable to generate reliable, unique responses with a $\mu_{\text{inter}} = 49.84\,\%$. Due to the crossbar-based approach and occurring biases from line resistance, the bit aliasing metric is slightly degraded with a mean value of $52.29\,\%$. This slight bias can be reduced by further optimization in layout and utilized materials.

The differential circuit architecture was investigated using an electrical simulation-based approach. The simulation results show an optimal input voltage biasing of the investigated inverter at $V_{\text{in}} = 0.4\,\mathrm{V}$, as highest variation in the output voltages and best physically unclonable function metrics can be achieved at this point. The simulation results highlight that the differential circuit architecture is capable to generate reliable and close-to-ideal unique responses, with a uniqueness of $\mu_{\text{inter}} = 50.02\,\%$ and is utilizable in real system implementations.

Chapter 6 shows the experimentally obtained results for an embedded differential circuit physically unclonable function platform in the form of a holistic, hybrid

system. Therefore, the printed differential circuit PUF core is incorporated within a silicon-based system. Before commissioning, a silicon-based differential circuit PUF core is utilized to commission and evaluate the full platform system. The obtained results show that the platform, incorporating the silicon-based differential circuit PUF core, is capable to generate highly reliable and unique responses at minimum bit errors. The obtained mean reliability is $99.20\,\%$ at a uniqueness of $\mu_{\text{inter}} = 48.84\,\%$. The silicon-based differential circuit system can be used as low-cost platform for application-based and software-focused research in order to generate unique responses. Finally, the printed differential circuit is utilized as intrinsic variation source within the silicon-based platform, forming a hybrid system. The embedded differential circuit physically unclonable function, utilizing a printed PUF core element is fully verified regarding physically unclonable function security metrics. It shows that differential circuit input voltage biasing at $0.4\,\mathrm{V}$ is beneficial, as highlighted in the prior investigated electrical simulation. The hybrid system is capable to generate almost ideal unique responses, with $\mu_{\text{inter}} = 51.09\,\%$. This investigated approach allows split-manufacturing of physically unclonable functions, as the printed element can be attached to the silicon-based control logic in a decentralized manner by inkjet-printing technology.

7.2 Outlook

The presented results provide a basis for further investigations. For the developed memristors, this includes reduction of crossing junction area and investigation on possible effects on variability and integration within crossbar architectures. Furthermore, hardware-based security primitives, such as true random number generators and physically unclonable functions, incorporating inkjet-printed memristors, can be explored.

The presented inkjet-printed full-wave rectifier can be combined with printed vibration energy harvesters to experimentally enable sustainable and self-powered applications. This includes new concepts to utilize large-area printed solutions.

Additionally, optimization for improved power conversion efficiency could be done by further tuning of the threshold voltage and corresponding reverse leakage current behavior.

For embedded PE-based DiffC-PUF platform, further investigations regarding improved temperature stability can be implemented to improve reliability and enable bit stability over temperature. Also, improvement in used materials can be made to increase operating frequency of devices and reduce parasitic line resistance. For printed physically unclonable functions, many intrinsic variation parameters can be further explored to enable hardware-based security for and by printed electronics. This highlights the possibilities non-impact printing technology can provide as disruptive technology.

A Appendix

A.1 Materials

A.1.1 Electrolyte-Gated Transistors

In the following, the materials used for EGT fabrication are shown.

Indium tin oxide, sputtered on silicon dioxide passivated glass substrate (PGO CEC020S, $20\,\mathrm{mm} \times 20\,\mathrm{mm}$, $R_{\square} = 20\,\Omega$, Präzisions Glas & Optik GmbH), Indium (III) nitrate hydrate ($99.9\,\%$ trace metal basis, MW = 300.83 , Sigma-Aldrich), Glycerol (MW = $92.09\,\mathrm{g\,mol^{-1}}$, Merck KGaA), Dimethyl sulfoxide anhydrous (DMSO, $99.9\,\%$, MW=$78.13\,\mathrm{g\,mol^{-1}}$, Sigma-Aldrich) Propylene carbonate anhydrous (PC, $99.7\,\%$, MW = $102.09\,\mathrm{g\,mol^{-1}}$, Sigma-Aldrich), Poly(vinyl alcohol) hydrolysed (PVA, $98\,\%$), Lithium perchlorate (LP, $99.99\,\%$ trace metal basis, MW = $106.39\,\mathrm{g\,mol^{-1}}$, Sigma-Aldrich), Poly(3,4 ethylenedioxythiophene):polystyrene sulfonate (PEDOT:PSS, 3.0 - 4.0 % in $\mathrm{H_2O}$, Sigma-Aldrich), Ethylene glycol anhydrous ($99\,\%$,MW = $62.07\,\mathrm{g\,mol^{-1}}$, Sigma-Aldrich)

A.1.2 Memristor

Chromium-layered gold substrate (in-house prepared, $5\,\mathrm{nm}$ Cr-adhesion layer on glass substrate, $45\,\mathrm{nm}$ gold layer on Cr-adhesion layer), Zinc nitrate hexahydrate (MW = $297.49\,\mathrm{g\,mol^{-1}}$, Sigma-Aldrich), Silverjet DGP-40LT-15C (nanoparticle-based silver dispersion, MW=$107.87\,\mathrm{g\,mol^{-1}}$, Sigma-Aldrich), Glycerol (MW = $92.09\,\mathrm{g\,mol^{-1}}$, Merck KGaA)

A.2 Fluid Preparation

A.2.1 Electrolyte-Gated Transistors

In the following the fluid formulations for EGT fabrication are shown.

The inkjet-printable precursor fluid for the indium oxide channel is based on dissolved $0.05\,\mathrm{M}$ $(\mathrm{H_2InN_3O_{10}})$ in double-deionized water and glycerol with a ratio of 4:1 [201]. The solution is stirred for two hours and filtered with a $0.2\,\mu\mathrm{m}$ polyvinylidene fluoride (PVDF) filter before usage. The CSPE is prepared with $1\,\mathrm{wt\%}$ $\mathrm{LiClO_4}$, dissolved in $9\,\mathrm{wt\%}$ PC and stirred for $2\,\mathrm{h}$ at ambient room temperature. In addition, $4.29\,\mathrm{wt\%}$ PVA is dissolved in $85.71\,\mathrm{wt\%}$ DMSO and stirred at $90\,^{\circ}\mathrm{C}$ for two hours. The two solvents are mixed together and stirred until a clear solution is obtained [201]. Before inkjet-printing, the solution is filtered using a $0.2\,\mu\mathrm{m}$ polytetrafluoroethylene (PTFE) filter. In the last step, $70\,\mathrm{wt\%}$ PEDOT:PSS is dissolved in $30\,\mathrm{wt\%}$ ethylene glycol and stirred for two hours, then filtered with a $0.2\,\mu\mathrm{m}$ PVDF membrane before printing. The PVA-based insulator follows the same formulation route as the CSPE, excluding $\mathrm{LiClO_4}$ and using $10\,\mathrm{wt\%}$ of PC.

A.2.2 Memristor

In the following the fluid formulations for memristor fabrication are shown.

The inkjet-printable precursor fluid for the zinc oxide storage layer channel is based on a $0.1\,\mathrm{M}$ $\mathrm{Zn(NO_3)_2 \cdot 6H_2O}$ dissolved in double-deionized water and glycerol in a 4:1 ratio. The solution is stirred over a $2\,\mathrm{h}$ period at ambient room temperature. Before inkjet-printing the fluid is filtered with a $0.2\,\mu\mathrm{m}$ PVDF membrane. The Silverjet DGP-40LT-15C dispersion is filtered with a $0.45\,\mu\mathrm{m}$ PVDF membrane before printing.

A.3 Layouts

All layouts for the ITO-based signal routing layer and gold electrodes were initially designed using the free software KLayout.

A.3.1 PE-Based DiffC-PUF Core Layout

The layout for the symmetrically and equidistant PE-based DiffC-PUF core is visualized in Figure A.1. The PE-based DiffC-PUF core layout incorporates a full ITO-covered glass substrate, as it is used for seamless integration. The purple square is shown to highlight the full substrate size. All I/O terminals are $500\,\mu\mathrm{m}$ distanced from the glass substrate edges.

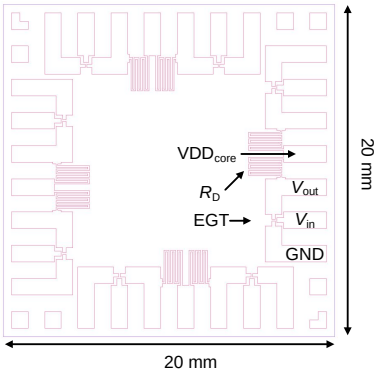


Figure A.1: PE-based DiffC-PUF core signal routing layer layout.

The design is chosen to reduce parasitic wiring resistance, avoid crossovers to enable large-scale fabrication and reduce systematical layout error within the PE-based DiffC-PUF core. As the amount of I/O terminals is fixed, to allow for seamless integration within the adapter PCB, always two inverters per side share a $\mathrm{VDD_{core}}$ terminal. Each inverter has a standalone input, output and ground

terminal. The L-shaped fiducials at top left and bottom right allow for a clear PE-based DiffC-PUF orientation during the integration step.

A.3.2 Inkjet-Printed Low-Voltage Full-Wave Rectifier Layout

The layout for the full-wave rectifier is shown in Figure A.2. Here, a focus was on reduction in possible parasitic capacitance due to high overlap capacitance from the CSPE with the source- and drain electrodes of the EGT.

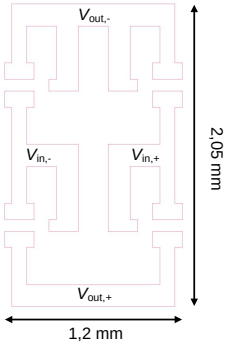


Figure A.2: Full-wave rectifier signal routing layer layout.

A.3.3 Inkjet-Printed Memristor Layout

For the memristor development, single strips for the inert bottom electrode are lasered. An additional contact pad for probing is used.

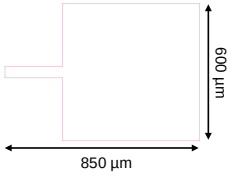


Figure A.3: Inkjet-printed memristor bottom electrode layout.

A.3.4 Inkjet-Printed Crossbar PUF Core Layout

Figure A.4 shows the printed crossbar PUF core layout signal routing layer.

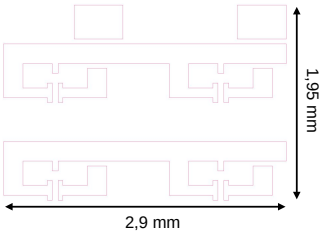


Figure A.4: Layout for printed crossbar PUF core signal routing layer.

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