# Tunable Multi-Bit Nonvolatile Memory Based on Ferroelectric Field-Effect Transistors

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**Ferroelectric field-effect transistors (FeFETs) with 2D semiconductors as channel materials have been fabricated to achieve miniaturized size, high storage, and low power consumption. The FeFETs are studied based on few-layer $MoS_2$ sheets on the non-lead $Bi_{0.85}La_{0.15}Fe_{0.92}Mn_{0.08}O_3$ (BLFMO) ferroelectric films with a large remnant polarization ($P_r$ ≈36 μC cm$^{-2}$). In FeFETs, the conductivity states of the 2D semiconductor can be tuned by the ferroelectric polarization. It is found that the $MoS_2$-based FeFETs display a large memory windows exceeding 25 V, a high on/off ratio (>10$^5$), remarkable program/erase ratio (≈10$^4$), competitive retention, endurance, and high-speed performance. Moreover, the 2D based FeFETs exhibit switchable multi-bit data storage by applying different amplitudes of negative gate voltage pulses to enhance the data storage density. On the basis of these characteristics, the 2D-FeFETs are potentially able to meet the need for scalability, capacity, retention, and endurance of nonvolatile memory.**

## 1. Introduction

2D materials have unique properties in electricity, optics, and magnetism.[1–6] In addition, combining 2D materials with dielectrics oxides and/or ferroelectric materials can produce photodetectors,[7–10] memories,[11,12] solar cells,[13] and field-effect transistors (FET),[14] etc., which greatly enriches the range of practical applications for 2D materials. Since a single-layer graphene was prepared by mechanical exfoliation in 2004,[15] more and more 2D materials have come out such as black phosphorus, hexagonal boron nitride, and transition metal dichalcogenides (TMDs).[16–18] TMDs based FETs have high carrier mobility and a large on/off current ratio. As a representative of mature 2D TMDs, $MoS_2$ has a high theoretically predicted mobility up to 1000 cm$^2$ V$^{-1}$ s$^{-1}$ and a high on/off current ratio (over 10$^6$).[19,20] Moreover, the band gap of $MoS_2$ gradually increases from an indirect band gap of ≈1.2 eV to a direct band gap of about 1.9 eV with reducing the thickness from bulk to a single layer.[21–23] Therefore, $MoS_2$ is widely used in field-effect transistors (FET), photodetectors, solar cells and other devices.

At present, there are mainly two types of ferroelectric memories. The first type is ferroelectric random access memories (FeRAMs) composed of a transistor and a ferroelectric capacitor (1T1C-FeRAM).[24] In order to achieve the storage data function, the digital logic "0" and "1" can be defined according to different polarized directions. However, in 1T1C-FeRAM, the previous storage state will be destroyed after applying a read pulse. As the use time of FeRAM increases, the fatigue resistance will decrease, resulting in the failure of storage data function. The second type is a ferroelectric field-effect transistor (FeFET). Ferroelectric materials are used as dielectric oxide to achieve the storage data function. The ferroelectric polarization will be tuned by applying positive or negative gate voltage pulses, which can realize the accumulation or depletion of channel carriers. Due to the effect of the residual polarization, FeFET can maintain the memory states when the gate voltage is removed.[25] Compared to FeRAM, FeFET is a kind of nonvolatile memory. The FeFET has similar structure with traditional transistors and it can be scaled down on the integrated circuit.

Previously, $MoS_2$-based FeFETs with $Pb(Zr_xTi_{1-x})O_3$ (PZT) based ferroelectrics as the dielectric oxides have been reported for nonvolatile memories.[11,12,26,27] When a gate voltage is applied to the $MoS_2$-based FeFETs, the transfer characteristic curves behaves like a ferroelectric hysteresis loop, with a clockwise direction, realizing the function of nonvolatile memory. However, Pb element of PZT based ferroelectrics is harmful to environment and physical health, limiting the application

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of Pb based ferroelectrics. Using organic ferroelectric polymer poly(vinylidene fluoride-trifluoroethylene) [P(VDF-TrFE)] as the dielectric oxide, electronic devices such as $MoS_2$-based nonvolatile memories and phototransistors have also been proposed.[25,28] However, compared to inorganic FeFETs, the slow dipole dynamics and low mechanical/thermal durability of organic FeFETs restrict their applicability. $BiFeO_3$ (BFO) is a rare multiferroic material with ferroelectric properties at room temperature. Fortunately, the leakage current problem of pure BFO can be resolved by element doping.[29] The combination of BFO with TMDs to achieve memory functions are significant to the development of FeFETs. In addition, high-capacity memories can significantly improve the data storage and computing speed. Multi-bit nonvolatile memories are an effective approach to improve the storage capacity of memories.[30]

Herein, we demonstrate multilevel nonvolatile memory devices (FeFET) adopting 2D $MoS_2$ sheets as the channel and $Bi_{0.85}La_{0.15}Fe_{0.92}Mn_{0.08}O_3$ (BLFMO) as the dielectric oxide. The BLFMO has a large remanent polarization and low coercive field. It is found that the interfacial charges strongly affect the transport hysteresis in $MoS_2$-based FeFETs. By deploying such hysteresis engineering, the FeFETs with memory windows are achieved, which exhibit an on/off current ratio about $10^5$ and a ratio of over $10^4$ between the program and erase states correlating to different gate voltage pulses. The conductivity of the $MoS_2$ channel can be switched between on-states (A, B, and C) and off-state by applying an appropriate amplitude of gate voltage pulses. Moreover, these four storage states remain stable for 1000 s. The $MoS_2$-based FeFETs exhibit excellent performance in cyclic endurance and data retention, paving the way for the application of high-density nonvolatile memories. The memory performances of the as fabricated FeFETs are compared with the other memory devices reported previously (cf., Tables S1 and S2, Supporting Information).

## 2. Results and Discussion

**Figure 1**a shows a schematic diagram of a FeFET with the structure of $MoS_2/Al_2O_3/BLFMO/n^+$- Si. The $n^+$- Si was selected to serve as the substrate and conducting back gate. Figure 1b presents the optical micrograph of a $MoS_2$-based FeFET with channel length of about 20 $\mu$m. Figure 1c illustrates the AFM image of a $MoS_2$ sheet on the BLFMO film. According to the profile, the $MoS_2$ sheet has a thickness of about 13 nm. Figure 1d depicts the Raman spectra of the Si, BLFMO/Si, and $Al_2O_3$/BLFMO/Si. Since $Al_2O_3$ is amorphous, and no peak was observed in the Raman spectra.[31] The BLFMO prepared by the sol–gel method has a polycrystalline structure and it belongs to the space group R3c ($C_{3v}^6$).[32,33] There are $A_1$-3, E-3, and E-nine

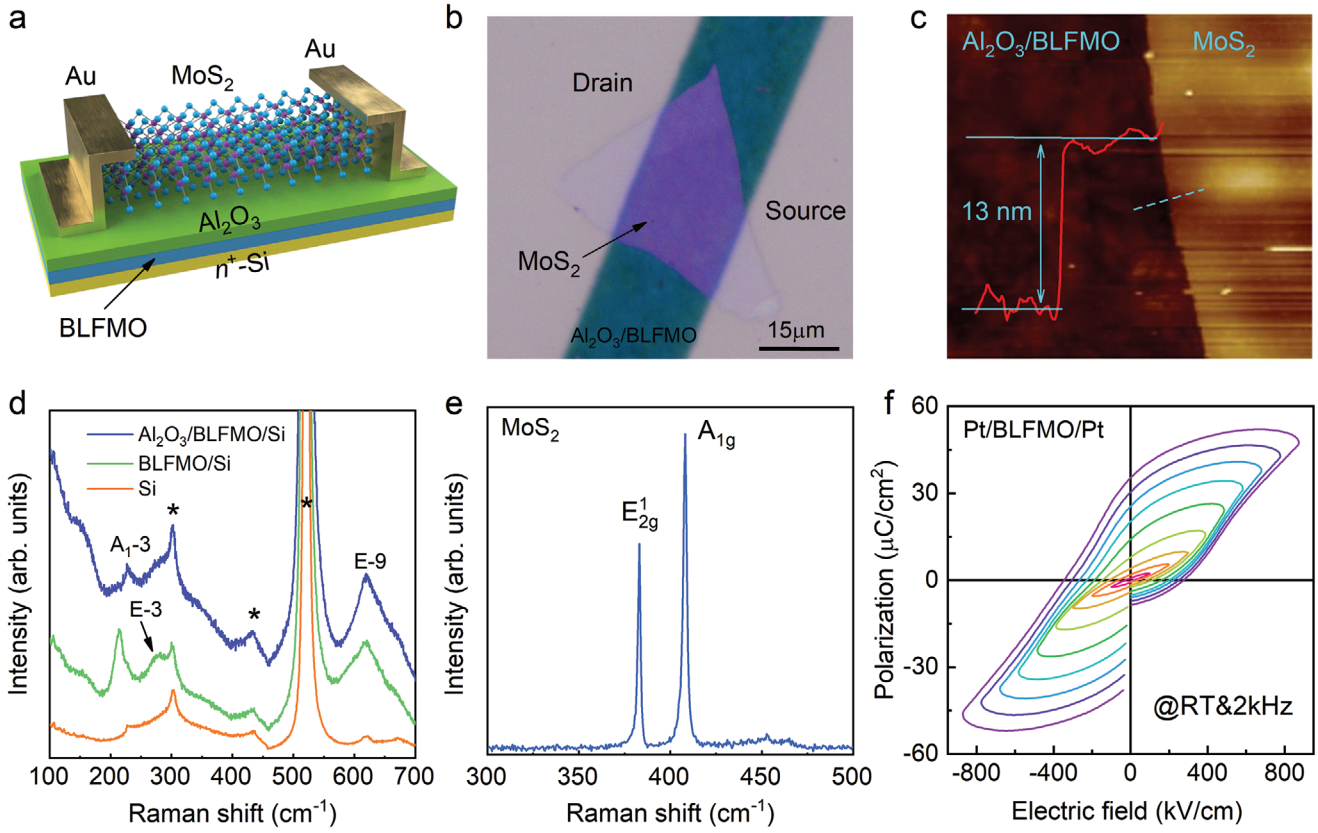


**Figure 1.** a) A schematic diagram of the $MoS_2$-based FeFET configuration. b) Microscope photograph of a $MoS_2$-based FeFET. c) An AFM image of a $MoS_2$ sheet on a $Al_2O_3$/BLFMO. Inset: cross-sectional height profile. d) Raman spectra of the Si, BLFMO/Si and $Al_2O_3$/BLFMO/Si. The symbol (*) indicates the observed trace from Si(100) substracts. e) A Raman spectrum of the as-transferred $MoS_2$ sheet. f) The polarization-electric field (*P*–*E*) curves of a Pt/BLFMO/Pt capacitor.

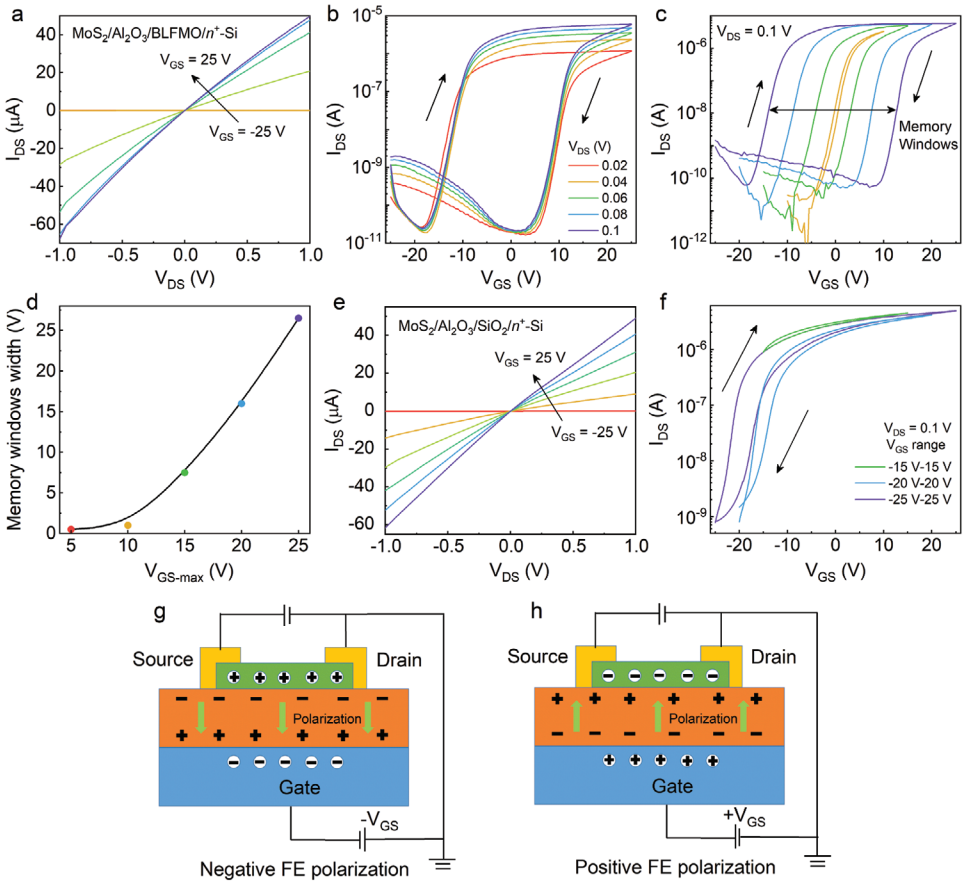


**Figure 2.** a) Output characteristic curves under various $V_{GS}$ from −25 to 25 V. b) Transfer characteristic curves of the FeFETs at various $V_{DS}$ from 0.02 to 0.1 V and c) at $V_{DS}$ = 0.1 V by applying different $V_{GS}$ ranges. d) The width of memory windows as a function of $V_{GS\text{-}max}$. e) Output characteristic curves of the $MoS_2/Al_2O_3/SiO_2$ FET under various $V_{GS}$. f) Transfer characteristic curves of the $MoS_2/Al_2O_3/SiO_2$ FET at $V_{DS}$ = 0.1 V. g,h) Ferroelectric polarization regulates the change of carrier concentration in channel by applying negative/positive $V_{GS}$.

first-order Raman-active modes of $BiFeO_3$ as well as some other modes labeled by the symbol (*) from Si(100) substrates. Moreover, the representative Raman spectrum of multilayer $MoS_2$ is shown in Figure 1e, where two characteristic vibration modes $E^1_{2g}$ (≈382.9 $cm^{-1}$) and $A_{1g}$ (≈408.1 $cm^{-1}$) were observed. The frequency difference between the two Raman modes has been generally utilized as a sign of the thickness of $MoS_2$ sheet.[34,35] The frequency difference $\Delta\omega$ is 25.2 c $m^{-1}$, which indicates that the layer number of the $MoS_2$ sheet is about 19 (≈13 nm).[36] In addition, the *P*–*E* curves of BLFMO films measured by a capacitor composed of Pt/BLFMO/Pt are shown in Figure 1f. As the applied electric field increases, $2P_r$ gradually increases and reaches about 72 $\mu$C $cm^{-2}$. Meanwhile, the coercive field $2E_c$ reaches about 700 kV $cm^{-1}$ at $E_{app}$ = 800 kV $cm^{-1}$ and $f$ = 2 kHz, which is relatively low compared to other ferroelectric materials, for instance, $Hf_{0.5}Zr_{0.5}O_2$ (≈1.5 MV $cm^{-1}$ at $E_{app}$ = 4 MV $cm^{-1}$ and $f$ = 10 Hz).[37] Since the switching speed of the ferroelectric polarization directly affects the operating speed of memory devices,[38] we obtained the polarization switching speed (<1 ms) according to the pulsed polarization positive up negative down (PUND) measurements as a function of pulse width at a given voltage of 15 V (cf., Figure S1a, Supporting Information).

**Figure 2**a depicts the output characteristic curves of $MoS_2$-based FeFETs. The drain–source current ($I_{DS}$) shows a linear increase in the drain-voltage ($V_{DS}$) range from −1 to 1 V, which suggests a good ohmic contact between $MoS_2$ and Au electrodes. Moreover, the concentration of carriers in $MoS_2$ increases with the increasing gate voltage from −25 to 25 V. Figure 2b shows that the memory windows of the FeFETs remain basically unchanged at various $V_{DS}$. The on/off ratio was observed to be about $10^5$ at around $V_{GS}$ = 0 V. It indicates that the $MoS_2$-based FeFETs have a robust performance for non-volatile memory. In addition, the transfer characteristic curves of the FeFETs measured at $V_{DS}$ = 0.1 V are presented in Figure 2c. The transfer behavior reveals a *n*-type feature and a large hysteresis. The electric hysteresis loop appears clockwise due to the combined effect of interface charge and ferroelectric polarization. Figure 2d shows the memory window width as a function of $V_{GS\text{-}max}$. It reveals that the memory window width increases with the sweep range of gate voltages. For comparison, the output characteristic curves of $MoS_2$ on the $Al_2O_3/SiO_2/n^+$- Si substrate are similar to those on the $Al_2O_3$/BLFMO/$n^+$- Si, as showed in Figure 2e. Note that the thicknesses of $SiO_2$ and BLFMO are almost the same (≈200 nm). Figure 2f presents the transfer characteristic curves of $MoS_2$

on the $Al_2O_3/SiO_2/n^+$- Si substrate. As the gate voltage sweeps from −25 to 25 V, the $MoS_2$ conduction channel clearly shows a switch from the off-state to on-state, indicating electron doping (*n*-type) in the as-transferred $MoS_2$ sheets. Interestingly, the $MoS_2$-based FeFET has a smaller Off-state current than $MoS_2/Al_2O_3/SiO_2/n^+$- Si FET since the latter $Al_2O_3$ insulating layer has leakage current, the $MoS_2/Al_2O_3/SiO_2/n^+$- Si FET has no memory window since the hysteresis between the forward and reverse transfer characteristic curves is almost negligible. A simplified model for ferroelectric gating operation in the FeFETs is sketched in Figure 2g,h to explain how the ferroelectric polarization can tune the channel carriers. The n-type $MoS_2$ indicates that electrons are majority carriers. When the BLFMO is down polarized by a negative gate voltage, the top surface of BLFMO is negatively charged, and the $MoS_2$ sheet is positively charged. Thus, the accumulation of holes induces a p-type doping in the $MoS_2$ channel (cf., Figure 2g). On the other hand, when a positive gate voltage pulse is applied, the polarization direction of BLFMO is up polarized. Hence, the depletion of electrons in the $MoS_2$ channel gives rise to the reduced conductivity, as shown in Figure 2h.

To investigate the data storage characteristics of $MoS_2$-based FeFETs, a series of single voltage pulse with various amplitudes was applied to the back gate, and the $I_{DS}$ was measured at $V_{DS}$ = 0.1 V as the reading voltage.[39] **Figure 3**a presents the program function of a FeFET. The $V_{GS}$ is swept from 25 V to different negative voltages (−25, −20, and −15 V) during the programming process. After a negative gate voltage pulse is applied to the FeFETs, the polarization direction of the ferroelectric material is changed, the $I_{DS}$ increases rapidly. As the amplitude of negative gate voltage pulse increases, the $I_{DS}$ increases. The behavior results in the function of multilevel memory. After a gate voltage pulse is applied to the FeFETs, the magnitude of the $I_{DS}$ remains nearly constant within 1000 s. Therefore, at an on-state, the

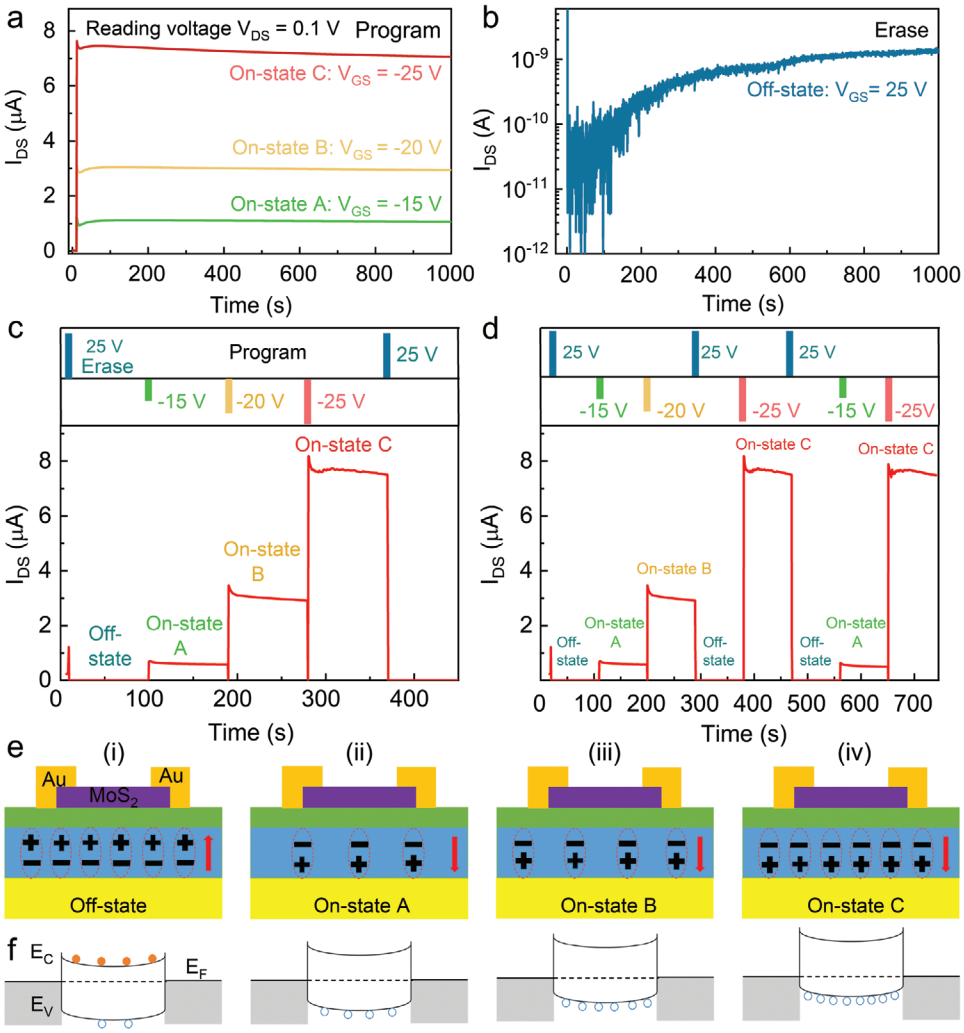


**Figure 3.** The $I_{DS}$ decay within 1000 s after a single gate voltage pulse with amplitudes swept a) from +25 V to −25, −20, and −15 V and b) from different voltages to 25 V at a reading voltage of $V_{DS}$ = 0.1 V. c) Evolution of read current of the memory device under various operation states, which indicates the multilevel data storage characteristics. d) The stability in inter-state variation. e) Polarization bound charge distribution of ferroelectric gating operation in a FeFET device and f) the corresponding energy band diagrams. Blue circles and orange dots represent holes and electrons, respectively.

$I_{DS}$ is observed with negligible decay after 1000 s, which realizes the function of nonvolatile multilevel memory. Figure 3b presents the erase function of the FeFET. The $V_{GS}$ is swept from different voltages to 25 V during the erasing process. When the $I_{DS}$ of FeFETs is still at a relatively large level, the $I_{DS}$ drops rapidly after a positive gate voltage pulse is applied. The larger positive gate voltage pulse applied to the FeFETs, the smaller the $I_{DS}$. It can also be observed that the $I_{DS}$ magnitude does not change much within 1000 s, which reveals that the device has a good erase function. Figure 3c outlines the dynamic multi-bit memory behavior of $MoS_2$-based FeFETs by modulating amplitudes of the programming voltage pulses. Initially, the device is excited under an erasing pulse of 25 V. Then, the conductivity of the $MoS_2$ channel can be switched between the three nonvolatile on-states by applying an appropriate negative gate voltage pulse with 250 ms pulse width. When one tunes the amplitude of gate voltage pulses from −15 to −25 V, the on-state is switched from A to B to C. From a practical perspective, the stability of the three on-states is a crucial factor for a memory device to maintain functionality. It reveals that $MoS_2$-based FeFETs can realize the function of continuous nonvolatile multilevel memory. Figure 3d reveals the stability in inter-state variation of the memory device. This memory switches randomly between the four states (off-state, on-state A, on-state B, and on-state C) by tuning the amplitude of gate voltage pulses. Each state can be switched quickly and remains stable, which depictes that this memory could realize the operation of free switching stably between the four states.[40] Generally, we can denote the on-states A, B, and C as digital logic "1," "2," and "3," and the off-state as digital logic "0," achieving multi-bit data storage.[30] These multi-bit memories could avoid the degraded endurance and high-power consumption caused by repeatedly programming/erasing processes. Due to the significant difference of $I_{DS}$ under different ferroelectric polarization, the conductivity of $MoS_2$ channel can be switched by applying negative or positive gate voltage pulse to the BLFMO dielectric oxide in an invertible, nonvolatile, and reproducible way. To explain the working principle of the FeFETs, we raise FeFETs working schematics and band diagrams to interpret the effect of the ferroelectric polarization under different $V_{GS}$ values, as shown in Figure 3e,f. Since ferroelectrics have remanent polarization, the carriers will be accumulated or depleted in the $MoS_2$ channel if they are not counteracted by interfacial states or traps in $Al_2O_3$. The different $V_{GS}$ values will change the gap between the Fermi level and the bottom of conduction bands. It can tune the conductivity of the channel to realize the function of multi-bit memory.[11] In addition, the switching speed of memory devices has been detected by a probe station with a testing limit of 50 ms, as shown in Figure S1b, Supporting Information. It reveals that the as-fabricated memory devices have a high-speed operation less than 50 ms. Therefore, FeFETs could be used for electronic synaptic devices to mimic the functionality of biological synapses in the nervous system owing to the ability of multi-bit memory.[41,42]

A further step, the retention and endurance characteristics of the FeFETs were evaluated to verify their reliability. **Figure 4**a shows the retention characteristic of the FeFETs by applying single gate voltage pulses of 25 V to erase and −25 V to program at $V_{GS}$ = 0 V and $V_{DS}$ = 0.1 V. The program and erase states with a high program/erase ratio about $10^4$ exhibit no degradation under a continuous $V_{DS}$ bias of 0.1 V during 2000 s. It suggests that it maintains for a longer time since the two states mainly depends on the polarization characteristic of BLFMO. Figure 4b depicts the endurance performance of the memory devices as a function of program or erase cycles number. The endurance cycle is formed by a gate voltage pulse amplitude of 25 V (erase) and −25 V (program) with a pulse width of 250 ms at $V_{DS}$ = 0.1 V in each cycle. The erase state decreases during the course of 1000 cycles due to charge-trapping, and the program/erase ratio increases above $10^4$ with the increase of cycle number, indicating a good performance of the $MoS_2$-based FeFET devices. Figure 4c reveals the extracted $I_{DS}$ as a function of pulse number at $V_{GS}$ = −15, −20 and −25 V. The $I_{DS}$ remains in the same order, and the change is not obvious. The memory states of the device remain stable under the continuous gate voltage pulses with various amplitudes (cf., Figure 4d). Three kinds of negative gate voltage pulses (–15, –20, and –25 V) were applied to the memory devices. Note that the pulse number was fixed at 50. The $I_{DS}$ rises from 4 to 8.8 μA with increasing $V_{GS}$ amplitude. It reveals that the memory states of the device remain stable under the continuous gate voltage pulses with various amplitudes, eventhough the $I_{DS}$ has a slight upward trend. The capability of the device as memories may enable numerous noval applications. The key feature of the devices is that the channel conductivity can be dynamically tuned by gate voltage pulse, which can enable dynamic reconfigurability between active-high and active-low logic in the memory output data.[43] In addition, Figure S2, Supporting Information shows the transfer characteristic curves of different memory devices to reveal the statistical distribution. All devices have relatively large memory windows with a nonvolatile memory function, which indicates that the yield of the memory devices is high.

## 3. Conclusion

In summary, FeFETs comprising 2D $MoS_2$ channels with BLFMO ferroelectric films have been demonstrated in details. The $MoS_2$-based FeFETs have a large memory window (25 V), which exhibits multi-bit storage with a high on/off ratio (≈$10^5$) by tuning the polarized states of the BLFMO. By applying gate voltage pulses with different amplitudes, the FeFETs exhibit an obvious multi-bit memory effect. The on-state is switched from A to B to C, which can be denoted as digital logic "1," "2," and "3," and the off-state corresponds to "0." From a practical perspective, the stability of the four states is a crucial factor for a memory device to maintain functionality. The retention characteristic of these nonvolatile states indicates that no obvious decay of $I_{DS}$ is observed during 1000 s. The high-yield 2D $MoS_2$-based FeFETs without lead element exhibit excellent performance in cyclic endurance, data retention, and high-speed operation, paving a way for the application of high-density and cost-effective nonvolatile multi-bit memories.

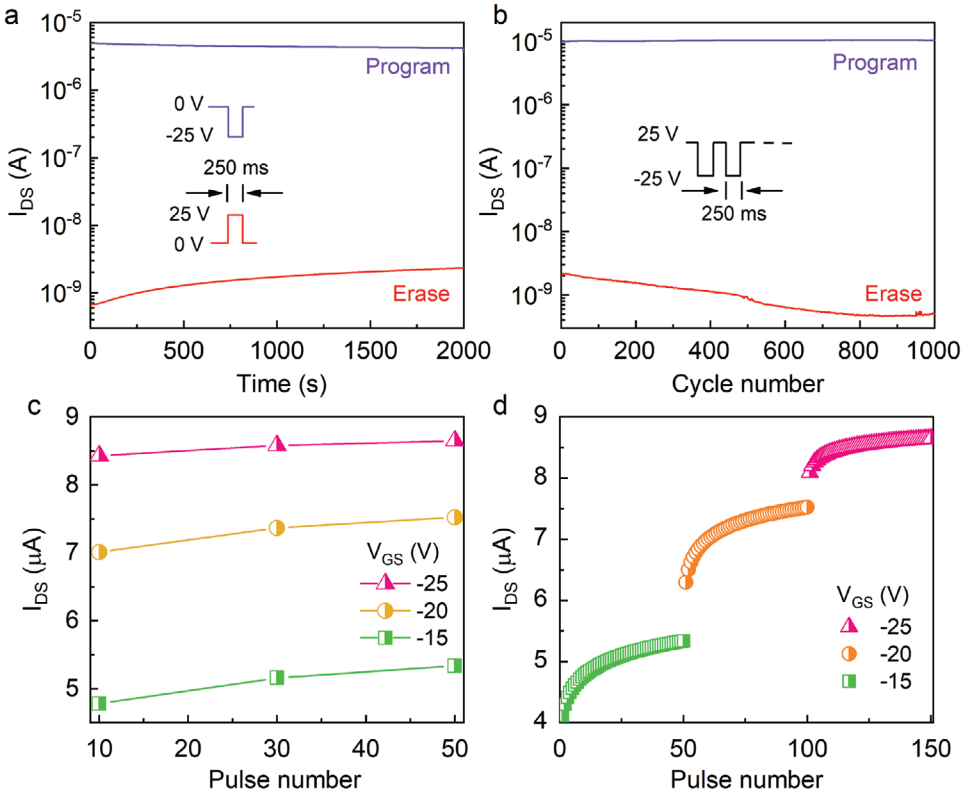


**Figure 4.** a) Retention performance of FeFETs based memory by applying a single gate voltage pulse at $V_{DS} = 0.1$ V. b) Endurance characteristics of the memory device. Program and erase operations were carried out under cyclic voltage pulses at $V_{DS} = 0.1$ V. c) $I_{DS}$ under various numbers of amplitudes of $V_{GS}$ (–15, –20, and –25 V) as a function of pulse number. d) $I_{DS}$ under several sequential gate voltage pulses with various amplitudes.

## 4. Experimental Section

*Synthesis of (Bi, La, Fe, and Mn)-Precursors*: Glycol methyl ether [$CH_3OCH_2CH_2OH$, 99.5%] and glacial acetic acid [$CH_3COOH$, 99.5%] were mixtured as a solvent, and citric acid [$C_6H_8O_7$, 99.5%] was added as a chelating agent. Wherein the molar ratio of citric acid and metal ions is 2:1. Analytically pure bismuth nitrate pentahydrate [$Bi(NO_3)_3{\cdot}5H_2O$, 99.0%], lanthanum nitrate hexahydrate [$La(NO_3)_3{\cdot}6H_2O$, 99.0%], ferric nitrate nonahydrate [$Fe(NO_3)_3{\cdot}9H_2O$, 98.5%], and manganese acetate tetrahydrate [$Mn(CH_2COOH)_2{\cdot}4H_2O$, 99.0%] were adopted as solutes. Note that adding 7 mol% excess Bi to make up for the loss of Bi during annealing. Finally, the 0.2 M precursor solution was stirred for 12 h at about 60 °C and was then cooled to room temperature.

*Deposition of $Bi_{0.85}La_{0.15}Fe_{0.92}Mn_{0.08}O_3$ and $Al_2O_3$ Films*: The $n^+$-Si (100) substrates were cleaned for 15 min with deionized water, alcohol, and ethanol in an ultrasonic machine. Then, the substrates were purged with nitrogen to keep the surface dry and clean. The $Bi_{0.85}La_{0.15}Fe_{0.92}Mn_{0.08}O_3$ films were deposited by spin coating the 0.2 M precursors onto the substrates at a speed of 3500 rpm for 35 s. The as-prepared layers were prebaked at 200 °C for 5 min, followed by annealing at 600 °C for 5 min in a nitrogen atmosphere for crystallization. The coating and annealing-treatment procedures were repeated seven times to obtain about 200 nm-thick films. A further step, 30 nm-thick $Al_2O_3$ films were deposited on the BLFMO films by atomic layer deposition at the 200 °C substrate temperature. Trimethy laluminium [$Al(CH_3)_3$, 25% w/w in hexane] and deionized water ($H_2O$, 18 MΩ) were used as Al and oxygen sources, respectively.

*Fabrication of Devices*: To fabricate the FeFETs, $MoS_2$ sheets were dry-transferred to the $Al_2O_3$/BLFMO/$n^+$- Si and $Al_2O_3/SiO_2/n^+$- Si substrates by mechanical exfoliation to form a channel. A copper mesh was used to form the source and drain electrodes on the $MoS_2$. Then, 100 nm-thick Au electrodes were directly evaporated on the as-transferred $MoS_2$ sheets by a thermal evaporator.

*Characterization*: A commercial AFM system (Dimension Icon, Bruker) was employed to detect the surface topography of the $MoS_2$ sheets on BLFMO films. A confocal micro-Raman spectrometer (LabRAM HR Evolution, Horiba Jobin-Yvon) in the backscattering geometry was used to carry out the Raman measurements. The wavelength of the argon ion laser line is 532 nm. A 50× objective lens with a working distance of 18 mm was provided to focus the laser beam on the few-layer $MoS_2$ sheets. The ferroelectric behaviors of BLFMO films were recorded using a ferroelectric test system (Precision Premier II: Radiant Technologies Inc.). The electrical measurements of FeFET were performed by an accurate semiconductor parameter analyzer Keithley 4200-SCS.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Author Contributions

Q.Z., H.X., and Q.W. fabricated the samples, W.X. and M.D. performed the structural analysis. Y.L. analysis the ferroelectric properties. H.X. and L.X. performed the electronic measurements. Q.Z. and J.Z. wrote the paper. J.Z., Z.H., and J.C. supervised the research. L.S., W.L., and Y.L. contributed to the discussions. All authors have given approval to the final version of the manuscript.

## Data Availability Statement

Research data are not shared.


## Keywords

2D layered semiconductors, ferroelectric films, ferroelectric field-effect transistors, multi-bit nonvolatile memories



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