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Entwicklung integrierter Detektoren für geladene Teilchen und Photonen

Development of integrated detectors for charged particles and photons

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M. Sc. Hui Zhang

geb. in: Xuzhou, Jiangsu, China

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Hauptreferent:	Prof. Dr. Ivan Perić
Korreferent:	Prof. Dr. André Schöning

Zusammenfassung

Das Thema meiner Dissertation ist die Entwicklung von mehreren innovativen anwendungsspezifischen ICs (ASICs) für verschiedene wissenschaftliche und medizinische Anwendungen.

Der erste von mir entwickelte ASIC ist ein Auslesechip (MPROC) für einen Hybridpixeldetektor für medizinische Anwendung. Der Chip kann für die Auslese eines CdTe-Sensors verwendet werden. Der zweite ist ein Sensorchip für einen kapazitiv gekoppelten Pixeldetektor (CCPD) (CCPD53). Es könnte für die Innenlage des ATLAS-Pixeldetektors angewendet werden. Der dritte Chip ist ein monolithischer Pixeldetektor (HVMAPS25) mit kleinem Füllfaktor für CLIC- oder CEPC Teilchenphysik-Experimente.

Ich war auch an der Entwicklung von ASICs (CLIC v1/v2 und v3 High Dynamic Range) für PANDA- und CLIC-Experimenten beteiligt. Sie bieten eine präzise Flugbahnrekonstruktion sowie Energie- und Impulsmessungen. Ich habe ebenfalls an einigen weiteren Projekten gearbeitet, die in dieser Dissertation nicht beschrieben wurden: Sensoren lFoundry Prozess, ATLASPIX1 und ATLASPIX3, MUPIX8.

Auch wenn diese Projekte unterschiedlich sind, verwenden sie ähnliche Schaltungen.

Die Pixelelektronik von jedem ASIC enthält ladungsempfindlichen Verstärker, RC-Filter, Rückkopplungsschaltungen, Komparator mit Tune-DACs.

Die Ausleseschaltung wurde ursprünglich für monolithische Sensoren entwickelt. Dieselbe Schaltung wurde auch im MPROC verwendet.

Die Chipperipherie ist bei allen Designs ähnlich. Sie enthält eine synthetisierte Ausleseteuereinheit.

Die Designs sind aus mehreren Gründen innovativ und komplex.

Bei monolithischen Sensoren: niedriges Rauschen (wegen schwacher Signale), niedriger Stromverbrauch (wegen hoher Kanalzahl) und hohe Bandbreite (wegen der spezifizierten hohen Zeitauflösung) der Verstärker ist erforderlich. Die langen Verbindungen zwischen den Pixels und Auslesezellen stellen Herausforderung dar.

Im Fall von MPROC: Das Übersprechen zwischen den Signalen kann vermieden werden, da es keine langen Verbindungen gibt. Das Pixel ist jedoch ziemlich komplex und enthält analoge und digitale Schaltungen.

Neben den vielen Gemeinsamkeiten, hat jeder Chip auch seine ganz besonderen Eigenschaften. Es gibt mehrere neuartige Schaltungen.

Beim MPROC-ASIC wurden in der Pixelelektronik zwei verschiedene Rückkopplungsarten entwickelt, damit der Chip Elektronen und Löcher verstärken kann. Es wurde eine spezielle Pixelanordnung implementiert, um einen kleinen Bonding-Pad-Abstand (55 Mikrometer) zu erreichen und die Ladungsteilung zu minimieren. Um eine hohe Energieauflösung zu erreichen, wurden die Spitzendetektoren und 10-Bit-Zählern implementiert. Eine hohe Zeitauflösung kann durch einen 7-Bit-TDAC erreicht werden. Sehr kleine Pixelgröße für eine 180nm Technologie wurde erreicht. Im Fall des CCPD-Projekts wurden auch einige Innovationen getestet. Eine tiefe p-Wanne wurde verwendet, um die Pixelelektronik vom Sensorsubstrat zu isolieren. Die Auslese von kleinen Pixels wurde durch Multiplexen von Signalen ermöglicht. Messungen mit kapazitiv gekoppelten Chips wurden gemacht.

Im Fall des HVMPAS25-Chips wurde eine kleine Ladungssammelelektrode im HVCMOS-Prozess implementiert. Sehr kleine Pixelgröße konnte erreicht werden. Die n-Wannen des Sensors sind mit den Verstärkern AC-gekoppelt und können an eine Vorspannung von 10 V gelegt werden.

Bei CLIC- und PANDA-ASICs werden verschiedene Versionen von Komparator und Verstärker beschrieben. Es wurden Schaltungen für mit einem hohen Dynamikbereich entwickelt.

Folgende Messungen wurden für alle ASICs durchgeführt.

1) Amplitudenmessung des Verstärkerausgangs mit Oszilloskop.

2) Chips-Bestrahlung mit Fe55-Quelle und Vergleich der Amplituden.

3) Schwelle-Scan-Messungen.

4) Messungen der Pulsbreite (ToT).

5) Messungen der Zeitwanderung (TW).

Abstact

The contribution of my dissertation are designs of several CMOS application specific integrated circuits (ASICs) for different scientific and medical applications.

The first ASIC developed by me is the readout chip (MPROC) for a hybrid pixel detector for medical application. The chip can be used to read out a CdTe pixel sensor.

The second ASIC is a sensor chip for a capacitively coupled pixel detector (CCPD) (CCPD53). It could be applied in the inner layer of the ATLAS pixel detector.

The third chip that I developed is monolithic pixel detector (HVMAPS25) with small fill factor for CLIC or CEPC particle physic experiments.

I was also involved in the development of the ASICs (CLIC v1/v2 and v3 high dynamic range) that could be applied in PANDA and CLIC experiments. They provide precise trajectory reconstruction, energy and momentum measurements.

I also worked on several other projects that are not described in the thesis: sensors in lFoundry process, ATLASPIX1 and ATLASPIX3, MUPIX8.

Although the applications are different, the circuits have similarities.

The pixel electronics of each ASIC contains charge sensitive amplifier, RC filter, feedback circuits, comparator with tune DACs. The readout circuit was as first developed for a monolithic sensor. The same readout circuit has been used in the MPROC as well. The chip periphery is similar to all designs. It contains synthesized readout control unit.

The designs are from several reasons challenging.

In the case of monolithic sensors: low noise (because of low signals), low power consumption (because of high number of channels) and high bandwidth (because of specified high time resolution) of the amplifiers is required. The routing of long lines between pixels and readout cells is challenging. In the case of MPROC: the crosstalk between signals can be avoided because there are no long connections. However, the pixel is quite complex and it contains analog and digital circuits.

In addition to the similarities, each chip has its own special properties. There are several novel circuits.

In the case of MPROC ASIC, two various feedback types have been designed in pixel electronics so that the chip can amplify electrons and holes. A special pixel arrangement

has been implemented to achieve small pad pitch (55 mircometers) and to cope with charge sharing. High energy resolution could be achieved by use of peak detectors and 10 bit counter. High time resolution can be achieved by a 7 bit TDAC. Very small pixel size for a 180nm technology have been achieved.

Also in the case of CCPD project I have tested several novelties. The deep p-well has been implemented in the technology for the first time and used for isolation the pixel electronics from the sensor substrate. The readout of a small pixels was achieved using a special output signal encoding. Measurements with capacitively coupled ASICs have been performed.

In the case of HVMPAS25 chip, small charge collection electrode has been implemented in HVCMOS process. Very small pixel size could be achieved. The sensor n-wells are AC-coupled to the amplifiers and they can be biased with 10 V with respect to the p-substrate.

In the case of CLIC and PANDA ASICs, different versions of comparator and amplifier are described. Circuits for high dynamic range were implemented.

I have performed detailed characterization of the chips that included following measurements:

1) Amplitude measurement of amplifier output with oscilloscope.

2) Chips irradiation with Fe55 source and comparison of the signal amplitudes.

3) Threshold scan measurements and calculation of the mean as well as sigma of the threshold dispersion from the fit data.

4) Pulse width (ToT) measurements.

5) Time walk (TW) measurements.

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1 Introduction

This dissertation aims to present the development of Application Specific Integrated Circuits (ASICs) for scientific applications such as high energy physics and x-ray detection for medical application. The ASICs are used to build silicon pixel detectors.

Semiconductor detectors play a very important role in commercial applications and have experienced a rapid development in the last years. They are widely used in science such as elementary particle physics, optical and X-ray astronomy, nuclear physics, medicine and many other field. These applications demand extremely low-noise, low power, single-particle detection capability and some other properties such as 100 % fill factor, high time resolution, high readout speed, radiation tolerance as well as the precise measurement of energy and position of particles [10]. The development of intelligent semiconductor sensors in commercial complementary metal oxide semiconductor (CMOS) technologies is the focus of my work and also of our research group (KIT-ADL).

1.1 My contribution

MAPS

Monolithic active pixel sensors (MAPS) in commercial high-voltage CMOS (HVCMOS) technology are one of our inventions. These monolithic ASICs have the potential to be the imaging lenses of current and future collider experiments consideration of many reasons [11]. They are one of the most advanced detectors for detecting high-energy particles. Examples of HVCMOS sensors are ATLASPix1, ATLASPix3, CLIC, HVMAPS25, etc. A monolithic pixel detector is essentially a system on chip (SoC). The sensor diode, analog and digital signal processing, storage, power regulation and test functions are implemented inside the same substrate. For some ASIC, the reverse bias up to -120 V could be achieved. The application of high voltage enhances the thickness of a depletion region and enlarges the active sensor volume. Following this idea, KIT-ADL develops HVCMOS pixel sensors in international collaboration.

My contribution to this invention was participation on ATLASPix1, ATLASPix3, and CLIC ASIC designs and design of LFoundary and HVMAPS25 sensors. Since the pixel electronic, readout cells, readout control unit (RCU) and pads are quite similar, I explain only the HVMAPS25 and the CLIC electronics, which are covered in chapter 4 and chapter 5. The concept of HVCMOS technology, general pixel electronics design, a special combination

between pixel electronics and readout cells, as well as some measurement results are presented.

Hybrid pixel detectors and CCPDs

Hybrid pixel detectors are another research theme that I followed. In the case of a standard hybrid pixel detector, each channel of a sensor chip and readout chip is connected via bump bond using flip-chip technology. Since the sensor and readout chip are separated, both can be tailored independently to meet the demands. In other word, the sensor can be optimized for radiation tolerance or for detection of x-rays, the readout chip can be made to process high particle hit rates of the order of MHz/mm^2 [1].

The readout chip named MPROC for medical X-ray detection has been implemented and tested. The design details, the properties of CdTe material compared with silicon, noise analysis, crosstalk influence, several simulation as well as measurement results are describes in chapter 2.

I was also involved in the development of capacitvely coupled particle detector (CCPD). Compared with standard hybrid detectors, the signals are transferred through capacitive coupling instead of bump bonds. For this innovation, a new concept has been proposed without glue. The sensor chip and the readout chip are mechanically connected with a small number of relatively large bump bonds. The bumps provide mechanical stability to the detector and no double side wire bonding is needed.

Two chips have been introduced in chapter 3 for proving the functionality of the new concept: CCPD53 sensor chip and PHOTON readout chip. The CCPD readout chip, which has not been produced, is also my contribution for this project. The design of CCPD53 sensor chip and PHOTON readout chip has been introduced with emphasis on special address encoding and arrangement of both chips.

Measurement setups, standalone sensor chip test, as well as both chip measurement results have been shown to prove the functionality of the new CCPD concept.

To summarize: Several developments have been introduced in my thesis. The developments can be classified as shown in figure 1.1. I have worked on a hybrid pixel readout ASIC for x-ray detection in medical imaging field. I have also worked on one hybrid pixel detector with new CCPD concept for high energy physics in ATLAS inner layer. Finally I developed monolithic pixel detectors with small and large diode sizes for particle detection.

Application and Requirements

Different applications lead to different requirements for the science-grade pixel sensors. In the case of high energy physics, pixel sensors are used to detect high-energy charged particles, more precisely to determine particle trajectories, their momenta and creation point [53]. Since particles tracking requires many layers of planar detectors, tracking sensors should be very thin and as transparent for particles as possible. Otherwise, the particles will be deflected by the inner-layers from their initial trajectories (multiple scattering) making impossible momentum, vertex and other measurements that require the data obtained by subsequent detector layers [2]. Silicon is the best material for such detectors since silicon-based technologies offer the possibility to implement any possible semiconductor device (from PN junction to the completed signal processing electronics) on the sensor. However, in the case of medical imaging, photon sensors should be thick enough to absorb the largest part of the radiation. Often another sensor material instead of silicon is chosen, due to its low absorption coefficient [33]. One example is CdTe material. X-ray detection is done in the CdTe pixel sensor. Since CdTe-based technologies do not allow implementation of electronic components, the sensor is connected to a silicon pixel readout chip.

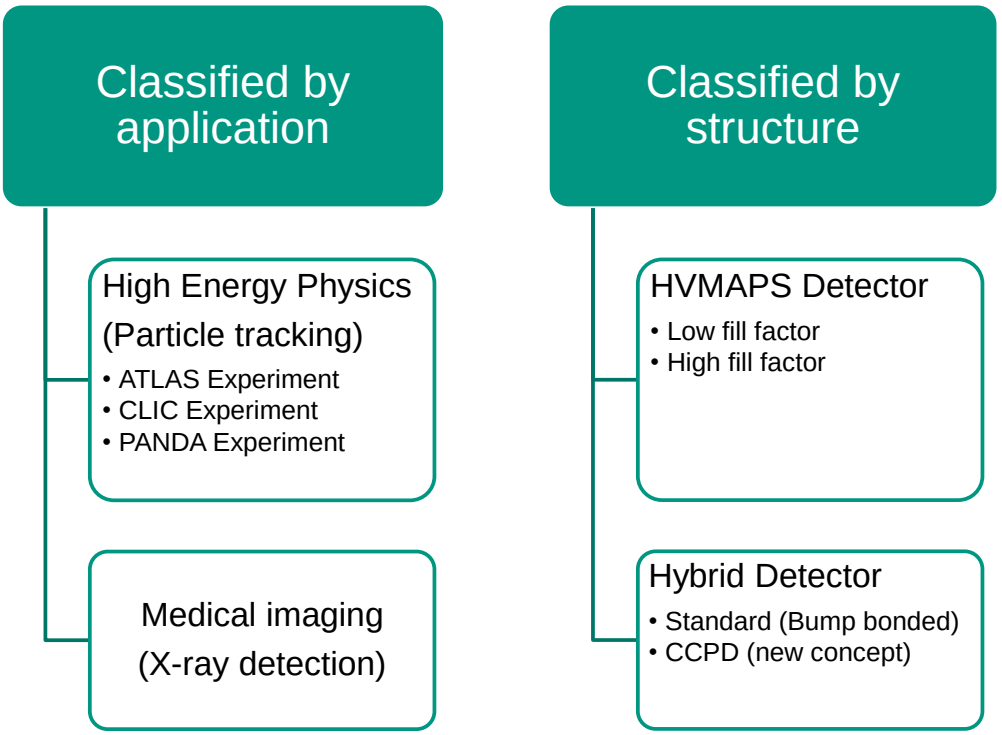


Figure 1.1: Classification of pixel detectors according to applications and structures (covered in my thesis)

Comparison Hybrid versus Monolithic

Following factors should be taken into account to decide whether hybrid or monolithic structure is used: 1) spatial resolution. 2) radiation tolerance. 3) complexity of readout circuitry. 4) power consumption. 5) area and cost, etc. Some characteristics of monolithic and hybrid pixel detectors are listed [45]:

Monolithic

- Lower noise
- Lower power consumption because of a small sensor capacitance
- Lower material budget
- Smaller pixels, since electronics are designed outside of the charge collection region.
- Higher spatial resolution with simplified interconnections.
- Usually limited radiation hardness
- Numerous metal lines are needed for connection pixels and readout cells

Hybrid

- The choice of materials and technologies can be optimized depending on the applications.
- Higher readout speed, since the pixel signal are transmitted without multiplexing and they can be processed in parallel.
- Usually fully depleted sensors.

- Costly interconnection between sensor and electronics process (bump bonding).
- Material: sensor usually 200 - 250 μm, electronics 100 - 200 μm
- Spatial resolution is limited due to the sensor thickness and pixel size
- Higher power consumption due to a large sensor capacitance.

1.2 Design Process

ASIC (Application Specific Integrated Circuit) design needs to be designed for the special needs of users, rather than intended for general-purpose use. According to different applications and customers, the challenge and requirements are quite different. Therefore, specific design ideas come into being for specific issues.

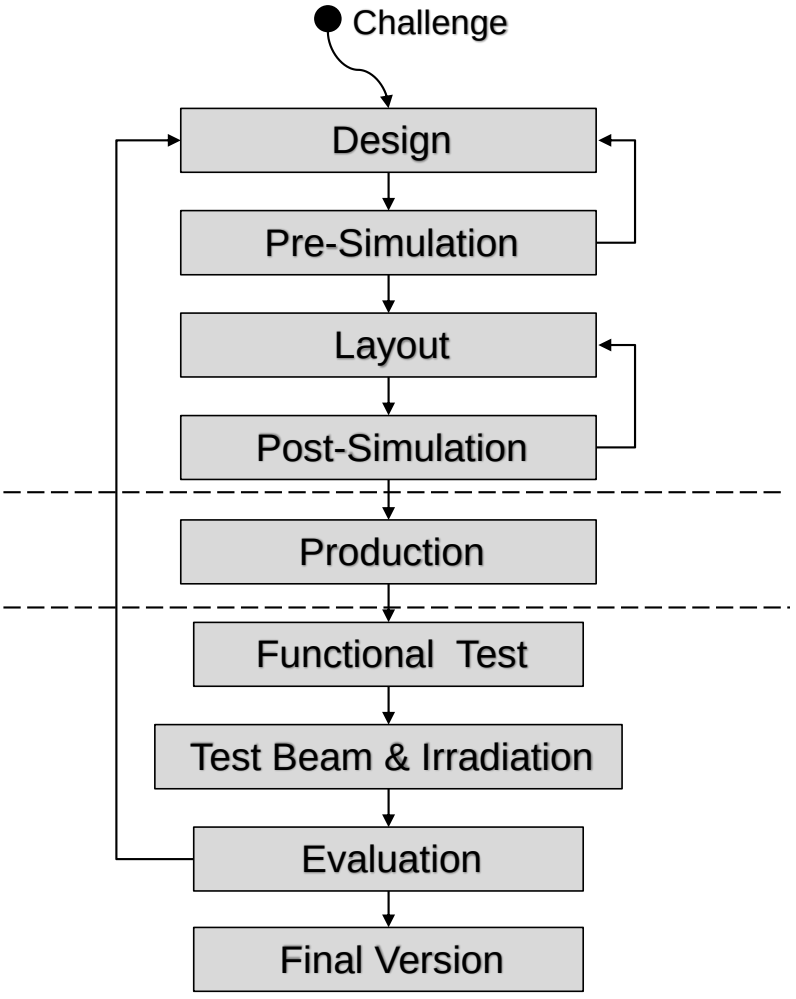


Figure 1.2: Full custom chip design process

Figure 1.2 presents the analog and full custom digital design flow.

The first step is to find a precise system architecture for a specific application. After that, pre-simulation step is indispensable. Even if the pre-simulation is not precise because for example, parasitic capacitances, cross talk, leakage currents are not considered, the fundamental functionality could be proved by this step. The layout is designed after that. In order to achieve compact, dense and short line routing, we need to optimize the layout in several steps. Voltage drops, crosstalk, shielding, antenna effects, matching should be taken into account. After both DRC (design rule check) and LVS (layout vs schematic) check passed, post-layout simulation is done. Cadence is suitable for the electrical simulation. For the readout architecture simulation, readout modelling environment (ROME) (designed by R. Schimassek, at KIT-ADL) [64] is normally applied for assess and optimize the overall architecture. This simulation framework was used to optimize the readout architecture of ATLASPIX chip. Our designs are produced by commercial vendors, for example: LFoundry, TSMC, AMS, TSI, UMC, etc. For different applications different production

technologies have been chosen. Before choosing a certain vendor, cost, production time, process characteristics, yield rate, should be considered.

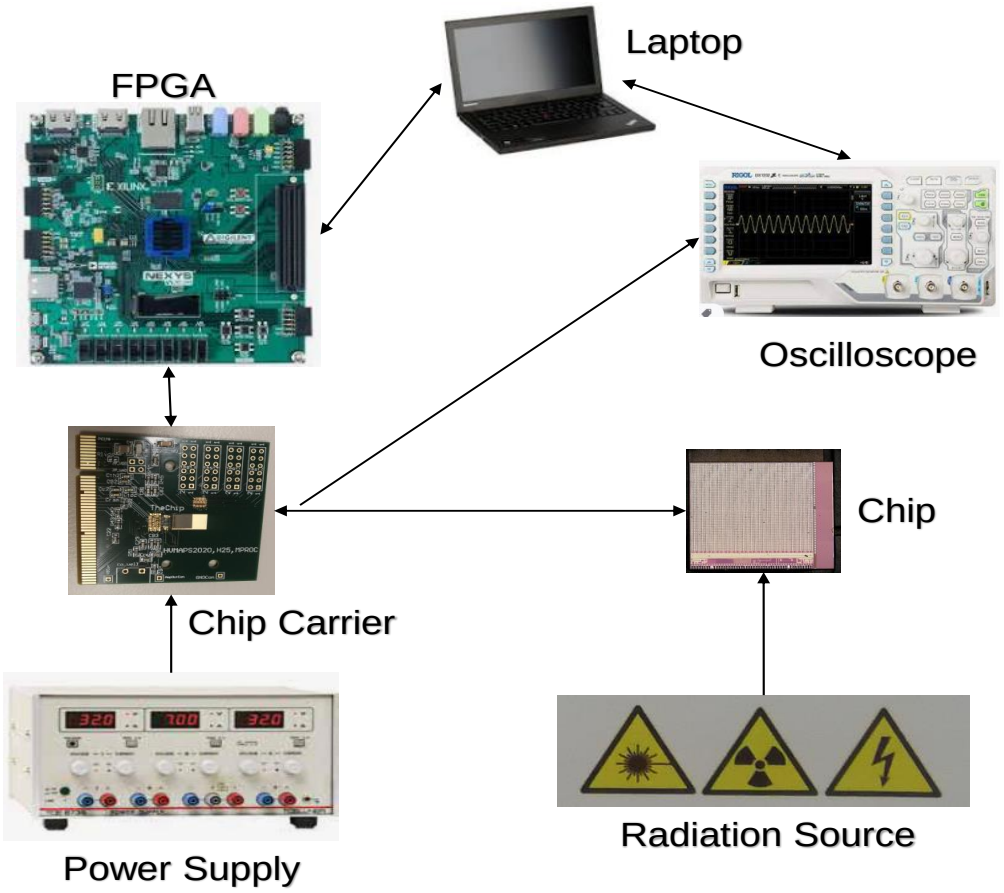


Figure 1.3: General experiment setup

Our test systems are based on test-PCB for the chip connected to adapter board (GECCO), connected to FPGA board, connected to PC (laptop) vias USB. The test-PCB is the carrier for the chip. The chip is directly bonded to the test-PCB. The test-PCB contains only passive components such as the PCI connector. It contains the bonding pads for the chip. The test-PCB is connected via PCI connector to the GECCO adapter board. GECCO board has an FMC connector for the FPGA board.

The GECCO system contains also firmware and software code written in Vivado and Qt. The code should be adjusted for different chips.

Figure 1.3 shows the general experiment setup. Laptop does data acquisition, storage and data analysis. Besides, it provides GUI and test environment. FPGA board performs data decoding and generate digital signals for ASIC. Oscilloscope measures and analysis the waveforms. Test PCB carries chip and routes power and signals. Power supply generates power supply voltages and some bias voltages. Test signals can be generated in many ways, for example, by charge injection via injection circuit, by radiation sources like 55Fe or 90Sr, by laser pulses, etc.

Typical measurements are: functional tests of all components in the signal chain, injection signal calibrations, pixel threshold measurements (threshold scan), threshold trimming, measurements of temporal and spatial resolution...

1.3 HVCMOS Pixel Sensors

HVCMOS pixel sensors can be implemented in commercial CMOS technologies. A high voltage is used to increase the sensor volume, improve time resolution, detection efficiency and radiation hardness.

Unlike the standard MAPs structure, where the signals are generated in the epi-layer or undepleted lowly doped bulk and the charge is collected by diffusion, the signals of HVCMOS pixel sensors are generated in the depleted region and are collected mainly by drift because of the strong electrical field. Thus the detector is suitable for the applications where fast signals are needed.

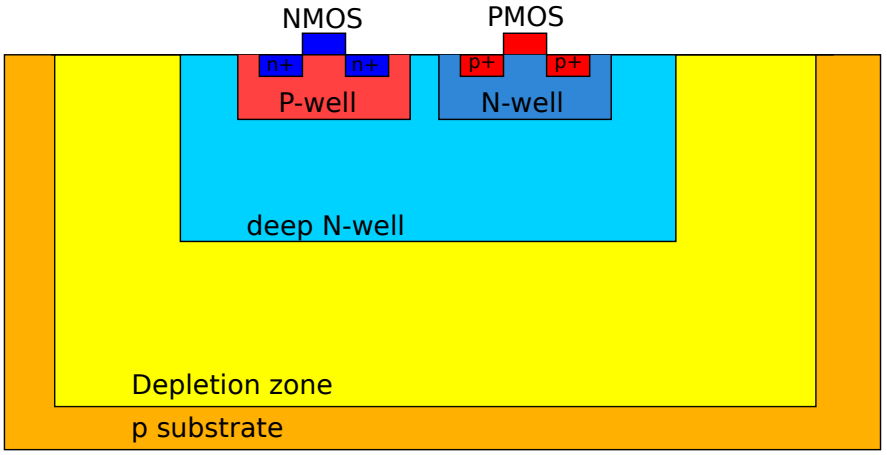


Figure 1.4: HVCMOS sensor

The HVCMOS sensor proposed here uses a lowly doped PN junction. The lower dopant concentration allows a higher reverse voltage bias than the typical PN junction in the standard CMOS process. The high negative bias voltage (up to -120V) is applied to p substrate.

The resistance of p-substrate depends on the doping concentration. It is typically 200 Ω for our design. Due to the high substrate resistivity, a depleted region up to 50 μm can be achieved, which is one order of magnitude larger than that in a standard CMOS technology.

A high radiation tolerance is expected as well. Owing to the small charge collection distance (from p substrate to deep n-well), the possibility of charge trapping after radiation is decreased. HVCMOS prototypes have shown a radiation tolerance up to 100 MRad and 1 x 10^{15} neq/cm^2 with an efficiency of 99.7 % in test beam [14].

Both PMOS and NMOS transistors can be implemented in a pixel of a HVCMOS sensor. The PMOS transistors are placed in the shallow n-well, which are ohmically connected with the deep n-well, the NMOS transistors are in the p-well which is inside the deep n-well. The deep n-well plays two roles. First, it is used for the charge collection. Second, the deep n-well is the substrate for PMOS transistors placed in it.

The pixel with deep n-well are arranged as matrix, their depleted region in this case partially overlap. When the particle hits the pixel, the charge below or between the n-wells will be collected to the nearest n-well. The pixel detector has therefore 100 % fill factor.

Modified HVCMOS Process with a implant deep P-well

Two improvements of HVCMOS sensor have been tested within this thesis: 1) implant a deep p-well and 2) to use a small charge collection electrode. Additionally a high resistivity

substrate of 200 Ωcm has been applied. This leads to a larger depletion region for a given reverse bias, which decreases detector capacitance, ensures low noise and increases input signal in the case of charged particle detection.

The deep p-well is implanted between the n-well and the deep n-well and is used to isolate PMOS transistor from the n-well. This structure is very helpful to reduce crosstalk from electronics to sensors. This is important when we have big amplitude of output signals. Deep p-well has been used in several designs presented in this thesis.

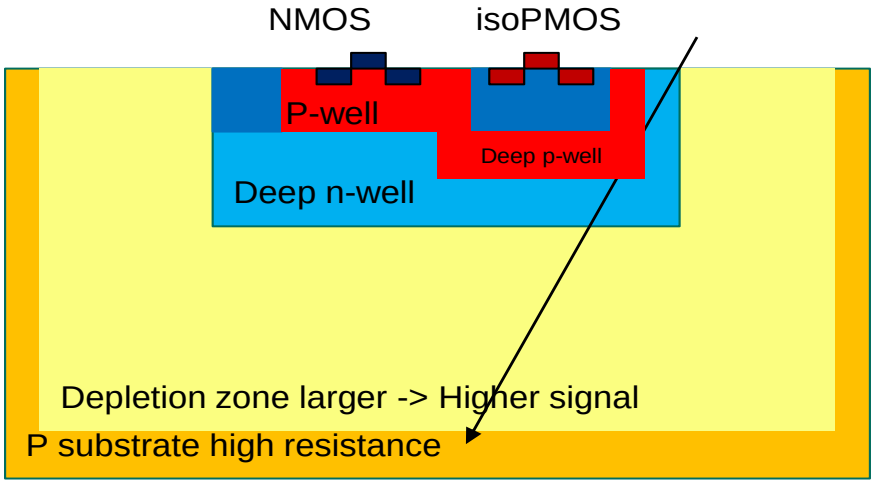


Figure 1.5: Modified HVCMOS senosor with a deep P-well implant

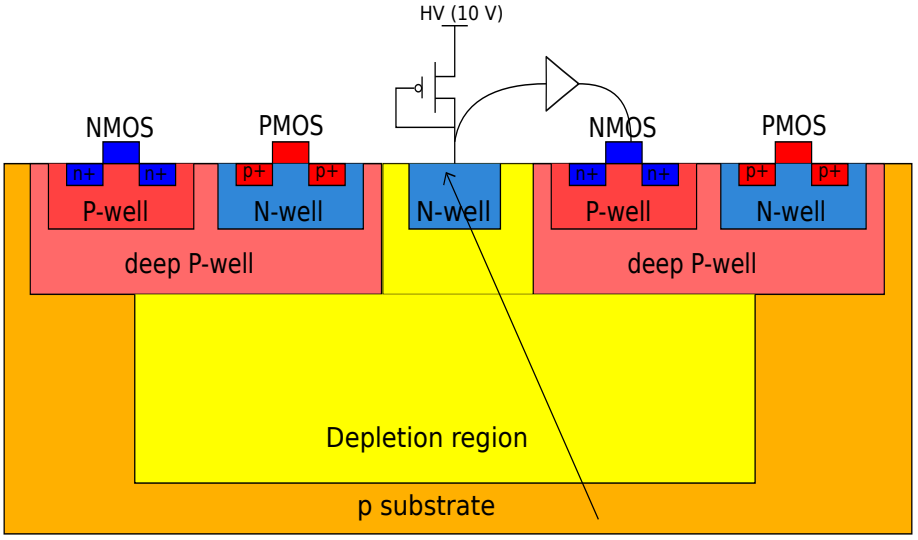


Figure 1.6: Modified HVCMOS senosor with small charge collection electrode

Modified HVCMOS Process with small charge collection electrode

Fig. 1.6 shows the modified HVCMOS sensor with small charge collection electrode (n-well). The electrode is biased to typically 10V. The sensor substrate is partially depleted. The pixel electronics is surrounded by a deep p-well that acts as potential barrier for electrons. In this way, the signal charge drifts towards charge collection electrode. The advantages of this design are: smaller input node capacitance and less crosstalk from electronics to sensor.

1.4 Silicon detector

The working principle of a silicon detector is charge generation in silicon. Electron-hole pairs are generated when energy is deposited by charged particles or photons in the silicon substrate. The movement of charge towards the electrodes generates a signal.

The ionization energy of silicon is 3.6 eV, this means that per 3.6 eV deposited energy one electron-hole pair is generated.

The mechanism of energy deposition depends on particle type. In the case of charged particles, the most important mechanism is interaction through electric field. In the case of photons, it is photo effect, Compton effect or pair production. High energy charged particles usually pass through the sensor and generate signal that is proportional to sensor thickness. The charge generated by a minimum ionizing particle is about 75 electron-hole pairs per μm path length in silicon.

Why do we need a large depletion region

Most silicon particle detectors are based on depleted PN junctions.

The electron hole pairs generated by particles within the depletion region are separated by electric field. This leads to a strong and fast signal.

A large depletion region is preferable from several reasons.

The depletion depth must be large enough in order to produce signals larger than noise level. These events are then detected with almost 100 % efficiency.

If a the response of semiconductor detector should be perfectly linear with energy, the depletion region should be sufficiently thick to completely stop all particles. Otherwise, a nonlinear response could be expected since the full energy is not totally deposited in the sensitive volume [17].

Furthermore, the depletion region behaves like a capacitor (ϵA=d), since charges are built up on either side of the PN junction. Thus, the value of the capacitance is inversely proportional to the depletion width [18].

How to achieve large depletion region

The approximate formulas for the width of the n side and p side of the depletion layer are [19]:

$$x_n = \sqrt{\frac{2\epsilon_{Si}}{qN_D(1+N_D/N_A)}(\phi_0 - V_0)} \tag{1.1}$$

$$x_p = \sqrt{\frac{2\epsilon_{Si}}{qN_A(1+N_A/N_D)}(\phi_0 - V_0)} \tag{1.2}$$

The total width of the depletion region is:

$$x_d = x_n + x_p = \sqrt{\frac{2\epsilon_{Si}}{q}(\frac{1}{N_A} + \frac{1}{N_D})(\phi_0 - V_0)} \tag{1.3}$$

If one side is more heavily doped than the other, the depletion zone will extend farther into the lighter doped side.

For example, $N_D \gg N_A$, then $x_p \gg x_n$. In other words, the depletion region is almost entirely on the p side of the junction. In our case, a shallow and highly doped n+ implant

(n-well) in a low doped bulk realizes silicon sensor. Therefore, the term $1/N_D$ in equation 1.3 can be neglected.

$$x_n \approx x_n = \sqrt{\frac{2\epsilon_{Si}}{qN_A}(\phi_0 - V_0)} \tag{1.4}$$

Thus equation 1.4 is widely used for calculating the depletion depth.

There are two methods to enlarge the width of the depletion region analysed from equation 1.4. A higher resisitivity material is necessary, which means using higher purity semiconductors or compensated material to improve the density of N_A or N_D.

Moreover, a reverse bias voltage will have the effect of attracting the electrons in the n-region away from the junction towards the n contact and similarly for the holes in the p-region.

The higher the external voltage, the wider the depletion zone.

However, a higher external voltage brings a greater risk of breakdown. The maximal voltage which can be applied is limited by the resistance of the semiconductor.

1.5 Detector Electronics

A general front end circuit of a particle detector chanel usually consists of a charge sensitive amplifier (CSA), a shaper, a comparator followed by digital processing cell.

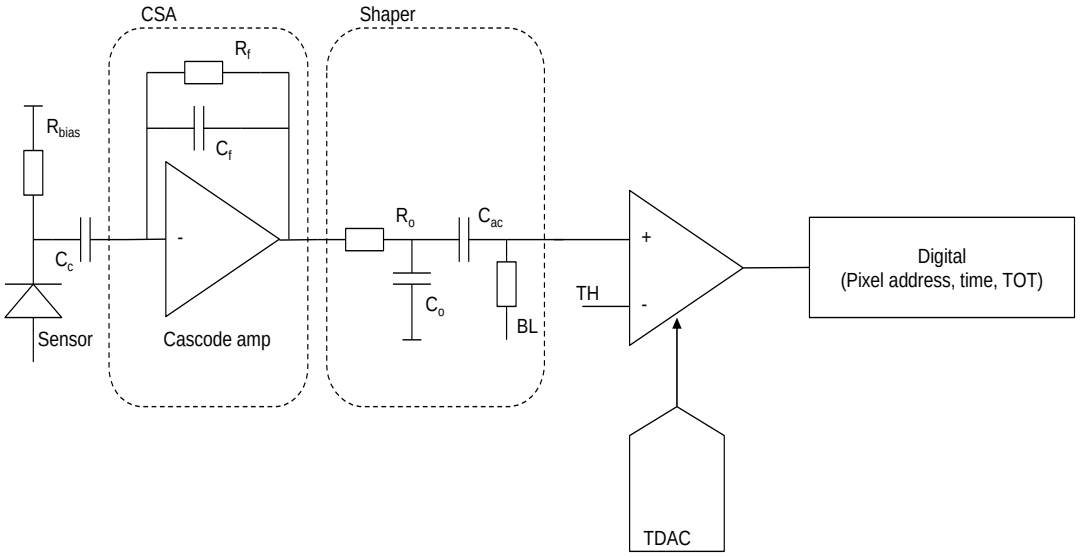


Figure 1.7: Detector electronics

The sensor is represented as a reversely biased PN junction - the diode symbol in the figure. The electrons generated by particle are collected by the cathode of the diode. The signal charge is integrated in the CSA. The voltage step pulse at the output of the amplifier is proportional to the amount of the charge collected in the sensor and inversely proportional to the feedback capacitance C_f, which is discharged by a continuous rest. Moreover, the continuous rest architecture is also suitable for the leakage current compensation, if necessary.

In the case of HVCMOS sensors, we usually connect the CSA and the sensor by AC-coupling (device C_c in figure). In this case we use the bias element R_{bias}.

A shaper follows the CSA, which is responsible for shaping the step voltage generated form CSA according to the timing requirements of the application. The shaper usually acts as a combination of low pass and high pass filter. Both filters reduce noise. Moreover, the pulse duration is usually shortened by high pass filter in order to reduce pile-up of subsequent events.

To digitize the signal, the output of a shaper is fed to a comparator. In this thesis different types of comparators were implemented, NMOS- and CMOS comparator.

Additionally, a local threshold tune could be applied by an on-pixel DAC, controlled by configuration bits, in order to compensate for the pixel-to-pixel threshold difference, generated from several reasons, for example, power supply voltage drops, transistor mismatch, etc.

Different methods could be used to readout the output of the pixel. It can be directly readout, or stored in a local memory for further processing.

In the case where the signal is processed using digital logic implemented in the chip, the logic can be placed in pixel or in the periphery.

In case of monolithic detector, the digital logic is located in the chip periphery for the purpose of reducing crosstalk from electronics to charge collection electrode. However, numerous lines are needed to connect each pixel to its readout cell. Time delay and parasitic capacitance between two metal layers should be taken into account.

In case of hybrid detector the readout logic are normally designed in pixel. Complex line connection is avoided, however each pixel amplifier should be connected to its bump bond pad implemented in top metal layer.

The information of the hit includes hit position, hit time and hit energy usually measured as time over threshold (ToT).

The spatial resolution of the detector depends on the pixel pitch and some other factors such as the charge sharing between neighboring pixels and the selected readout architecture. Binary readout is the simplest case, where the only information stored in the pixel is whether a hit was detected or not. The spatial resolution of a detector with binary readout is given by equation, where p is the pixel pitch [3].

$$\sigma_{position} = \frac{p}{\sqrt{12}} \tag{1.5}$$

To improve the spatial resolution and obtain more information about the timing and energy of the detected particle, ToT method is applied. The amount of time is proportional to the amount of charge generated in the sensor.

By knowing the information of the signal energy, the charge sharing can be studied. Analysing the amount of charge detected by each pixel at an event where the signal is induced to two or more neighbor pixels, can provide more information on the position of the hit, thus achieving sub-pixel spatial resolution.

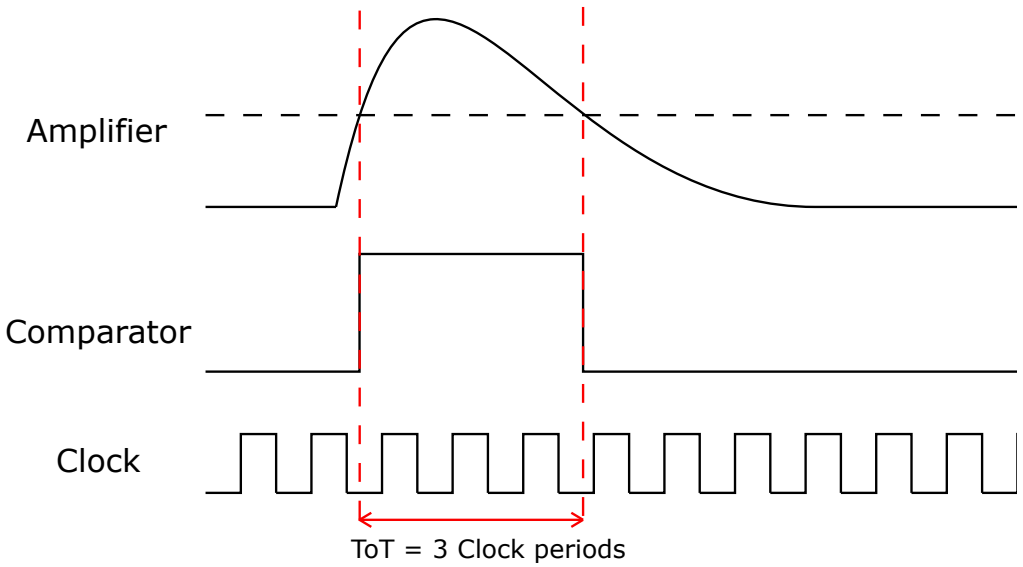


Figure 1.8: Time diagram that describes ToT measurement

1.6 Charge Sensitive Amplifier

Transistor level schematics of a typical charge sensitive amplifier CSA used in this work is shown in fig. 1.9. The CSA contains of following blocks: folded cascode amplifier, feedback block, bias block, source follower, high pass filter and output amplifier stage. The folded cascode amplifier is used as the active part of CSA.

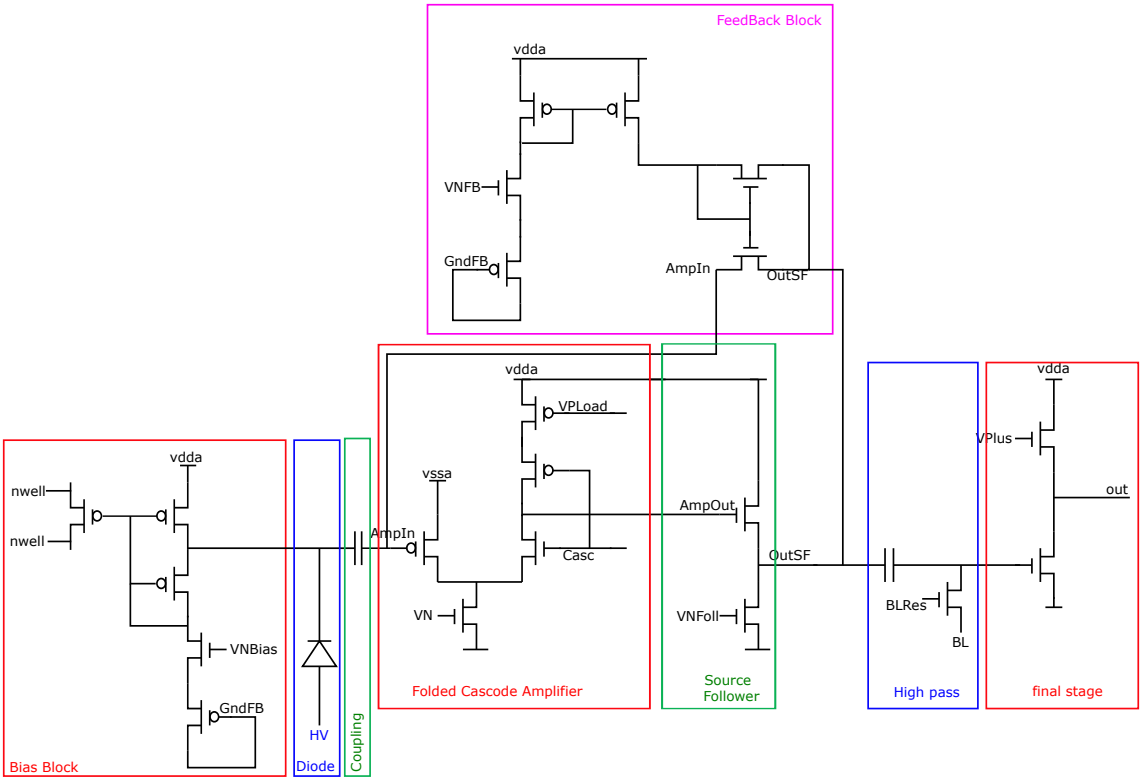


Figure 1.9: Transistor level schematic of the amplifier

1.6.1 Folded Cascode Amplifier

Figure 1.9 shows the transistor level schematic of the folded cacode amplifier, which is a common choice for low-voltage and high gain amplifier.

A source follower is used as the output stage. It provides fast time constant and shifts voltage level. A quiet analogue supply VSSA is used to alleviate the impact of supply voltage fluctuation on CSA.

Current mirror in bias DAC at chip periphery is applied to provide the bias voltages VN and VPLoad. It makes sense to keep IPLoad relatively small and INBias large because IPLoad flows through the load PMOS transistor and the NMOS cascode. INBias flows through the NMOS bias source. The difference INBias - IPload flows through the input transistor. For a large g_m, the bias current (DC current) through the input transistor must be large. For a large load resistance, the bias current through load transistor must be small. Therefore, to some extent, the smaller the current IPLoad, the better. A good choice is normally IPload = 10 % INBias.

1.6.2 Continuous reset and rising time optimization

The feedback capacitance C_f should be reset after each signal.

An NMOS transistor is chosen for the feedback device, because the input of the CSA has negative polarity and it generates a positive output pulse. The output and input potential

of the CSA are equal in the stationary state. When the output pulse gets higher than few thermal voltages Ut, the current of feedback transistor saturates. The feedback capacitor is thus discharged by constant current, the output pulse has approximately a triangular shape. This feature can be used for the digitization of the output signal amplitude by measuring ToT.

The response function of CSA with feedback is given by equation (1.6 - 1.8). Factor gm is the transconductance of the input transistor, C_i and C_o are the capacitances of the input and output respectively and C_f is the feedback capacitance. Normally T_f is 10 times bigger than T_r.

$$A_{FB} = \frac{A_{in}A_{oL}}{1 - \beta AoL} = \frac{-1}{(s\tau_f + 1)(s\tau_r + 1)} \tag{1.6}$$

$$\tau_f = R_f C_f \tag{1.7}$$

$$\tau_r = R_o \frac{C_i C_f + C_f C_o + C_i C_o}{AC_f} \tag{1.8}$$

A short rise time T_r is essential for high time resolution and count rate. In order to reduce rise time and avoid time walk, increasing g_m and C_f or decreasing C_o are helpful, as seen from equation 1.8. Unfortunately increasing g_m is not always feasible because the transconductance is proportional to the DC current that flows through the input transistor of the CSA in the stationary state, given by equation 1.9. A higher bias current leads to a higher power dissipation, which is a problem.

$$g_m = \frac{I_D}{V_{gs}} = \frac{I_D}{nU_T} \tag{1.9}$$

1.7 Time Walk

The output signal of the pixel amplifier is electronically compared with a threshold potential. The comparison is done by the circuit called comparator. A high time resolution required in most of particle detectors. For example, in the particle physics experiments at the LHC, hits must be associated to one particle bunch crossing with a precision better than 25 ns. Time resolution is to a large extent limited by the time walk, which is an effect caused by the fluctuation of the input charge signal. Figure 1.10 shows the time walk of two input signals and for two pixels with different thresholds. Vmin and Vmax are the minimum and maximum signal amplitude at the output of the amplifier. Vth1 and Vth2 are the random values of threshold. Tpk is the peak time. Tmin and Tmax are the minimum and maximum times of the signal crossing the threshold (Vth1). Hence, the difference between them is defined as time walk (TW), which can be estimated geometrically and expressed by the following equation [62].

$$TW = t_{max} - t_{min} = T_{pk}(\frac{V_{th}}{V_{min}} - \frac{V_{th}}{V_{max}}) \tag{1.10}$$

Intuitive analysis from equation 1.10 and figure 1.10 shows that either decreasing the signal rise time or decreasing the threshold value should be done for the purpose of ensuring the time walk smaller than 25 ns.

Shorter peak time is in favor of reducing time walk, which means fast rising time of the signal is required. Equation 1.8 shows that a larger value of C_f and smaller value of C_o are in favor of fast signal.

Additionally lower threshold value is also good for reducing time walk, which are demonstrated with red and blue color in figure 1.10. Shorter time walk corresponds to lower threshold. However, considering the influence of threshold dispersion, the minimal threshold value is limited.

Therefore, the threshold should be carefully adjusted that should not be too high to ensure low time walk and also not too low to avoid electronic noise.

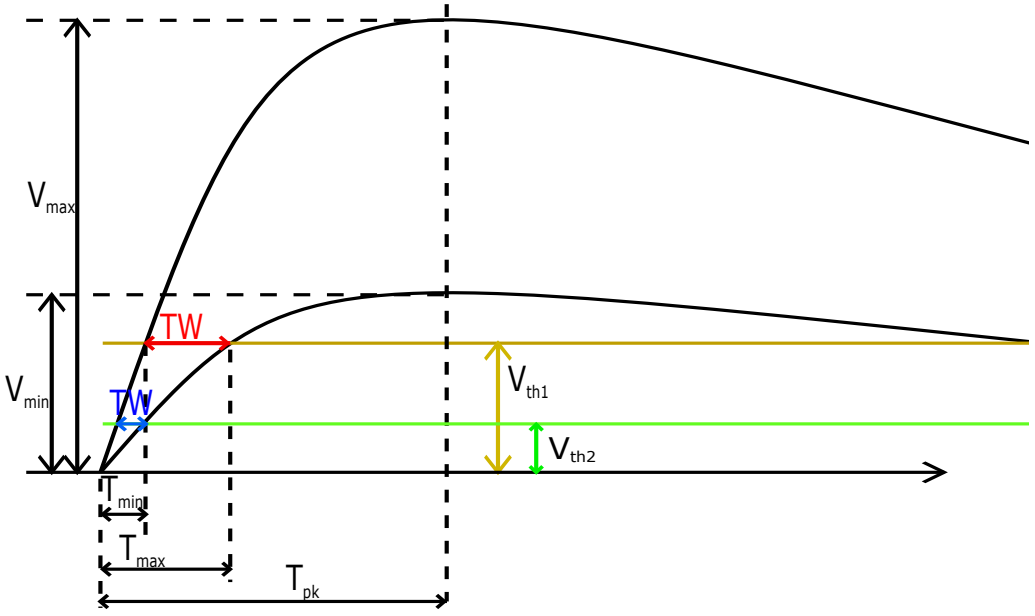


Figure 1.10: Time walk definition and time walk of two input signals for different threshold values

We can deal with time walk effect in several ways [12]:

Using the peak height, the actual time of hit can be calculated. The signal height can be measured directly or by taking the time over threshold (ToT) into account.

A thicker depletion zone increases signals, reducing the time walk effect.

1.7.1 Noise analysis in Charge Sensitive Amplifier

Figure 1.11 shows the equivalent circuit for the calculation of the nose at the output of the amplifier. The MOSFET thermal and flicker noise, the sensor shot noise and the Rf resistor thermal noise have largest contributions.

The total noise power is the sum of individual contributions.

$$< v_o^2 >= \int_0^\infty (S_{IR}(f)|H_{IR}(jw)|^2 + S_{VT}(f)|H_{VT}(jw)|^2 + S_{IS}H_{IS}(jw))df \tag{1.11}$$

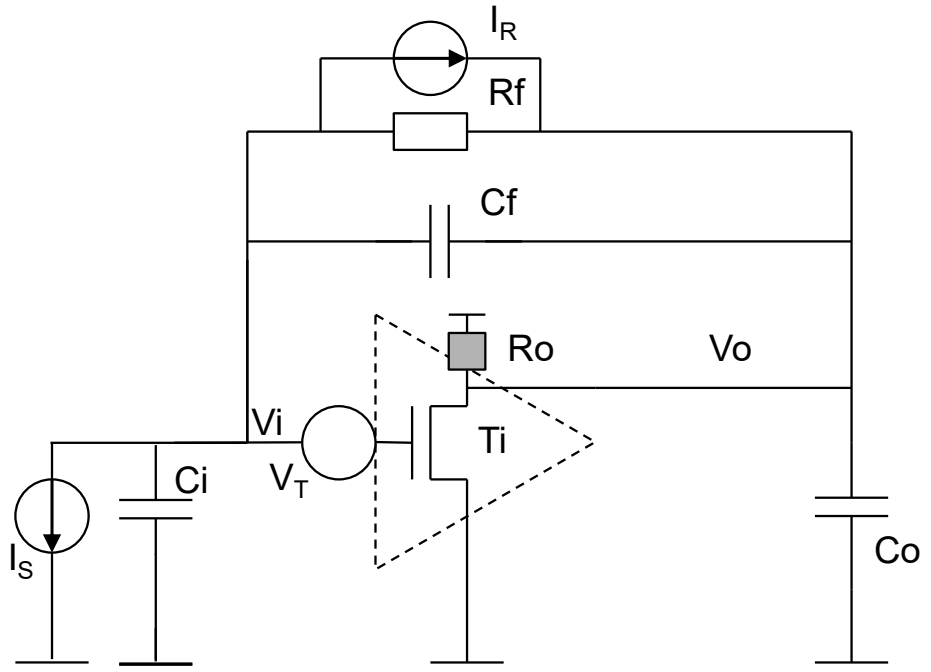


Figure 1.11: Noise sources in charge sensitive amplifier with feedback

Thermal noise of a resistor can be modeled by a parallel connection of current source and resistor. The spectral power density of feedback resistance R_f is:

$$S_{IR} = \frac{4kT}{R_f} \tag{1.12}$$

The transfer function from source I_R to amplifier output is:

$$H_{IR}(jw) = -Z_f = \frac{R_f}{1 + sR_fC_f} \tag{1.13}$$

The output noise (square mean value) caused by source I_R is:

$$\begin{aligned} < v_{oIR}^2 > &= \int_0^\infty \frac{4kT}{R_f} |\frac{R_f}{1 + sR_fC_f}|^2 df \\ &= \frac{4kTR_f}{2\pi} \int_0^\infty |\frac{1}{1 + s\omega R_fC_f}|^2 df \\ &= \frac{4kTR_f}{2\pi} \frac{\pi}{2} \frac{1}{R_fC_f} \\ &= \frac{kT}{C_f} \end{aligned} \tag{1.14}$$

MOS transistors exhibit thermal noise with the most significant source being the noise generated in the channel. The noise of the transistor can be modeled either with the current source between drain and source or with a voltage source at the gate.

Since for gate voltage Vg, a drain source current gm x Vg is generated, and since the power density is proportional to the square of the voltage, following applies:

$$S_{VT} = \frac{S_{IT}}{{g_m}^2} = \frac{4kT2/3}{g_m} \tag{1.15}$$

Transfer function from source V_T to amplifier output is:

$$H_{VT}(jw) = \frac{1 + jw\tau_z}{(1 + jw\tau_r)(1 + jw\tau_f)} \tag{1.16}$$

with the time constants:

$$T_r = \frac{C_iC_o + C_iC_f + C_oC_f}{C_f g_m} \tag{1.17}$$

$$T_f = R_f C_f \tag{1.18}$$

$$T_z = R_f(C_f + C_i) \tag{1.19}$$

$T_z > T_f > T_r$

Therefore, the equation 1.16 can be simplified as follows:

$$H_{VT}(jw) \approx \frac{\tau_z}{\tau_f(1 + sw\tau_r)} = \frac{C_f + C_i}{C_f}\frac{1}{1 + sw\tau_r} \tag{1.20}$$

The output noise (square mean value) caused by source V_T is:

$$\begin{aligned} < v_{oVT}^2 > &= \int_0^\infty \frac{4kT2/3}{g_m}(\frac{C_f + C_i}{C_f})^2 |\frac{1}{1 + s\omega T_r}|^2 df \\ &= \frac{kT2/3}{g_m}(\frac{C_f + C_i}{C_f})^2 \frac{1}{T_r} \end{aligned} \tag{1.21}$$

The spectral power density of leakage current is:

$$S_{IS} = 2eI_{leak} \tag{1.22}$$

The transfer function from source I_S to amplifier output is given by 1.13.

The output noise (square mean value) caused by source I_S is:

$$
\begin{aligned}
< v_{oIS}^2 > &= \int_0^\infty 2eI_{leak} |\frac{R_f}{1+sR_fC_f}|^2 df \\
&= \frac{2eI_{leak}R_f^2}{2\pi} \int_0^\infty |\frac{1}{1+s\omega R_fC_f}|^2 df \\
&= \frac{2eI_{leak}R_f^2}{2\pi} \frac{\pi}{2} \frac{1}{R_fC_f} \\
&= \frac{2eI_{leak}T_f}{4C_f^2}
\end{aligned}
\tag{1.23}
$$

The total output noise is:

$$
< v_o^2 > = < v_{oIR}^2 > + < v_{oVT}^2 > + < v_{oIS}^2 > \tag{1.24}
$$

2 MPROC

2.1 Background

The technology of hybrid pixel detectors have been developed at CERN for tracking detector systems in particle collider experiments in later 1980's [25]. With some modifications in the ASIC architecture the same technology can also be used in other imaging applications. For example, medical X-ray imaging, material analysis using X-ray diffraction, dosimetry, space dosimetry, synchrotron radiation application, etc [26]. The study of X-ray has been quickly established in the late nineteenth and early twentieth centuries and the potential for medical imaging has been soon realized.

Hybrid detectors are suitable for X-ray imaging since they can convert X-ray to an electric signal directly. A significant higher amount of charge are provided compared to indirect detection mechanisms.

2.1.1 Photon interaction with matter

There are three principal types of photon interactions, shown in figure 2.1.

- Photoelectric effect: primarily for energies E lower than 200 keV.

  Photoelectric effect is significant in diagnostic radiology. This involves the absorption of a photon by an atomic electron with the subsequent ejection of the electron from the atom [17]. The energy of the outgoing electron is then

  $$E = hv - B.E. \tag{2.1}$$

  where B.E. is the binding energy of the electron.

  This effect always happens on bound electrons with the nucleus absorbing the recoil momentum, because a free electron cannot absorb a photon and also conserve momentum [27].

- Compton scattering: primarily for energies 200 keV $<$ E $<$ 5 MeV.

  Compton scattering is dominant in radiotherapy. This effect is the scattering of a γ-quantum with frequency on a free or weakly bounded electron [28]. If the photon energy is high with respect to the binding energy, this latter energy can be ignored and the electrons can be considered as essentially free.

- Pair production: E > 1.022 MeV.

  Pair production does not play significant role in radiotherapy. This process involves the transformation of a photon into a electron-positron pair. In order to conserve momentum, this can only occur in the presence of a third body, usually a nucleus [17].

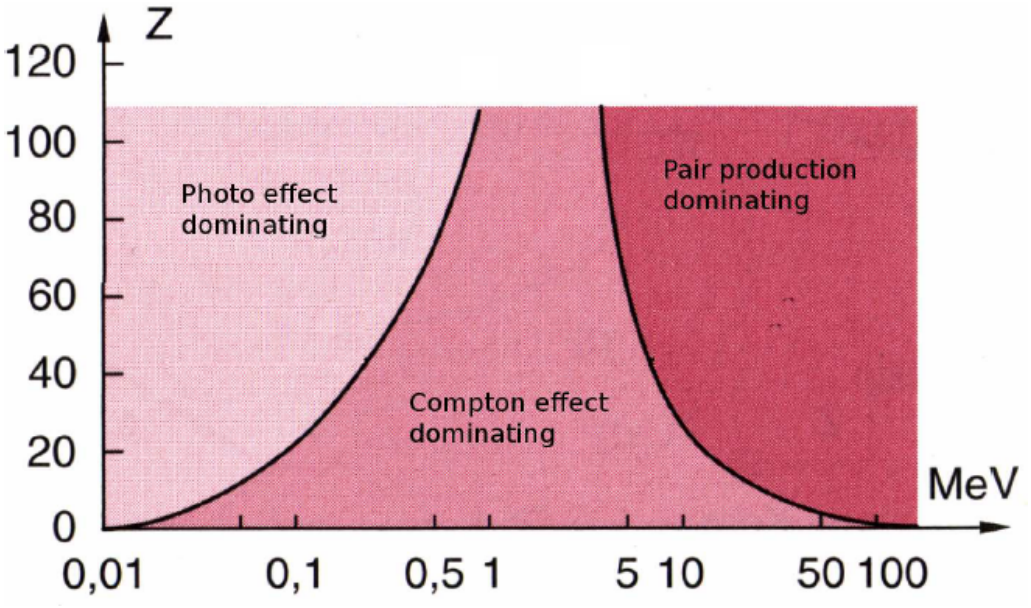


Figure 2.1: Three types of photon interactions depending on energy and atomic number [29]

2.1.2 X-rays interaction with matter

Among these three effects, only photoelectric effect and Compton effect are related to CT diagnose.

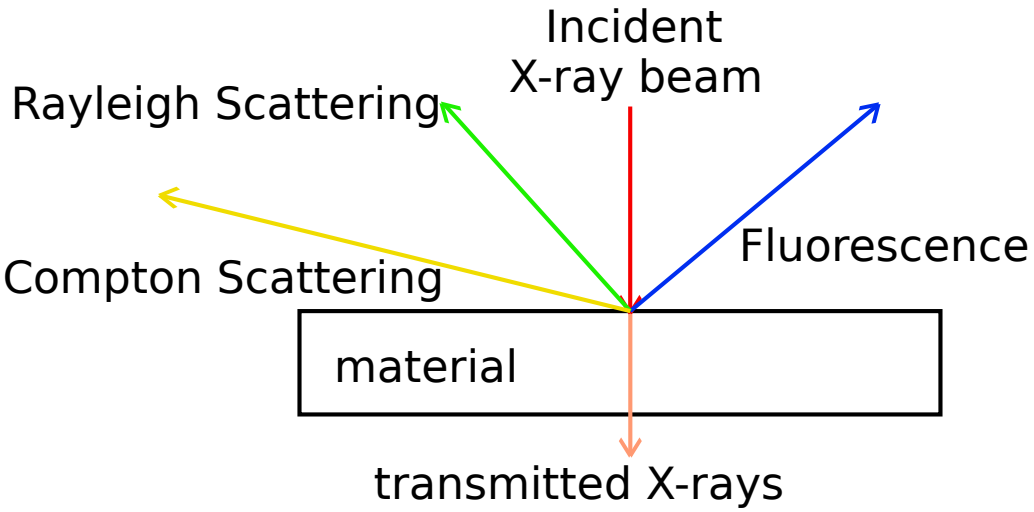


Figure 2.2: X-ray interaction with matter [30]

The interaction of X-rays with matter is more complex than simply ”passing through”. When X-rays interact with matter, some of the x-rays will be absorbed, some scattered and the rest of them will be transmitted through the material.

When absorption occurs, the X-rays interact with the material at the atomic level and can cause subsequent fluorescence. Moreover, the X-rays can also be scattered from the material. This scattering can occur both with and without loss of energy, called Compton and Rayleigh scattering respectively.

The ratio of absorption and Compton scatter depends on the sample thickness, density, composition and the X-ray energy [30].

2.1.2.1 Direct and Indirect X-ray conversion

An important characteristic of an X-ray imaging is the way that the radiation quantum is transformed into an electrical signal before it is processed by the readout electronics [26]. From this point of view, system is classified into indirect and direct method, presented in figure 2.3.

In the case of indirect method, the incident X-ray is converted into visible light through scintillation layers. The visible light is then detected in a pixelated sensor with photodiodes. Due to the two-step process, the spatial resolution and efficiency are degraded.

When the direct X-ray detection process is combined with a readout chip, signal photons can be counted at typical X-ray exposure conditions. Via a metal contact layer, the sensor is connected to a negative high voltage bias U_b, which causes depletion of the diode junction from charge carriers. A metal bond-pad allows the connection of the sensor to the readout system via bump-bonds.

The amount of created charge is proportional to the energy of the photons.

$$q = \frac{E_x}{E_i} \tag{2.2}$$

E_i is the ionization energy and E_x is the energy of the absorbed X-ray photon.

The incident X-ray photon is therefore converted to electron-hole pairs that drift quickly to the collection electrodes by a strong electric field and generate signal.

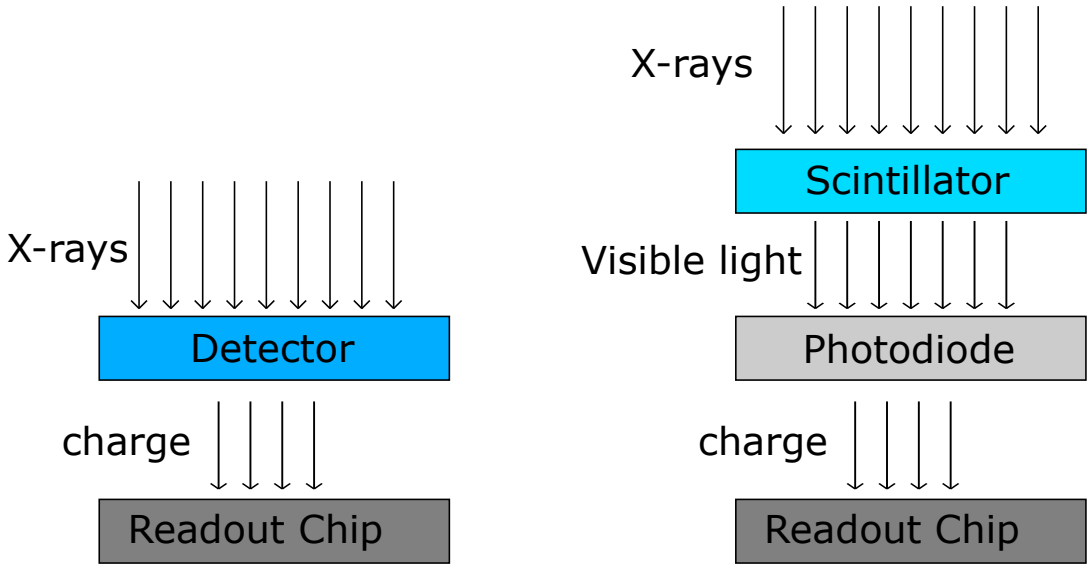


Figure 2.3: Comparison between direct (left) and indirect (right) detection of X-rays

For the X-ray energies used in medical applications, each impinging photon releases a charge from 4000 to 25000 electrons in a CdTe semiconductor detector. In an indirect

conversion system, the detected electrical signal is in the range from 100 to 1000 electrons depending on the scintillator characteristics [26].

Therefore, direct conversion method offers higher spatial resolution and efficiency.

2.1.3 Unwanted Effects

Specific to the field of particle interaction with pixel detector, scattering and fluorescence result in several undesired but unavoidable effects. Additional problems arise from charge sharing and pile-up [31]. These effects lead to spectral distortions and degrade both the spatial and spectral resolution.

Figure 2.4 illustrates the distortion of the energy measurement in a pixel detector.

- A: Ideally a photon deposits all its energy in a single pixel.
- B: Charge sharing effect between neighboring pixels caused by lateral diffusion and Coulomb repulsion. When a photon hits the sensor close to a pixel boundary, the total charge may spread to two or more neighboring pixels. A charge cloud has a broadening path to sensor electrodes during drift. This effect brings some undesired effects. For example, the signal amplitude is reduced in the corresponding pixel. This signal is not detected or counted when its amplitude in the corresponding pixel is lower than threshold. The spatial resolution is degraded. The broadening σ of the initial charge during the collection time can be obtained by using the Einstein relations of the diffusion coefficient D and the carrier mobility. Where k is the Boltzmann constant, T is the temperature and e the elementary charge. Therefore, the amount of charge sharing could be deceased by using a large pixel size, thinner sensor and higher bias voltages, as shown in equation 2.3.

$$\sigma = \sqrt{2Dt_c} = \sqrt{2\frac{kT}{e}\frac{d^2}{U_b}} \tag{2.3}$$

- C: Scattering in pixels. The incoming photon scatters and reaches a neighboring pixel before the energy is absorbed completely.
- D: Fluorescence escape. A certain amount of the absorbed energy is re-emitted by means of x-ray fluorescence. The overall spectral distortions introduced by charge sharing, scattering and fluorescence emission are quite similar. They could be corrected to some extent by inter-pixel connections on the ASIC.
- E: Pile-up effect, especially occurs in the case of high flux. When two photons arrive shortly after each other, pile-up effect occurs. The second signal is added to the tail of the first one, before it reached to the baseline. The detected signal amplitude ASIC is thus higher than without pile-up. Pile-up leads to a drop of count rate and incorrect energy measurement. The effect of pile-up could be diminished by signal filtering which is explained in appendix.

2.1.4 CdTe material and the application in X-ray imaging

One of the initial goals of medical imaging is to reach high detection efficiency with maintenance of a proper energy resolution. Semiconductor detectors applied for x-ray detecting of medical image should be thick enough to absorb the largest part of the radiation. Silicon is not the best material for high-energy photon detection, due to its low absorption coefficient [33].

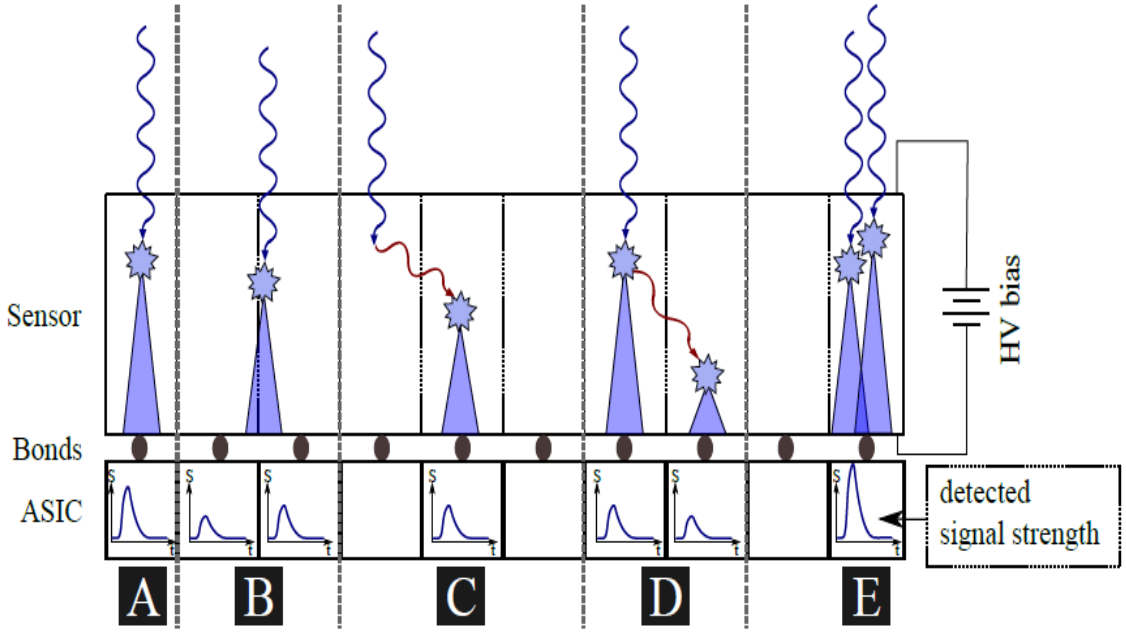


Figure 2.4: Illustration of spectral distortion effects in pixel detectors [31]

Novel high-Z semiconductor materials are being developed throughout the world, not the least driven by requirements in medical imaging applications. In the last decades, several high-Z semiconductor materials have been investigated at room temperature but only two candidates showed promising results. These materials are Cd(Zn)Te and GaAs. Both CdTe and CdZnTe show an excellent performance for X-rays from 40 keV up to 200keV energies. GaAs is suitable for the energy range from 10 keV up to 80 keV [32].

Some parameters of silicon and CdTe are presented in Table 2.2. Where E_{gap}, ϵ and X_0 represent the band gap energy, the ionization potential and the radiation length respectively. By comparison CdTe has many good properties:

- Higher bandgap (E = 1.44 eV): allows use at room temperature;
- Higher atomic number (Cd: 48 and Te: 52): gives a higher quantum efficiency suitable for a detector operating typically in the energy range 10-500 keV;
- Higher density ($5.85 g/cm^3$): gives a higher quantum efficiency suitable for a detector operating in the energy range 10-500 keV;
- Shorter radiation length, shorter scattering path of charge particles.

Since CdTe-based technologies do not allow implementation of electronic components, the sensor is connected to a silicon pixel readout chip.

Table 2.1: Properties of the Semiconductor [33]

Semiconductor	Density [g/cm^3]	Z	E_{gap} [eV]	ϵ [eV]	X_0 [cm]
Si	2.33	14	1.12	3.6	9.37
CdTe	5.85	48, 52	1.44	4.43	1.52

2.2 Project Introduction

The MPROC readout ASIC has been implemented in TSI 180 nm HVCMOS technology with seven metal layers. The chip can be applied in a PLASMED X project (Plasma and laser-based medical imaging diagnostic with X-rays). The aim of the project is to build a detector for golden nanoparticles. The x-rays would be generated by a plasma wakefield accelerator, they will excite atoms of gold and the secondary x-rays will be detected by a hybrid detector. A detector for the gold fluorescence signal with very good energy resolution is highly desired.

The transmitting electrode pitch of the MPROC readout ASIC is 55 μm x 55 μm, its pixel size is 18.3 μm x 165 μm. Three pixels are arranged as one group in layout and a special connection is used to connect transmitting electrode pitch to each pixel, fig. 2.7a. There are in total 8100 pixels and each has two thresholds.

Each pixel should measure precisely the time when the particle is detected and its amplitude. The MPROC can measure two signal polarities (electron and holes) and the crosstalk caused by charge sharing has been also taken into account.

Table 2.2 describes the main characteristics of MPROC chip.

Table 2.2: Main Characteristics of MPROC chip

Technology	TSI 180 nm HVCMOS
Pad Size	55 μm x 55 μm
Pixel Size	18.3 μm x 165 μm
Matrix Size	5 mm x 5 mm
Energy Resolution (simulated)	600 SNR ($\sim$120eV@69keV)
Time Resolution (simulated)	20 ps (27 bits)
Data Rate	1.6Gbit/s = 32 bits / 25ns ($\sim$1 hit / 50ns)
Two Polarities	Electrons and Holes

2.2.1 TSI Process

The MPROC chip has been implemented in Juli 2020 in TSI 180 nm HVCMOS technology. TSI is a foundry in USA. Since AMS and TSI processes were progenies of the same parent, Global Foundary (former IBM) CM7RF process, both of them are compatible with aH18 and H18 (cm7hv) process. The HVCMOS collaboration came up with post-silicon results proving a nearly 100 % correlation between the MOSFET I-V characteristics and the sensor diode characteristics between TSI and AMS processes [34].

The TSI 180 nm process offers seven routing layers, which became an added advantage during chip design.

The metal top has lower resistance defined by sheet resistance and it is used for power supply voltage.

Additionally, TSI offers high-resistive substrate for engineering runs at a lower cost.

2.2.2 Different Operation Modes

There are three operation modes for a readout ASIC: counting mode, hit mode and ToT mode. The description of these three modes is presented in figure 2.5. Only hit mode and ToT mode is implemented in MPROC readout chip.

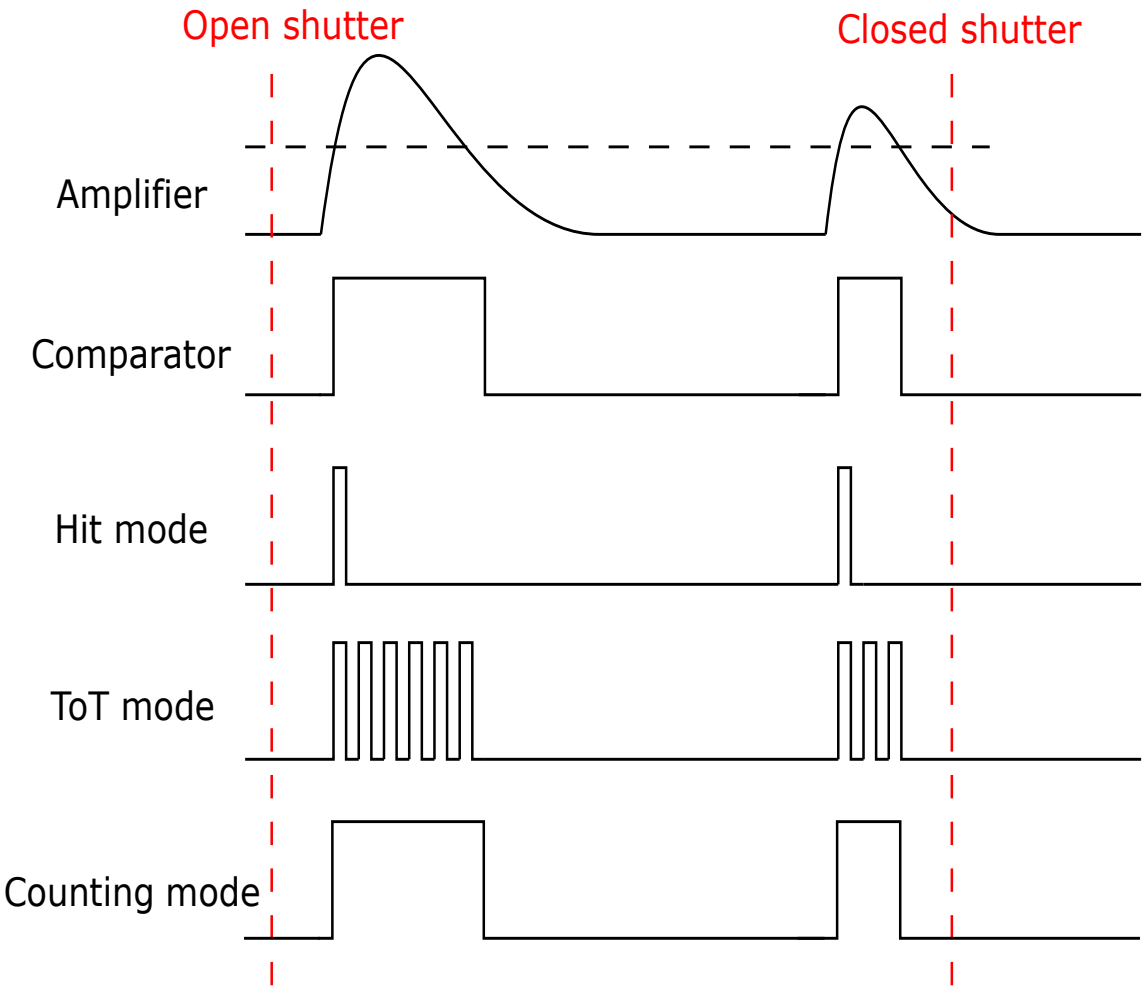


Figure 2.5: Three operation modes

- Counting mode: The ASIC counts the incoming particles, integrate data from multiple hits in a pixel and provide the images in the form of frames [35]. If the analogue signal is over the threshold, the comparator generates signal. The pulses are counted during the shutter window.
- Hit mode: A counter works as a timer and measures the exact time when the particle is detected. ASIC sends as much information about individual interactions as possible off-chip for further data processing.
- ToT mode: The counter is used as an ADC allowing direct energy measurement in each pixel. The length of comparator signal is proportional to the height of the amplifier output, which is proportional to the charge deposited in the pixel of a particle.

2.3 Design and Implementation

As shown in figure 2.6, the whole matrix is 5 mm x 5 mm large and consists of 8100 pixels in total. The size of a pixel is 18.3 μm x 165 μm. Each pixel contains one two-stage amplifier, two peak detectors, and two readout channels each with a comparator, a tune DAC and a hit buffer block. The pixels are connected to bump bond pads arranged as a matrix with 55 μm x 55 μm pad pitch.

One column contains 270 pixels, configuration register with 25 bits (18 bits for read/write and 4 bits for input of DAC-RAM, 1 bit injection enable, 1 bit analog buffer enable and 1 bit enable negative polarity) and EoC (end of column) logic. The whole matrix consists of 30 columns.

The chip periphery contains readout control unit (RCU), PLL, bias DACs, serializer as well as pads placed at the bottom of the chip.

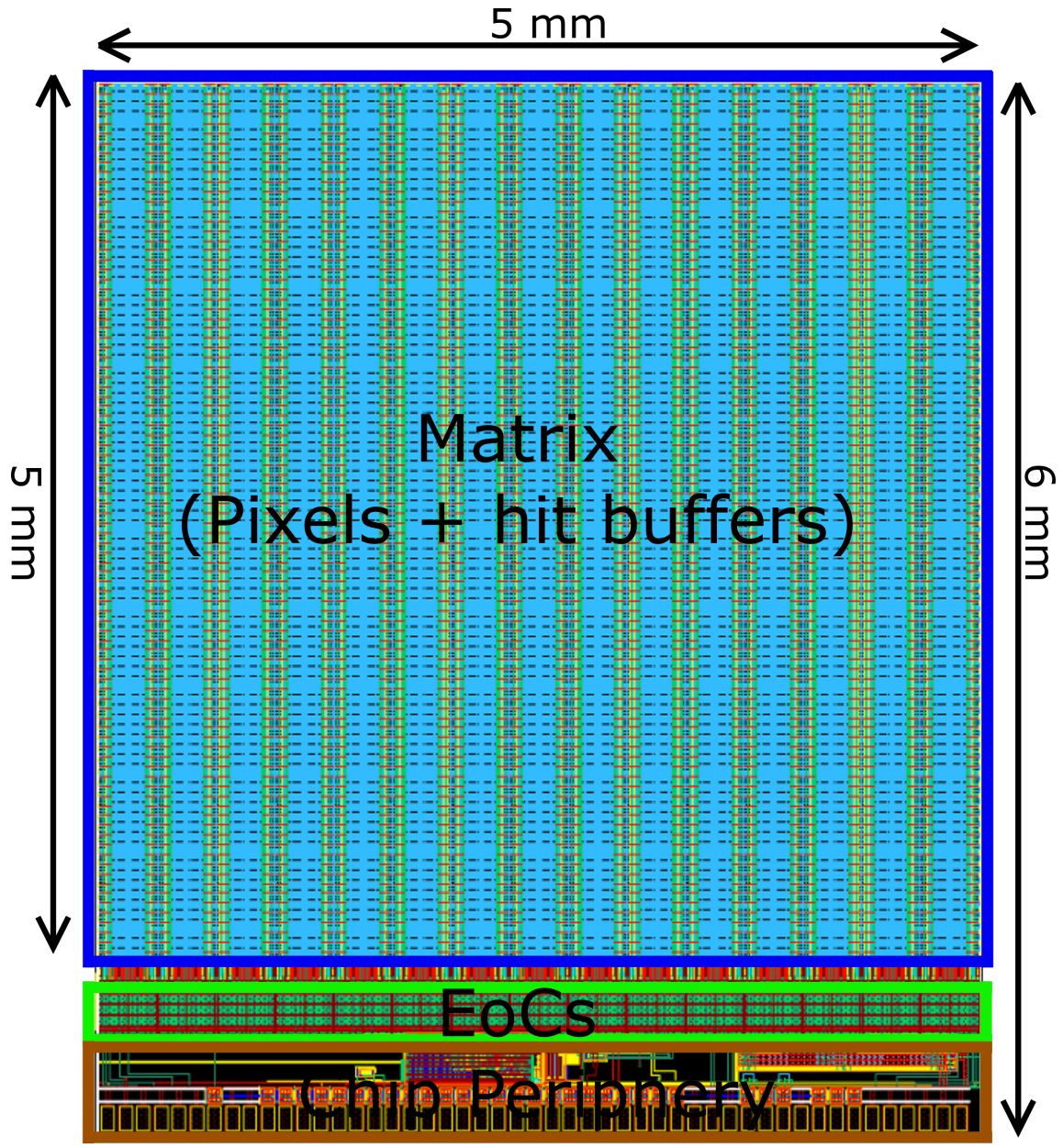
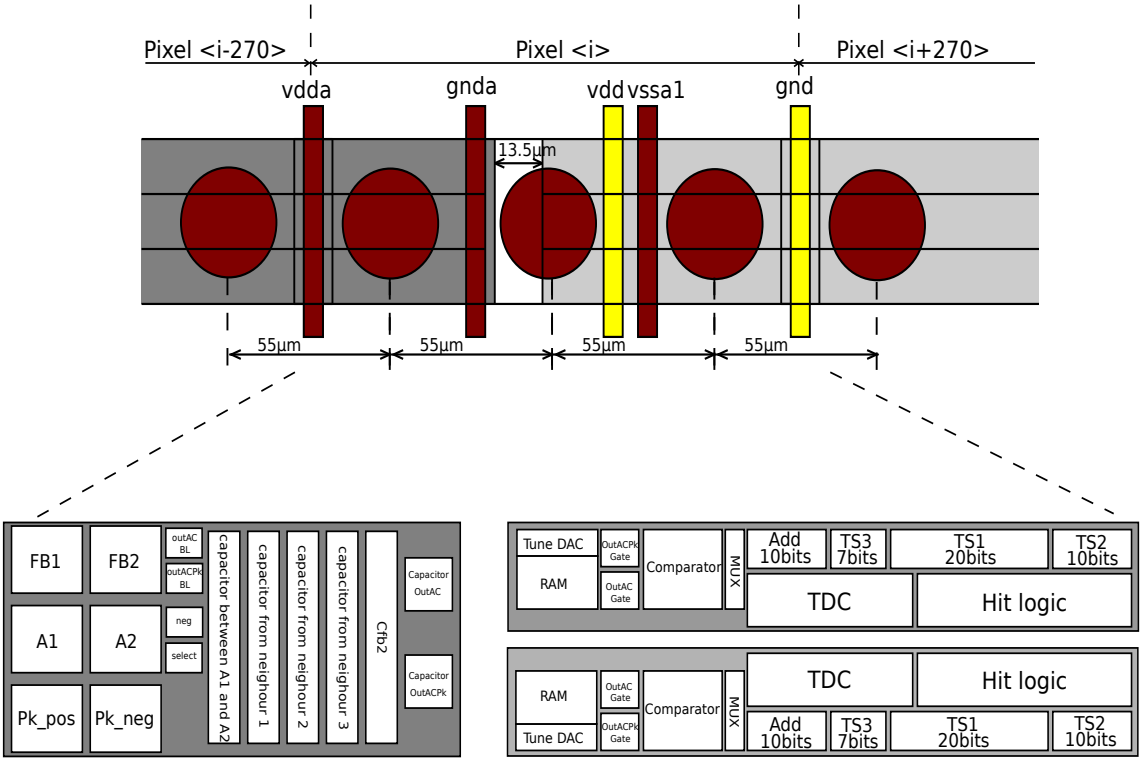


Figure 2.6: Chip layout of MPROC

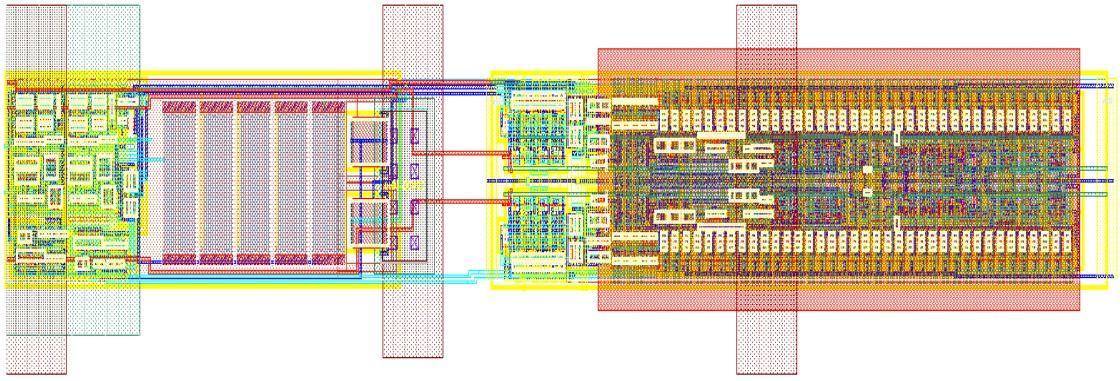
2.3.1 Pixel Electronics

Pixel structure

Figures 2.7a and 2.7b show the structure and layout of MPROC pixel.



(a) The structure of pixel electronics



(b) The layout of pixel electronics

Figure 2.7: The structure and layout of the pixel electronics

Three pixels are arranged in one group and the size of each group is 55 μm $\times$ 165 μm.

The left side (dark grey) is analog cell, that contains two amplifier stages A1 and A2, two types of feedback (FB) circuits, two peak detectors and RC filters.

Every pixel contains two identical readout cells (right side in figure 2.7a). Every readout cell contains comparator with 4-bit tune DAC and SRAM, hit logic and logic for fine time stamp (time to digital converter), DRAM memory cells for time stamps TS1, TS2 and TS3 and ten bit address ROM.

In order to decrease the pick-up of the digital activity that propagates through the bulk, the analog and digital blocks in a pixel are separated as much as possible and placed in different deep n-wells. For TSI process, the distance between two deep n-wells should larger than 13.5 μm.

Furthermore, the pixels are flipped horizontally and columns are flipped vertically. VDDA and GNDA of neighbouring columns are shared to make the chip more compact.

The distance between pads (dark red circle) is 55 μm. Three pixels are making one group. The pixels and pads are connected in the following way: the bottom pixel is connected to left pad, the middle pixel to middle pad and the top pixel to the right pad.

Pixel schematic

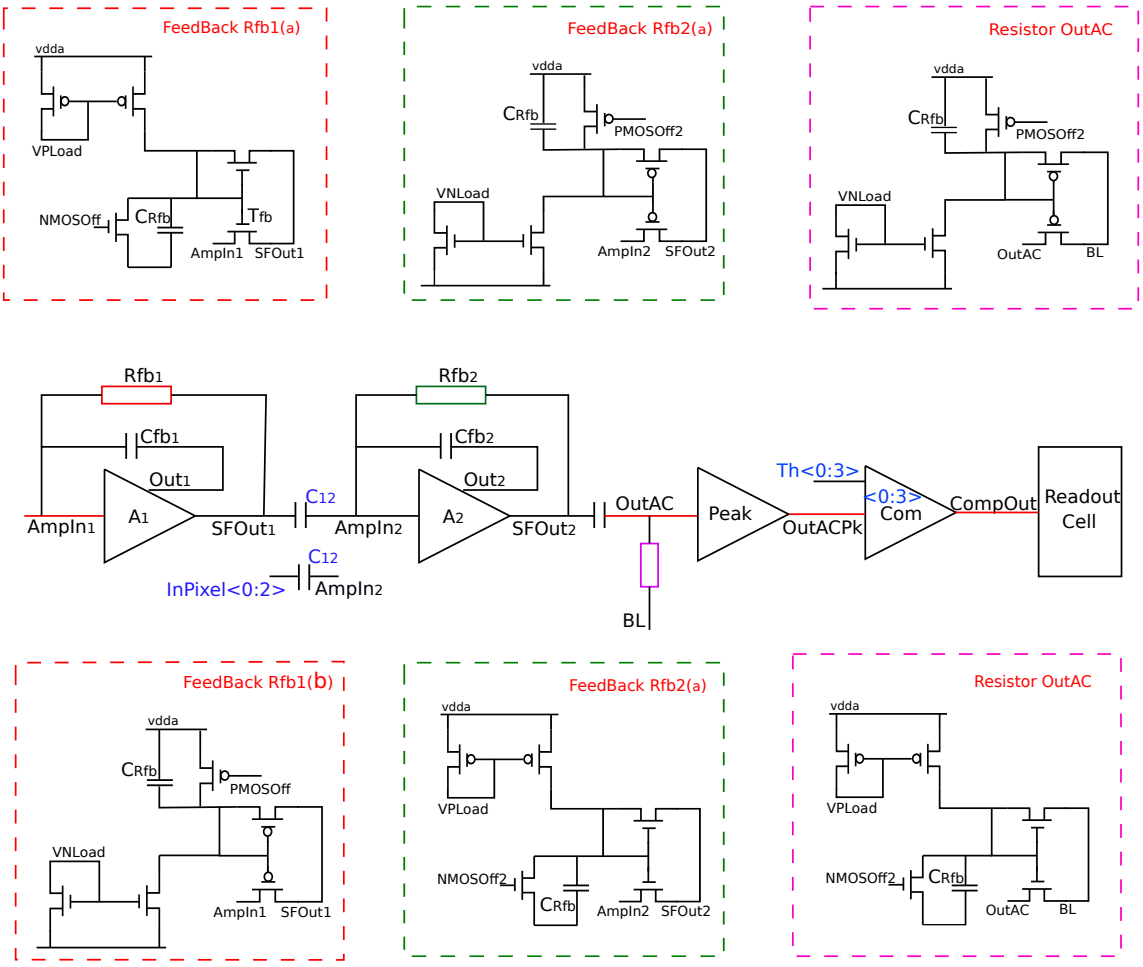


Figure 2.8: Schematic of pixel electronics

Figure 2.8 describes pixel electronics. Two stage amplifier is used in pixel. The first stage is a CSA connected to the bonding pad. The second stage is a capacitive voltage amplifier. It is used to sum the signals of four neighbouring pixels. For this purpose, four coupling capacitances are implemented. The values of C_{12} and C_{fb2} are 50 fF, which is 10 times larger than C_{fb1}.

A high pass filter follows the second CSA. It improves SNR and defines a stable baseline.

The noise can be explained by formula 1.21. A high pass filter reduces the time constant T_f, which reduces the detector leakage and the R_{fb1} noise contributions.

The peak detector is connected to the high pass filter in order to enlarge the falling time. The peak detector should improve SNR when amplitude is measured. As mentioned before,

we measure amplitude by measuring discharge time. If we measure discharge time of a feedback capacitance, the noise of feedback resistance would cause relatively large time jitter. The peak detector avoids this problem.

These output signal of peak detector is connected to comparator. Comparator output is connected to readout cell for further processing.

2.3.2 Feedback Circuit

Two types of feedback circuits, RC filters and peak detectors are implemented, for two signal polarities.

The feedback blocks (FeedBack Rfb in fig. 2.8) should discharge the feedback capacitance C_{fb} after signal amplification. In the absence of signal the potentials of SFOut and AmpIn nodes are equal and the transistor connected between SFOut and AmpIn (feedback transistor) is in linear region with equal drain and source potentials.

It is advantageous that the feedback transistor works in saturation after signal amplification. In this case C_{fb} is discharged with constant current and the dependence pulse width versus signal charge is liner.

We assume that the electrode of the feedback transistor connected to SFOut is its drain and the electrode connected to AmpIn is source. We assume also that the gate voltage of the feedback transistor is constant. This should be assured with capacitor C_{Rfb}.

If we use NMOS in feedback (Feedback Rfb1(a)) and if the signal at the amplifier output (SFOut1) is positive, then the drain-source voltage of the transistor increases and the NMOS works in saturation. This is why NMOS feedback device is a good choice in the first amplifier when the signal output SFOut1 is positive or the input charge is negative.

From the same reasons, in the case of negative signal at first amplifier output (positive input charge) it is better to use PMOS feedback (Feedback Rfb1(b)).

Since the second amplifier has opposite signal polarity at its output, the feedback transistor for the second amplifier should be of opposite type compared with the feedback of the first amplifier.

During measurements we have discovered a design mistake. C_{Rfb} is not large enough. From this reason, the gate voltage of NMOS in the first amplifier follows the drain voltage and NMOS current increases when we have a positive signal at the amplifier output. This will be shown in measurements presented later.

2.3.2.1 Influence from neighbor pixels

A charge deposited on a single pixel can induce parasitic signals on neighbor pixels due to the coupling capacitance C_c. Figure 2.9 shows a simplified cross section of an infinite sensor with capacitances C_{dep} and capacitances C_c. Every pixel is connected to a CSA with a feedback capacitor C_f [39].

It can also happen that one particle hits not only one pixel, but also 2 or 4 at the same time. The deposited charge in a single pixel is in this case smaller than the total charge particle generated and the energy measurement is not accurate.

To cope with charge sharing between neighbouring pixels we have implemented the connection arrangement between pixels and pads shown in figure 2.10.

The pad size is 55 μm x 55 μm and the readout pixel size is 18.3 μm x 165 μm. The connection scheme between pads and readout pixels is illustrated by black arrows.

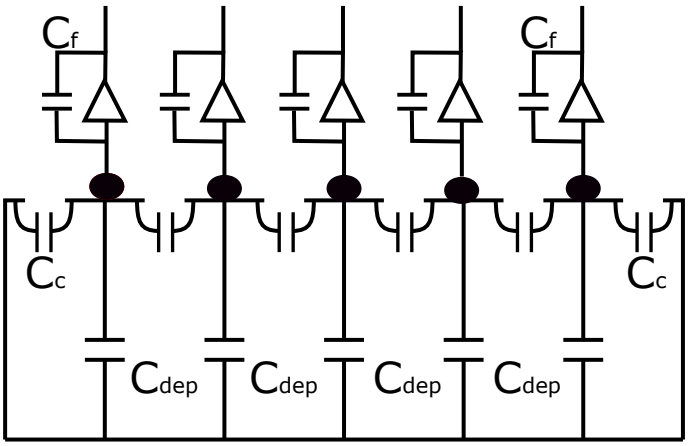


Figure 2.9: Model used for the estimation of cross talk to neighbor pixels

As mentioned before, there are two amplifiers in each pixel. The first is used to amplify the signal from sensor. The second amplifier is used to add the signals from top, from right and from top right sensor pixels.

Every 4 pads are seen as one group. The pad shown as pink circle in figure 2.10 is connected to the AmpIn1 of the pink readout pixel. The three yellow pads are connected to their amplifiers and the corresponding SFOut1 signals to InPixel<0:2> of the pink readout pixel. In this way the second amplifier in the pink readout pixel measures the sum of the signal in 4 sensor pixels.

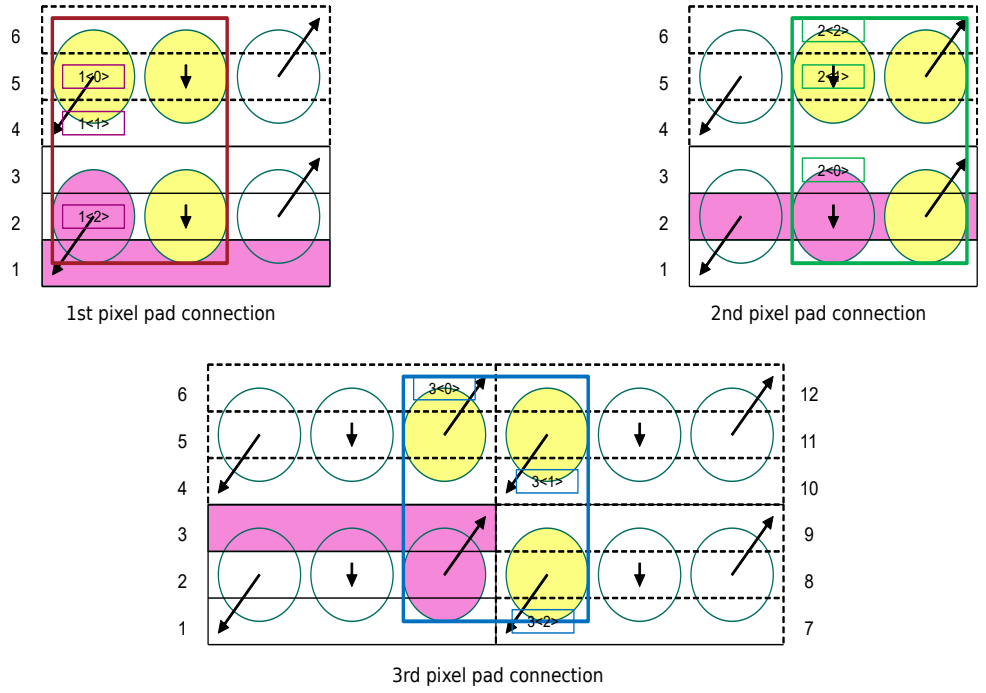


Figure 2.10: The influence from neighbor pixels

2.3.2.2 Peak Detector

There are several ways to measure energy of particle using a silicon detector that is readout by a CSA.

- Oscilloscope: Use oscilloscope is the simplest and intuitive way to observe and analyse

the waveform generated by CSA. However, if we have numerous channels, this method is not adoptable.

- ToT (Time over threshold): Through measurement of the width of comparator output signal, the input charge signal amplitude can be calculated. By knowing the input charge, particle energy can be calculated. However, this method is not exact. Usually the discharge time of the feedback capacitor determines the comparator pulse width. Because the feedback capacitor is very small, the noise of the current source that discharges capacitor causes large noise in time over threshold.
- Peak detector: Another way to measure the input signal amplitude is by using a peak detector. A peak detector is connected to CSA. The simplest peak detector consists of a diode and a capacitor. It extends the signal peak. This gives possibility to use ADC and digitize amplitude of CSA output signal. By knowing the CSA gain, input signal can be calculated. The output signal of peak detector is slowly reset to base line. This gives another possibility to measure ToT of the peak detector signal. This ToT is less noisy than the ToT of the CSA signal because the capacitor used in the peak detector is much larger than the feedback capacitor. Peak detector usually does not work well in the case of small signals.

Each method has its own advantages and disadvantages. Through comparing the simulation results of above methods and taken into account of the specification of SNR, peak detector is chosen for pixel electronics.

The peak detectors suitable for negative (a) and positive (b) signals are displayed in figure 2.11. Unlike the normal differential amplifier, the bias current for the second stage is much smaller than the bias current of the first amplifier stage.

The CSA output is connected to non inverting input INP, while the output of the peak detector is connected to its inverting input that makes feedback.

The peak detector is an unity gain amplifier. If follows the input signal. Let us consider the peak detector for positive signals. When CSA output increases, the peak detector output follows the CSA output quickly. When CSA output is falling down from maximum value, the output of the first stage of peak detector increases quickly, while peak detector output decreases slowly, because the large output capacitor is discharged by small second stage bias current. Hence, the peak detector can not only detect the peak but also delay the signal. The value of the current and the capacitance determine the speed the output voltage decrease from peaking value. The smaller the current or the bigger the capacitor, slower the signal decreases from its maximal value.

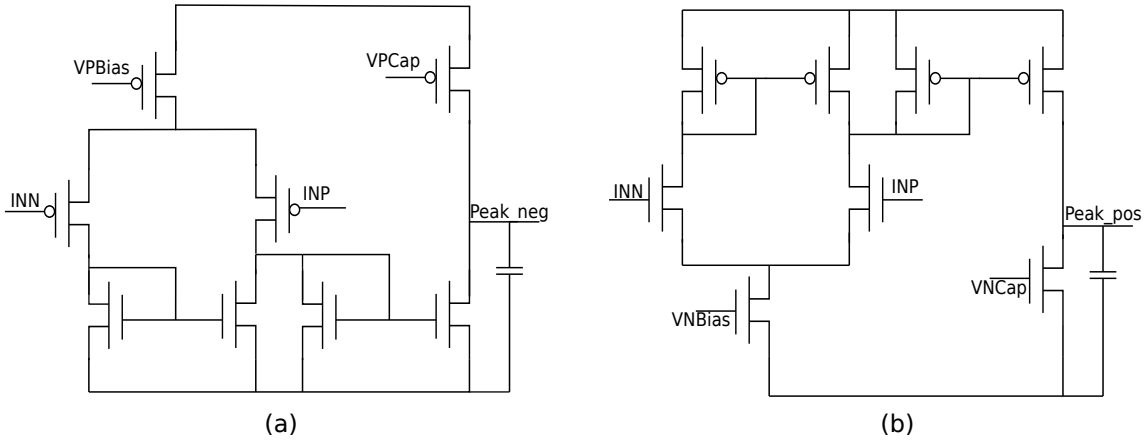


Figure 2.11: The peak detector for negative (a) and positive (b) polarities

2.3.2.3 Simulation results of pixel electronics

A full transient simulation has been performed starting from the sensor to the digital hit signal. The purpose of simulation in this section is to verify the functionality of amplifier, peak detector, high pass filter and comparator.

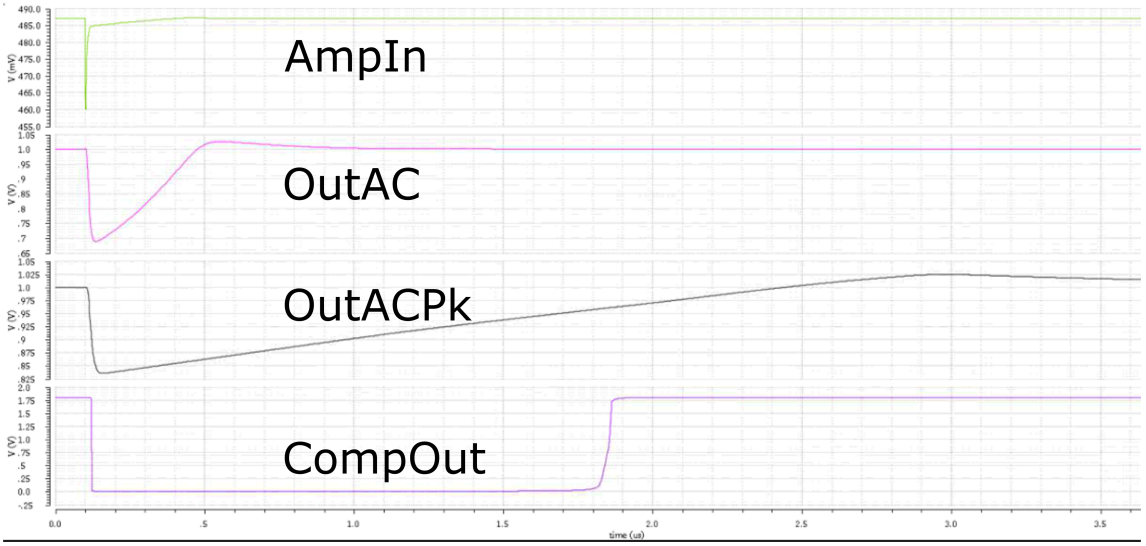


Figure 2.12: Test of the functionality of amplifier, peak detector and comparator

Figure 2.12 shows the simulation results of some important signals.

A negative charge signal is applied to charge sensitive amplifier. Detector capacitance C_{dep} is 100 fF, input current signal is 3 μA and the pulse duration is 1 ns. The voltage change of input node AmpIn observed from simulation is around 25 mV. OutAC, the input of the peak detector, has the same polarity as AmpIn after two amplifier stages. The falling time is approximately 380 ns and it depends on the value of capacitance C_{ac} and MOS transistor based resistor. The baseline is determined by the bias voltage, which is generated at chip periphery. OutACPk, the output of peak detector has much larger falling time (2850 ns) compared to OutAC. The falling time depends on the current value and load capacitance. When OutACPk exceeds threshold, the CompOut signal is generated and transmitted to hit buffer.

Table 2.3: Simulation setup for pixel electronics

I_{signal}	duration	C_{dep}	C_{fb}	I_{pk}	C_{pk}
3 μA	1 ns	100 fF	50 fF	20 nA	200 fF

Furthermore, the linearity in a certain signal range and the smallest detectable signal are also necessary to determine.

A better linearity, less noise as well as shorter measurement time are desired.

The duration of the comparator output = 1 (time over threshold), is proportional to the signal amplitude. Different signals presented in figure 2.13 are caused by different input current pulses (Isignal from 0.5 μA to 5.5 μA) . The comparator output approaches to saturation when Isignal is bigger than 3 μA.

1 ns wide signal with 3 μA amplitude produces about 18000 e or 3 fC (1 fC = 6250 e, or 1e = 1.6 x 10^{19} C).

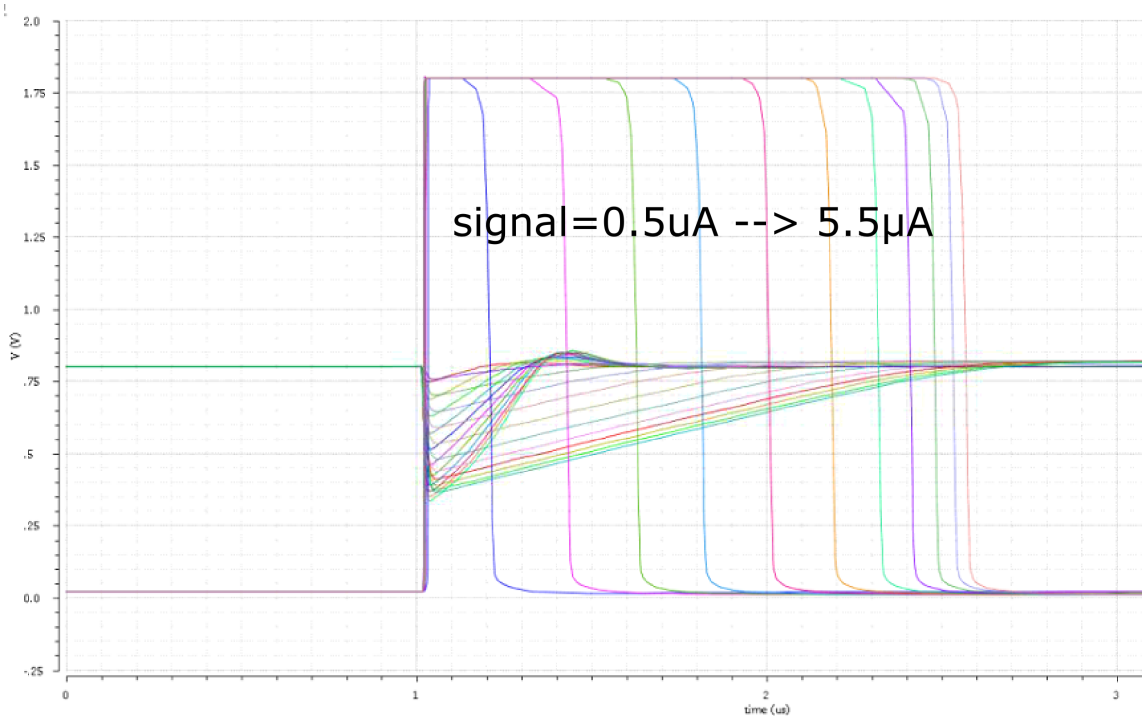


Figure 2.13: ToT response to different inputs

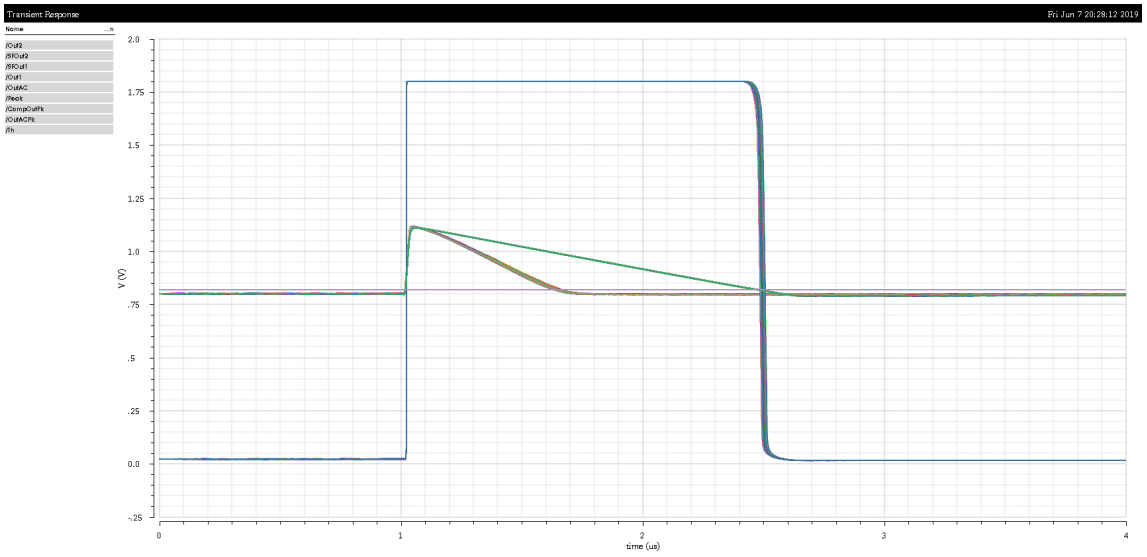


Figure 2.14: Transient noise analysis

Noise analysis in Cadence

There are two methods to simulate noise in Cadence. The first is transient noise simulation. This method is good for simulation of time jitter in ToT. The second one is AC noise analysis, which is good for small signal and baseline noise analysis. This method uses the equations for power spectral density and small signal transfer functions.

Figure 2.14 presents the transient noise analysis of ToT. Since the comparator output duration is proportional to input signal amplitude, through simulating the time jitter of CompOut we can determine the energy resolution of a pixel.

For the purpose of improving SNR, one should first know the source of the noise and should also know how to reduce it. The main noise source is the input PMOS transistor (22.3%)

followed by the NMOS bias current source (16.2%). The other transistors contribute significantly smaller.

In order to achieve high SNR, the noise reduction of the input transistor is important.

2.3.3 Readout Cells

Every pixel has two readout cells, they are horizonatlly flipped in layout. Layout is dense and complicated.

The purpose of readout cell is to measure time and amplitude, generate signal address and hit bus signal, temporary store hit information. There are totally 52 bits of information per hit. 20 bits time stamp 1 (TS1) and 7 bits TS3 for time measurement, 10 bits TS2 for energy measurement, 10 bits row address and 5 bits column address.

The readout cell contains following blocks, presented in figure 2.15: CMOS comparator with 4-bit tune DACs and RAM, fine time stamp circuit (time to digital converter), row address generator (address ROM), time stamp memory and hit buffer logic.

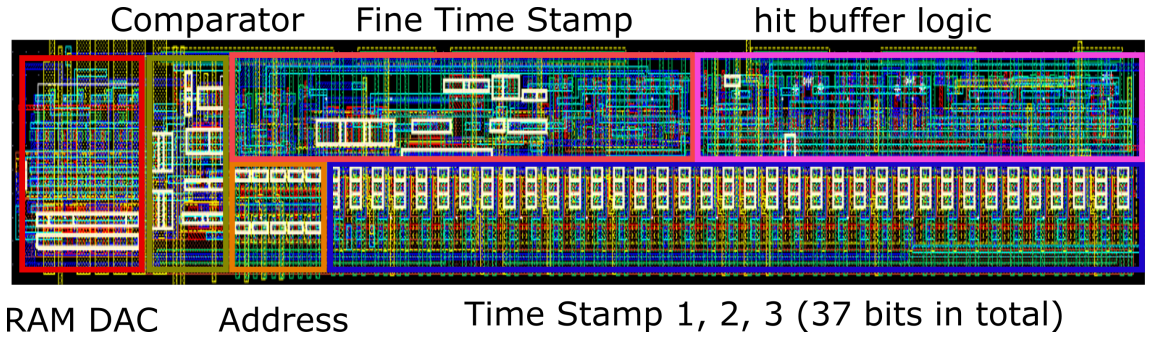


Figure 2.15: Layout of readout cell

2.3.3.1 Hit Buffer

Figure 2.16 presents the CMOS logic inside the hit buffer. It consists of edge detector, SR flip flop, D latch and some more digital logic cells.

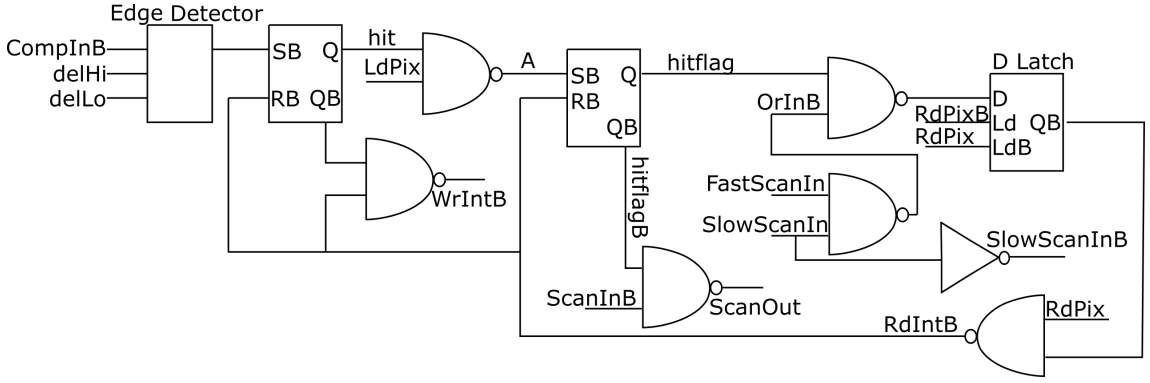


Figure 2.16: The CMOS logic in hit buffer

As soon as the signal OutACpk exceeds the threshold, the comparator reacts. The edge detector produces a signal with a defined duration (delHi, delLo) that is controlled externally. The output of edge detector is connected to the set input of the SR flip-flop.

Signal hitflag is produced when hit is one and after LdPix is generated from periphery.

The hitflag is connected to the priority logic that selects the first hit buffer in the colum for readout. The output of priority logic is connected to D latch.

ROM in hit buffer is used to generate the pixel address, it uses only single PMOS transistors with source connected to VDD or GND, depending whether address bit is one or zero.

DRAM cells, consisting of three PMOS transistors, figure 2.17, are attached to time stamps to measure the time of the rising edge of hit signal (20 bits TS1) and the time over threshold (10 bits TS2). Fine time stamp consist of logic circuit with comparator that will be explained later and 7 bit RAM cells to store the fine time stamp, which is used to measure the exact moment when hit exceeds the threshold.

Externally generated signal RdPix activates reading of hit information via bus.

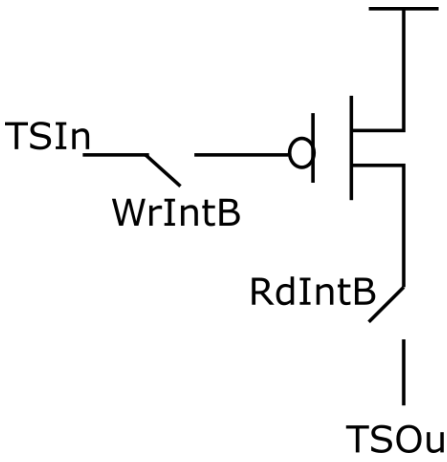


Figure 2.17: DRAM for storing of time stamp

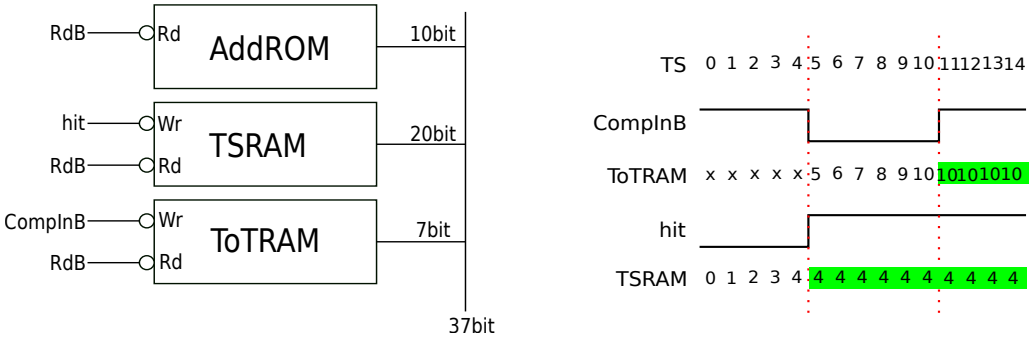


Figure 2.18: DRAM loigc

Figures 2.17 and 2.18 present the schematic of DRAM cell.

The read and write function of RAM/ROM cell is controlled by signals WrIntB and RdIntB.

Figure 2.18 shows working principle of RAM for storing time stamp and ToT. The time interval for TS is 25 ns, the width of one hit signal is from TS 5 to TS 10. WrIntB input of TSRAM is connected to signal signal hit. When hit goes to high, the TSRAM stores the exact time stamp of the hit signal. WrIntB of ToT RAM is connected to signal CompInB. ToTRAM stores the time stamp that corresponds to falling edge of comparator signal. ToT is calculated as difference between values stored in ToTRAM and TSRAM.

Work principle of priority logic and read logic

The priority logic generates ScanOut and Enable signals. Simplified schematics is shown in figure 2.19.

ScanOut is OR function of ScanIn and the hit flag. All the pixels are serially connected together, Scanout<i> = ScanIn<i+1>.

Enable is AND function of the negated ScanIn and the hit flag. It is used to select the highest set hit flag in a column.

As mentioned before, the reading of hit information is activated by signal RdPix (generated by EoC).

If many hits occurs in one column, only the pixel with highest place in hierarchy responds to the read signal. The pixel then opens the RAM/ROM gates and transfers the data to the bus lines. RdPix also deletes the hit information. When the new read signal is issued, the next pixel in the hierarchy transmits its data.

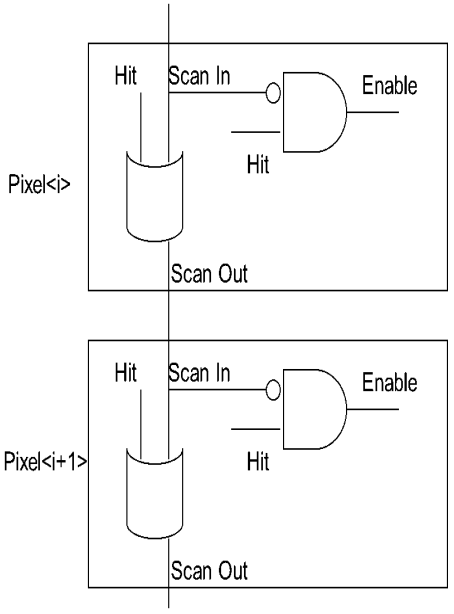


Figure 2.19: Enable logic and ScanOut logic of priority in readout cell

Fast and slow OR signals are used to speed up the logic. The combination logic implemented in chip is shown in figure 2.20.

As mentioned before, there are in total 540 hit buffers in each column (270 pixels and each has two hit buffers).

The hit buffers are grouped in groups of 30. The signals "Fast" in each group are connected together. The Fast signal in one group is connected to ScanOut from previous group, except in the first group, where it is connected to ground.

For example, Fast[29 : 0] is connected to ground, Fast[59 : 30] = ScanOut<29>, Fast[89 : 60] = ScanOut<59>.

All of the Slow signals, except the first one in each group, are connected to previous ScanOut, namely Slow<i+1> = ScanOut<i>. The first Slow signal in each group is connected to ground.

The last ScanInB signal in each group is connected to OrB (green color), the remaining ScanInB signals are connected to SlowB.

Assume that a hit occurs in a pixel with purple spiral in figure, Q = 1 and QB = 0. Its ScanOut and the next Slow signal are 1. All the ScanOut signals in the following cells inside this group are all high.

The Fast signal of the next and all following groups are one. The propagation of the Fast signal is faster than of Slow signals because there are less number of gates in the chain.

Enable is AND function of signal OrB and the hit flag. It is used to select the highest set hit flag in a column. Enable will be generated only if both Fast and Slow signals are zero.

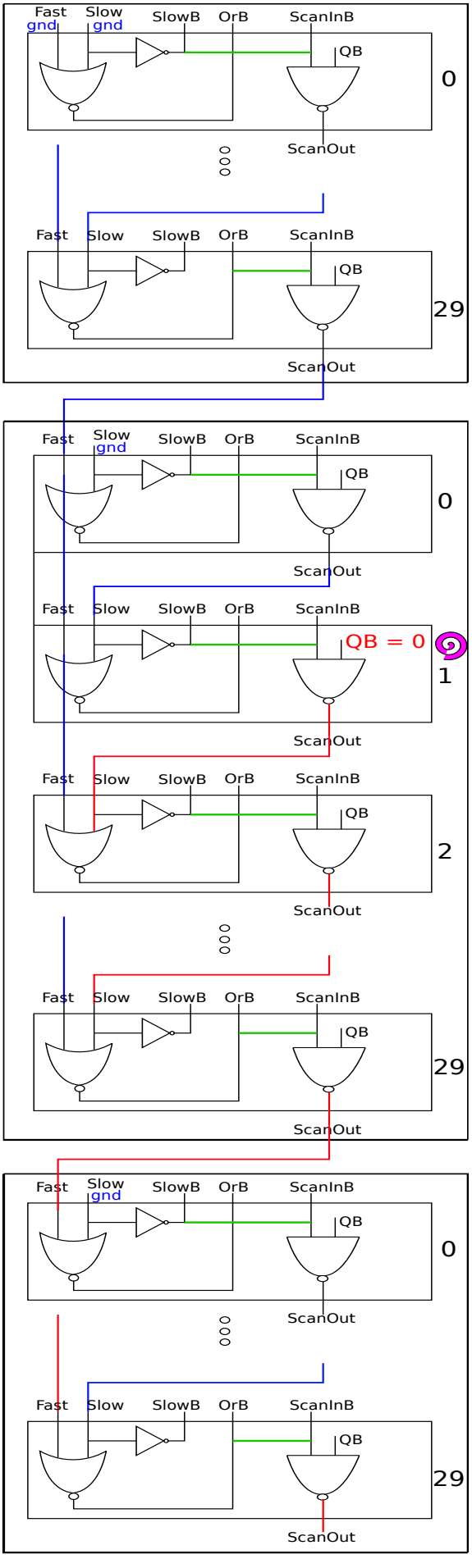


Figure 2.20: Fast and slow logic of ScanOut in readout cell

2.3.3.2 Time to digital converter

Time to digital converter TDC (called also fine time stamp circuit) is a novel feature in the chip, which is used to improve time resolution. The time resolution should less than 30 ps.

The time stamp has 2 fields, a fine (7 bits TS3) and two coarse time stamps (20 bits TS1 and 10 bit TS2). The clock frequency of all time stamp counters (TS1, TS2 and TS3) is equal - 100MHz. The purpose of TS1 and TS2 is to measure the coarse time when hit comes. TS3 measures the time with greater precision.

Figure 2.21 presents the schematic of the TDC. The transmission gate (switch) between nodes A and B is controlled by clocked hit signal. When DFF = 1, switch gets open and nodes A and B are separated. The current generated by VPBias transistor is nearly 100 times bigger then the current generated by VPBiasSmall transistor. Figure 2.21 bottom shows the waverforms of the signals. When hit arrives, the potential of node B increases quickly because the MOSFET capacitance is charged by the summed current of VPBias and VPBiasSmall transistors. The output of DFF changes from zero to one at the first clock edge after hit signal. In this moment switch gets opened and the potential of node B increases from now on slowly. The MOSFET capacitance is charged only by smaller current VPBiasSmall. When the potential of node B exceeds Vth, time stamp TS3 is stored.

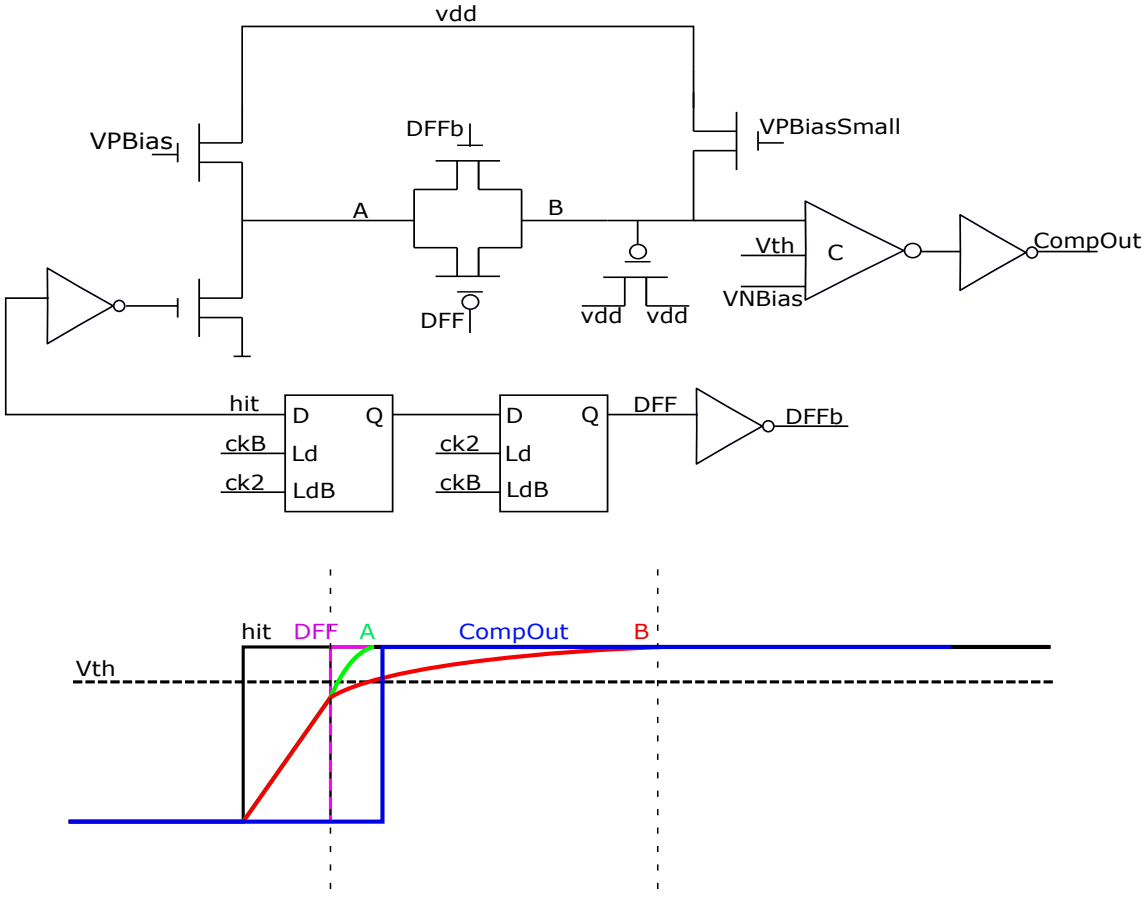


Figure 2.21: Schematic of TDC (fine time stamp)

Figure 2.22 shows three signals (green, blue and red) that are in time quite close. All three signals lead to the same TS11. However, the TS3 is different and can be used to measure the time precisely. The graph at the bottom of figure shows the TS3 response versus the hit time. When the hit time is shortly after the rising clock edge (green signal), the voltage of node B increases nearly to Vth before the switch gets opened. TS3 value is small (in our

case 5). When the hit time is shortly before the rising clock edge (red signal), the voltage of node B increases just a little before the switch gets opened. TS3 value is large (in our case 10).

The figure shows how the delta TS3 changes (dTS3 = TS3 - TS11) when the hit time increases.

We see that the time dTS3 increases from ts3min to ts3max and then jumps back to ts3min. The jumps occur when hit time is coincident with rising clock edges.

Three signals have different starting time but the same slope.

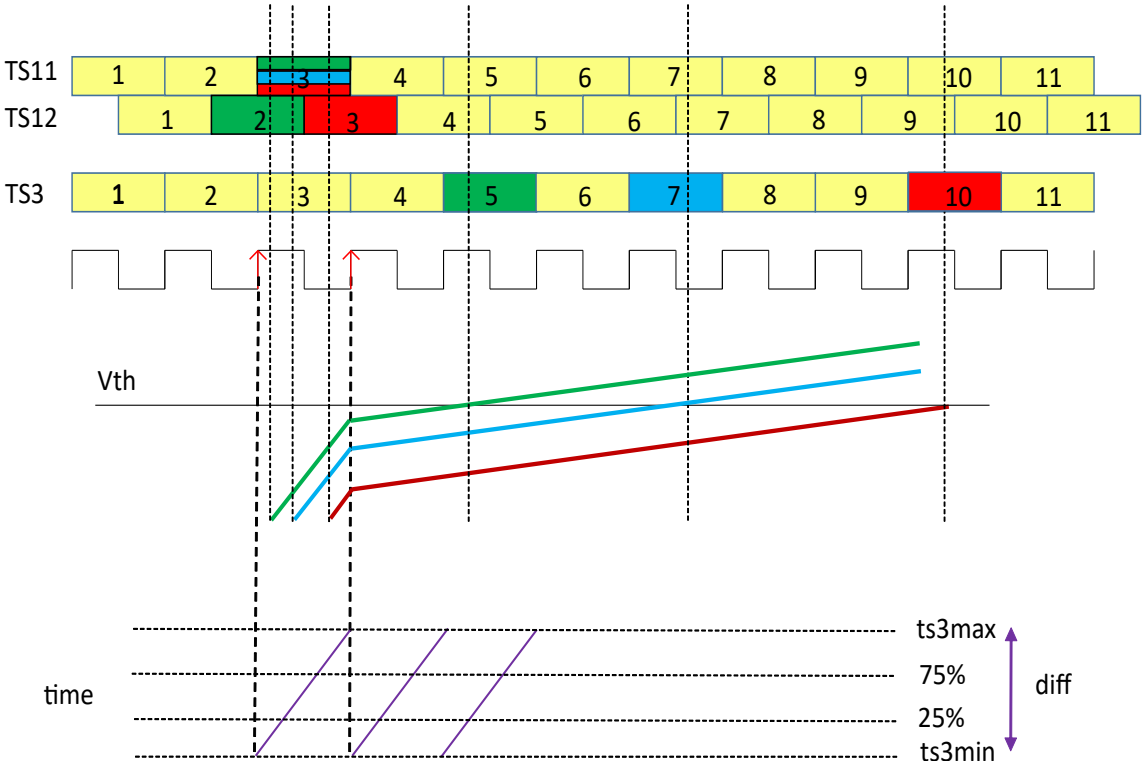


Figure 2.22: Explanation of fine time stamp

In order to find the exact comparator reaction time, the measured time dTS3 = TS3 - TS11 is divided into three sections:

1. If the measured dTS3 is less than (ts3min + 0.25 x diff), green signal in figure, the TS12 is in this case stable. We see however that the value of TS12 (value 2) is by one less then TS11 (value 3). Therefore in the formula + 1 should be added. The time can be calculated as:

$$time = Tck \times (TS12 + 1) + Tck \times (dTS3 - ts3min)/diff. \tag{2.4}$$

This expression is in the range TS11 x 1.0 x Tck to TS11 x 1.25 x Tck.

2. If the measured dTS3 is in the middle of the range, from (ts3min + 0.25 diff) to (ts3min + 0.75 diff), blue signal in figure, the TS11 has the stable value. Therefore the time can be calculated as:

$$time = Tck \times TS11 + Tck \times (dTS3 - ts3min)/diff. \tag{2.5}$$

This expression is in the range TS11 x 1.25 x Tck to TS11 x 1.75 x Tck.

3. If the measured dTS3 is greater than (ts3min + 0.75 x diff), red signal in figure, the TS12 is also stable. We see that the value of TS12 is equal to TS11. Therefore the time can be calculated as:

$$time = Tck \times TS12 + Tck \times (dTS3 - ts3min)/diff. \tag{2.6}$$

This expression is in the range TS11 x 1.75 x Tck to TS11 x 2.0 x Tck.

2.3.3.3 End of Column (EoC)

The purpose of EoC is to store temporarily the hit information and add additional column address. EoC of different columns form a directed array. It generates signal RdPix that is transmitted to the hit buffer and it pulls down the bus lines which is necessary because RAM and ROM cells only can pull up due to PMOS transistor.

EoC block also contains the driver for TS and other signals that distribute across hit buffers. The logic parts in EoC are similar as in hit buffer, for example priority logic, read function, slow and fast logic.

The connection between hit buffer, EoC and RCU (readout controll unit) is described in figure 2.23.

The inputs of EoCs are signals LdPix, LdCol, RdCol, pull down, VMinusPD, ScanOut<540>, FastIn, SlowIn, ScanInB, Pixel address and global time stamp.

LdPix: buffered with a driver and passed to pixels.

LdCol: based on this signal and on column level scan signal, the RdPix is generated.

RdCol: it has the same function for the array of EoC blocks as RdPix for the array of hit buffers.

Global TS: that are buffered with drivers in EoCs.

The output of EoCs are data out, FastOut, SlowOut, SlowInB, OrInB, time stamp buffer, RdPixBuff and LdPixBuf.

Data Out: hit buffer outputs (20 bits TS1, 10 bits TS2, 7 bits TS3 and 10 bits address) and 5 bit column address.

FastOut/SlowOut: that is the OR function of the 2nd hit flags in the EoCs.

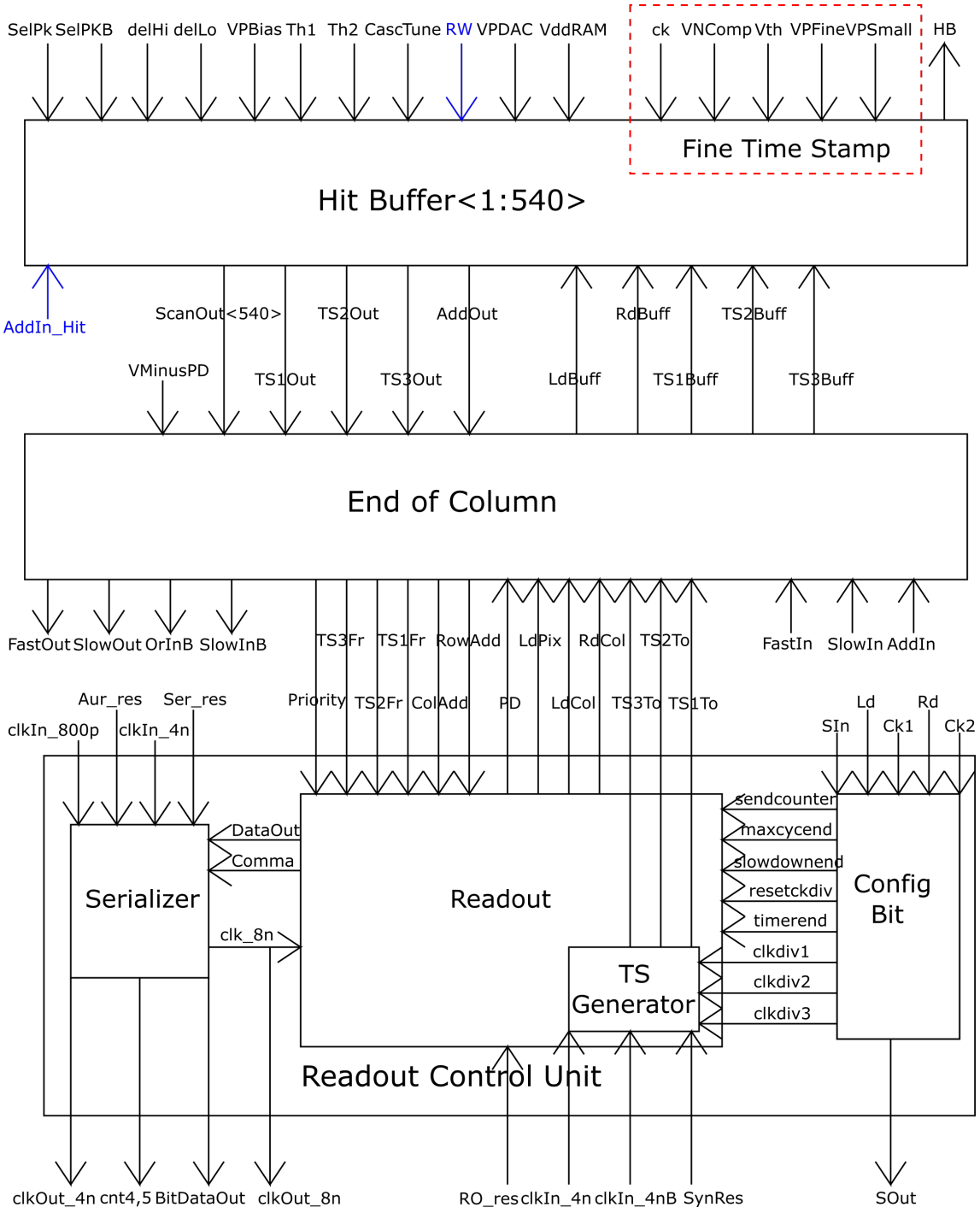


Figure 2.23: The connection between hit buffer and EoC

2.3.4 Chip Periphery

The chip periphery contains two blocks: one is a full custom part with the PLL, an analogue 2->1 serializer, configuration register. The other one is the synthesized digital part RCU (Read Control Unit). The RCU is rather complicated and it is implemented as synthesized block, which is designed and automatically generated via Verilog code. Place and route could be performed by Verilog netlist synthesis.

2.3.4.1 Readout Control Unit (RCU)

RCU consists of follow blocks: state machine and time stamp generator.

State machine receives the signal ScanOut and the hit data from the EoC buffers, transfers the data to the serializer, and generates the control signals, such as PullDN, LdCol, LdPix, RdCol. Each of these signals has its own control functions.

The time stamp generator generates three time stamps, TS1[19:0], TS2[9:0], TS3[6:0]. TS1 and TS3 of 25 ns length is transmitted to the hit buffers. When there is a hit, the hit data are stored in EoC, which include pixel address, row address, column address, ToT and the TS.

The time stamps are generated using binary counters and later gray coded to facilitate error correction.

RCU recives the signal PrioFromDet (called also ScanOut<540>) and the data from EoC.

TSFromDet(19:0) is the time stamp of the signals rising edge.

TS2FromDet(9:0) is the time stamp of the signals falling edge.

TS3FromDet(6:0) is the fine time stamp coming from TDC.

ColAddFromDet(4:0) and RowAddFromDet(9:0) are the column- and row addresses.

RCU generates the signals PullDN, LdCol, LdPix, RdCol.

RCU generates the following Grey coded time stamps:

TsToDet(9:0) that changes with rising edge of TSCk.

TsToDet(19:10) that changes with falling edge of TSCk.

TSToDet2(9:0) clock for the falling edge measurement.

TSToDet3(6:0) clock for TDC.

RCU also generates two bit data output BitDataOut(1:0).

To avoid signal delays from one column to the other, strong drivers between the RCU outputs and the horizontal signal lines are implemented. Additionally, signals between EoCs to RCU have also driver cells, these cells include D latches to extend the duration of the signals after the RdPix gets low.

2.3.4.2 Bias DAC with Diode

This chapter briefly describes the design of the bias block. It generates the bias voltages for the current sources for the amplifiers, feedback circuits, RC filter and comparator. The bias voltages are generated by a current flow through a diode-connected MOSFET. Every bias voltage can be adjusted using a current-mode 6-bit DAC. Each DAC register segment consist of 7 bits (one spare bit). The DACs are written using a shift register.

The DC current should be as small as possible. Small DC current brings small power consumption and little voltage drops. However if it is too small, the amplifiers are slow. The value of these current, maximal up to 12 μA, are generated by DACs in bias block. The 6 bits DACs (0-63) are stored in shift register, which is loaded from FPGA.

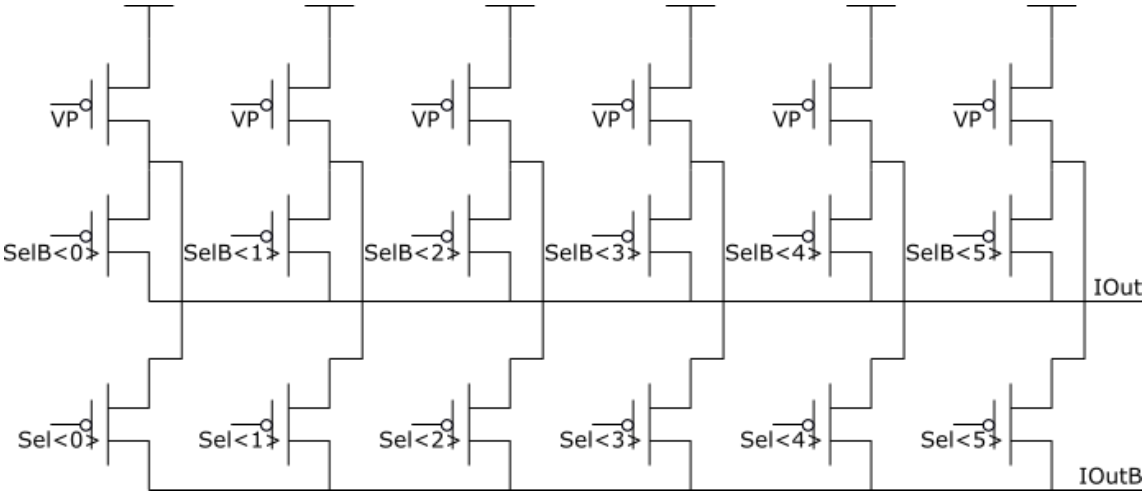


Figure 2.24: Schmatic of bias DAC

One of the key component is the DAC to allow adjustable bias current. Generally, a DAC converts a digital input value into an analog signal. As illustration in figure 2.24, the DACs are designed as differential current source topology. The current sources are grouped into 6 groups consisting of 1, 2, 4, 8, 16, 32. Three PMOS transistors consist of each bit in current mode DACs, the drains are connected together, DAC current flows from vdda to output. All transistors can be switched on and off according to the binary weighted scheme. If the signal sel is positive, the bottom transistor turns off and then the current flow through the middle transistor to Iout, which are used for all the bias current. If the signal sel is negative, the current flow directly into the bottom transistor to IoutB. The 6 bits sel and selB signals are generated by register block with triple modulator redundancy.

A basic element for biasing current is the current mirror. In an ASIC, current mirrors are always implemented as MOS transistors. Depending on the current polarity, two types of diode-connected transistor connect to the DAC for the sake of biasing current source in pixel, shown in figure 2.25. The DAC current makes voltage when it flows through the diode-connected device. The voltage is distributed in pixels and connected to the gates of the current sources.

If the needed current value bigger than 200 nA , it could be directly generated from bias DAC. Because the MSB 63 corresponding to 12 μA, so the LSB 1 is 200 nA. If smaller than 200 nA is required, current dividers topology is necessary, shown in figure 2.26. The current divider consists of distributed current mirrors with multiple outputs. One of the outputs is connected to diode-connected transistor to generate the desired bias voltage for the ASIC.

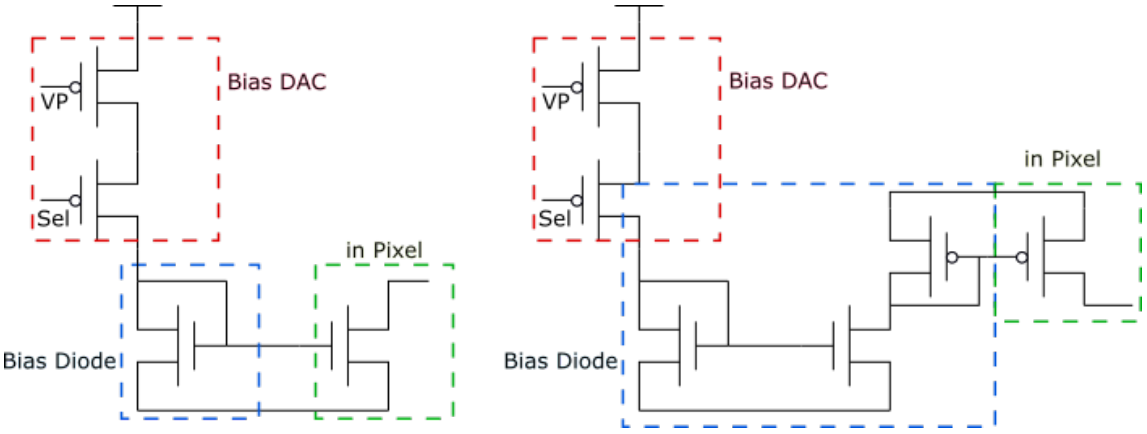


Figure 2.25: Two types of bias diode depending on current polarities

For example the current for feedback VPFB, one NMOS source (out of possible 4) is connected to PMOS diode connected FET. One PMOS source is connected to input of the second divider. This has a consequence that the current in second divider is by 32 smaller than in flowing in the first divider. Because the NMOS mirror has ratio 4:1, PMOS mirror 8:1. The current flow out is 32 times smaller than the current flow in the first divider. For feedback current, the total attenuation is 32 x 32 x 8 x 8 = 65536. If we want to have a 100 pA current, then we need 6.5 μA (100 pA x 65536 = 6.5 μA). This corresponding to a DAC setting of 34 (6.5 μA/12 μA x 63 bit).

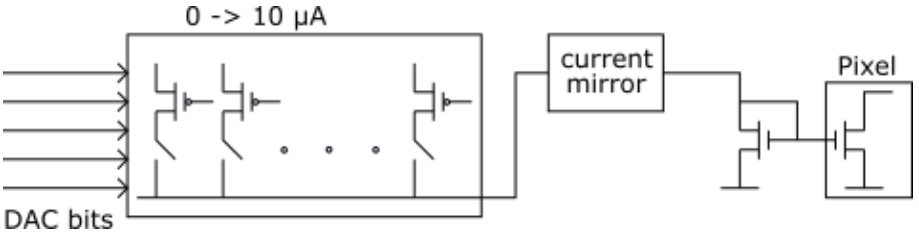


Figure 2.26: Current divider designed between DAC and diode connected transistor

2.3.4.3 Configuration Register

All of these configuration registers are implemented via a serial shift registers. These registers store setting for the DACs that generate bias block, threshold voltage and injection voltage. They are also used to control the injection and the pixel RAM. All shift registers use full custom made cells and they are connected in the form of daisy chain.

Each register contains a triple redundant data latch followed by majority logic. Triple redundancy makes the register tolerant to single bit flips that can be caused by ionization (single event upset). The cells have an auto-refresh feature. When a logic detects a single flip in 3 data latches, the majority output is reloaded into the latches.

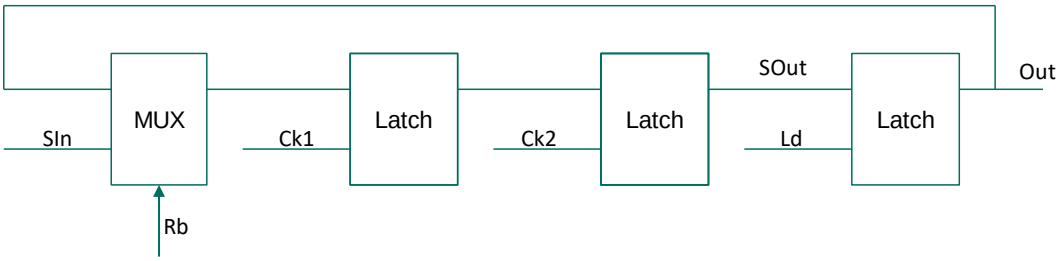


Figure 2.27: Structure of one bit

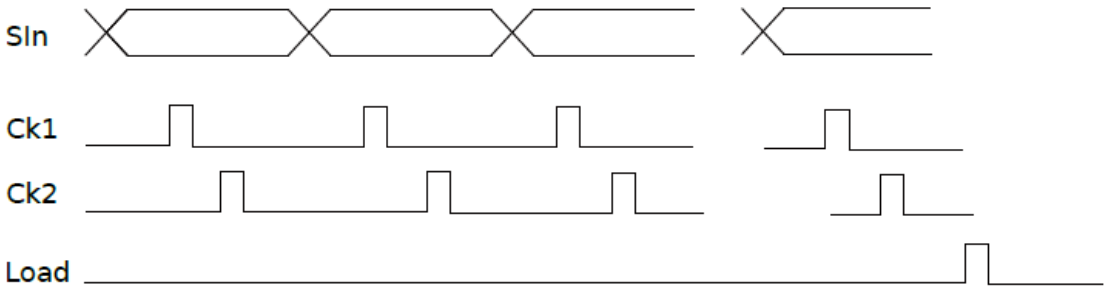


Figure 2.28: Configuration sequence

Figure 2.27 illustrates the structure of one register bit. The bit uses following interfaces: Ck1, Ck2, Sin, Sout, Rb, Load. These signals are connected to analogue pads. In order to robust clock and avoid hold violation meanwhile, ck1 and ck2 are non-overlapped. The data moves only when ck1 and ck2 are positive edge in turn. The bits of the registers are connected to switches and DAC configuration bits to control the functionality of the MPROC. By applying the ck1 and ck2 signals, the logic level at the serial input CSIn is stored in the flip-flop.

Write and read functions are contained in shift register. The write sequence uses the signals SIn, Ck1, Ck2 and Load, shown in figure 2.28. After the Load signal is issued, the content of the shift register is stored in the latches. The latch memory attached to each bit of the shift register. An additional signal Rb is used to implement a read back functionality.

2.4 Measurements

2.4.1 Measurement setup

In addition to ASIC development, PCB, firmware and software design are important aspects of ASIC development.

PCB Design

The ASIC is wire bonded on a carrier board and connected to FPGA board.

Since the carrier board uses PCI (Peripheral Component Interconnect) connector, and FPGA FMC connector, an additional board GECCO is used as interface.

The carrier PCB connects its distinct in- and outputs to the standardized interface of the GECCO board.

GECCO is in-house developed and it is intended to be more flexible offering a number of standardized connectors for the application of powers, bias voltages, data and configuration signals. Since the GECCO system is designed be generic, the differential topology of signals offered by the FPGA is maintained.

The connection between GECCO and carrier board is established via a PCI connector [57].

Figure 2.29 presents the complete setup of the GECCO system used for MPROC project. The carrier PCB is connected to GECCO board by PCI adaptor and the GECCO is connected to FPGA board by FMC interface.

The ASIC is protected with cover designed via FreeCAD and produced via a custom 3D-printed plastic casing.

The GECCO system has been designed by Felix Ehrler and Rudolf Schimassek. The carrier board was designed by me.

Figure 2.29: Test setup for MPROC

2.4.2 Measurement results

The laboratory measurements have been performed to test the functionality of the pixel and readout electronics. The measurements were done using the test injection circuit based on the injection capacitance C_{inj} (4.87 fF, obtained from simulation), which is connected to the input of the CSA.

Measurements with oscilloscope

Figure 2.30 shows the output of the CSA when NMOS feedback (left) and PMOS feedback (right) are used. In both cases the first input signal is negative.

The output of the CSA is blue line. The injection signal is yellow and the hit bus is purple.

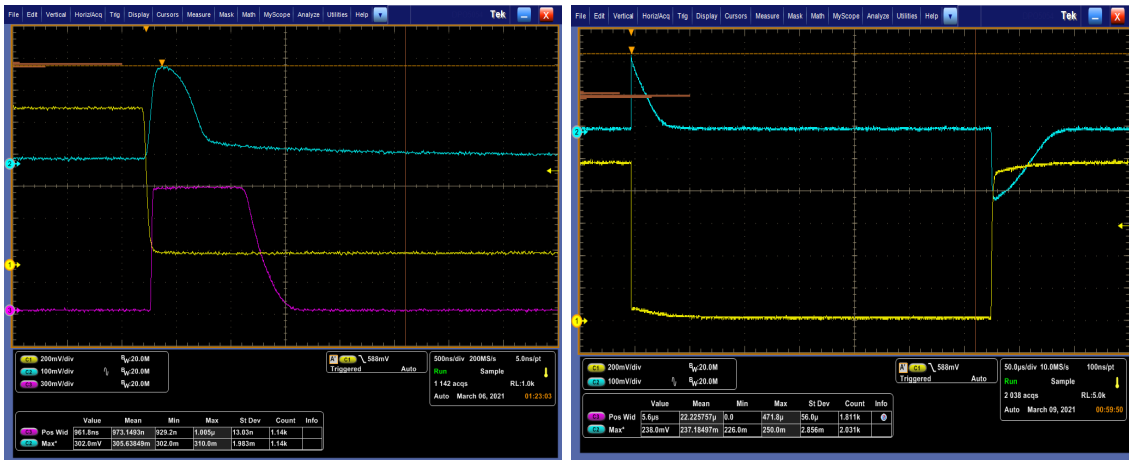


Figure 2.30: Waveform of positive feedback (NMOS) (left) and negative feedback (PMOS) (right)

Figure 2.31 shows the CSA response to different injection signals. NMOS feedback has been used.

Figure 2.32 shows the maximum signal amplitude as function of injection signal.

The amplitude with NMOS feedback is larger in the whole signal range than the amplitude with PMOS feedback. The amplitude versus signal dependences are linear until saturation around injection equals 1.4 V is reached.

Let us compare this with expected signals when the detector is used to detect golden nanoparticles. The x-ray fluorescence peak from gold nano particles is 69keV. About 4.43eV is required in CdTe to generate one electron hole pair. Therefore the charge signal is 15.6ke. This signal is generated by injection pulse of about 0.51V. The corresponding amplitudes at the CSA output are 120 mV and 150 mV.

$$V_{inj} = \frac{Q}{C_{inj}} = \frac{69keV \times 1.6 \times 10^{-19}}{4.43 \times 4.87 \times 10^{-15}} = 0.51V \tag{2.7}$$

Figure 2.33 shows the waveform of hit bus signal versus injection voltages. The hit bus is the comparator output. The peak detector was connected to comparator input. The chip was configured in the way that the signals of four neighbouring pixels are summed (cluster mode).

Figure 2.34 shows hit bus pulse width versus injection voltage. Red symbols are measurements when peak detector is connected to comparator. Black symbols are measurements when second amplifier output is connected to comparator.

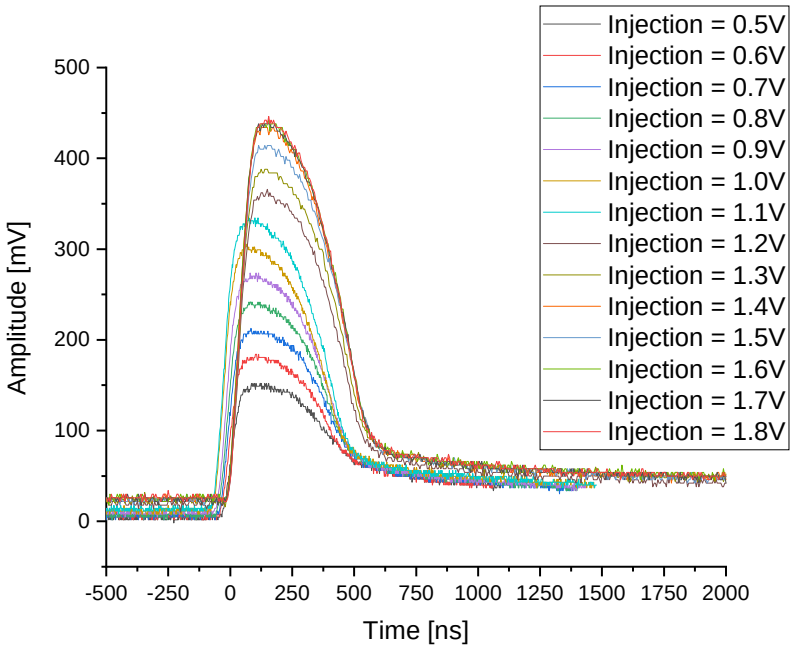


Figure 2.31: Amplitude of amplifier output versus injection voltage (with positive feedback)

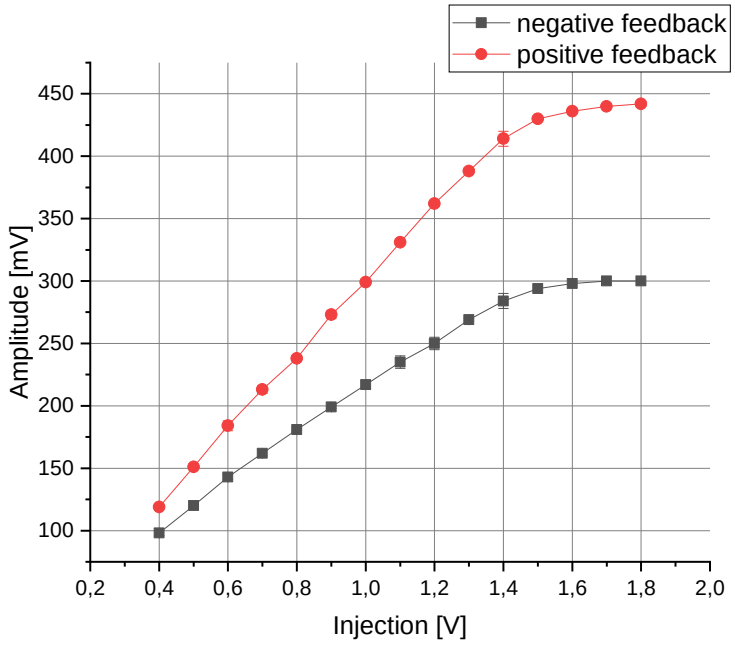


Figure 2.32: Amplitude of amplifier output with positive feedback (NMOS feedback) and negative feedback (PMOS feedback)

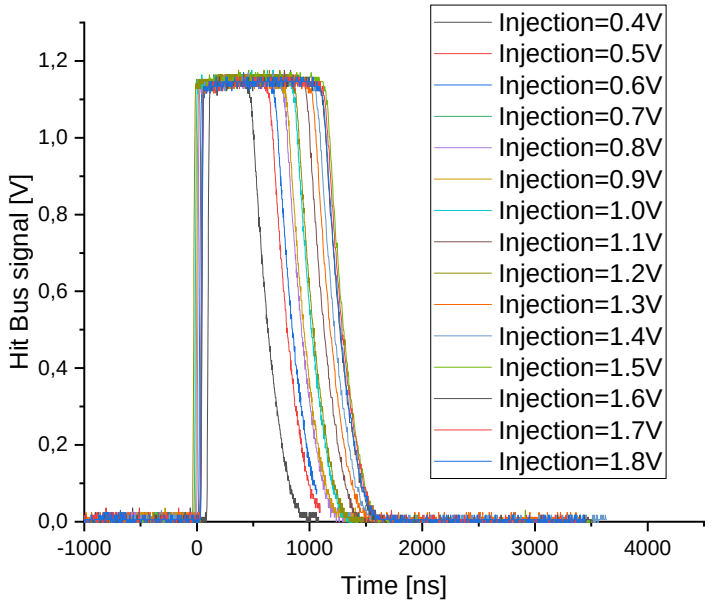


Figure 2.33: Hit bus signal versus injection voltage

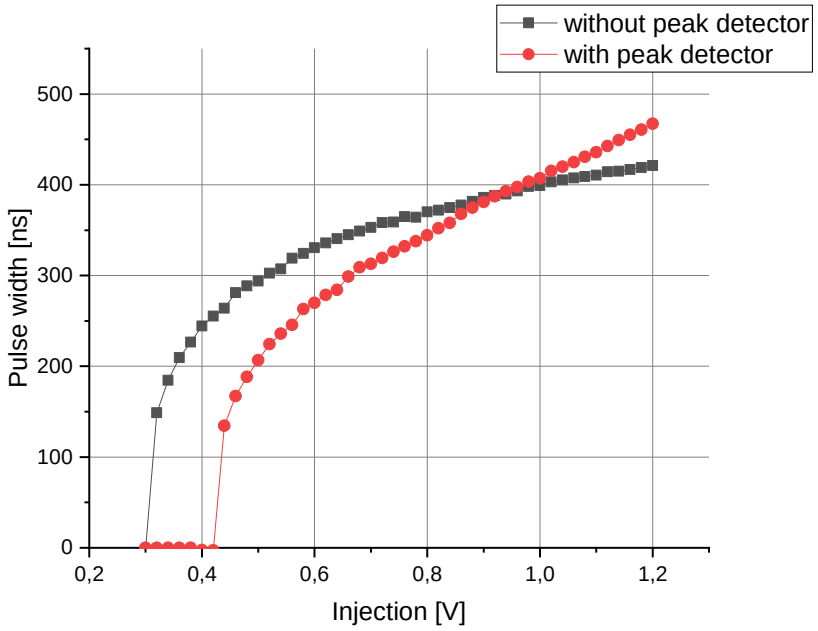


Figure 2.34: Single pixel pulse width versus injection voltage, with and without peak detector

3 CCPD

3.1 Background of hybrid pixel concept

The first hybrid pixel detectors were developed in the 1980s and '90s for high energy particle physics experiments at CERN. Since then, many large collaborations have continued to develop and implement these detectors into their systems, such as the ATLAS, CMS and ALICE experiments at the LHC (Large Hadron Collider). Using silicon pixel detectors as part of their inner tracking systems, these experiments are able to determine the trajectory of particles produced during the high-energy collisions that they study [51].

The key innovation for the construction of such large area pixel detectors was the separation of the sensor and the electronics into independent layers. Hybrid design allows to optimize each element individually. Assuming that particle sensor can be optimized for radiation tolerance, which requires high high resistivity silicon, while the readout ASIC can be made for high particle hit rates of the order of MHz/mm^2 with low resistivity substrate [52].

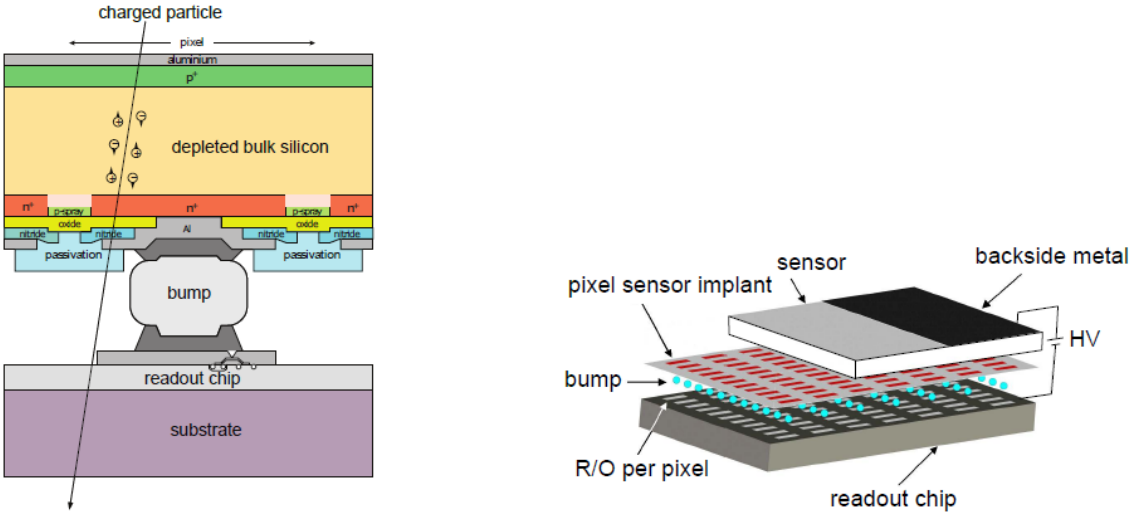


Figure 3.1: Hybrid pixel detector

Compared with standard hybrid technology (the signal is transmitted through bumps and each readout channel needs one bump), another option is CCPD (capacitively coupled pixel

detector), the signal is transmission through capacitive coupling. One advantage of CCPD compared with standard hybrid detector is cost, because CCPD does not need special small pitch of bumps. So far the CCPD were usually made by gluing two chips together.

3.2 Project Introduction

The classification of hybrid pixel detectors is illustrated in figure 3.2. In the case of standard hybrid detector, each pixel on the sensor chip has its own channel on the readout chip. Bump-bonding is used to connect chips. The pixel signals are transmitted without multiplexing and processed in parallel. This detector is complex and expensive. The bumps add to the material budget.

In the case of CCPD (capacitively coupled particle detector)[43] [44], signals are transmitted from the sensor to the readout chip capacitively. CCPD has been proposed for several experiments such as CLIC or ATLAS [45] [48]. For simplicity, the first CCPD prototypes used chips glued together. Since power supply could not be transmitted capacitively, both chips had to be wire bonded to power supply lines on PCB.

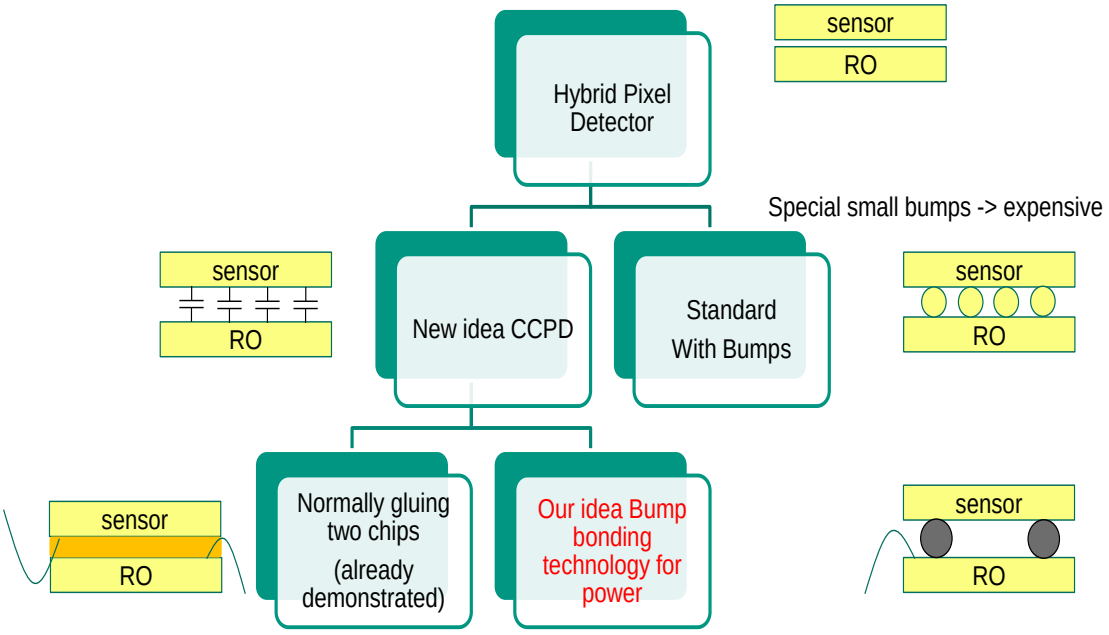


Figure 3.2: Hybrid pixel detector classification

In this chapter, a new concept of CCPD has been presented (figure 3.3). The sensor chip and the readout chip are mechanically connected with a small number of relatively large bump bonds. The signals from the sensor chip are transmitted over the gap via capacitive coupling. The benefit of this concept is that a conventional flip chip technique can be used to build the detector. Since the bumps can be large, an industrial bumping process can be used which assures low cost. The bumps provide mechanical stability to the detector. If the bumps are used for powering, only one chip needs to be connected to power supply lines on PCB with wire bonds. One issue with the new concept is larger spacing between the chips. The gap is larger than the case of glued CCPD. This was solved by a rail-to-rail output amplifier in sensor chip which has large signal amplitude and makes capacitive signal transmission easier.

In order to test the concept, a sensor chip called CCPD53 has been implemented.

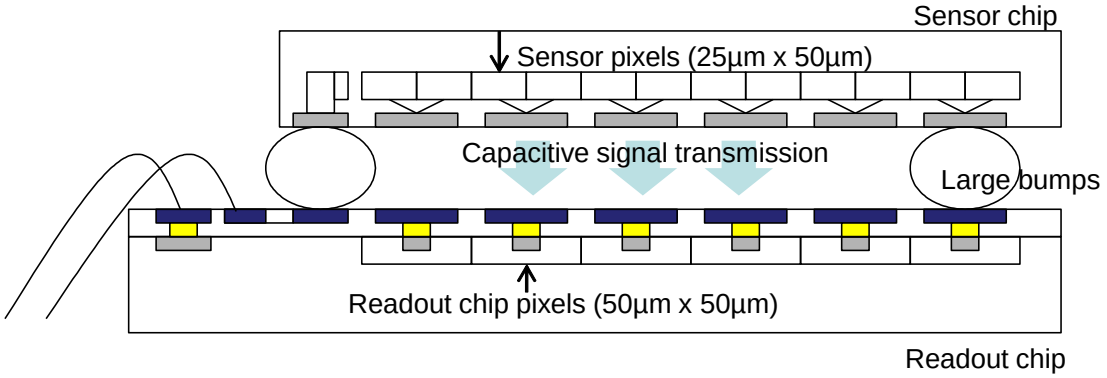


Figure 3.3: A new concept of CCPD. Sensor and readout chip are connected with several large bumps, signals are transmitted capacitively [44].

3.3 CCPD53 Sensor Chip

CCPD53 has been implemented in AMS ah180 nm HVCMOS technology. The technology has been improved by adding additional deep p-well implant and by use of high resistivity substrates.

We have tried to fulfill the specifications for ATLAS pixel detector listed in Table.

The size of the sensor chip is 2.5 mm x 2.7 mm. There are in total 2560 pixels (64 x 40) in the pixel matrix and each 25 μm $\times$ 50 μm in size. Every pixel has a sensor based on a deep n-well in p-substrate diode, which is depleted by biasing the substrate with a negative high voltage of about -50 V. Pixel electronics is placed inside the deep n-well. The signal transmission pads have a size of 32 μm x 38 μm and they are arranged with 50 μm pitch, the same as in the RD53 IC. The sensor has been done in the way that it can be readout by the standard readout ASIC for CMS and ATLAS the RD53 IC [49]. Pixel to readout pad multiplexing has been done to enable readout of smaller pixels with larger electrodes. In other words, a group of 16 pixels connect to 8 pads for capacitive signal transmission. Shift registers are used to select pixels for injections and provide a multiplexer for amplitude output and comparator output. There is a test circuit based on a capacitor for charge signal injection in every pixel on the CCPD53. All the pads are placed at the bottom of the chip and the pitch is 100 μm.

Table 3.1 presents the specification of CCPD sensor chip [70] [72].

Table 3.1: Specifications for ATLAS vertex detector

Technology	AMS 180 nm HVCMOS
Pixel Size (our chip)	25 μm x 50 μm
Pixel Size (specification)	25 μm x 25 μm
Particle of detector	charged particles
Radiation hardness	500 Mrad and 5 x 10^{15} n_{eq}/cm^2
Energy Resolution	
Spatial resolution	3 μm (transversal and long)
Charge measurement (ToT)	6 bit
Time Resolution	$<$ 25 ns
Data Rate	1.28 Gbps
In time threshold	$<$ 1 ke
Hit Rate	3 GHz/cm^2
Trigger Rate	1 MHz
Latency	12.8 μs
Dynamic range	
Power consumption	$<$ (clic) 50 mW/cm^2
Hit efficiency	$>$ 97 %
Material budget per payer	(clic) 0.2% X_0
Maximal granularity	1 - 10 mm pixel size (long)

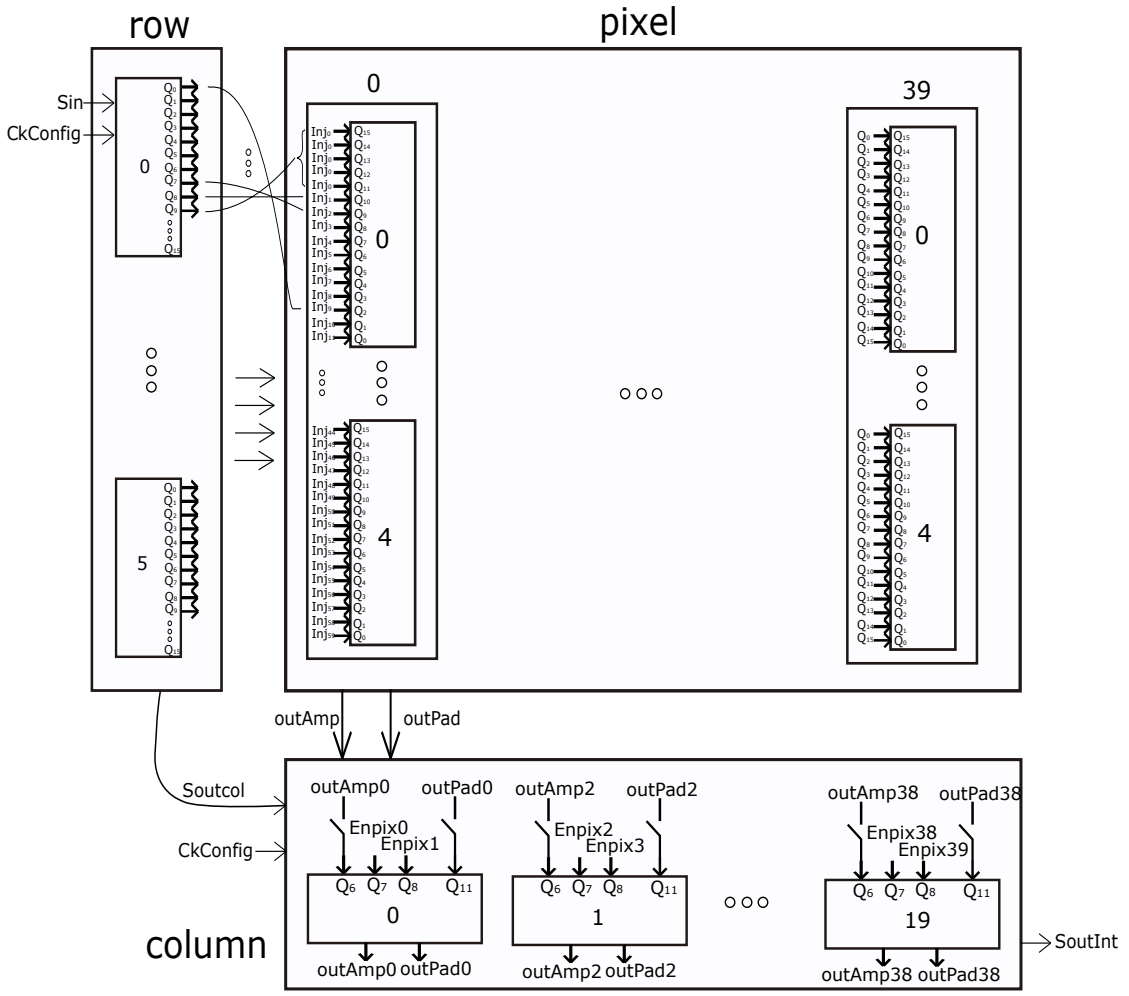


Figure 3.4: Structure of the CCPD53 sensor chip

3.3.1 Design and Implementation

3.3.1.1 Sensor chip structure

The block scheme of CCPD53 chip is shown in figure 3.4.

There are 64 pixels (size 25 μm x 50 μm) in a column and 40 columns build up the whole matrix. The pixels are grouped in groups of 16. There are 4 such groups per column.

3.3.1.2 Sensor chip pixel electronics

The schematic of sensor amplifier is shown in figure 3.5. The pixel electronics is placed in the deep n-well that is the sensor electrode.

The n-well is biased using a highly resistive element Rb. The input of amplier is capacitively connected using Cin to the n-well. The feedback capacitor Cf, which is shown in this

figure, is actually hidden in transistor level schematic. It is a parasitic capacitor between drain and n-well. It is connected between p+ diffusion and N-well. The feedback resistor Rf connects Ampout and Ampin. The signal detection is based on the following principle: the signal charge Qs (electrons) are collected by the positively biased n-well. This leads to a small voltage drop in the n-well equals Qs/Cnwell, that is detected by the amplier. The

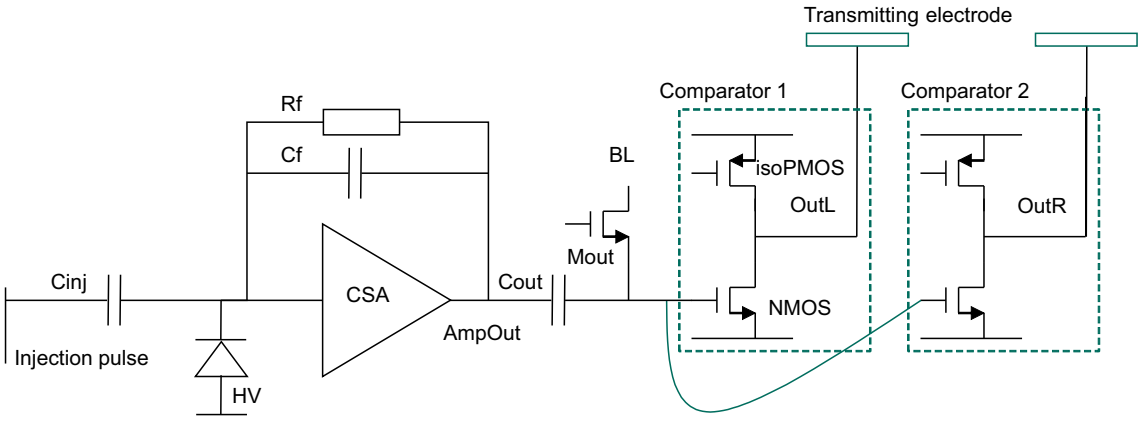


Figure 3.5: Pixel schematic of the CCPD53 sensor chip

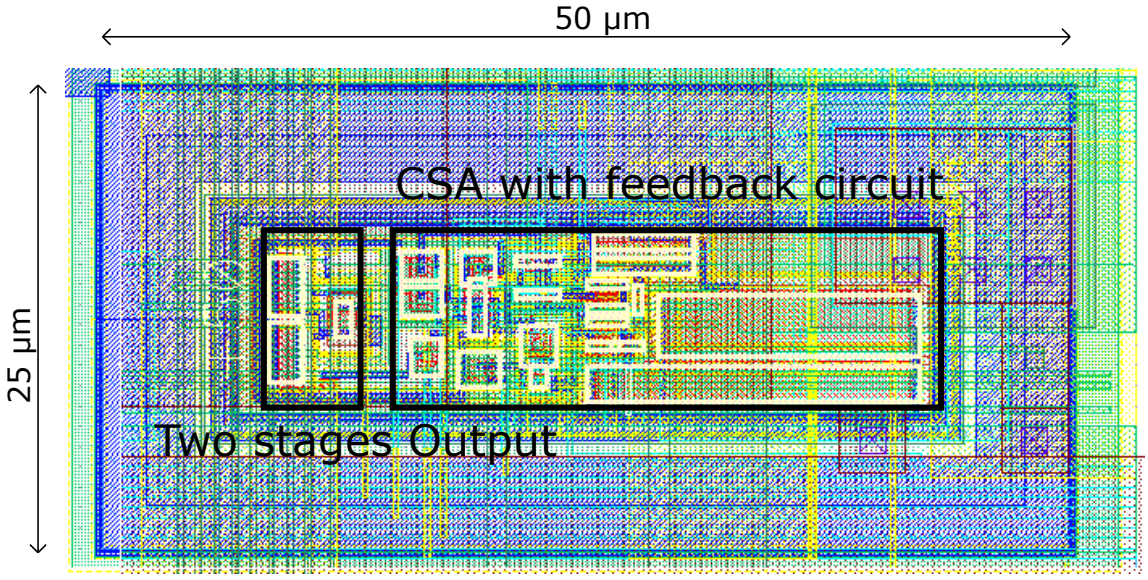


Figure 3.6: Pixel layout of the CCPD53

charge Qs is then ”absorbed” by the feedback capacitance Cf and the amplfiied signal at the output of the amplfiier equals Qs/Cf. The purpose of the DC feedback is to clear Cf after the signal amplification. Finally the original n-well voltage is restored by the bias element Rb.

The amplifier output is AC coupled (with Cout) the the input of two simple CMOS comparators with rail to rail outputs. The novelty is that the PMOS pull up transistor in the CMOS comparator is isolated by a deep p-well from the sensor n-well. The deep p-well is a new implant that AMS introduced for this project.

To assure strong amplification a novel CMOS based comparator with rail to rail output swing has been implemented in pixel. The pixel electronics is presented in figure 3.5. It contains a CSA (charge sensitive amplifier), two comparators, coupling capacitors, bias circuits and injection circuit.

The outputs of the two comparators are labeled OutL and OutR.

Capacitance C_{inj} is used to generate test signal to n-well.

Since the pixels are 25 μm x 50 μm in size and the electrodes are two time bigger, special address encoding has been used to connect a group of 16 pixels to 8 transmitting electrodes. The address encoding is done in the way shown in figure 3.7. The pixels are grouped into

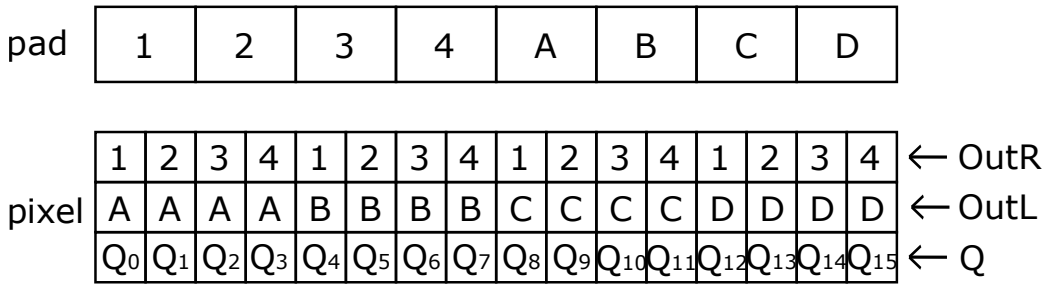


Figure 3.7: Address encoding

four subgroups A, B, C, D. Every pixel has index 1–4. The eight pads are connected to comparator outputs OutR and OutL in the way that for instance pad 1 is connected to OutR outputs of all four pixels with index 1 or pad A to OutL outputs of all pixels in the subgroup A. If for example, the particle hits pixel C 1 (Q8), signals at the pad C and at the pad 1 will be generated. The signals have full swing of 1.8 V and are easy to transmit over larger gaps between chips. By recording two signals in the readout chip, the exact hit position can be detected and reconstructed. In the case of single hits, which occur in most of cases, the scheme works well.

3.4 PHOTON Readout Chip

Since we could not obtain the RD53 ASIC for our measurements, we have used pixel readout chip named PHOTON for capacitively coupled readout to prove the new concept CCPD. This chip was designed in our group.

The PHOTON readout chip has been implemented in the UMC 180 nm CMOS technology. It consists of a matrix of 32 x 30 identical square pixels with 150 μm x 150 μm size. The PHOTON chip allows counting and integration of charge signals.

Each pixel can be addressed for electrical test or masked during acquisition individually. A shutter allows for switching between the counting and integrating modes.

3.4.1 Pixel electronics

The schematic of a pixel in the PHOTON chip is presented in figure 3.8. The charge sensitive amplifier A1 receives, in our case, the signals from the CCPD53 via the chip-to-chip coupling capacitance C_c. The CSA is followed by the voltage amplifier A2, a high pass filter, a comparator (Com) and a 13-bit counter (Count).

The difference between ThP and ThN potentials defines the detection threshold. The voltages ThN and ThP are generated on chip by Digital to Analog Converters (DACs). A shutter signal enables the counter and in this way defines the measurement time.

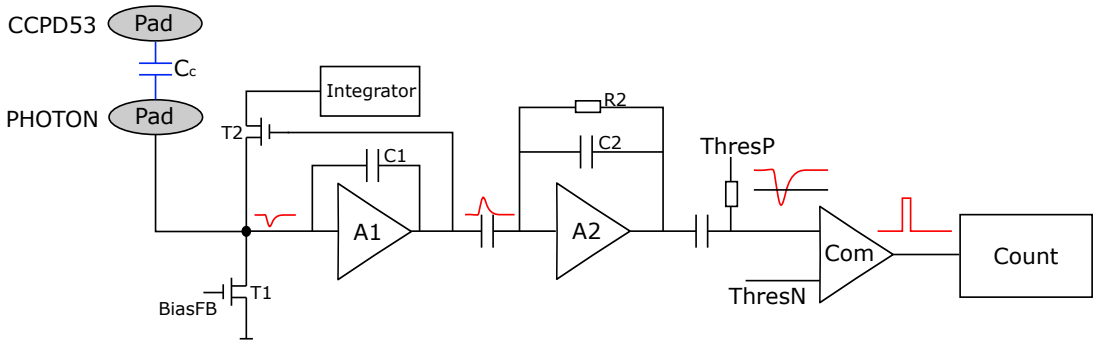


Figure 3.8: Schematic of a pixel in the PHOTON chip

3.5 Measurements

In order to test the performance of the chips, two test systems have been built. One is used to test the sensor chip stand-alone (figure 3.9), either with a test signal that is applied to the injection capacitor or with a radiation source. The other one is used to test the sensor and readout chip together (figure 3.21), to check whether the signal can be transmitted from the sensor to the readout chip.

3.5.1 Standalone Sensor Chip Test

3.5.1.1 Experimental Setup

The test system is shown in figure 3.9, it is the similar test system as used for MPROC chip.

This system includes software, the Nexys Video FPGA board, FMC connector and adapter board, carrier board and mother board. It is explained in [54].

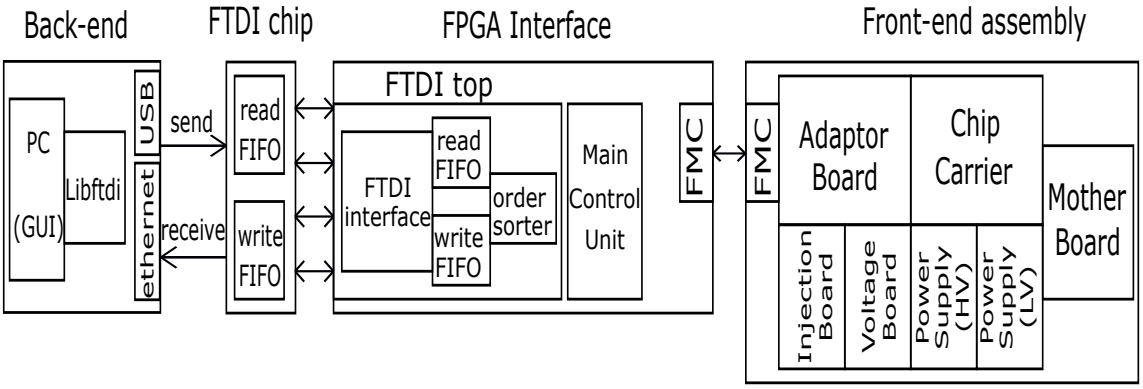


Figure 3.9: Experimental setup

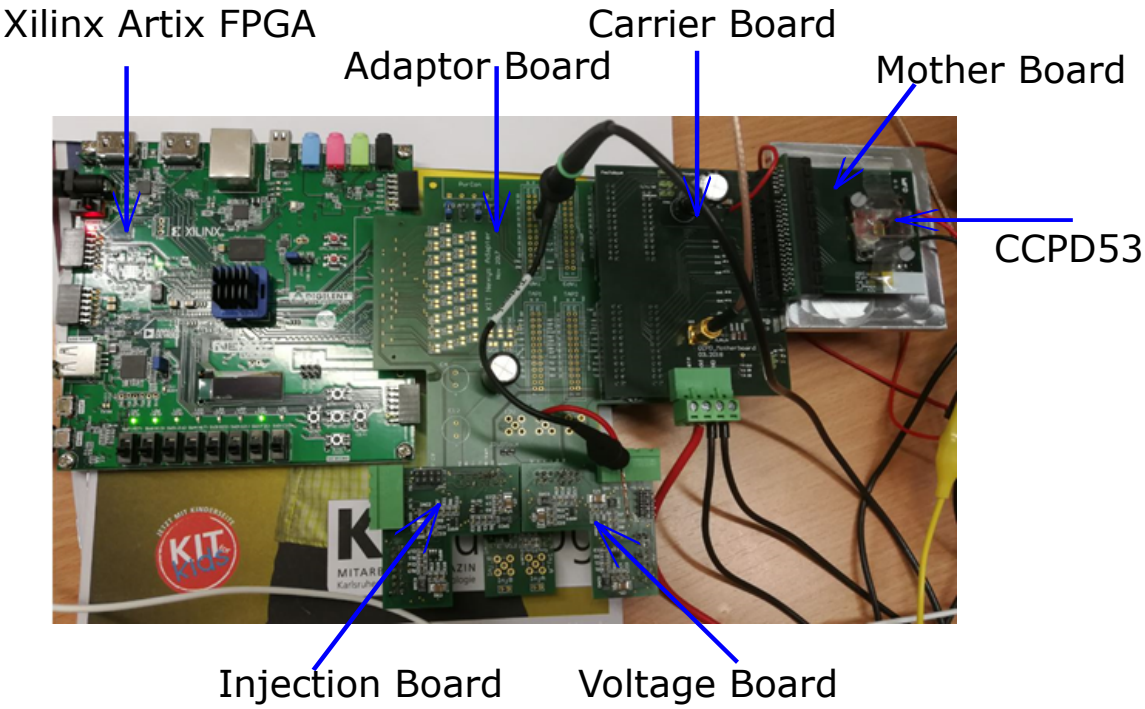


Figure 3.10: Photo of experimental setup for standalone chip test

3.5.1.2 Measurements with electrical test signals

It is possible to inject charge into a single pixel using a capacitive injection circuit. In this way the sensor can be tested using only electrical input signals. It is also possible to measure the amplifier- and readout pad output through a test multiplexer. These two features allow standalone chip tests without a readout chip.

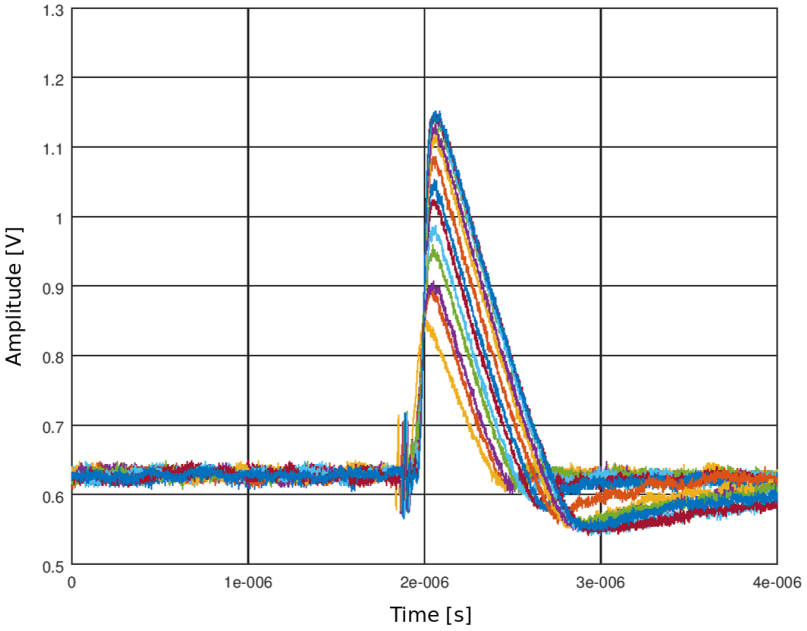


Figure 3.11: Amplifier output versus injection voltages

Figure 3.11 shows the signal amplitude at the amplifier output versus different injection voltages (0.3 V – 1.7 V). By knowing the injection capacitance (C_{inj} = 0.64 fF), we could calculate using equation 3.1 that 0.3 V injection generates 1200 electrons. The RMS base line noise corresponds to the input signal of 35 electrons. The amplitude is linearly proportional on the input signal, as shown in figure 3.12.

$$\frac{0.3V \times 0.64fF}{1.6 \times 10^{-19}C} = 1200e \tag{3.1}$$

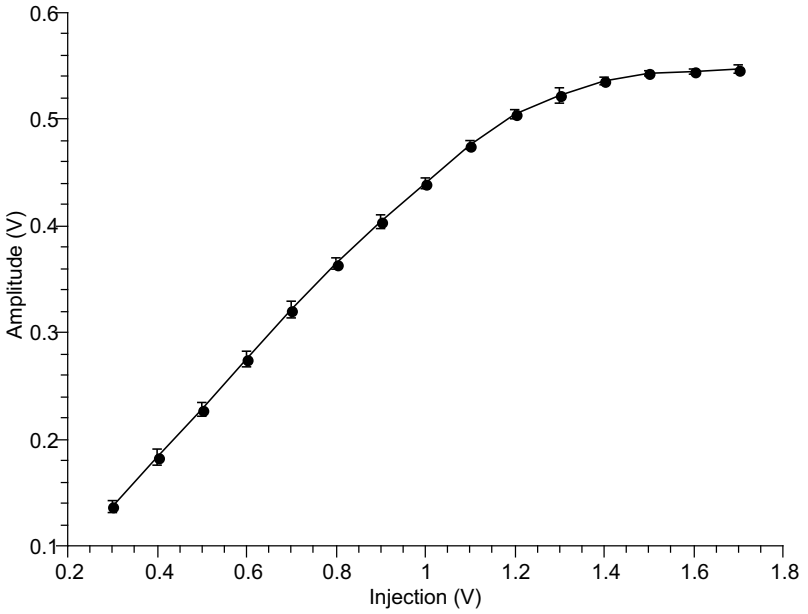


Figure 3.12: Signal amplitude versus injection voltage

3.5.1.3 Measurements with radioactive sources

The sensor chip was also irradiated with a Fe55 radioactive source that generates photons with two energies: 5.9 keV (Ka) and 6.5 keV (Kb) and the spectrum was measured to calibrate the amplifier gain, injection circuits and to determine noise. Amplifier output signals have been measured via the output multiplexer and recorded by scope. This measurements were done using different methods and under different temperatures.

There are three methods to measure the spectrum: (1) From maximal signal level, (2) From peak to peak amplitude and (3) the whole waveforms have been recorded and a numerical filter has been used to calculate the mean value of the waveform before the signal and the mean value of the waveform after the signal. Figure 3.13 and 3.14 show as comparison the histograms obtained with the second and third method at room temperature. The noise is lower in the later case. The Gaussian fits are shown in both figures. Generally, the third method leads to the best signal to noise values.

Figure 3.15 shows histogram obtained with numerical filter when the sensor was cooled using a Peltier element to about -10 C. Temperature did not affect the peak mean value, however the noise is lower when the temperature is lower. The noise of 43 e sigma value has been measured from the Fe55 peak at the sensor temperature of about -10 C. That is for our application a relatively low noise, since we expected that the typical signal of a minimum ionizing particle is approximately 2200 e when we have a depletion layer of 30 μm.

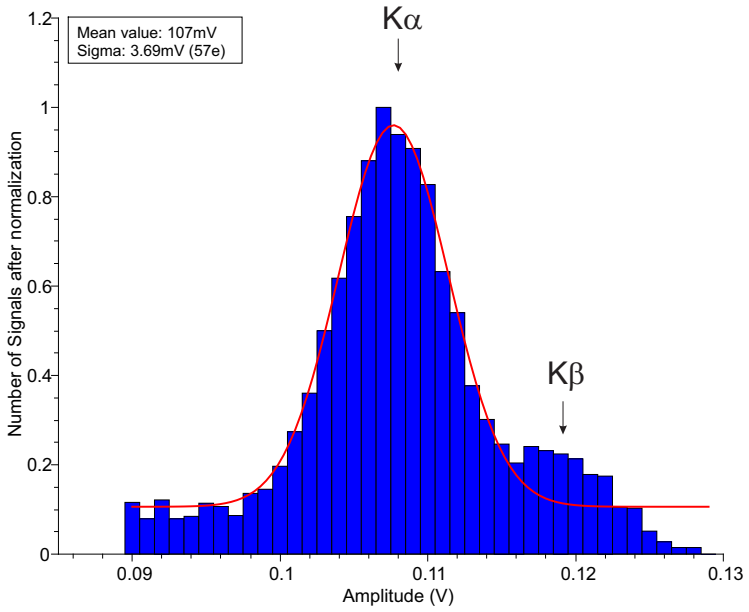


Figure 3.13: Fe55 spectrum obtained using a numerical filter at room temperature

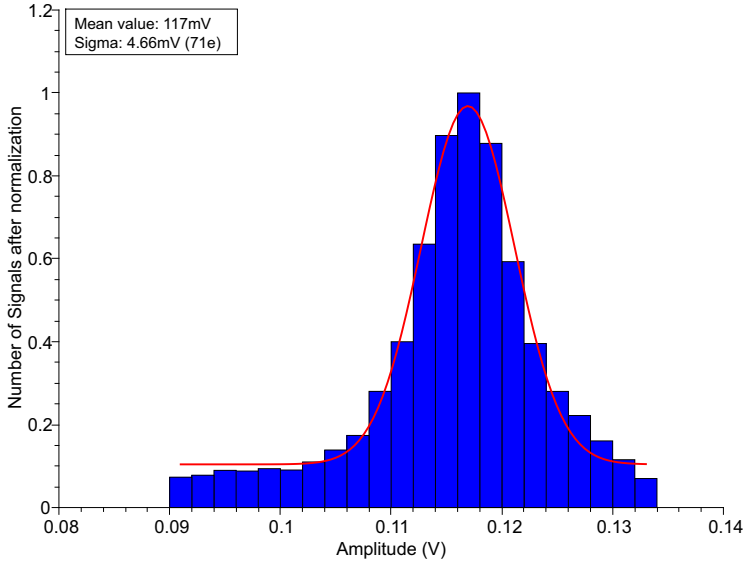


Figure 3.14: Fe55 spectrum obtained using peak to peak method at room temperature

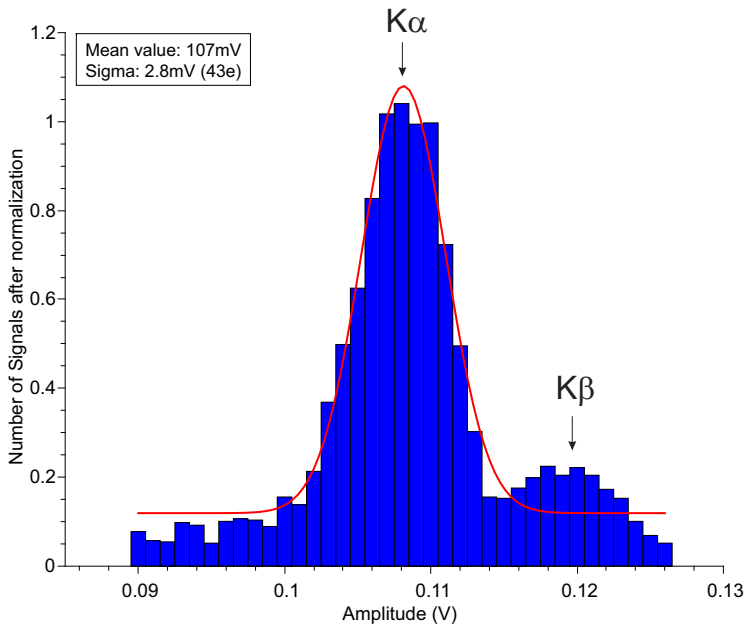


Figure 3.15: Fe55 spectrum obtained using numerical filter at low temperature (Peltier cooler)

3.5.2 Both Chip Test

This section describes several measurements performed on CCPD. It is possible using a capacitive injection circuit to inject charge into a single pixel of the CCPD53 sensor chip. The charge signals can be also generated using radioactive source. The preamplifier of the readout chip receives the signals through the chip-to-chip capacitance that can be roughly estimated from the equation.

$$C_c = \frac{A}{t}\epsilon_r\epsilon_o = \frac{32\mu m \times 38\mu m}{32\mu m} \times 4 \times 8.85 \times 10^{-12} F/m = 1.35 fF \tag{3.2}$$

where A is the pad area, t is the distance between two chips for which we assume 32 μm, ϵ_o is the value of the vacuum permittivity which is 8.85 $\times$ 10^{-12} F/m and ϵ_r is the permittivity of the dielectric medium between the two plates, for glue it is 4.

Using a capacitance extraction tool that calculates the electric field, we obtain a slightly smaller value of 1.10 fF.

Since the pixel pitch of the PHOTON chip and the CCPD53 sensor chip are 150 μm and 50 μm respectively, the capacitively coupling can not be fulfilled one by one, only every third readout pad could be received the coupled signal from the sensor chip.

The complex connection diagram is shown in figure 3.16. From the vertical direction, the column 1 to 6 of the readout chip, for example, are corresponding to the column 1, 3, 4, 6, 7, 9 of the sensor chip. From the horizontal direction, the row 29, 28 of the readout chip are corresponding to the pad D and A of the sensor chip in group 5. Row 27 is connected to pad 2 for group 4. Row 26 is connected to pad C for group 4. Row 25 and 24 are corresponding to pad 4 and 1 for group 3.

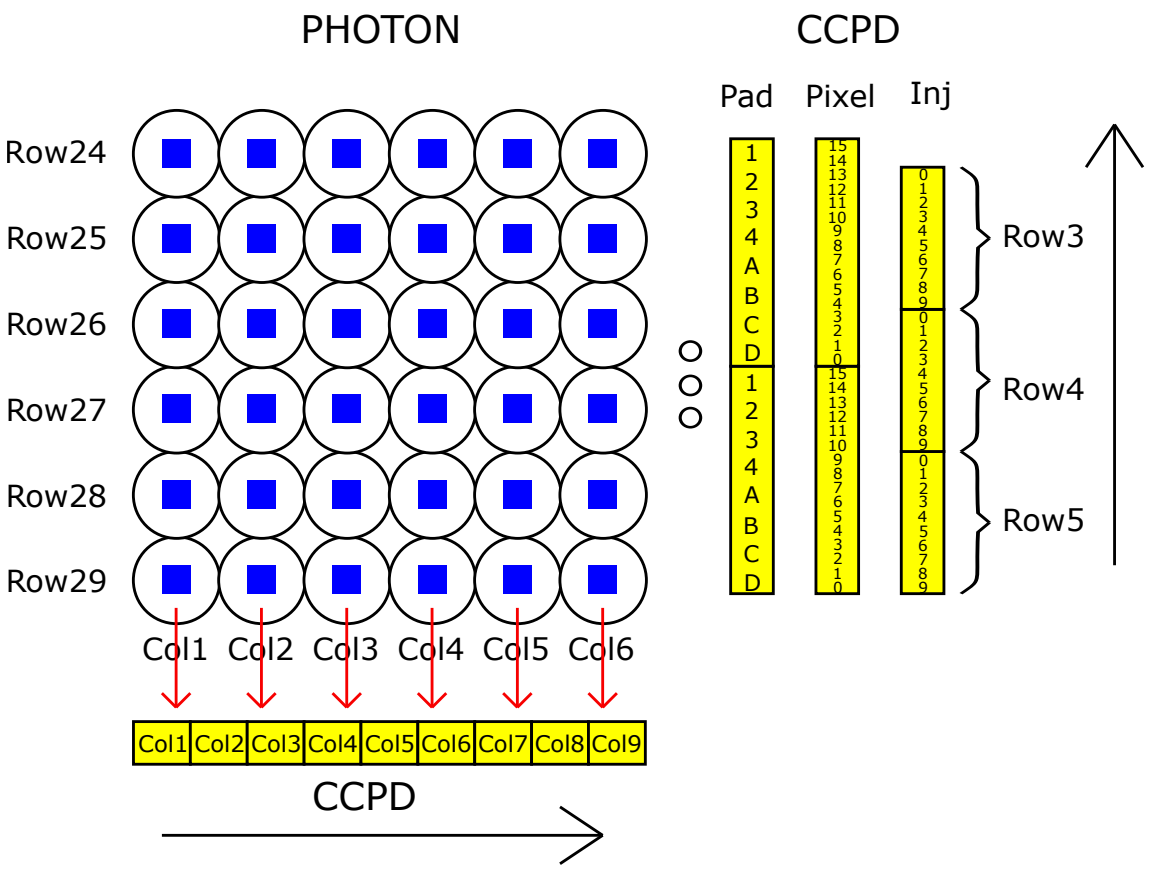


Figure 3.16: Arrangement of the PHOTON readout chip and the CCPD53 sensor chip

3.5.2.1 Experimental Setup

The heights of gold studs used as bumps are about 15 μm (option 1) and 32 μm (option 2). Gold studs has been only placed on the PHOTON readout chip and then the sensor CCPD53 sensor chip is connected onto it using flip-chip machine.

Since the size of the PHOTON chip (5 mm x 5 mm) is larger than the CCPD53 chip (2.5 mm x 2.7 mm), the sensor chip is only flipped on the lower right corner of the readout chip. Both chips are then connected to its respective FPGA boards, illustrated in figure 3.19. Firstly, both chips are wire bonded on photonV2 PCB and then CCPD53 board is glued contact onto the photonV2 board, both PCBs are fixed through screws. Afterward, the sensor chip is wire bonded through the other side to the pads on the CCPD53 board.

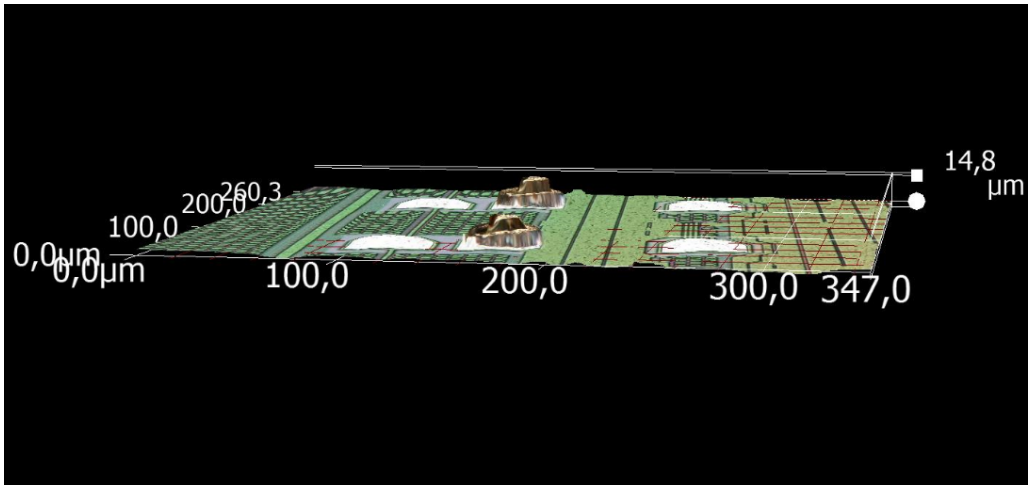


Figure 3.17: The height of bumps

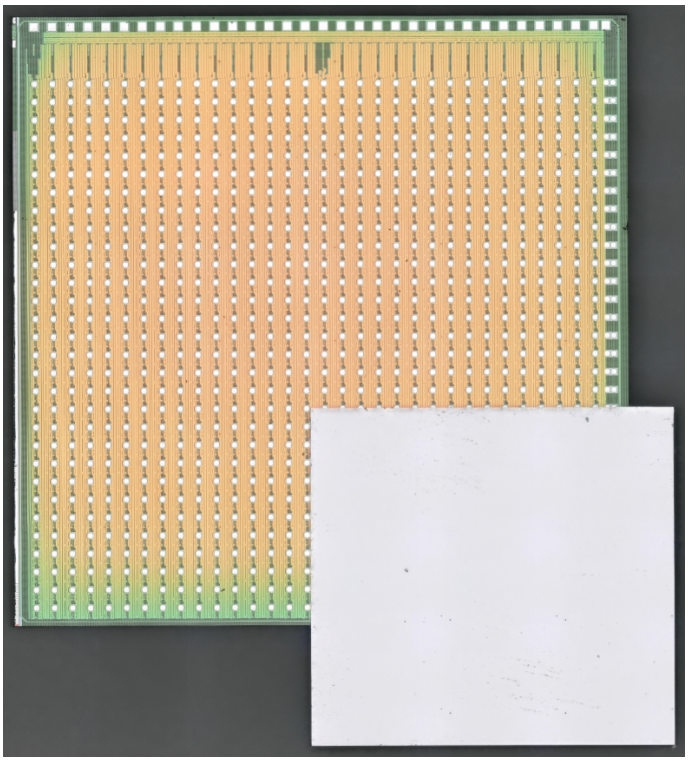


Figure 3.18: Photo of the assembly with the CCPD53 chip and the PHOTON chip

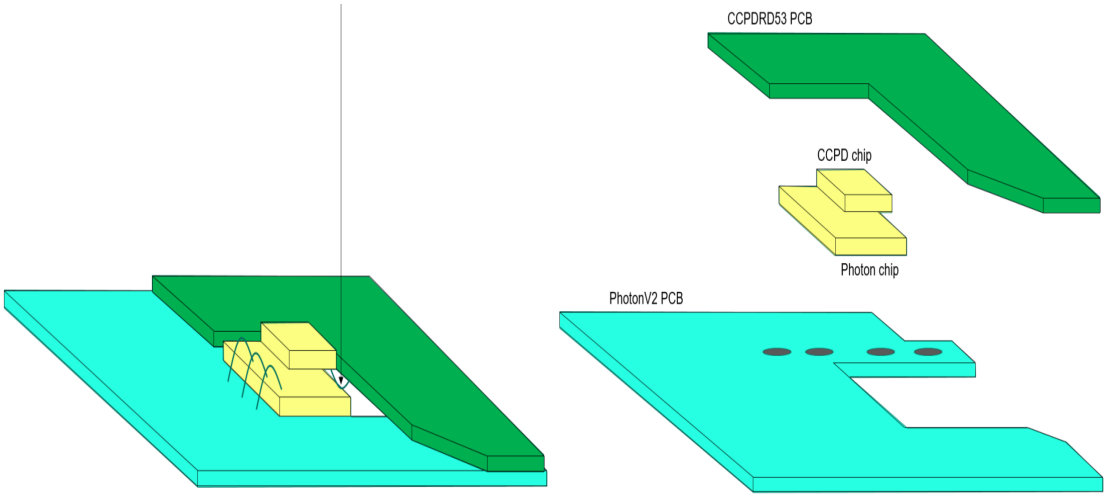


Figure 3.19: Assembly with the CCPD53 chip and the PHOTON chip. The chips are wire bonded to different PCBs.

The structure and the photo of the complete experimental setup for both chips test is presented in figure 3.20 and 3.21. This system is different than standalone chip measurement setup. One extra PC, FPGA Nexys board and carrier board were needed additionally in this system. Each ASIC require one PCB, FPGA and back-end assembly.

The CCPD53 sensor chip and the PHOTON readout chip are mounted and wire bonded respectively on two chip carriers from top and bottom sides, these two PCBs are glued together. Two glass covers are screwed fixed and used on both side for the ASICs protection. The carrier board contains supplies, bias voltages, two low and one high power supplies connections, monitoring capability, etc. These both PCBs are then connected to Xilinx Artix-7 board via FMC connectors. Two PCs are available for providing GUIs for sensor and readout ASICs. Single pixel or matrix readout, bias voltage DACs, configuration bits, injection values as well as oscilloscope options could be set through GUI. The time condition and constrain are defined in the firmware.

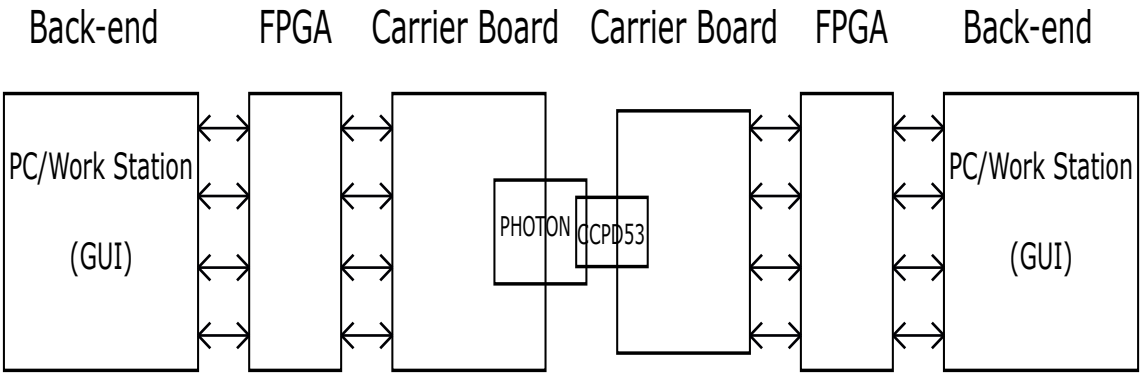


Figure 3.20: Experimental setup for testing of both chips

3.5.2.2 Counting

As mentioned, the PHOTON chip has two operation modes: integration and counting. In the first measurement, counting mode has been used. We have used the test circuit at the beginning of the pre-amplifier to inject charge signals of about 6000 e into the CCPD53 with different frequencies up to 1 MHz. The number of counts are read out during the

Figure 3.21: Photo of experimental setup for testing of both chips

measurement. The counting time was set by 4.096 ms per measurement. The PHOTON chip could correctly count the signals in the frequency range up to 1 MHz with small errors as can be seen in figure 3.22.

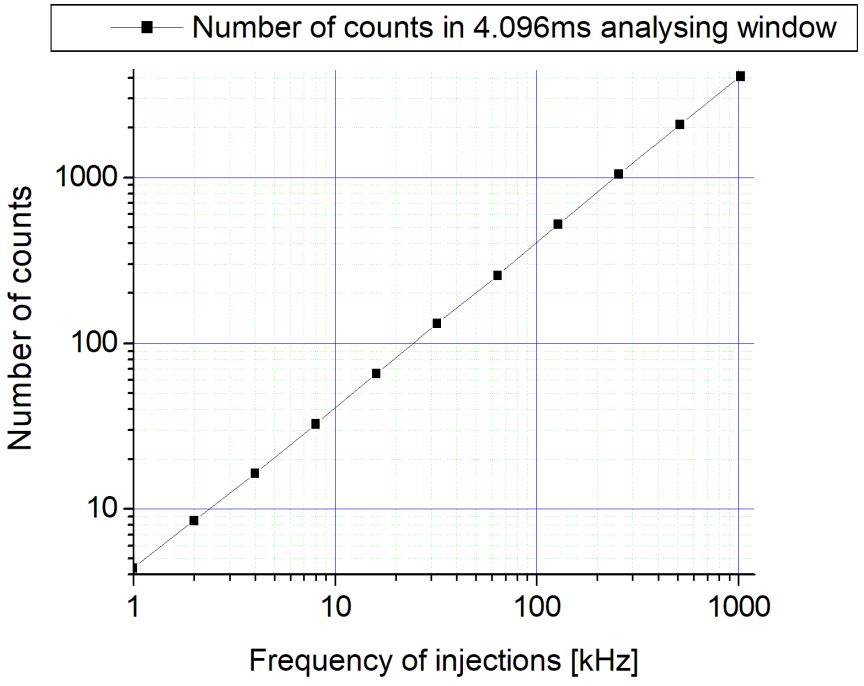


Figure 3.22: Measurement result obtained with the CCPD53 that is read out using the PHOTON chip. Test signals were injected into the CCPD53 at different frequencies. The number of detected signals is shown over the generation frequency.

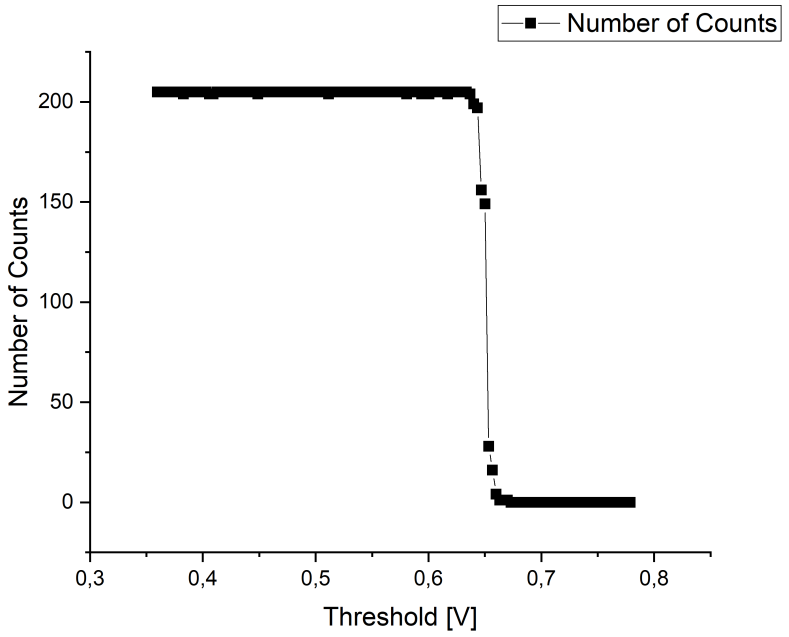


Figure 3.23: Threshold scan for single pixel. 205 injections of 2600 e have been applied to one CCPD pixel sensor and the threshold voltage of PHOTON chip has been varied. For each threshold setting the number of counted signals has been plotted.

3.5.2.3 Threshold measurement for a signal pixel

Both, the pixel of the CCPD53 chip and the pixel of PHOTON chip contain comparators. The comparator of the CCPD53 pixel introduces the particle detection threshold. The output signal of this comparator is digitally encoded and transmitted capacitively to the PHOTON chip. The comparator of the PHOTON pixel defines the threshold for the reception of the digital signal from the CCPD53.

In order to estimate the chip-to-chip capacitance C_C and demonstrate the feasibility of capacitive signal transmission, we have measured the threshold voltage (ThP-ThN) in the PHOTON chip required to detect a test signal. This test signal has been generated by injecting 2600 e into the CCPD53 pixel. A simulation performed with an analog circuit simulator shows that the injection of 2600 e generates a nearly squared pulse shape with an amplitude of 1.8 V and a duration of 500 ns at the pad of CCPD53. In order to obtain the threshold value in the PHOTON chip required for detection of this signal with 50 % probability, threshold voltage ThP - ThN has been varied from 0.39 V to 0.59 V; 205 test signals were generated for every threshold setting and the number of counted signals recorded. Figure 3.23 presents the efficiency curve for a single pixel of the readout chip. At large threshold values no pulses are seen from the readout chip as they are all below the threshold. Lowering the threshold, more and more pulses are seen until all injected pulses are detected. The inflection point is about 0.526 V, which corresponds to the threshold ThP - ThN. Comparison of the measured threshold to simulations with various inter-chip capacitances delivers the estimation for $C_C = 1.1$ fF.

3.5.2.4 Threshold measurement for whole matrix

The measurement from figure 3.23 has been performed for every PHOTON chip pixel. Due to device- and glue amount fluctuations, the threshold varies from pixel to pixel as can be

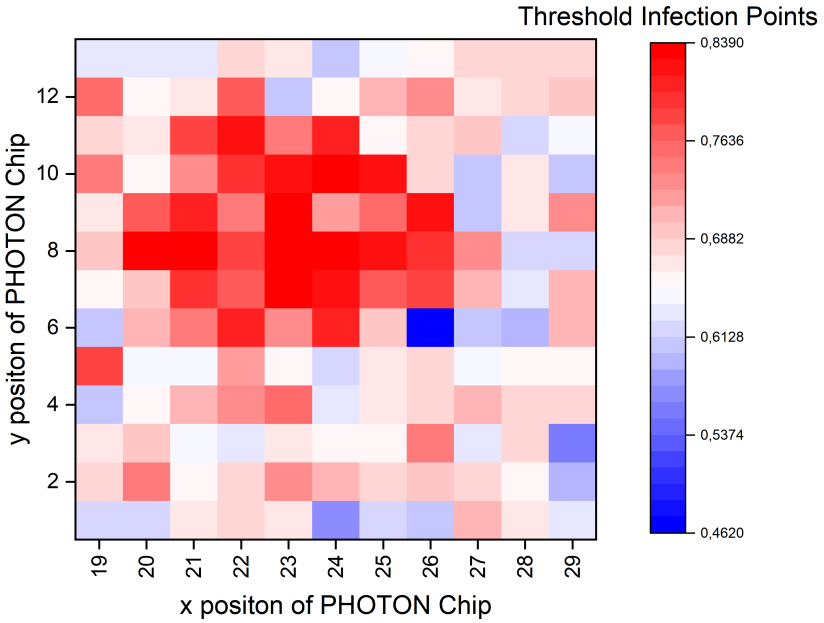


Figure 3.24: Threshold scan for the whole PHOTON chip matrix. Injections of 2600 e applied to the pixels of the CCPD53. Threshold values in the pixels of the PHOTON chip required for detection the signals from CCPD53 with 50 % probability are plotted. X-position corresponds to pixel row and y-position to pixel column.

seen in figure 3.24. The variation of the thresholds is from 0.44 V to 0.63 V (minimum to maximum). The distributions mean value is 0.56 V with a standard deviation of 35 mV. The values of CC estimated from simulations vary from about 0.65 fF for the pixel with position (x, y) = (27, 3) to 0.95 fF for the pixel (23, 8). This variation can be explained by inhomogeneous glue distribution. In the regions with less glue, capacitance is smaller due to a smaller ϵ_r . The pixel from the measurement shown in figure 29, (x, y) = (27, 3) is in the region with smaller thresholds.

4 HVMAPS25

4.1 Project Introduction

The monolithic particle pixel sensor HVMAPS25 has been implemented in the 180 nm HVCMOS technology of TSI Semiconductors. The sensor could be applied as a vertex detector for some future experiments such as CLIC and CEPC.

The physics aims of CLIC include high-precision measurements of the Higgs boson interactions with other particles and with itself. Unlike protons, electrons and positrons are truly point-like elementary particles. Therefore, compared to proton - proton collisions at the LHC, electron-positron collisions at CLIC could provide complementary and more accurate information about the Higgs boson. In addition, precise measurements of the top quark at all three energy stages would provide sensitivity to potential new physics scenarios. Some of the proposed studies at CLIC could even allow physicists to probe phenomena that originate at energies much higher than that of the collisions themselves [71].

Significant progress has been made to develop silicon pixel technologies for use in the vertex and tracker regions of the proposed CLIC detector design via a comprehensive R & D programme [70].

Many monolithic pixel sensors have been designed in our group.

Analog and digital parts were always separated as far as possible, in order to reduce the crosstalk caused from digital part to sensor electrode.

However, in the case of HVMAPS25, the analog and digital parts are placed inside the pixel.

The signal charge collection electrodes are small n-wells (2 μm x 4 μm) embedded in the high resistivity p-type substrate.

The pixel electronics contains a fast and low power charge sensitive amplifier, comparator, threshold tune DAC and a digital circuit that measures the arrival time of the hit with 10 bit resolution and the amplitude (time over threshold) with 6 bit resolution. Time resolution better than 10 ns can be achieved.

Table 4.1 shows the specifications for HVMAPS25 ASIC [70].

Table 4.1: Specifications for HVMAPS25 ASIC

Technology	TSI 180 nm HVCMOS
Pixel size	25 μm x 35 μm
Particle of detector	charged particles
Radiation hardness	100 Mrad and 5 x 10^{15} n_{eq}/cm^2
Energy resolution	
Spatial resolution	3 μm (transversal and long)
Time resolution	5 ns
Data rate	
Power consumption	$<$ 50 mW/cm^2
Hit efficiency	99.7 - 99.9 %
Material budget per payer	0.2 % X_0
Sensor surface	0.84 m^2
Charge measurement (ToT)	5 bits

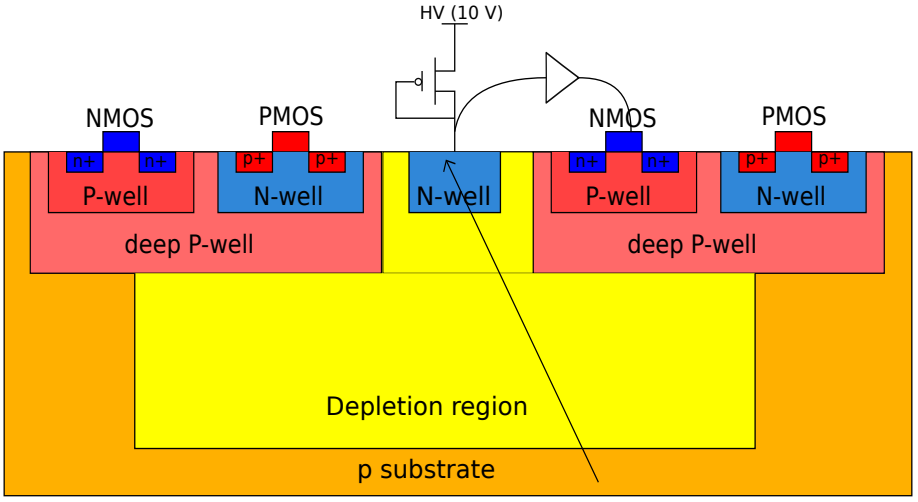


Figure 4.1: HVCMOS sensor with small fill factor

4.2 Design and Implementation

Figure 4.2 shows the layout of the HVMAPS25 ASIC. It consists of the following major blocks: pixel matrix, row control, column control, digital part and periphery.

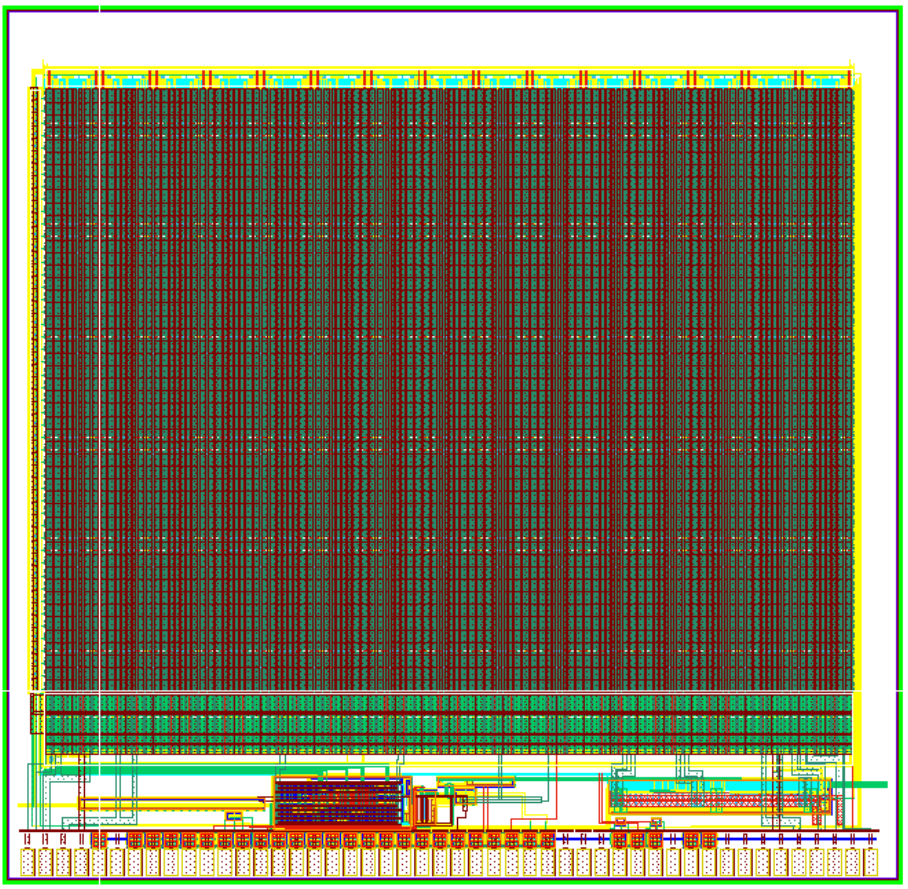


Figure 4.2: Layout of HVMAPS25

The pixel matrix is organized in 30 columns with 150 μm width. Each column has 48 pixel groups with 12 pixels and 70 μm height. Therefore, there are in total 17280 pixels for the entire ASIC.

The pixel size is 25 μm x 35 μm (height x width). Each pixel contains sensor diode, charge sensitive amplifier (CSA), comparator with threshold tune DAC, four bit RAM and hit buffer (75 μm x 4.2 μm) .

The hit buffer stores the time stamp (TS) at rising and falling comparator signal edge and generates hit address. The hit data is transferred to the end of column for data processing.

Additionally, 48 blocks of row control with shift register are placed at the left side of the matrix and each block has 6 bits (q<0:5>) for RAM write enable. Among of them, q4 and q5 in each block are also used for enable injection and enable amplifier output respectively. 30 blocks of column control are placed at the top of the matrix and each has 8 bits (q<0:7>). Q<0:5> are used for RAM inputs, q<6> for disable hit bus and the last bit is free.

Digital periphery, placed at the bottom of the chip, consist of two blocks, one is the synthesized digital part RCU (configuration register, TS generator, readout block and serializer), which is generated from Verilog Code. The other one is a full custom part with the PLL and analogue 2->1 serializer, which uses differential current mode logic instead of CMOS logic. Around 10 % of the whole chip is occupied by the periphery.

4.2.1 Pixel structure

12 pixel with its analogue pixel electronics, hit buffers (dig) and sensor diodes (dio), are arranged into one group.

The size of one group is 150 μm x 70 μm. The arrangement is shown in figure 4.3.

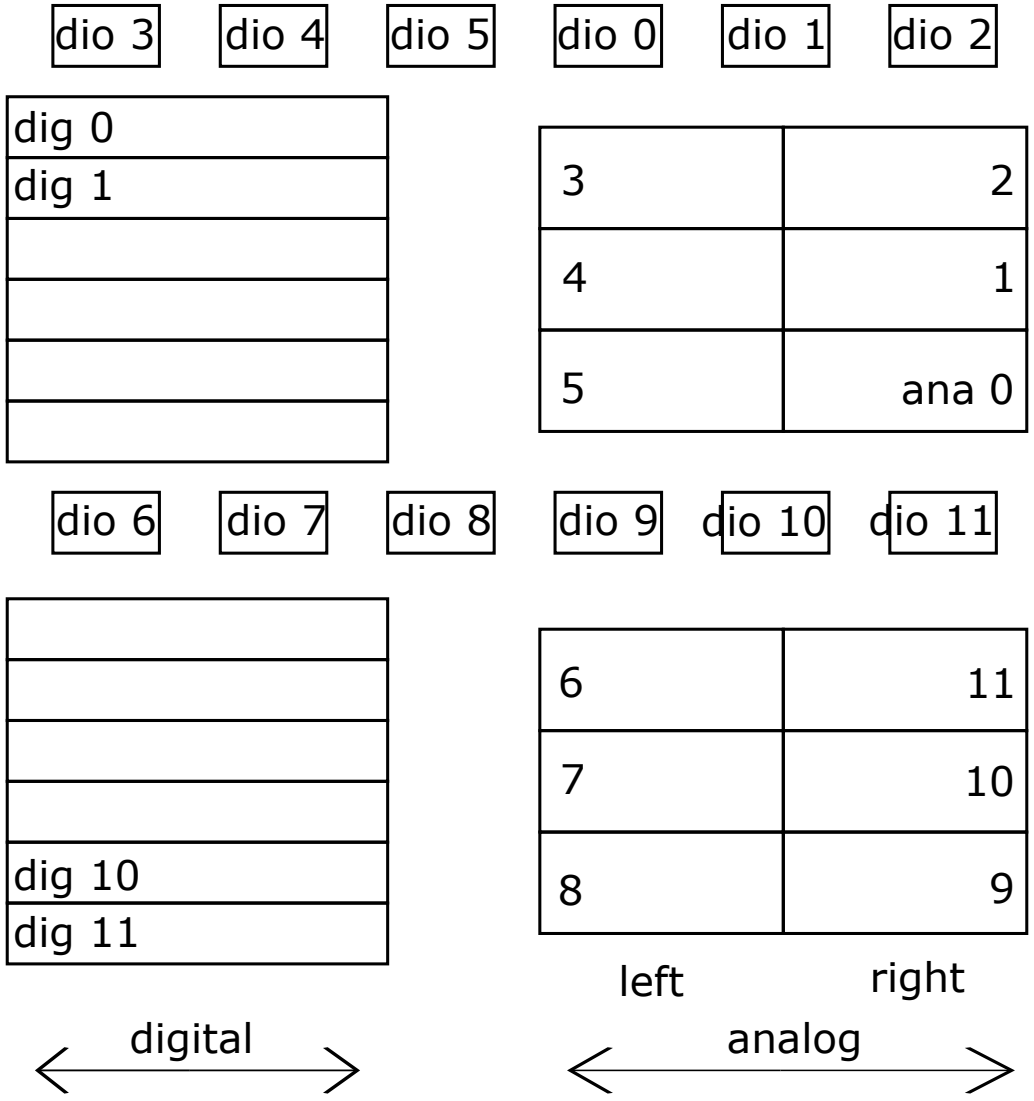


Figure 4.3: Pixel floor plan

In order to match the size of both parts and facilitate metal line connection in layout,

Six analog parts are placed left (pixel 3 to pixel 8) and the other 6 are placed right (pixel 0 to 2 and pixel 9 to 11). Their readout cells are numbered from top to bottom.

The size of analog pixel electronics is 37 μm x 7 μm and the size of pixel readout cell is 65 μm x 4 μm.

12 diodes are AC coupled to input of charge sensitive amplifier of each pixel. The value of the coupling capacitor C_c is 20.4 fF. Diodes 0 to 5 are placed at the top of a group and diodes 6 to 11 are in the middle of the group.

4.2.2 Analog pixel electronics

Figure 4.4 illustrates all the components in each pixel, which include injection circuit, CSA, feedback circuits, RC filter, 2 bits tune DAC with RAM and CMOS comparator.

The analog pixel electronics works in the same way as explained in CCPD chapter. When a particle hits a pixel, a small voltage drop is generated at the diode. The charge is amplified by CSA and a voltage pulse is produced at the output of the amplifier.

The input AmpIn is AC coupled through capacitance C_c to the HV sensor. The senor is biased by a PMOS to a voltage in the range 5 - 15V. The value of the feedback capacitor C_f is 1.42 fF. It connects to diode and output of the first preamplifier stage. The implementation of feedback capacitance is different than in CCPD. CCPD uses p+ diffussion in n-well as feedback capacitance, H25MAPS uses metal metal capacitor.

The amplifier output SFOut is fed to the comparator in the pixel.

Injection line is connected to injection capacitor (a few fF).

The signal outcomp is connected to the hit buffer for later signal processing. Comparator can be disabled by bit q<2> stored in RAM. The bits <0:1> are used to tune the threshold.

The row control bits Q<4> and Q<5> are used to select injection and outsf respectively. If we want to measure response of only one pixel we must disable all other pixels using bit q<2>.

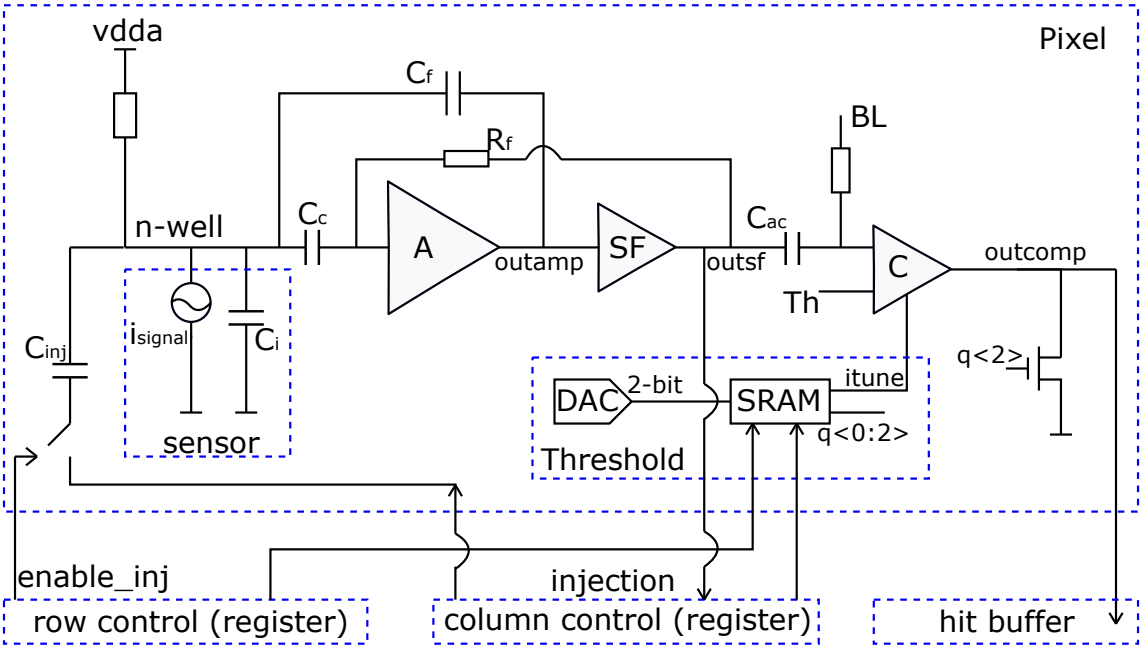


Figure 4.4: Pixel structure of HVMAPS25 ASIC

4.3 Measurements

For the measurements with H25MAPS, the same measurement setup as used for MPROC was used.

Figure 4.5 shows the components of experimental setup, their controlling and configuration parts (PC and FPGA), electrical supply (power supply and voltage supply), source (particle or test signal) and analysis tools (oscilloscope).

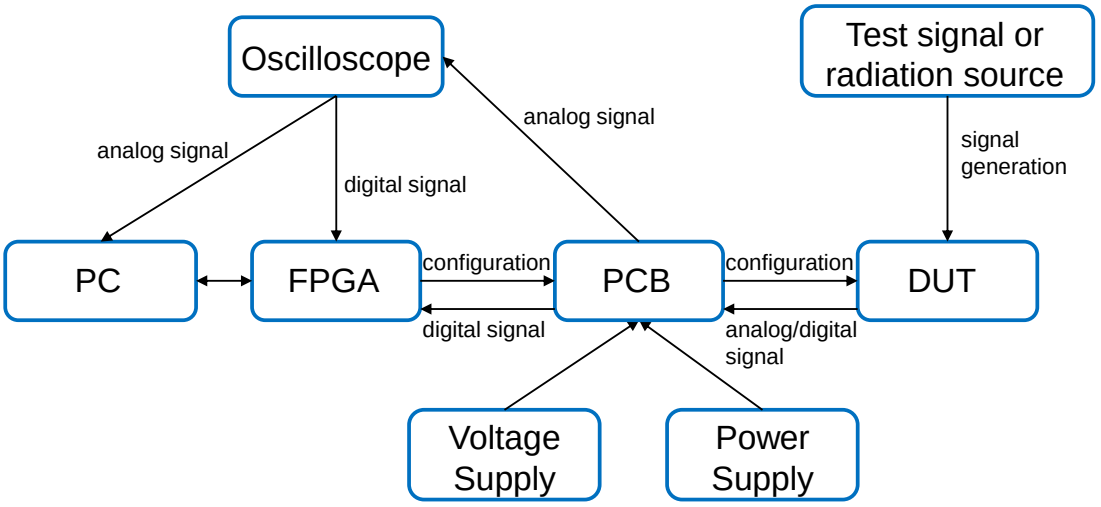


Figure 4.5: A typical setup for characterization of a device under test (DUT)

The relationship between different software is presented in figure 4.6.

In addition to Cadence Virtuoso (for chip design before production), Altium Designer Environment has been applied for designing carrier board [58].

Qt Creator has been used to design software with GUI for chip configuration and readout.

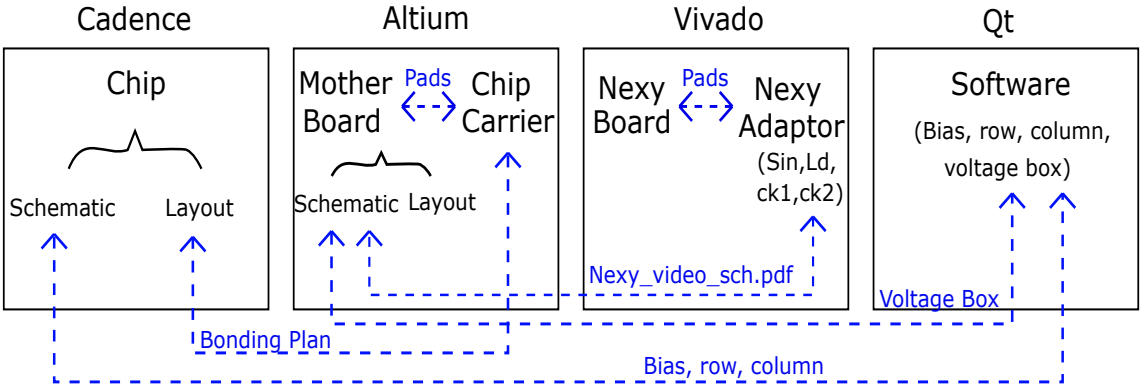


Figure 4.6: Components of the test system and development tools used to design

4.3.1 PCB Desgin

Within this work the chip carried PCB has been designed. An universal carrier PCB for both HVMAPS25 and MPROC chips was designed by Altium Designer.

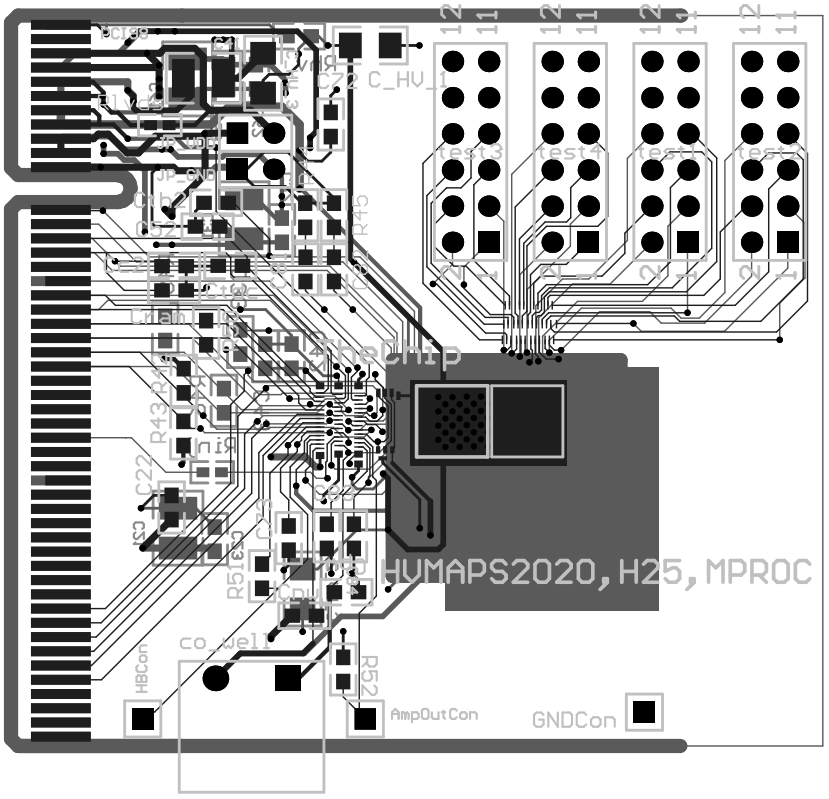


Figure 4.7: PCB layout for both MPROC and HVMAPS25 chips

Figure 4.7 presents the PCB layout.

It is a four layer PCB. The top and bottom signal layer are complemented by power and ground planes.

The ASIC is mounted on the middle of the board and wire bonding to the pads, which are placed at the middle of the PCB.

On the left side of the board, the connector for the GECCO board is located. Next to it, terminations for the differential siganl lines are placed.

All signals are routed to a PCI connector that fits on the GECCO interface board.

Several signals are located on the interface board:

- the configuration lines for the DACs on the PCB (data, clock, load)
- the analogue and digital injection signals
- the hitbus output
- the data lines for the digital readout (fast and slow clock, serial outputs)
- differential inputs and outputs (CkRef, Synreste, CkExt, Dataout)

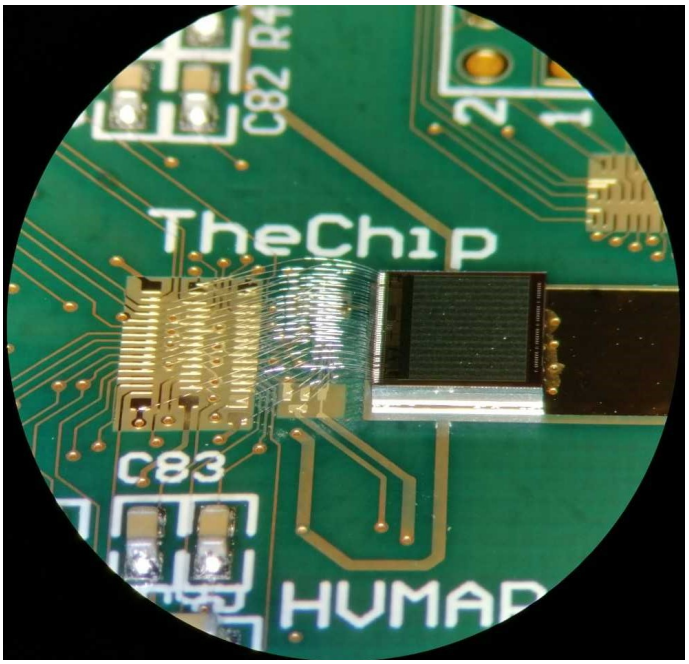


Figure 4.8: Wire bonding

4.3.2 Measurement Results

This part describes some measurement results of the HVMAPS25 chip. They include: measurements of the amplitude and pulse width, threshold scans and trimming and Fe55 radioactive source measurements.

4.3.2.1 Measurement with injection circuit

The amplitude of the signal can be measured in two ways. 1) Amplifier output can be measured directly via test pad. 2) The time over threshold is digitized in hit buffer and is readout using digital part.

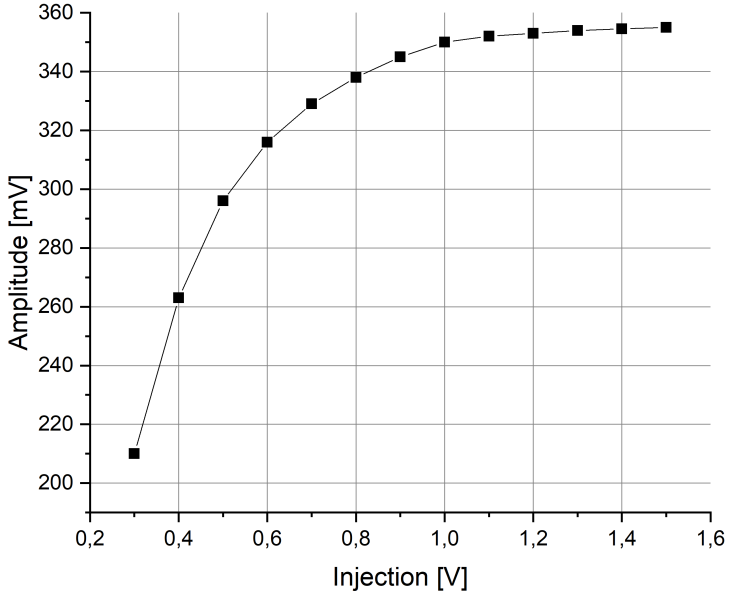


Figure 4.9: Amplitude of amplifier output versus injection voltage (from 7029 e to 39829 e) (analogue signal)

Figures 4.9 and 4.10 illustrate the amplitude and width pulse change versus different injection values. The amplitude increases steeply from 0 to the 0.6 V and then it saturates at 1.0 V injection value. The pulse width of HVMAPS25 ASIC is in the range between 2000 μs to 2400 μs. It growths linearly from beginning to the around 1.2 V injection value. After that it saturates.

Threshold Scan and trimming

The threshold and the noise can be measured by threshold scan. The scan is performed in the following way: For each data point injections are sent into the pixel diode. The pulses crossing the set threshold of the comparator are counted. The efficiency is given by:

$$E = \frac{detectedsignal}{injections} \tag{4.1}$$

The efficiency versus injected charge is plotted. If we had a system without noise, the resulted efficiency would be a step function. For injected charge below threshold efficiency would be zero and for the injected charge above threshold the efficiency would be 1. Since we have noise, the resulting efficiency vs injection line has the form of the error function.

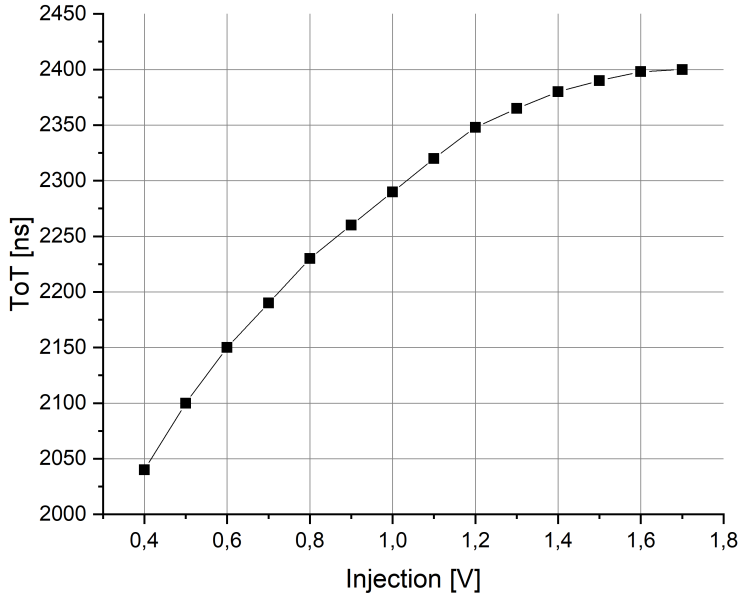


Figure 4.10: ToT versus injection voltage (digital signal)

The input referred threshold corresponds to the injection leading to the efficiency of 50 % and the noise to sigma of the error function fit.

The threshold dispersion is caused mainly by the gain mismatch of the CSA and the mismatch between the thresholds of the input transistors of the discriminator. The threshold dispersion can be alleviated using the threshold tune DACs.

Two bit DACs can be used to adjust the threshold of each comparator. The local threshold is the sum of the externally set threshold and the DAC value.

The tune method starts by setting all TDAC values to maximum. Threshold scan is performed with the aim to find the minimum threshold. This minimum threshold is chosen as the target value. After that for every pixel, TDAC is decreased until the closes value to the target is found.

The threshold dispersion of before and after trimming are listed in table 4.2.

Table 4.2: Threshold dispersion

	Threshold mean value	Noise value
Before trimming	110.8 mV (2577 e)	21.5 mV (503 e)
After trimming	69.7 mV (1633 e)	9.9 mV (232 e)

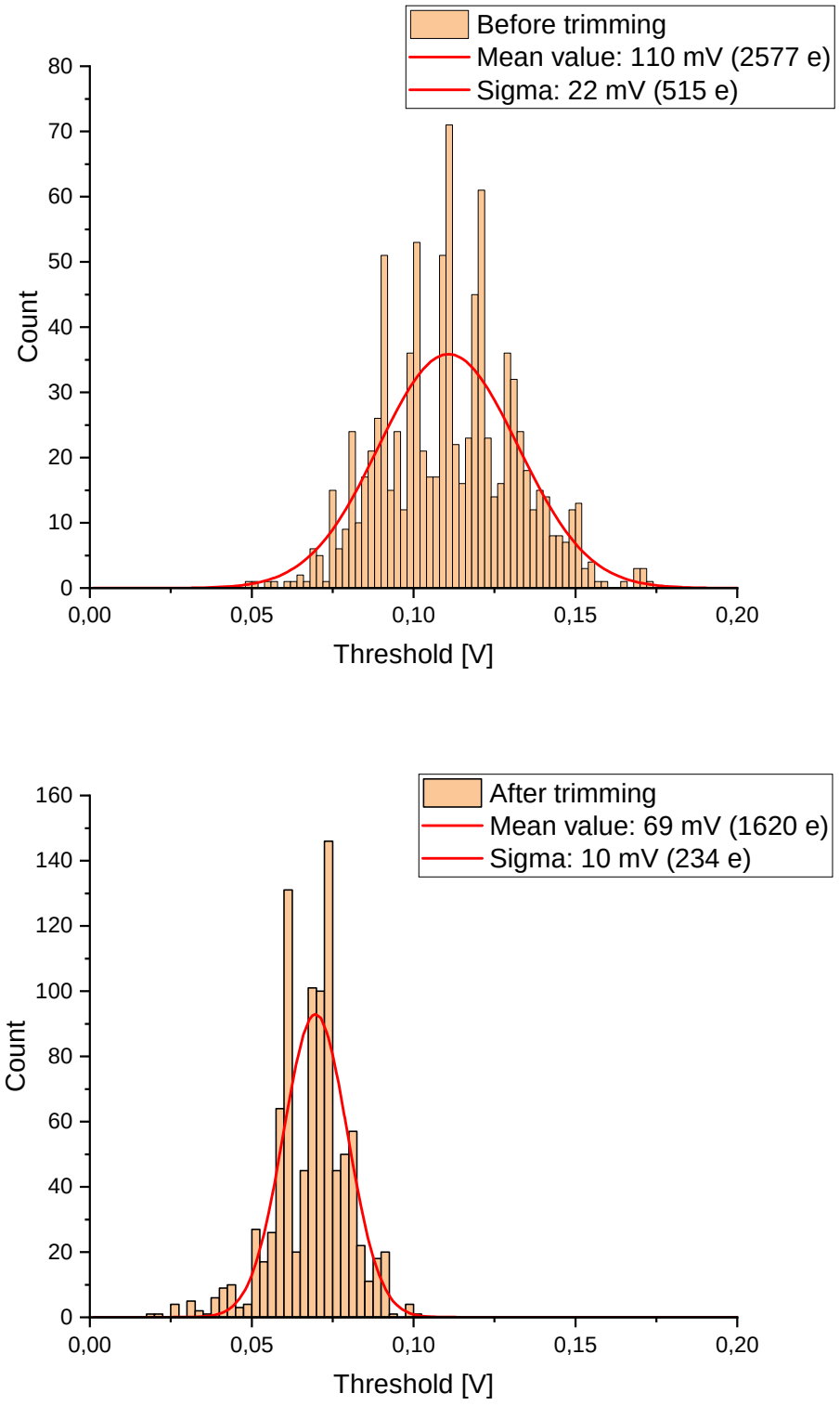


Figure 4.11: Input referred threshold dispersion before trimming versus after trimming

4.3.2.2 Measurement with Fe55 radioactive source

HVMAPS25 AISC has also been tested using Fe55 radioactive source. This source is suitable for calibration because it generates photons of know energies (5.9 keV and 6.1 keV) that produce charge signals of 1640 e and 1695 e. One measurement result is presented in figure 4.12. The maximum value of the amplifier output has been histogrammed. The average signal is 55 mV. The same value could be achieved when with injection pulse of 0.07 V is used. Figure 4.13 shows an amplifier output waveform response to Fe55 photons.

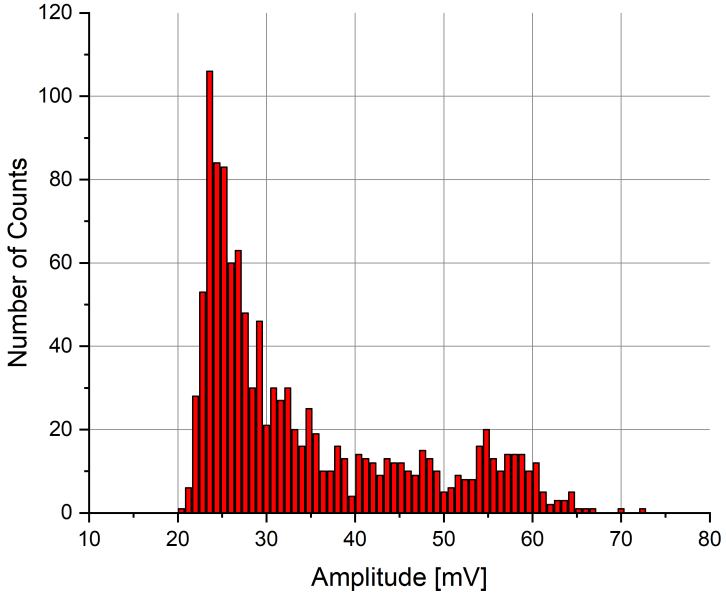


Figure 4.12: Histogram of measured signal amplitudes when chip is irradiated with Fe55

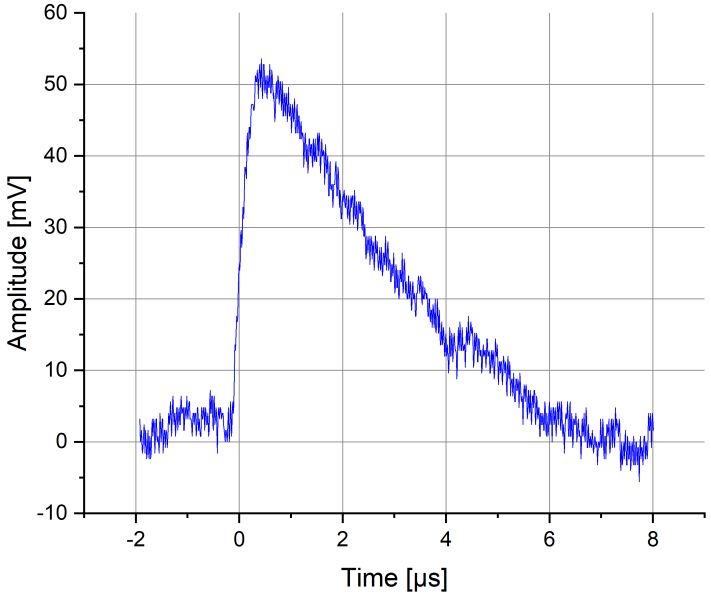


Figure 4.13: Amplifier output waveform response to Fe55 photons

5 CLIC

5.1 Introduction

The last part of my work is related to the monolithic sensors implemented in H2020 engineering run in 180 nm HVCMOS technology using 200 Ωcm substrate. These chips could be applied in CLIC, PANDA and CEPC experiments for particle trajectory reconstruction, energy and momentum measurements and identification of charged particles.

Different pixel sizes, amplifier types and comparator types were employed. The pixels are in following variants:

- Pixels width: 25 μm (CLIC, CEPC), 50 μm-100 μm (PANDA)
- Comparator types: NMOS (CLIC), CMOS (CLIC, PANDA) with deep p-well and differential (distributed) (PANDA and CEPC)
- Amplifier types: PMOS (CLIC, PANDA), NMOS (CLIC, CEPC) and CMOS (CLIC)

The table 5.1 shows the possibilities. The following section introduces the structure of the comparator and amplifier types. Furthermore, the design and structure of PANDA ASIC with high dynamic range has also been presented.

Table 5.1: Different variants of CLIC/PANDA ASICs

	NMOS Comp	CMOS Comp	Distributed Comp
PMOS Amp		V2 (CLIC) V2 hidr (PANDA)	V3 (CLIC) V3 hidr (PANDA)
NMOS Amp	V1 (CLIC)	V2 (CLIC)	V3 (CEPC)
CMOS Amp	V1 (CLIC)		

CLIC sensor: There are 29 columns in each CLIC chip. The size of all pixels is the same, 25 μm x 165 μm. Different amplifier types were implemented e.g. columns 0 to 13 use PMOS and columns 14 to 28 NMOS comparator. There are three CLIC sensor types v1, v2 and v3. They use different comparator types according to table 5.1.

PANDA sensor: There are two comparator types and two pixel sizes (50 μm x 165 μm and 100 μm x 165 μm). The novelty of the design is that each pixel has two comparators and

readout channels, which can measure signals with two threshold values. There are in total 16 variants pixels in the whole matrix.

5.2 CLIC Experiment

The Compact LInear Collider (CLIC) is a proposal for a future high-luminosity, high-energy linear lepton collider. The accelerator will achieve three different centre-of-mass energies due to its staged design: 380 GeV, 1.5 TeV and 3 TeV [68]. The generated electron-positron collisions will provide a clean, low-radiation environment for the inner detectors. However, physics-driven performance targets, the CLIC beam structure, and occupancies from beam-induced backgrounds place challenging requirements on detector technologies for this region [69].

Table 5.2 demonstrates the specification for Tracking Detector of CLIC [70].

Table 5.2: Tracking Detector of CLIC

Technology	TSI 180 nm HVCMOS
Pixel Size	25 μm x 165 μm
Particle of detector	charged particles
Radiation hardness	
Energy Resolution	
spatial resolution	7 μm (transversal)
Time Resolution	5 ns
Data Rate	
Dynamic range	
Power consumption	< 150 mW/cm^2
Hit efficiency	99.7 - 99.9 %
Material budget per payer	1 - 2% X_0
Sensor surface	137 m^2
Maximal granularity	1 - 10 mm pixel size (long)

5.2.1 Design and Implementation

5.2.1.1 Comparator

For CLIC sensors we have implemented three types of comparator.

CMOS Comparator

The schematics of CMOS comparator is shown in figure 5.1. It is the standard differential transconductance amplifier with two stages. The PMOS transistors are isolated from the sensor deep n-well using the deep p-well.

The advantages of CMOS comparator are: low current consumption, CMOS output and radiation tolerance.

NMOS Comparator

NMOS-based comparator is normally preferred in order to avoid crosstalk to the deep n-well used as sensor. The schematics of NMOS-based comparator is shown in figure 5.2. It is based on three differential stages with diode connected NMOS transistors Tload1 and Tload2 as active load. The gain of one stage is defined by the ratio of the transconductances of the load- (Tload) and input transistors (Tin). Three stages are used to assure sufficient gain.

The disadvantages of NMOS-based comparator higher power consumption, larger area and less radiation hardness.

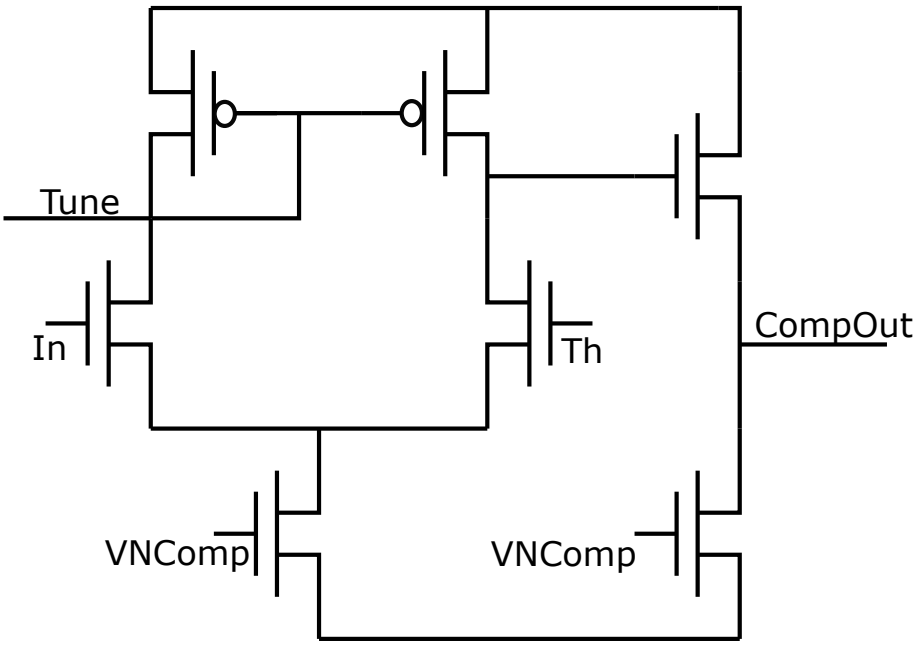


Figure 5.1: CMOS comparator

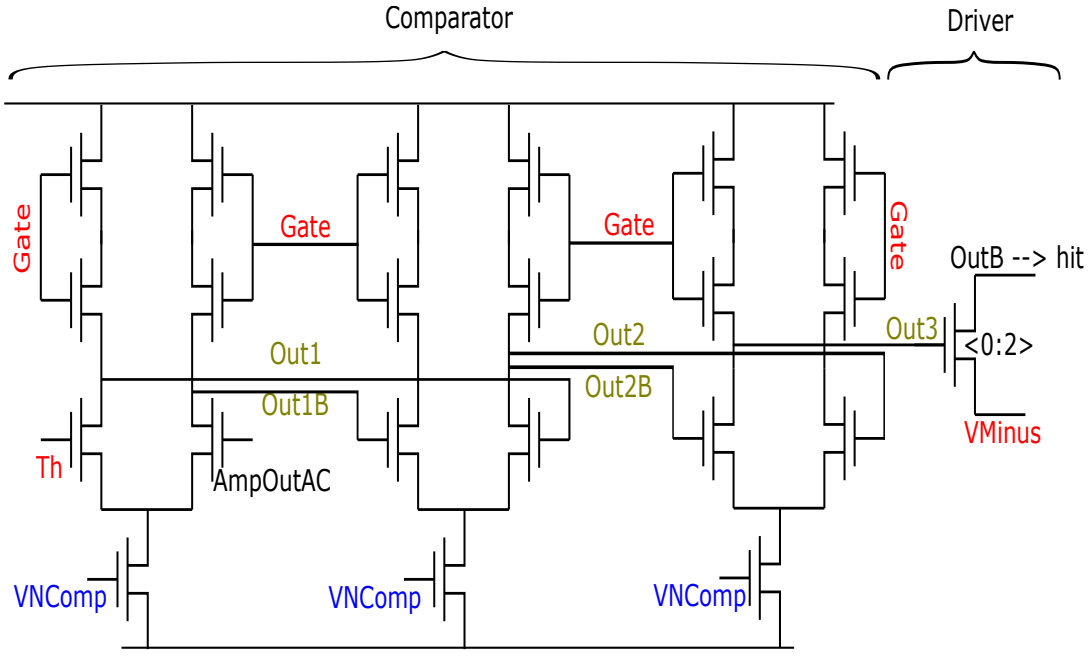


Figure 5.2: NMOS-based comparator

Distributed Comparator

This comparator type is similar as CMOS comparator. The difference is that the PMOS part of the comparator is placed in hit buffer, instead of pixel. In this way, a small pixel size could be ensured and there is no need for deep p-well.

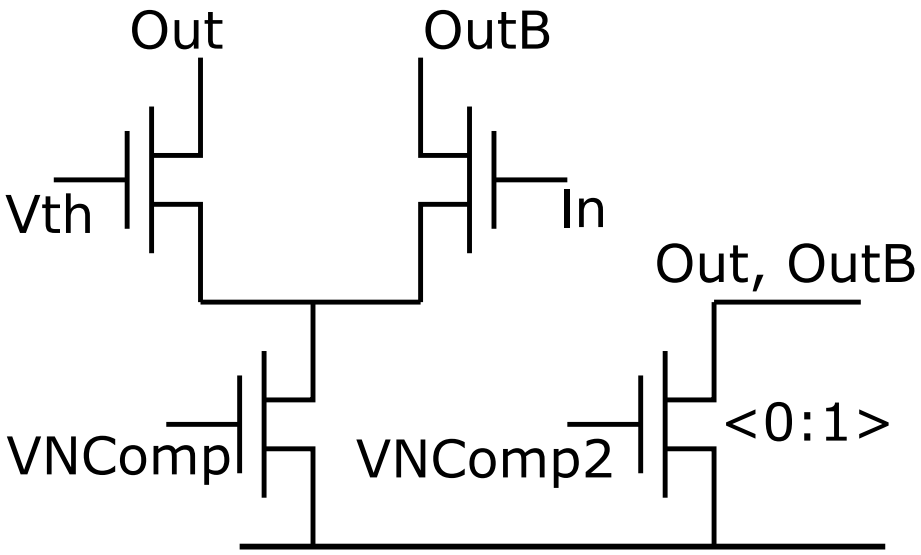


Figure 5.3: Distributed comparator

5.2.1.2 Charge sensitive amplifier

A general charge sensitive amplifier is presented in figure 5.4. Its structure is similar as used in CCPD chip. It consists of bias block, folded cascode amplifier, source follower, feedback block and a high pass filter.

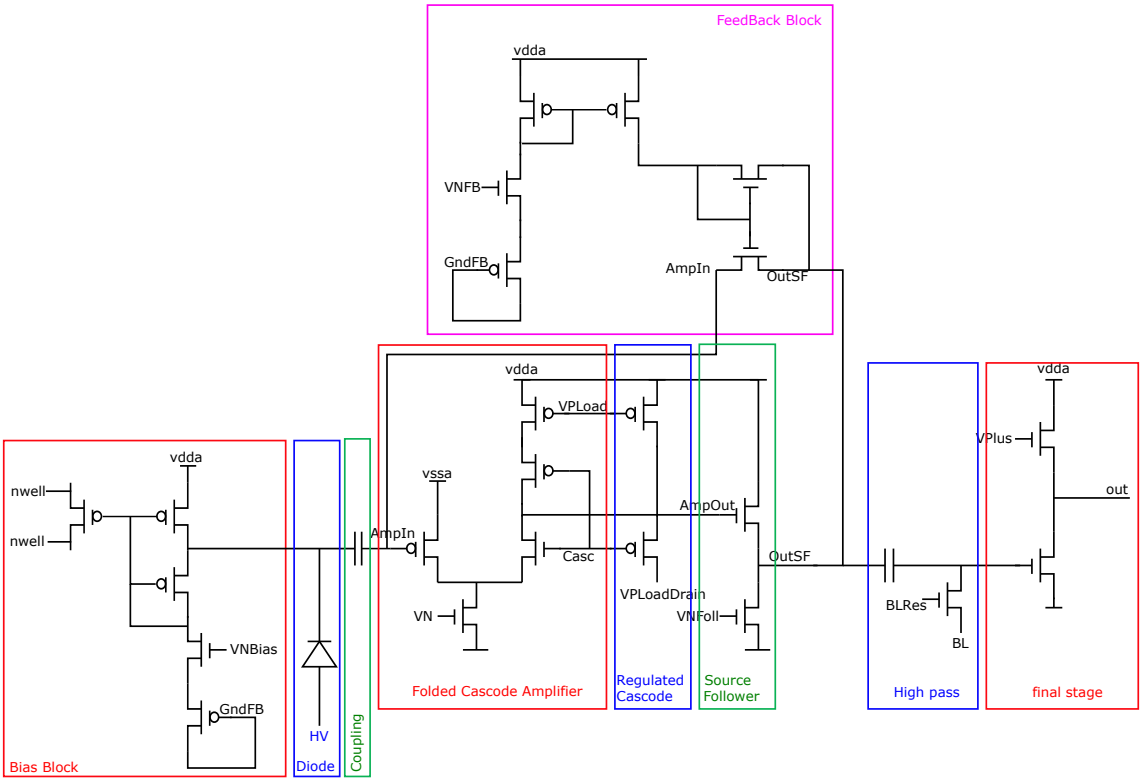


Figure 5.4: Transistor level of Charge Sensitive Amplifier with PMOS input transistor

PMOS Amplifier

Normally PMOS is chosen as the input transistor, because of its smaller 1/f noise coefficient as compared with NMOS device.

NMOS Amplifier and CMOS amplifier

Figure 5.5 presents the NMOS and CMOS amplifier used in CLIC ASICs. Only the highlighted input transistors are different. The open loop gain is proportional to transconductance, respectively the mobility of charge carriers in a transistor. Usually, the mobility of electrons in NMOS transistor is 2 times larger than mobility of holes in PMOS. Hence, NMOS amplifier has larger open loop gain compared with PMOS amplifier. CMOS amplifier has even larger equivalent transconductance, which is the sum of NMOS and PMOS contributions.

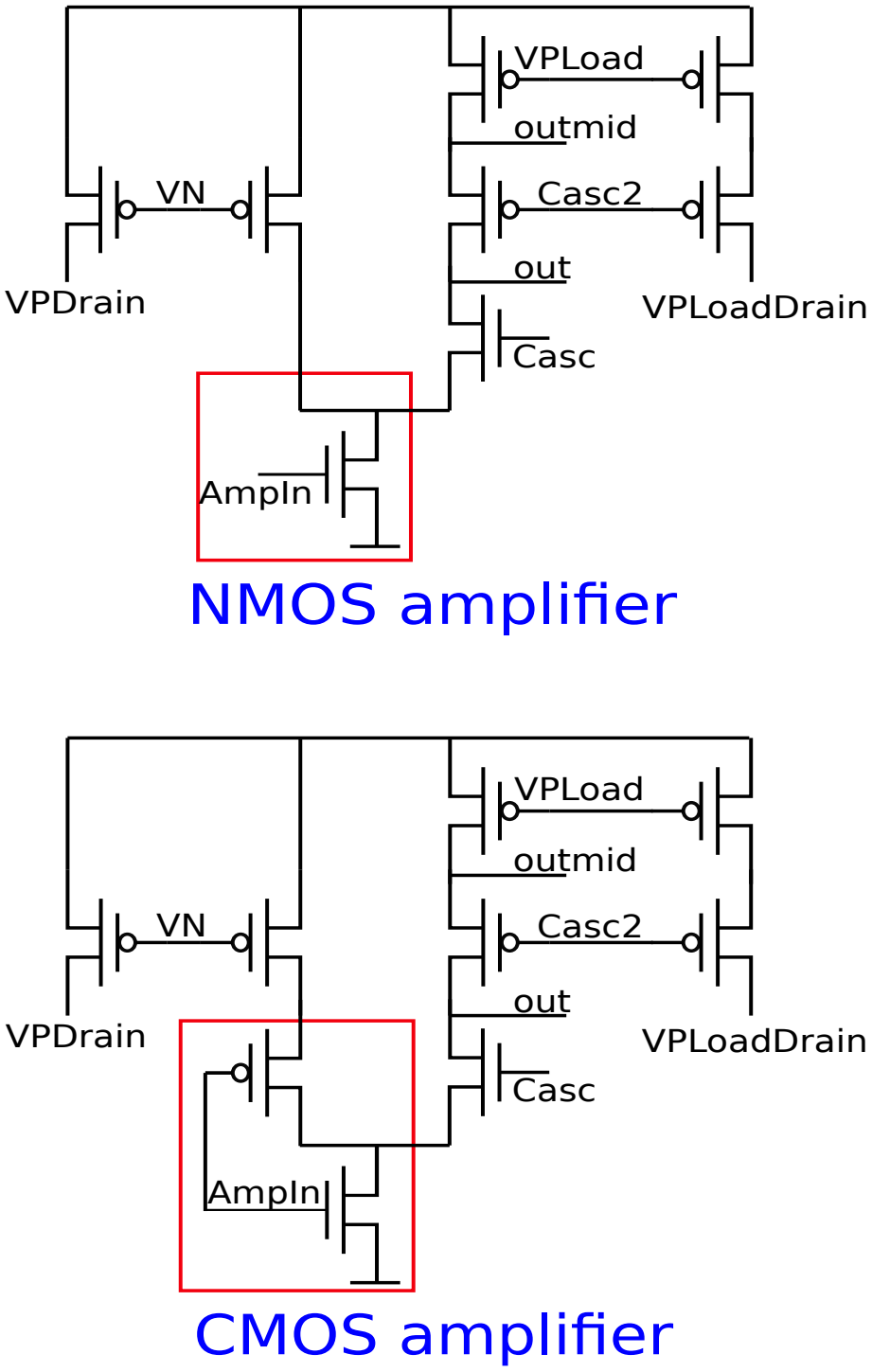


Figure 5.5: NMOS and CMOS amplifier

5.3 PANDA Experiment

The PANDA Collaboration intends to do basic physics research on various topics around the weak and strong forces, exotic states of matter and the structure of hadrons. In order to gather all the necessary information from the antiproton-proton collisions a versatile detector will be build being able to provide precise trajectory reconstruction, energy and momentum measurements and very efficient identification of charged particles [66].

Table 5.3 describes the specifications for Micro-Vertex Detector for PANDA [67]. Especially important is the high time resolution and the large dynamic range. The time resolution is required in order to assign the particle signals to one track and the high dynamic range is important for particle identification because different particles have different average energy loss.

Table 5.3: Specifications for Micro-Vertex Detector for PANDA

Technology	TSI 180 nm HVCMOS
Pixel Size (test chip)	50 μm x 165 μm and 100 μm x 165 μm
Pixel Size specification	80 μm x 80 μm
Particle of detector	charged particles
Radiation hardness	
Energy Resolution	
Charge measurement	12 bits and linear over 7 bits
Time Resolution	1ns
Data Rate	
Dynamic range	1-100 $(dE/dx)_{mip}$ (in our case e.g. 1000 - 100000e)
Power consumption	
Efficiency	

5.3.1 The structure of PANDA ASIC

Figure 5.6 presents the structure of the PANDA ASIC with 4.8 mm x 4.2 mm chip size. It consist of pixel matrix, configuration bits, hit buffers, EoC logic and chip periphery.

The hit buffers of PANDA and CLIC chips have the similar structure as hit buffers of MPROC. They also contain the time to digital converter.

There are in total 29 columns in pixel matrix, which is divided into four variants.

1) From column 0 to column 7 is the first variant. It uses the standard CSA, which means with single source, linear cascade, 4 μm input transistor.

2) In this variant, the width of input transistor is 8 μm instead of 4 μm

3) Doubled load transistors are applied in columns 16 to 23 (TP8), in order to enlarge the load current and decrease the rising time of the signal.

4) The last variant uses circular NMOS transistor (column 24 to column 28) for radiation hardness.

Furthermore, the pixels in each column have two sizes. 50 μm x 165 μm pixels are placed in row 0 to row 61 and the pixels with 100 μm x 165 μm size are placed in row 62 to 123.

Each pixel has two comparators and readout channels: fast and slow. In the case of the fast channel, the output of the CSA is connected direct to comparator. In the case of slow channel, a low pass filter is placed between CSA and comparator, in order to enlarge the falling time of the signal.

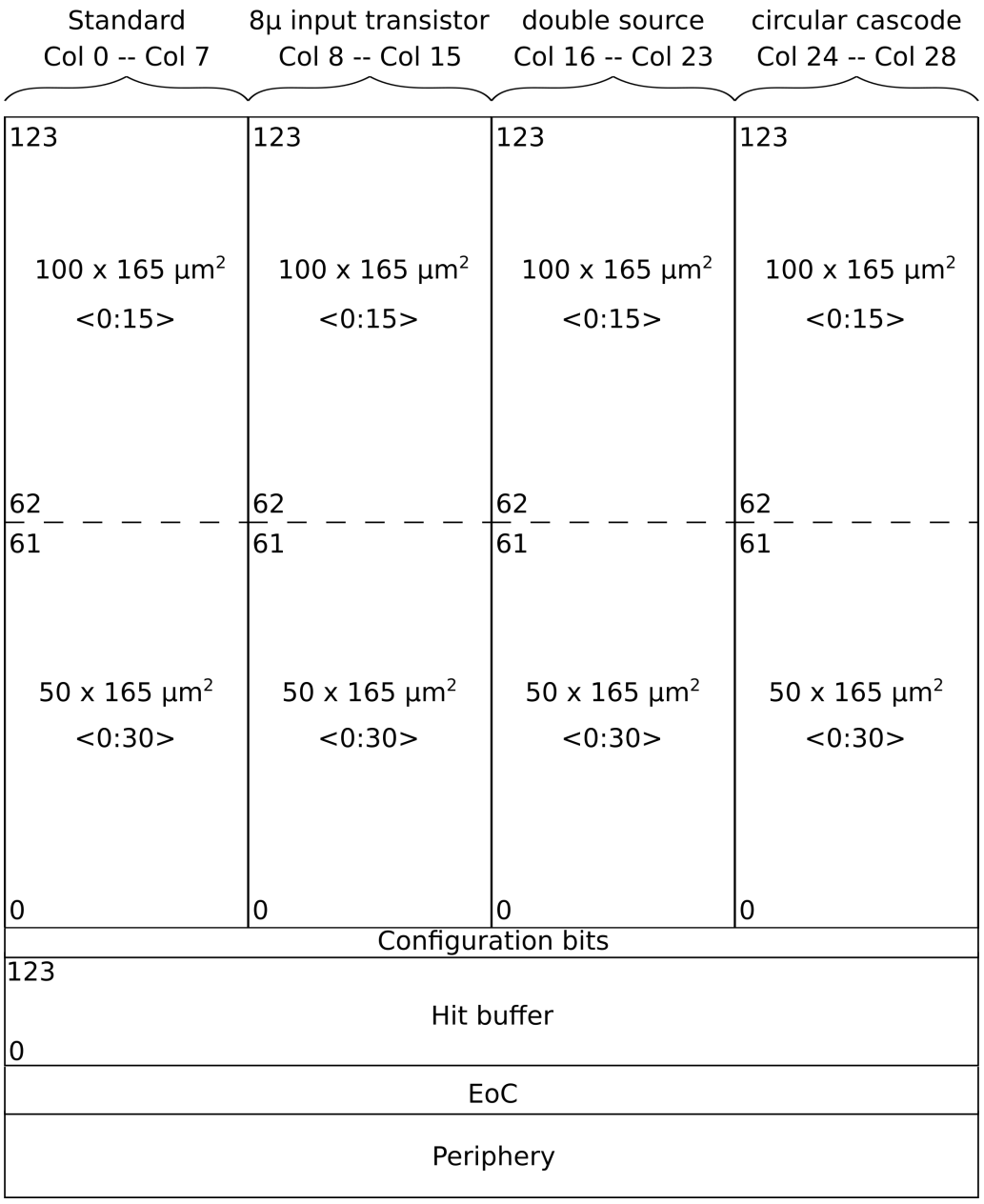


Figure 5.6: The structure of CLIC ASIC

The design of pixel electronics is described in figure 5.7.

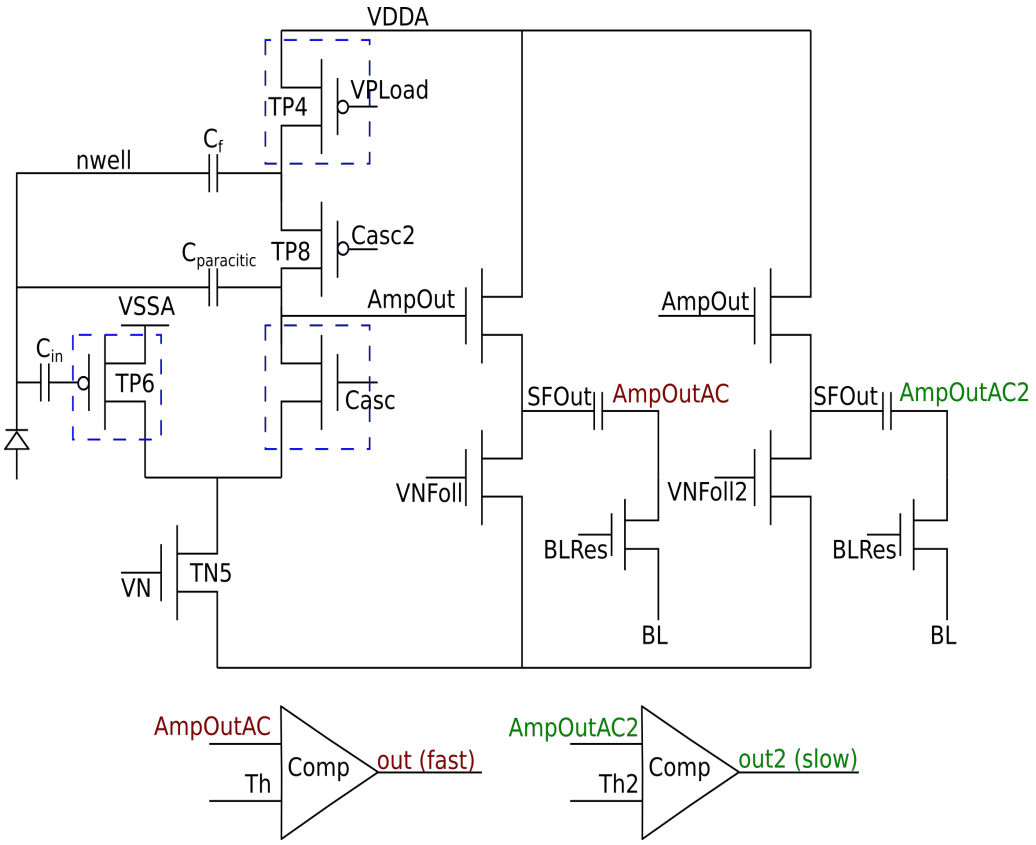


Figure 5.7: Schematic of pixel electronics of CLIC

The bias current of the second source follower (VNFoll2) is smaller than of the first source follower (VNFoll), and the falling time of AmpOutAC2 takes longer than the falling time of AmpOutAC. This increases SNR when ToT of AmpOutAC2 is measured.

The PMOS transistor TP8 is added compared to the standard CSA. The higher potential of Casc2, the higher amplitude can be achieved. The CSA is designed to have larger gain when the signals are low and smaller gain when signals are high. For low signals the source voltage of TP8 is nearly constant and capacitance Cf does not introduce feedback. The gain is 1/Cparasitic. For larger signals at AmpOut than Casc2 + Vth, the source voltage of TP8 follows the AmpOut and the gain is 1/(Cf + Cparasitics).

5.4 Measurement Overview

We have done following measurements:

- Measurements of amplifier output with oscilloscope.
- Measurements of response to Fe-55 and to injections.
- Calibration: Comparing the average peaking amplitude as response to Fe55 and as response to injections, table 5.4, the injection capacitance can be calculated.
- Threshold scan measurement. Here we measure the response probability of comparator versus injected charge for a group of pixels. We use digital readout. The error function (s-curve) can be fit to data (probability versus injected charge). The 50% value of the fit is the input referred threshold. The sigma of the fit is the input referred noise. Mean and sigma of the threshold dispersion can be calculated.
- Pulse width (ToT) measurement. We measured the time over threshold using digital readout for different injected signals. We can calculate SNR as ToT difference for small and large signal divided by sigma value of ToT for large signal.
- Time walk (TW) measurement. We measured the threshold crossing time using digital readout for different injected signals. Due to time walk effect the measured time is larger (comparator fires later) for smaller signals. We determine time walk as difference of measured time for small and large signal.
- Time walk correction can be done when we measure both TW and ToT for one pixel. These measurements are shown in the chapter about PANDA chip.

Table 5.4: Source amplitude correspond to input injection voltages

Chip	**Injection voltages**	**Source Amplitude**
MPROC (Chapter 2)	500 mV	120 mV
HVMAPS25 (Chapter 4)	70 mV	55 mV
PANDA (high dynamic range)	48 mV	42.5 mV
CLIC v1/v2	300 mV	100 mV

5.5 Measurement results of PANDA ASIC (v3 high dymanic range)

The PANDA ASIC has been tested by test signals (injection circuit) and Fe55 radioactive source.

5.5.1 Measurement with Fe55 radioactive source

The Fe55 source is used for calibration because it generates photons of know energies (5.9 keV and 6.1 keV) that produce charge signals of 1640 e and 1695 e. A histogram of amplitudes is presented in figure 5.8. The Gaussian fit has a mean value of 42.54 mV.

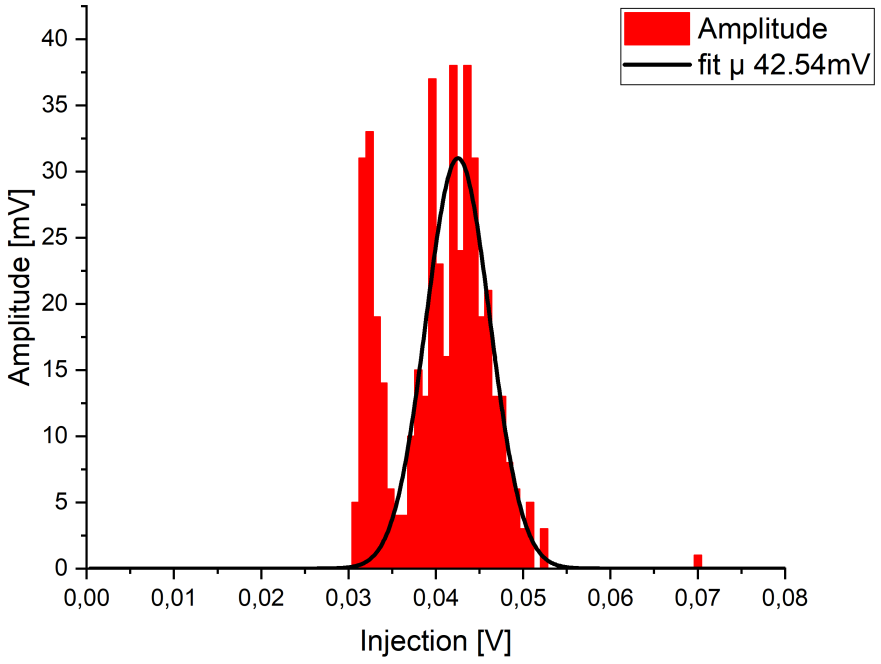


Figure 5.8: Histogramm of measured signal amplitudes when chip is irradiated with Fe55

5.5.2 Amplitude and pulse width calibration with injection circuits

The injection circuit can be also used to generate the signals. The amplifier output can be measured directly via test pad and the waveform captured with the oscilloscope. In the case of digital measurements, the time over threshold is digitized in hit buffer and is readout using digital part.

Figure 5.9 and 5.10 illustrate the amplitude and ToT versus different injection values. The amplitude increases steeply from injections smaller than 0.6 V and slowly until 1.2 V. This is the result of the variable gain that was explained above. From figure 5.9, we can see that injection of about 48mV generates signal amplitude similar as Fe55. This allows us to calibrate injections and express them in electrons. The x-axis in figure 5.10 is expressed in electrons.

As mentioned, there are two channels inside of each pixel, slow and fast. The pulse widths are different.

The fast channel uses source follower with larger bias current and the slow channel the source follower with smaller bias current.

Therefore, the pulse width of fast signal (red) is shorter than the pulse width of slow signal (black).

Figure 5.11 shows the sigma values (RMS) of the pulse widths. The sigma value for slow channel is smaller, leading to sigificantly larger SNR.

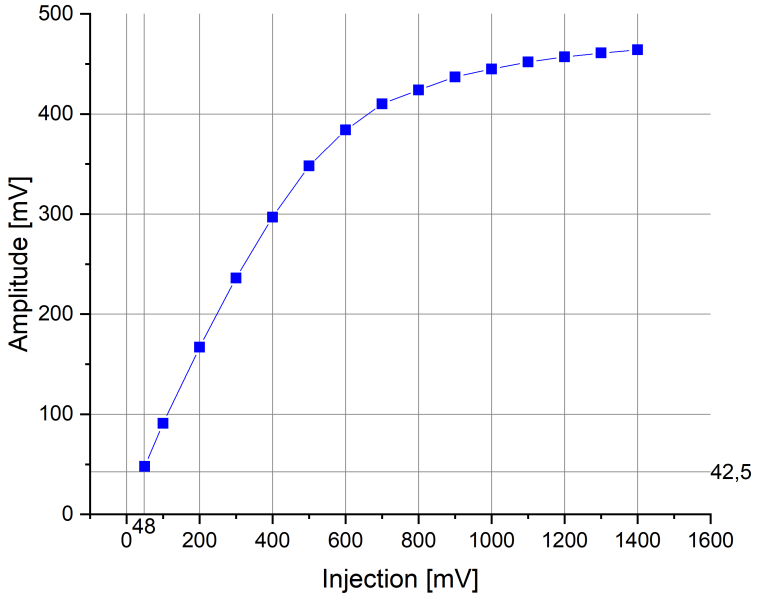


Figure 5.9: Amplitude of amplifier output versus injection voltage (from 1708 e to 47833 e)

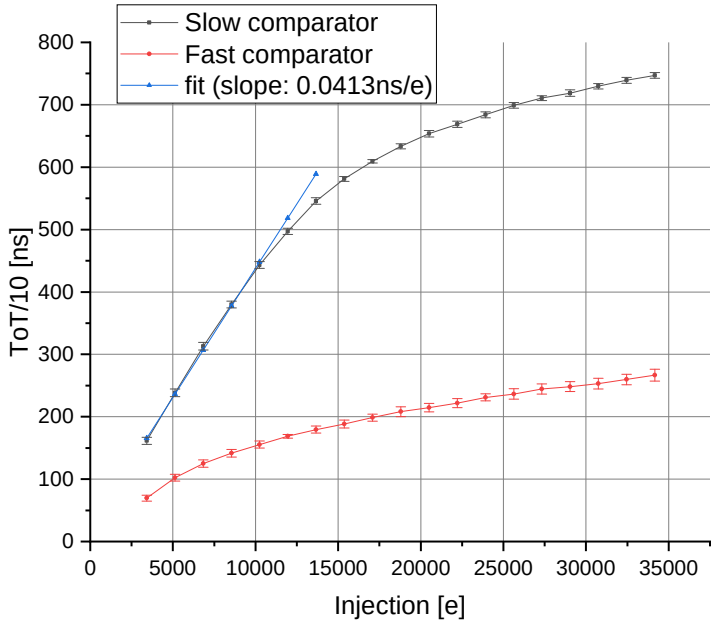


Figure 5.10: Pulse width of the slow and fast comparator versus injected amplitude (from injection = 50 mV and clock period = 10 ns)

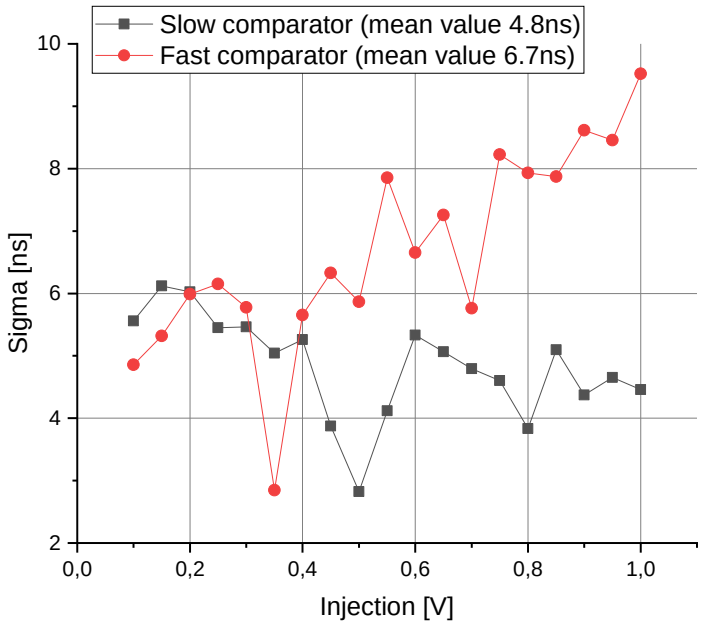


Figure 5.11: Sigma of calculated pulse width versus injection amplitude

The signal in figure 5.9 has been varied from about 2000 e to 35000 e. The maximum signal was limited by supply voltage and the sensor could measure also larger signals with linear response (without saturation).

The average ToT noise is about 4.8 ns for slow comparator. The gain for small signals can be obtained by fit and it is 0.0413 ns/e. If we divide the TOT by gain we obtain the noise in electrons as 116 e. The ratio of maximum measured signal (35000 e) and noise in e is abut 300.

This is promising result and shows that particle signals in the specified range 1 - 100 MIPs can be measured. We can vary MIP signal by adjusting depletion voltage. We can set MIP to be 10x noise 1000 e.

5.5.3 Time walk measurement versus injection value

For PANDA the time resolution of 1ns is specified. Time resolution is normaly limited by the time walk effect, illustrated in figure 5.12. The bigger the signal, the earlier comparator fires.

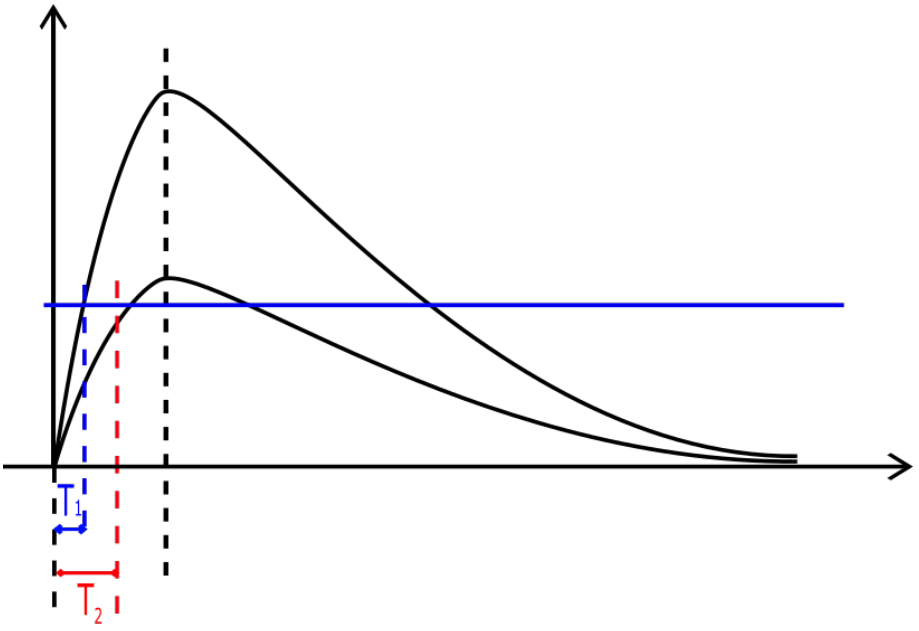


Figure 5.12: Time walk definition

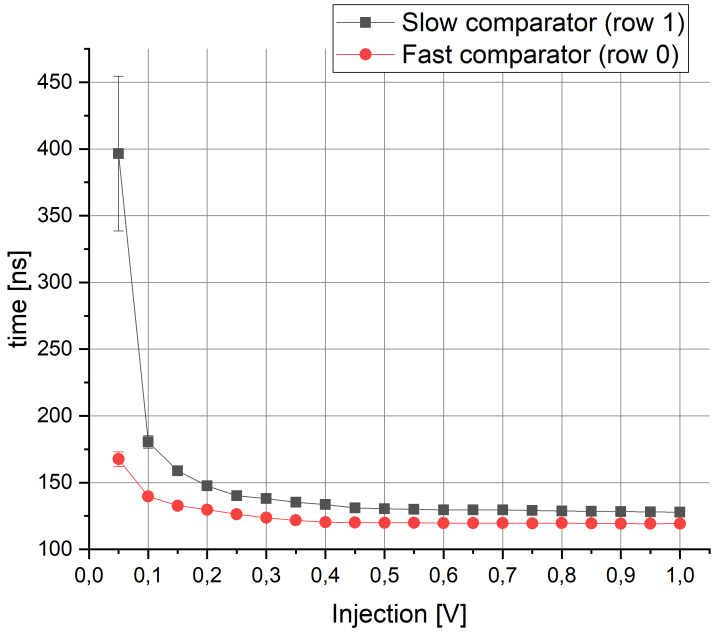


Figure 5.13: Measured comparator response time versus different injections (clock period = 10 ns)

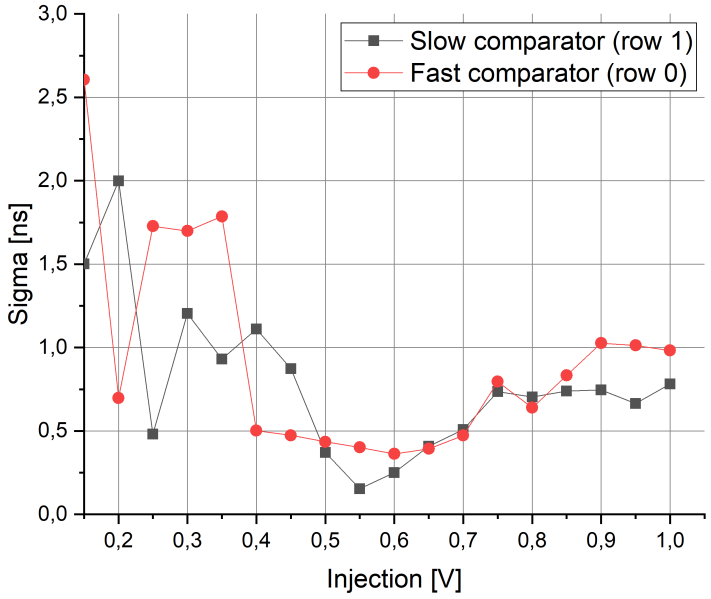


Figure 5.14: Sigma of the calculated time versus injection amplitude

Figure 5.13 shows measured response time for different signal amplitudes. The time walk of the fast comparator (red) is smaller than the time walk of the slow comparator (black) since its rising time is shorter. For small signals, the time walk for both fast and slow comparators are large.

The sigma value of the measured response time is shown in figure 5.14.

5.5.4 TDAC versus FPGA delay

As mentioned, PANDA chip also implements the TDC circuit explained in MPROC chapter.

Figure 5.15 shows the measured time stamp TS3 generated by TDAC versus delay of the injection pulse (setting in FPGA).

This result is as expected, as shown in figure 2.22.

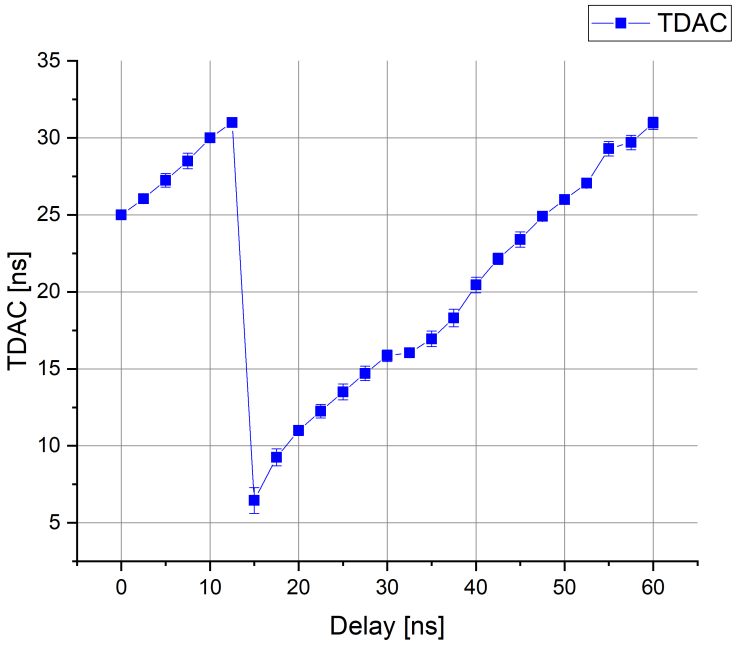


Figure 5.15: Measured time stamp TS3 generated by TDAC versus delay of the injection pulse (setting in FPGA)

5.5.5 Time versus Delay

The TS3 values from figure 5.15 can be used to calculate the response time. The result has been shown in figure 5.16.

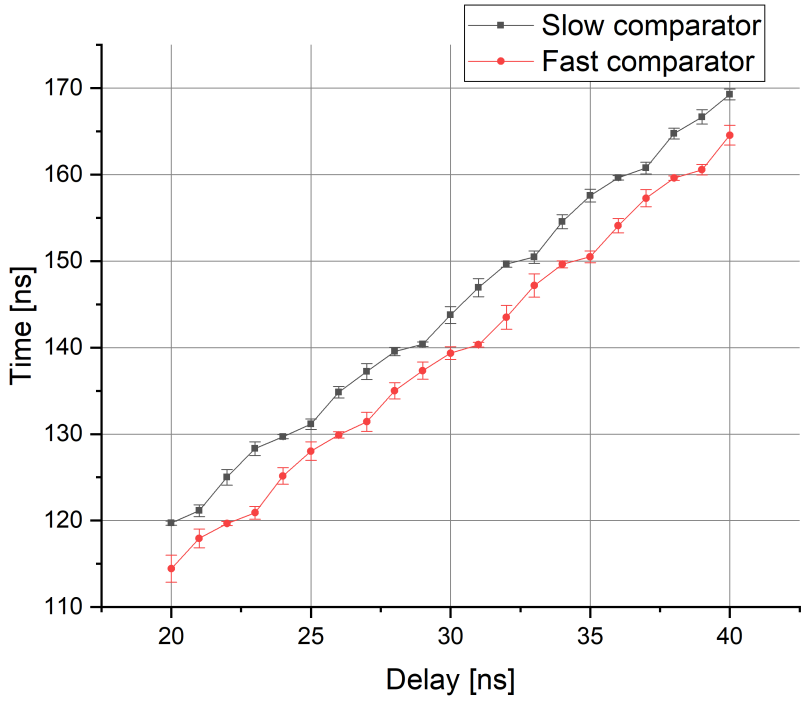


Figure 5.16: Calculated comparator response time versus injection delay (setting in FPGA) (clock period = 10 ns)

5.5.6 ToT and TDAC calibration

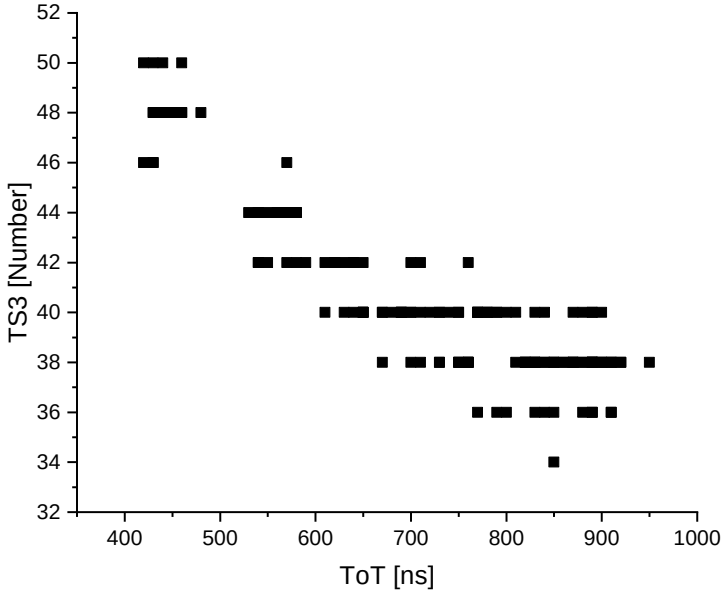


Figure 5.17: TDAC values for different pulse widths. X coordinate of each point is measured ToT (fast comparator) and y coordinate is measured TS3 (fast comparator). Each point is result of one injection. Injections have been varied from 0.3 V to 1 V

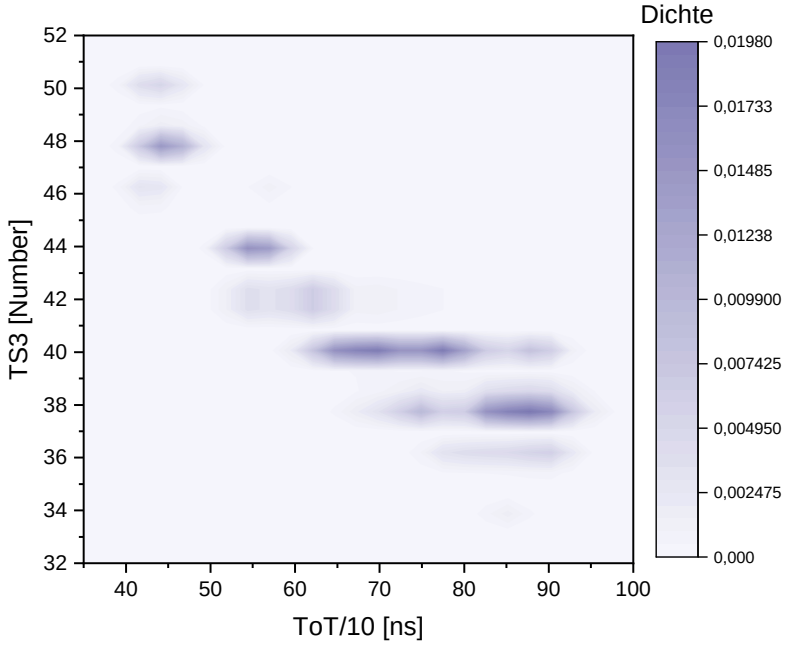


Figure 5.18: The density of points instead of single point for figure 5.17

Figure 5.17 shows the TDAC value for different pulse widths. X coordinate of each point is measured ToT (fast comparator) and y coordinate is the measured TS3 (fast comparator).

Each point is result of one injection. Injections have been varied from 0.3 V to 1 V.

We see that the TS3, which is proportional to response time, gets smaller when measured ToT is larger. However there is noise because the fast comparator does not measure amplitude with large SNR which leads to spread of the points. The density of points instead of single points are presented in figure 5.18.

5.5.7 Time and corrected time versus pulse width

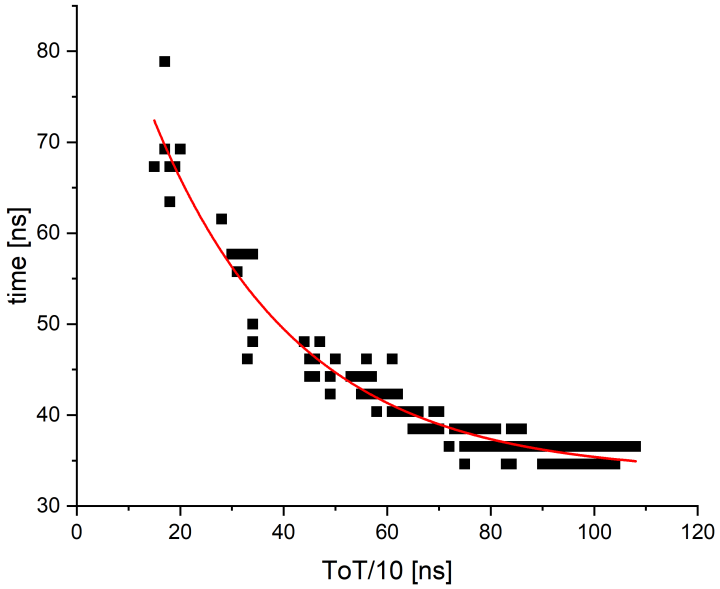


Figure 5.19: Time versus different pulse widths. X coordinate of each point is measured ToT with slow comparator and y coordinate is calculated response time measured with fast comparator. Each point is result of one injection. The injections have been varied from 150 mV to 800 mV with 50 mV step.

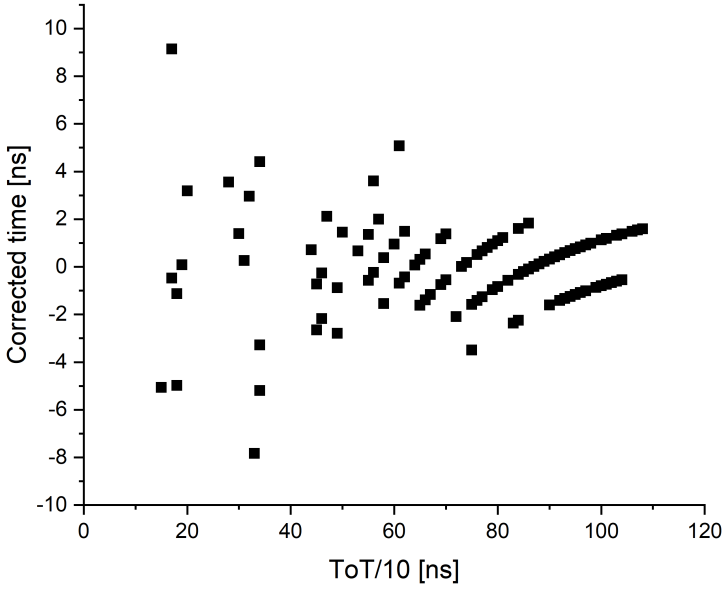


Figure 5.20: The corrected time (distance to fit) versus measured ToT (TS2)

The relationship between time and pulse width is presented in figure 5.19. X coordinate of each point is measured ToT with slow comparator and y coordinate is measured response

time. Each point is result of one injection. The injections have been varied from 150 mV to 800 mV with 50 mV step.

We see that the time of signal crossing threshold is smaller when measured ToT is larger.

Exponential function has been fitted to data, which could be used for time walk correction.

$$y = 33.52 + 35.06e^{(-(x-17.88)/28.08)} \tag{5.1}$$

The corrected time versus measured ToT and its histogram distribution are illustrated in figure 5.20 and 5.21. The time resolution is RMS 1.28 ns.

The specification for PANDA is almost fulfilled.

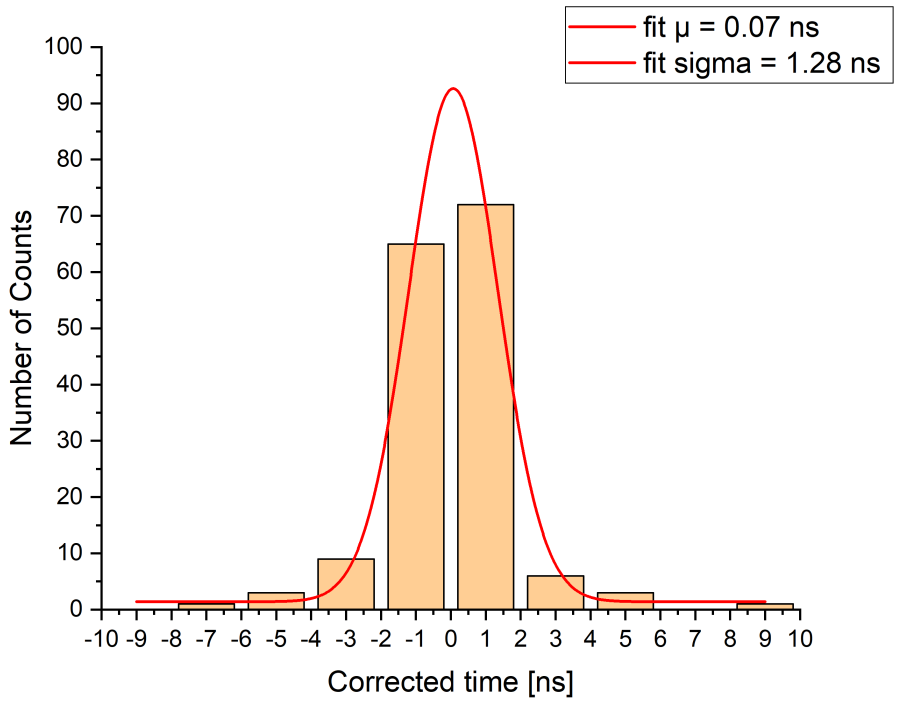


Figure 5.21: Corrected time (the data from figure 5.20) shown as histogram

5.5.8 Comparison of big and small pixels with large and small current

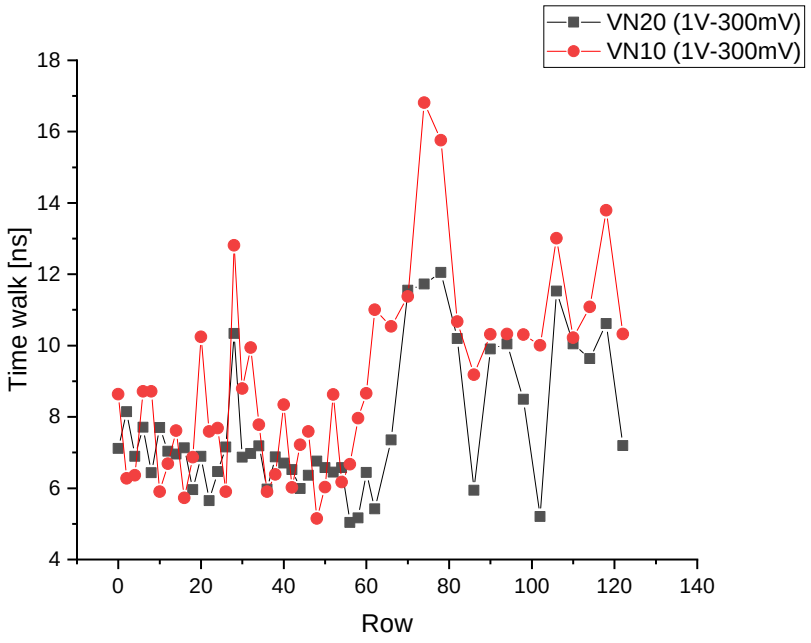


Figure 5.22: Time walk versus different rows of VN10 (1.6 μA) and VN20 (3.1 μA)

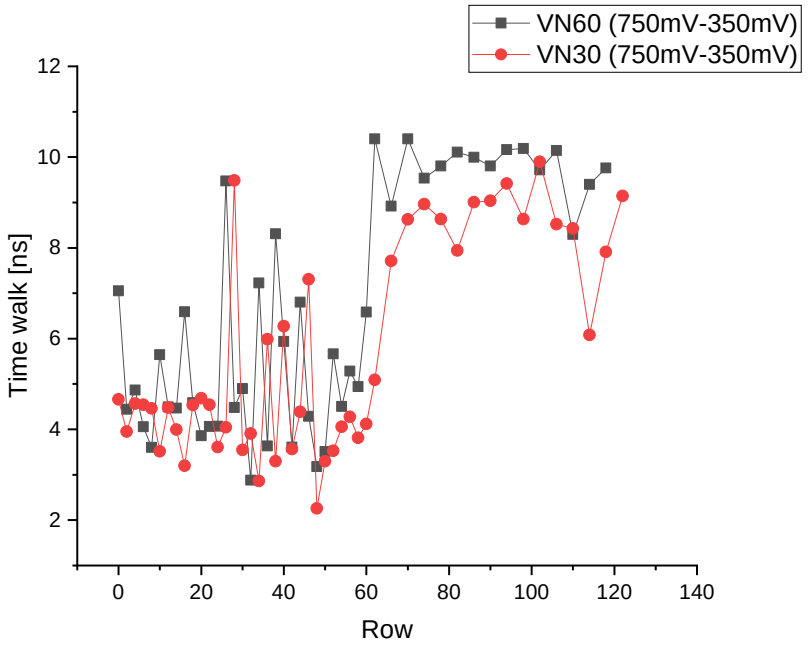


Figure 5.23: Time walk versus different rows of VN30 (4.7 μA) and VN60 (9.4 μA)

As mentioned, the PANDA ASIC has two pixel sizes - small pixels (50 μm x 165 μm) in the rows 0 - 62 and big pixels (100 μm x 165 μm) in the rows 63 - 123. It is interesting to compare the time walk of big pixels with twice more current with small pixels with twice less current because in both cases the current consumption is equal. In figures 5.22 and 5.23, we see that small pixels (row 0 to row 62) have in average better time walk even with

twice less current and big pixels have larger time walk. Furthermore, we see that doubling of amplifier current does not change time walk significantly.

5.5.9 Threshold scan

The threshold scan for fast and slow pixels of column 0 are presented in figure 5.24 and 5.25. The mean value of tunned threshold is smaller and its distribution is narrower than the untunned threshold for both cases. The exact mean threshold value and sigma are listed in table 5.5.

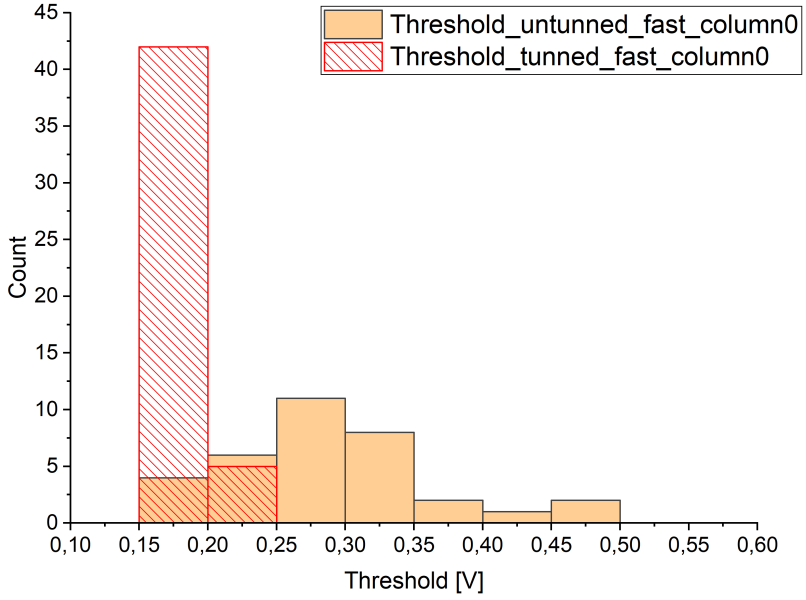


Figure 5.24: Input referred threshold dispersion with fast comparator before trimming versus after trimming

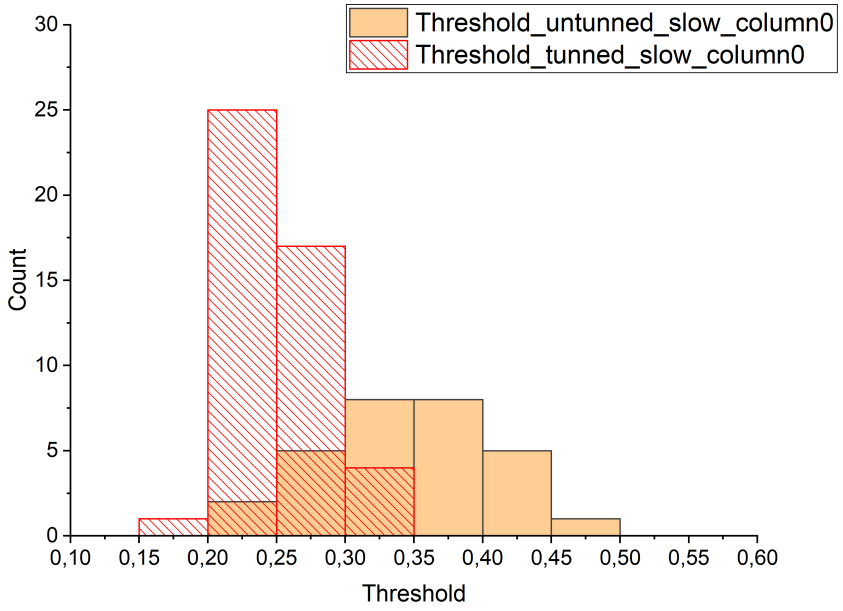


Figure 5.25: Input referred threshold dispersion with slow comparator before trimming versus after trimming

Table 5.5: Threshold scan for the fast and slow comparators

	Untunned mean	Untunned δ	Tunned mean	Tunned δ
Fast comparator	0.287V	0.073V	0.176V	0.021V
Slow comparator	0.349V	0.061V	0.247V	0.035V

5.6 Measurement results of CLIC ASIC (v1/v2 chip)

The CLIC ASIC contains pixel matrix of 124 x 29 pixels. The pixel size is 25 μm x 165 μm.

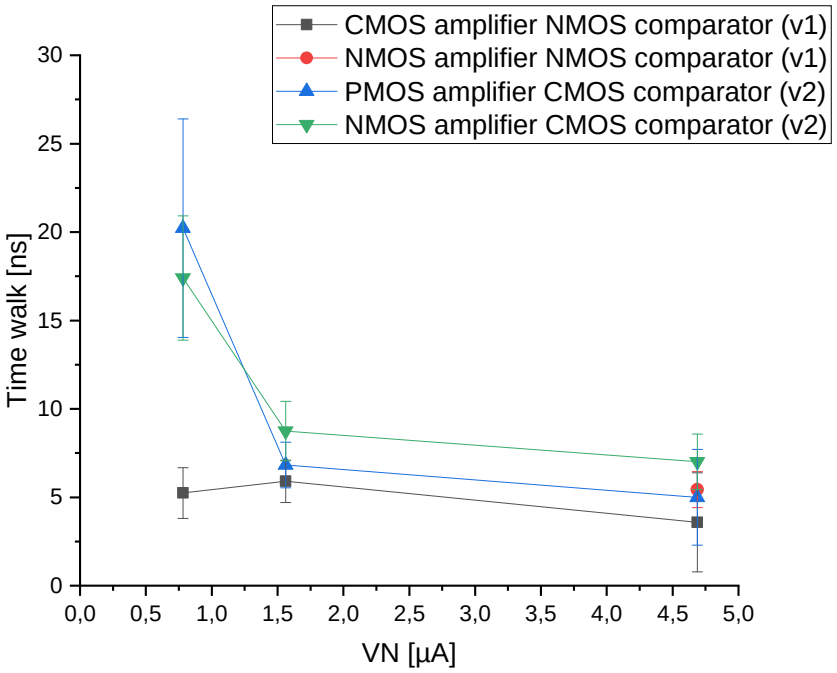


Figure 5.26: Time walk versus different amplifier bias current setting of CLIC ASICs

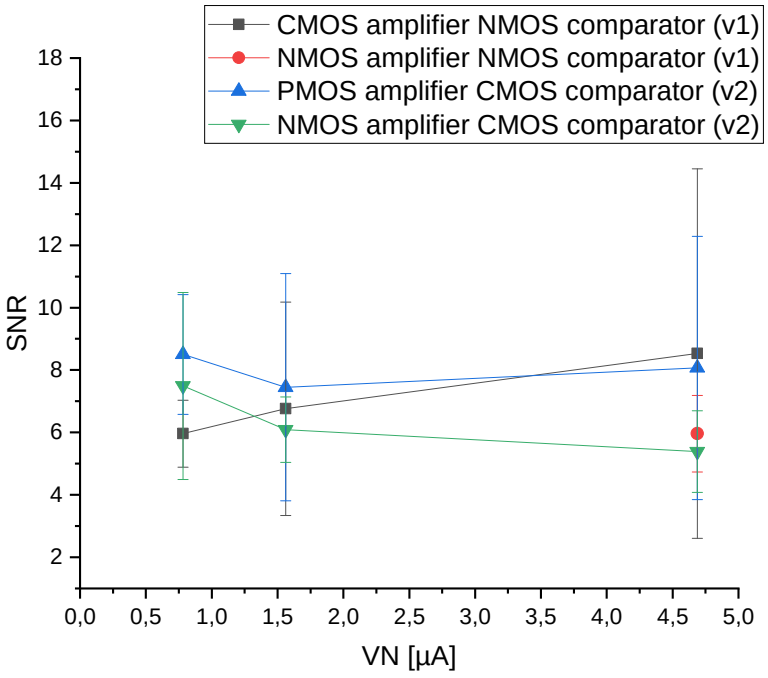


Figure 5.27: SNR versus different amplifier bias current setting of CLIC ASICs

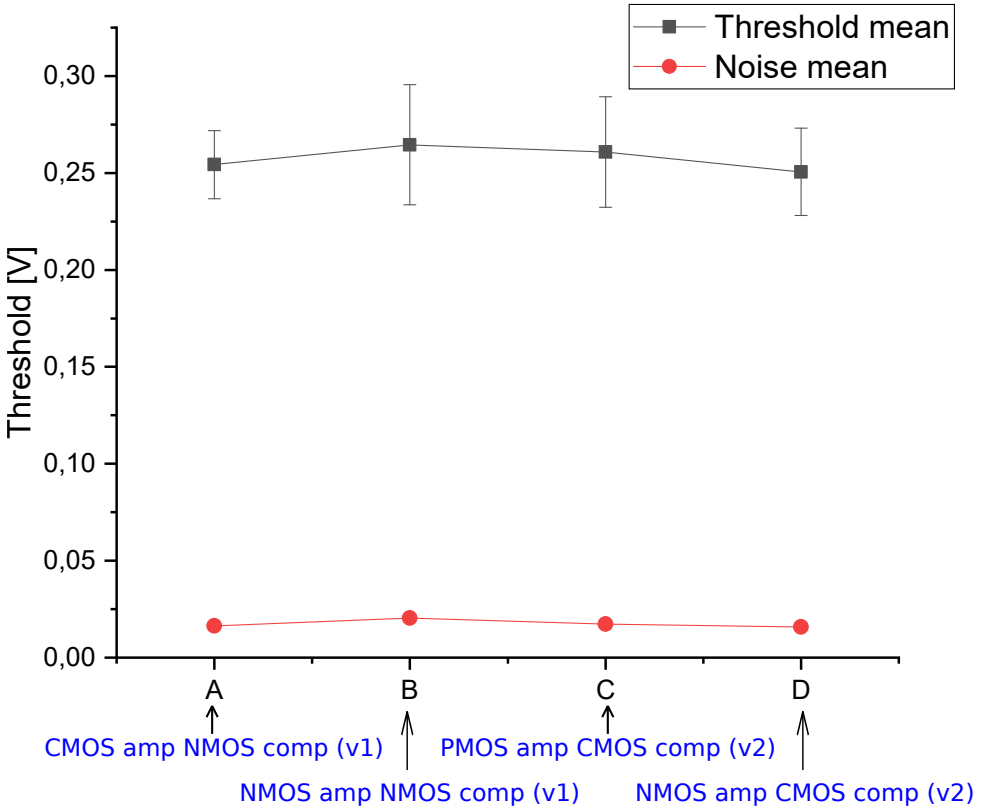


Figure 5.28: Four variants threshold of CLIC ASICs

V1 and V2 chip versions have NMOS, PMOS and CMOS amplifier. The aim of the measurements was to compare the NMOS, PMOS and CMOS amplifier type in terms of their time walk and SNR.

We measured the first 10 pixel rows and the SNR is defined as (ToT(1V) - ToT(600mV)) / sigma (1V), and calculated time walk as time(600mV) - time(1V). Additionally, we calibrate that 300mV of injection voltage corresponds to Fe55 (1664e) source.

Figures 5.26 and 5.27 show the average value of time walk and SNR versus VN bias setting for all cases. As the bias voltage increases, the time walk for all combination decreases. However, the change of SNR is different for each situation.

Furthermore, the threshold value with deviation and noise is illustrated in figure 5.28. They are nearly the same for all four variants.

6 Conclusion

MPROC

The aim of PLASMED X project is to develop a detector for golden nanoparticles. X rays will be generated by a plasma accelerator. These x-rays will excite the gold atoms that will emit fluorescence photons. These photons can be detected by a hybrid pixel detector with CdTe sensor. A very good energy resolution is desired.

For this detector I have designed the MPROC ASIC.

The MPROC chip has been implemented by TSI 180 nm HVCMOS technology. The transmitting electrode pitch is 55 μm x 55 μm, the pixel size is 18.3 μm x 165 μm.

There are in total 8100 pixels and each has two thresholds.

There are several novel circuits and concepts. The pixel geometry and bonding pad geometry are different. This allowed very small pixel size for a 180nm technology. The pixel amplifier can cope with both signal polarities. Time to digital converter has been implemented. For energy measurement peak detector has been implemented. The peak detector signal is digitized by a time based ADC.

The chip has been designed produced and successfully tested. Measurement results have been presented.

CCPD

A new concept of CCPD (capacitively coupled particle detector) has been realized and tested. The sensor chip and the readout chip are mechanically connected with a small number of relatively large bump bonds instead of glue.

A capacitively coupled sensor chip named CCPD53 has been implemented by me in 180 nm modified HVCMOS technology on a high resisitivity wafer and with the deep p-well option. The readout electrode pitch is 50 μm x 50 μm.

There are several novel circuits: Special encoding has been designed, 16 pixels are connected to 8 transmitting electrodes. The deep p-well has been for the first time used in this technology.

The ASIC PHOTON has been applied for capacitively coupled readout of CCPD53. Measurements have been performed. The functionality of the sensor and signal transmission has been demonstrated.

HVMAPS25

The monolithic particle pixel sensor HVMAPS25 has been implemented by me in the 180 nm HVCMOS technology of TSI Semiconductors on 200 ohmcm substrate. The sensor could be applied in a vertex detector of some future experiment such as CLIC and CEPC.

The diode with very small size (2 μm x 4μm) is embedded in the high resistivity p-type substrate.

Sensor electrodes are biased to typically 10V. In this way the sensor substrate is partially depleted. The pixel size is 25 μm x 35 μm. The pixel electronics are placed in shallow p- and n-wells and these wells are embedded in the deep p-well used as potential barrier for signal electrons.

I have performed tests of the overall functionality, measurements of the amplitude response, threshold scans and threshold tune measurements and tests with radioactive sources.

HVMAPS25 ASIC can measure the arrival time of the hit with 10 bit resolution and the amplitude (time over threshold) with 6 bit resolution. Time resolution better than 10 ns can be achieved. Small power consumption has been shown, and the current consumption is < 1 μm for the pixel amplifier.

CLIC

Eight variants monolithic sensors have been implemented by TSI 180 nm HVCMOS technology from H2020 run, which could be used in for various experiments, for example PANDA, CLIC and CEPC.

Different combinations of amplifier types and comparator types have been designed in order to find the bast circuit in terms of threshold diserpation, time walk, signal noise ratio and time resolution.

Several novel features have been implemented such as the variable gain amplifier, the TDC, the double comparator pixel and the CMOS amplifier.

The design was done together with outher group members, I have performed detailed characterization of the chips.

The measurements include: Scope measurements of amplifier and hit output, calibrations of injection with Fe55, threshold scans and threshold tuning. I have shown that the PANDA sensor can detect signals in the range 1 - 100 MIPS and has a time resolution of 1.3ns. These are very promising results.

Appendix

A Radiation Damage

Semiconductor detectors are sensitive to radiation damage. We can distinguish between permanent and transient effects. The transient effects, such as SEEs (single event effects), lead to failure in signal processing are related to the instantaneous generation of charge carries. This can be corrected through logic design, for example triple modular redundancy. The permanent effects are related to the structural modification of the materials. These effects are be classified into displacement damage and ionization damage [13].

A.1 Displacement Damage

Displacement damage is caused mainly by high energy charged particles and neutrons, and it is linearly proportional to the particle flux and to the nonionizing energy loss of an incident particle per collision. Since the electrical characteristics of MOS transistors depends mainly on the properties of the SiO2 insulating layer (gate oxide) and the quality of the Si-SiO2 interface, and these interface and layer are amorphous, thus CMOS or the oxide layer is not sensitive for displacement damage. Table A.1 gives a rough comparision of displacement damage for several particles and energies.

Table A.1: Rough comparison of displacement damage for several particles and energies [18]

Particle	Proton	Proton	Neutron	Electron	Electron
Energy	1 GeV	50 MeV	1 MeV	1 MeV	1 GeV
Relative Damage	1	2	2	0.01	0.1

A.2 Ionization Damage

Ionization damage is caused by charged particles and photons, it depends on the total energy of ionizing radiation absorbed in SiO_2. It brings two effects on MOS transistors: One is the activation the interface traps between the oxide and the silicon bulk, the other one is the generation of positive oxide charge. Both effects shift threshold voltage and increase sub-threshold leakage current [14].

The oxide is not only present in the gate isolator of the MOS structure. The transistors are also isolated by a trench filled with amorphous SiO_2, this insulation is called the field oxide. Field oxide is exposed to a higher radiation dose due to its thickness. The positive charge induced by radiation and trapped in the field oxide lowers the threshold of a parasitic NMOS transistor, increases its leakage current and in worst case turns it on [13].

It is important to note that only n+ layers (NMOS transistors) are affected by trapping in the field oxide. The positive oxide charge cannot induce the hole currents between two p+ diffusion layers which are separated by the n type bulk material. That is the reason why PMOS transistors are not affected by radiation damage.

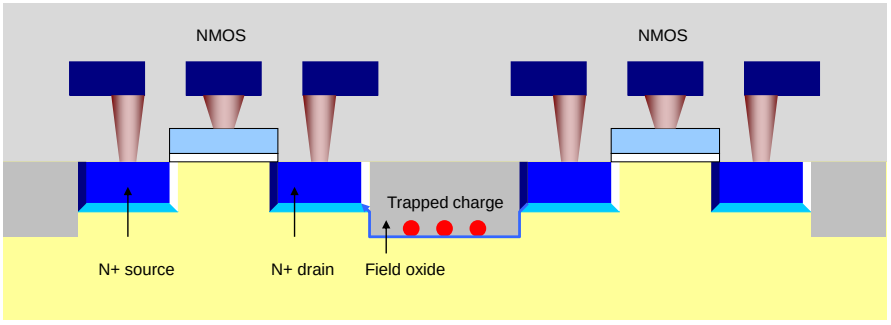


Figure A.1: Radiation influence on IC structure

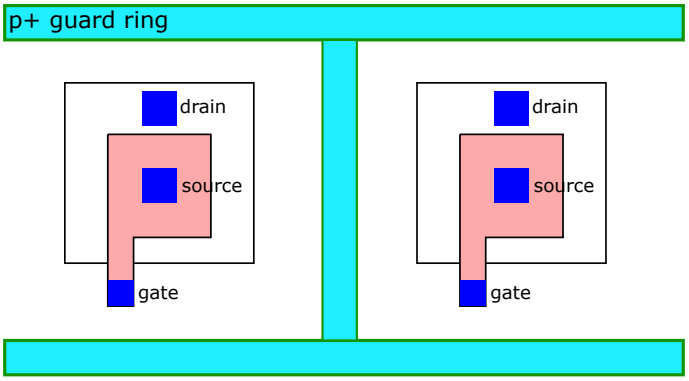


Figure A.2: p+ guard ring is applied for preventing leakage current flows between two NMOS transistors

A.3 Radiation tolerant IC Desgin

In order to reduce the influence from radiation, a few techniques are used. For the purpose of preventing the leakage current between two NMOS transistors, a p+ guard ring is applied, shown in figure A.2. The electron density in a p+ region is so low that the trapped oxide charge cannot collect enough electrons to produce the channel. The parasitic channels are therefore cut by the guard rings. For the purpose of preventing the leakage current flowing around the gate from drain to source of a single transistor, an annular (circular) gate electrode is applied.

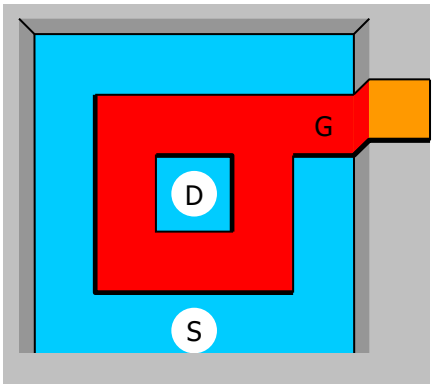


Figure A.3: Annular gate electrode for preventing leakage current flows from drain to source

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