

X-ray characterization of BUSARD chip: A HV-SOI monolithic particle detector with pixel sensors under the buried oxide

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ABSTRACT: This work presents the design of BUSARD, an application specific integrated circuit (ASIC) for the detection of ionizing particles. The ASIC is a monolithic active pixel sensor which has been fabricated in a High-Voltage Silicon-On-Insulator (HV-SOI) process that allows the fabrication of a buried N⁺ diffusion below the Buried OXide (BOX) as a standard processing step. The first version of the chip, BUSARD-A, takes advantage of this buried diffusion as an ionizing particle sensor. It includes a small array of 13×13 pixels, with a pitch of 80 μm, and each pixel has one buried diffusion with a charge amplifier, discriminator with offset tuning and digital processing. The detector has several operation modes including particle counting and Time-over-Threshold (ToT). An initial X-ray characterization of the detector was carried out, obtaining several pulse height and ToT spectra, which then were used to perform the energy calibration of the device. The Molybdenum K_{α} emission was measured with a standard deviation of 127 e⁻ of ENC by using the analog pulse output, and with 276 e⁻ of ENC by using the ToT digital output. The resolution in ToT mode is dominated by the pixel-to-pixel variation.

KEYWORDS: X-ray detectors, Pixelated detectors and associated VLSI electronics, Electronic detector readout concepts (solid-state), Front-end electronics for detector readout

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Contents

1	Introduction	1
2	Design of the sensor and builtin electronics	2
2.1	Pixel analog subsystem	2
2.2	Pixel digital subsystem	4
2.3	General chip design and layout	5
2.4	Pixel response calibration procedure	8
3	Low energy X-rays characterization	8
3.1	Pulse height spectra	9
3.2	Time-over-Threshold	11
4	Conclusions	13

1 Introduction

Over the last decades the scientific community has been trying to develop more faster, accurate and low cost ionizing particle detectors, and for these purposes the CMOS technology has been the preferred choice because of its maturity and simple design flow. CMOS technology has been used for the development of readout integrated circuits in the so called *hybrid* pixel detectors, in which the sensor is produced on a special fabrication process different from the readout chip. This type of approach has been explored and developed successfully since more than three decades ago and a history review can be found in [1]. Since then, hybrid detectors have been used for several experiments, like the LHC's ATLAS and CMS pixel detectors [2, 3], and they were used also by the *Medipix* collaborations [4]. This collaboration developed hybrid detectors for medical imaging and high-energy particle physics experiments [5], like *Medipix* and *Timepix* detectors.

However, hybrid detectors suffer from serious drawbacks in terms of costs associated with the assembly of hybrid parts. With the advancement of the CMOS consumer electronics and CMOS imaging applications, the development of *Monolithic* Active Pixel Sensors (MAPS) rapidly emerge [6]. In a monolithic detector, the sensor and electronics are produced in the same piece of silicon as part of one single fabrication process and there is no need of additional post-processing steps, which can reduce the cost and failure rate in comparison with their hybrid counterpart. Since then, several MAPS have been designed that take advantage of different properties of CMOS technology: diffusion in the epitaxial layer [7], high-voltage CMOS [8, 9], Partially-Depleted SOI (PD-SOI) [10], Fully-Depleted SOI [11], just to name a few. The main idea behind SOI MAPS is to make the particle-sensitive device in the handle wafer—possibly taking advantage of a high-resistivity substrate and thus a larger depletion region with a stronger electric field—and the active electronics in the top silicon film. The success of these devices was leveraged by the progress of the SOI

technology, which made possible the fabrication of wafers with less defects both in the thin silicon film and in the handle wafer [10]. More recently, several works [12–18] presented the design and characterization of a MAPS on a 180 nm PD-SOI fabrication process which exploits the buried oxide to isolate the sensor device from the active electronics, connecting both through a hole in the BOX. These works include the description of the design and several tests like radiation hardness, charge collection in the sensitive junction, Total Ionizing Dose (TID) and even Single Event Effect (SEU) tolerance.

Following the same principle of using a SOI fabrication process to make a monolithic sensor, in this work the BUSARD-A is presented. This chip is a prototype of a MAPS with the ability of counting particle hits and also measuring particle energy. It is intended to perform a basic energy discrimination of ionizing particles and energy resolved imaging on a future bigger array. Section 2 presents the design of the detector. A pixel cross-section is shown with the radiation-sensitive device and its connection to the active electronics. Then, the analog signal processing, digital blocks and general chip architecture are described. Next, section 3 presents the characterization of the device using the emission of fluorescence X-rays of different materials. BUSARD's analog output and digital ToT data are used to obtain the energy spectra of the emitted photons. Then these spectra are used to trace energy calibration curves and to calculate the sensor's readout noise. The article finishes with a short conclusion highlighting the most relevant properties of the ASIC.

2 Design of the sensor and builtin electronics

The integrated circuit was designed and fabricated using the partially depleted Silicon-On-Insulator (SOI) 180 nm fabrication process from XFAB XT018. This process allows the creation of an n-type diffusion in the silicon substrate under the buried oxide and allows the connection of this buried diffusion to the active electronics located on the top silicon film.

Figure 1 shows a pixel cross section. The NBUR/p-sub device is the radiation sensitive element. The charge generated by impinging ionizing radiation is collected in its depletion region, which extends mostly on the p side of the junction, it flows to the device terminals and it is amplified by a charge amplifier located in the top silicon film. The NBUR/p-sub diode can withstand up to 110 V applied in reverse without entering avalanche breakdown mode. This allows a large depletion region and thus a larger charge collection volume than standard low-voltage CMOS technologies. With the standard handle wafer resistance, the extension of depletion region into the p substrate gives approximately 33 μm at 110 V.

The pixel also comprises one analog and one digital part, which are isolated from each other and from the NBUR connection using Deep Trench Isolation (DTI) isolation.

2.1 Pixel analog subsystem

The analog subsystem is comprised by three cascaded stages: a first stage which is a charge amplifier, a second summing stage, and a comparator/discriminator stage. The buried N diffusion is biased through a diode-connected standard PMOS transistor T_{bias} built in its own pocket, so applying a high voltage to this device does not affect the rest of the electronics.

The first stage is responsible for the amplification and translation from charge to voltage pulse. The conversion factor is 6.3 μV per e^- of charge collected in the buried N diffusion, and, as will

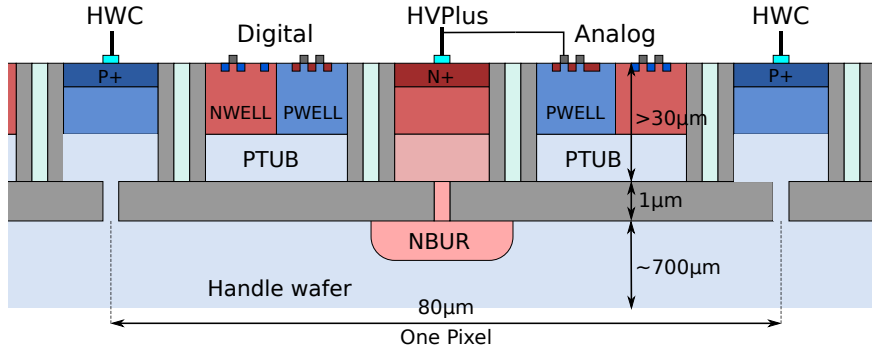


Figure 1. Pixel cross section. The fabrication process allows to make a diode in the handle wafer and to contact it from the top thin-silicon film. The buried diffusion is surrounded by the analog and digital parts in the silicon film, which are isolated by deep trench isolation.

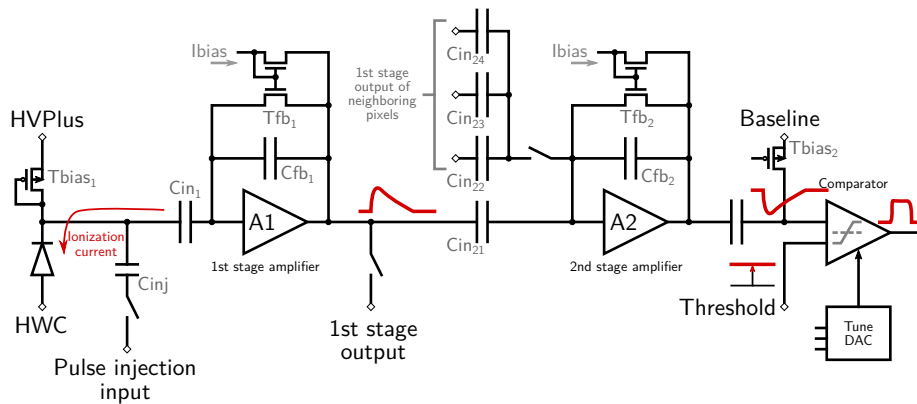


Figure 2. Schematic of the analog part of the pixel.

be shown later, it was measured by fitting the spectrum of several known radiation sources. The feedback capacitor, C_{fb1} , has a MOS transistor in parallel, T_{fb1} , biased with a voltage in such a way that most of the time is off, and during a pulse it will discharge the capacitor at a programmable rate allowing the adjustment of the tail length. Table 1 shows the values of the capacitors and some key parameters of this stage.

The purpose of the second stage is to sum the pulses produced by the first stage of neighboring pixels and, in this way, perform an analog binning, avoiding the loss of charge due to incomplete charge collection. This function can be enabled or disabled at any time with a configuration bit. When disabled, the pulse of the first stage passes unattenuated to the comparator stage.

The output of the second stage is AC coupled to the comparator and this allows tuning the *baseline* DC level, which is set by a voltage generated outside the chip. Then the comparator/discriminator compares this level with the *threshold* voltage, also generated outside the chip. A digital pulse is generated and maintained each time the analog signal drops below the threshold voltage. Both the baseline and the threshold voltages are common and distributed to the whole pixel matrix.

The comparator offset can be adjusted by means of a Tune DAC circuit located in every pixel. This circuit is a 3-bit current steering DAC that introduces an unbalance into the differential amplifier

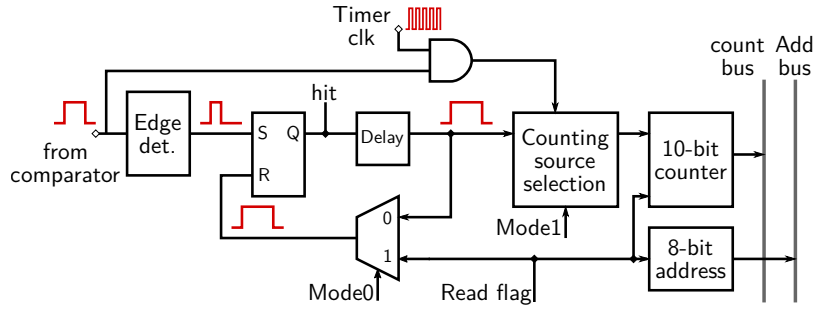


Figure 3. Block diagram of the digital subsystem inside each pixel.

of the comparator proportional to the digital word set.

In order to test the device there is a *test pulse input* that is very useful for testing, but also for calibration of the whole matrix. A memory bit on each pixel allows opening or closing the switch that enables/disables this function. A voltage step injected to this input produces certain amount of charge to be transferred to the input of the first stage, producing a signal similar to the one produced by a particle interaction.

It is also possible to route off chip the output of the 1st stage amplifier of one pixel in order to measure its response. This was made possible only on the first column of the matrix in order to reduce the layout complexity.

2.2 Pixel digital subsystem

The digital subsystem inside each pixel is depicted in figure 3. The output of the analog comparator passes through an edge detector generating a fast pulse that sets an SR flip-flop, rising the *hit* signal. Here there are four modes of operation: (1) standard particle counting, (2) hit mode, (3) time-over-threshold (ToT), and (4) hit mode plus TOT. In the particle counting mode, the same *hit* signal is used to reset the flip-flop. A short configurable delay—implemented as a MOS current source and a capacitor—was added to assure the proper operation and avoid racing conditions or missing counts. In this mode the same *hit* pulse is used to increment a 10-bit counter, so each time a particle hits the sensor the count gets increased by one. When a read operation begins, the counter is blocked and its tristate output is connected to the count bus, which is shared across all pixels. There is also a hardcoded address block in each pixel and a shared address bus, and each time a read operation is performed the pixel that is being read takes both buses.

In the second mode (hit mode) the difference is that the flip-flop is not reset by its own generated hit signal, but it is reset by a read operation instead. So, when particle interaction is detected the counter increases by one but then the pixel gets locked waiting until a read operation is performed.

Modes (3) and (4) are similar to (1) and (2), respectively, but in this case the counter increment is done with a fast clock signal generated of chip and distributed to the whole matrix. The count keeps increasing for as long as the comparator is in a high state, which is the same time as the pulse is below the threshold voltage. The result is a count that is proportional to the time the signal has been below the threshold and this, in turn, is proportional to the charge produced by the particle interaction.

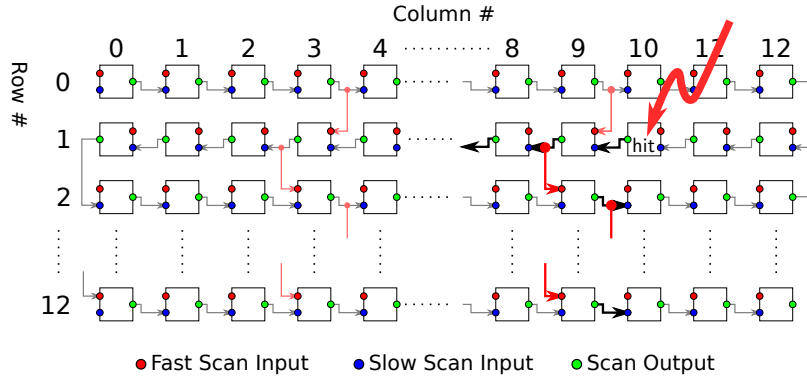


Figure 4. Scan chain logic connection. All pixels are connected in a zig-zag slow chain with two fast propagation lines in columns 3 and 9. The thicker lines illustrate how the signal is propagated through the fast chain. All floating inputs are connected to ground.

In order to select a pixel for reading out its counter and address there are two possibilities: direct addressing and scan chain selection. In direct addressing the pixel is selected by setting a 1 in the desired position of the row and column selection registers. These registers are 13 bits long, so each bit corresponds to a row or column and the pixel that has both set is selected.

The scan chain logic allows the automatic selection of the pixel to be read [9, 19]. Pixels are connected together in a daisy chain array by using a special logic and the pixel that has been hit by a particle takes control of the data buses, locking access to every other pixel down the chain. A diagram of this chain is shown in figure 4.

There are two inputs `slowScanI` and `fastScanI`, and one output `outScan`. When a pixel is marked as hit (`hit=1`), the `outScan` output will be set. The next pixel in the chain will receive a '1' in its `slowScanI` input and this prevents this pixel from being read. This signal will propagate to the `outScan` of the second pixel and then to the third pixel down the chain, and so on. This is called the *slow* scan chain because it passes through every pixel, therefore the signal delay from the hit position to the last pixel in the chain can be significant.

In order to reduce this delay time, two *fast* propagation lines were made in columns 3 and 9. The `outScan` of pixels in those columns is connected to pixels of the next row. In this way the information arrives faster to the next rows and there is a tree-like propagation. The worst case scenario is when a particle hits the pixel located in first row and first column. In this case, in order for the information to get to the last pixel in the chain the signal must pass through 26 pixels.

Only when a pixel is selected for reading, by either using direct addressing or the scan chain, its counter can be cleared with a reset signal.

2.3 General chip design and layout

It is a small test chip comprising a matrix of 13 by 13 square pixels, each with a lateral size of 80 μm . Figure 5 shows a diagram of the chip architecture. The pixel array has several row and column configuration registers whose functions are pixel addressing, loading tune-DACs, enabling the test pulse input for one or several pixels and enabling the 1st stage output. There are also 14 global 6-bit DACs whose purpose is to give some flexibility to the analog biasing of the pixel matrix. With the global DACs it is possible to fine tune the biasing of the first and second stage amplifiers and

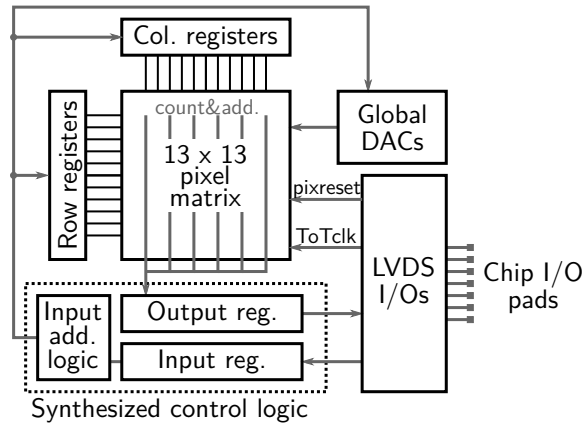


Figure 5. Diagram showing the chip architecture. There is a digital synthesized logic that controls the configuration input and readout of the matrix.

also to adjust the biasing of the MOS resistive feedback. In addition, the comparator DC current and Tune-DAC current reference can be tuned separately, allowing the calibration of the tune-DAC LSB step, and thus the threshold offset, with more precision. The digital 6-bit word of each DAC is stored in its own memory register.

In order to load a register, the desired value and the register address are loaded in series into the input register by using a data and clock input lines. After receiving 18 bits, the control logic decodes the input and stores the value in the addressed register (row, column, configuration or DAC register).

The matrix is readout one pixel at a time by pulsing a clock line and reading the data coming out in series of the output register. This register contains the 10 bit count and 8 bit address of the pixel that is being read out. Its content must be loaded from one of the pixels in the matrix before reading it. In order to select a pixel—or several pixels—for reading, there is a special line called `pixHitLoad`. A pulse applied to this signal loads into the scan chain the pixels flagged as *hit* (in hit mode), or pixels selected by direct addressing using the row and column selection registers. Then, a pulse applied to a second line called `pixRead` transfers the count and address from the pixel already set in the scan chain to the output register, also clearing its hit flag and allowing the read of the next in the chain. After reading out the output register the sequence repeats until the desired number of pixels is accessed. The advantage of this system is that it is not necessary to read the whole matrix every time, but instead just the pixels that have been hit or flagged for reading.

The time needed for reading one pixel is the time required to send the signals `pixHitLoad` and `pixRead` plus the time it takes reading out in series 18 bits from the output register. According to simulation results, the output clock can run as fast as 200 MHz and the total time for reading a pixel at maximum speed is 100 ns. However, while the output register is being read, the whole matrix—even the pixel whose count and address were stored in the output register—is active and prepared to detect ionization events. The only dead detection time introduced by this readout system is when the `pixRead` signal is high, which halts the pixel’s counter to avoid data loss.

Figure 6 shows the layout of the fabricated device. The 13 by 13 pixel matrix takes most of the area of the 1.5 mm chip. The digital controller and global DACs are located below the matrix

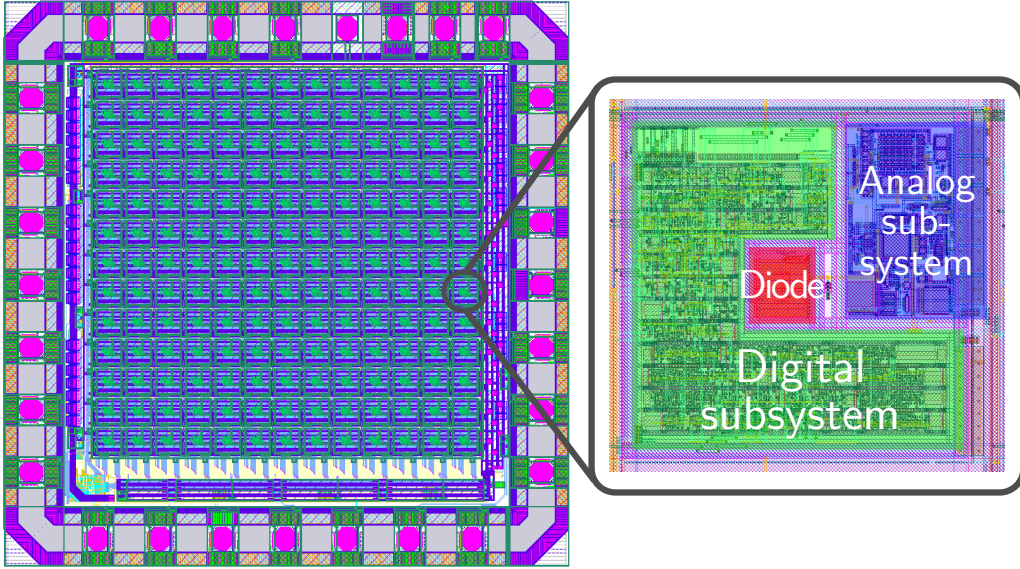


Figure 6. Layout of the integrated circuit with a lateral size of 1.5 mm. Most of the area is used by the 13×13 pixel matrix, with a pixel pitch of $80 \mu\text{m}$. The global DACs are located below the matrix and the synthesized digital controller is fabricated in a 180 nm PD-SOI fabrication process. A detailed view of one pixel is also shown.

Parameter	Value	Unit	Comments
C_{det}	≈ 1	fF	
$C_{\text{in1}}, C_{\text{in2x}}, C_{\text{fb2}}$	50	fF	
C_{fb1}	5	fF	
1st stage amp. peaking time	1 to 5	μs	Var. with 6-bit DAC for I_{bias} T_{fb1}
1st stage amp. discharge rate	50 to 4.25	$\text{mV } \mu\text{s}^{-1}$	Var. with 6-bit DAC for I_{bias} T_{fb1}
1st stage amp. power consumption	10	μW	
2st stage amp. power consumption	18	μW	
Comparator power consumption	1.8	μW	
Baseline voltage	900	mV	Generated outside the chip
Threshold voltage	885	mV	Generated outside the chip
Pixel size	80×80	μm	
Pixel power consumption	30	μW	Only accounting for static power
Matrix size	13×13	pixels	
Chip power consumption	20	mW	Mainly consumed by I/O drivers

Table 1. BUSARD-A key parameters.

and the LVDS drivers near their output pads. All the digital input and output lines are Low-Voltage Differential Signals (LVDS) in order to reduce the digital noise coupled to the I/O ring.

Table 1 show some key parameters of the BUSARD-A chip.

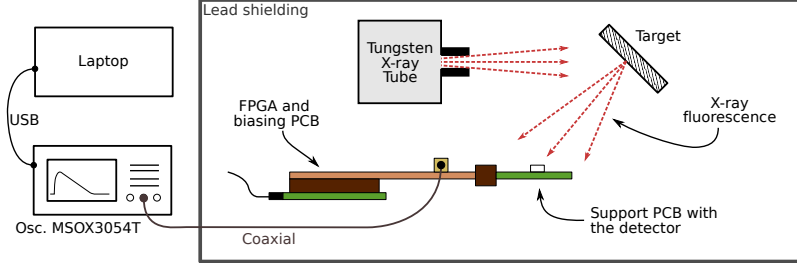


Figure 7. X-rays fluorescence experimental setup.

2.4 Pixel response calibration procedure

Due to process variations and gradients it is expected to have a different response to the same input on each pixel. An equal pixel response is specially relevant when using the ASIC in ToT mode, in which a count proportional to the particle energy is expected. Differences come from the amplifiers gain, the feedback current sources and the comparators offset. In order to simplify the analysis, all these deviation sources can be modeled as a variation in gain and offset in the response of each pixel, according to the following equation

$$y_i = m_i x + b_i, \quad (2.1)$$

where x is the stimulus, m_i and b_i are the gain and offset respectively, and y_i is the pixel's output. For the purpose of generating a stimulus in an easy way is that the test pulse input was added to the chip.

The calibration is based in the calculation of two arrays of constants K_1 and K_2 that can be used to equalize the pixel's output to the same mean value

$$\bar{y} = K_{1,i} y_i + K_{2,i}, \quad \begin{cases} K_{1,i} = \frac{\bar{m}}{m_i} \\ K_{2,i} = \bar{b} - K_1 b_i \end{cases} \quad (2.2)$$

The first step in the calibration procedure is to measure the response of every pixel to the same variable stimulus, this means applying test pulses of different amplitudes through the test-pulse-input, and extracting the average output \bar{y} , the average gain \bar{m} , and the average offset \bar{b} . Then, the calibration constant arrays are calculated as shown in equation 2.2. The length of these arrays is equal to the amount of pixels in the matrix. Finally, the calibrated mean output is obtained by multiplying the output of each pixel by its corresponding constant in the K_1 array and then adding the corresponding constant of the K_2 array.

3 Low energy X-rays characterization

The detector response was characterized by using low energy fluorescence X-rays. The setup shown schematically in figure 7 was used to produce the fluorescence of different materials. These elements along with their most significant x-ray emissions are listed in table 2. The sensor junction was biased at 60 V.

Z-Mat shell	[keV]	Z-Mat shell	[keV]
29-Cu $K_{\alpha 1}$	8.04	42-Mo $K_{\beta 1}$	19.60
30-Zn $K_{\alpha 1}$	8.63	47-Ag $K_{\alpha 1}$	22.16
29-Cu $K_{\beta 1}$	8.90	48-Cd $K_{\alpha 1}$	23.07
30-Zn $K_{\beta 1}$	9.57	49-In $K_{\alpha 1}$	24.20
82-Pb $L_{\alpha 1}$	10.55	47-Ag $K_{\beta 1}$	24.94
82-Pb $L_{\beta 1}$	12.61	50-Sn $K_{\alpha 1}$	25.27
40-Zr $K_{\alpha 1}$	15.78	48-Cd $K_{\beta 1}$	26.09
42-Mo $K_{\alpha 1}$	17.47	49-In $K_{\beta 1}$	27.27
40-Zr $K_{\beta 1}$	17.67	50-Sn $K_{\beta 1}$	28.48

Table 2. Most intense emission lines of the elements used in the detector characterization [20].

First, the response of the first stage amplifier of one pixel located on the leftmost column of the matrix was measured (this column is the only one with analog outputs available). The analog output of this amplifier, shown in figure 2, was connected to an oscilloscope with its threshold level set to capture the output pulses. In this way, each photon impinging the sensor produces an output pulse with a height proportional to the ionization charge generated and collected in the sensor junction. Then, the signal waveforms were transferred to a laptop and stored for post-processing. The result is shown in section 3.1.

In another experiment, maintaining the same setup, the digital readout was used in order to acquire data. Using an FPGA, an USB connection to a computer, and a custom software, the detector was configured in ToT mode and the 169 pixels were read while the sensor was exposed to the x-ray fluorescence photons. In this case, a counter value different than zero means that the pixel was hit, and that value multiplied by the ToT clock period is the time that the pulse generated by the particle was above the threshold. On the other hand, if the pixel count is zero, that means that the pixel was not hit, so it can be skipped. The whole matrix was read in successive operations, storing the digital TOT per pixel when it was different than zero, and as many times as needed to acquire enough data. Section 3.2 shows the result of this second experiment.

3.1 Pulse height spectra

As it was mentioned before, the output of the first stage amplifier was connected to an oscilloscope and each time a photon produced ionization the output pulse was digitalized and stored. Hundreds of waveforms were recorded and then analyzed with a Python script. The analysis consisted in looking for the baseline of the pulse by averaging the samples before the rising edge and then measuring the pulse height as the difference between the waveform maximum voltage and the baseline level. Figure 8 shows the calculated pulse height histograms for each of the target elements.

With this monolithic detector it was possible to distinguish the most intense emission lines of each of the elements used in the experiment, although the resolution does not allow to resolve between the copper $K_{\alpha 1}$ and $K_{\beta 1}$ emissions.

The emission peaks were fitted with a gaussian curve in order to extract their mean pulse height and standard deviation. These values were used in figure 9 to plot the pulse heights against the

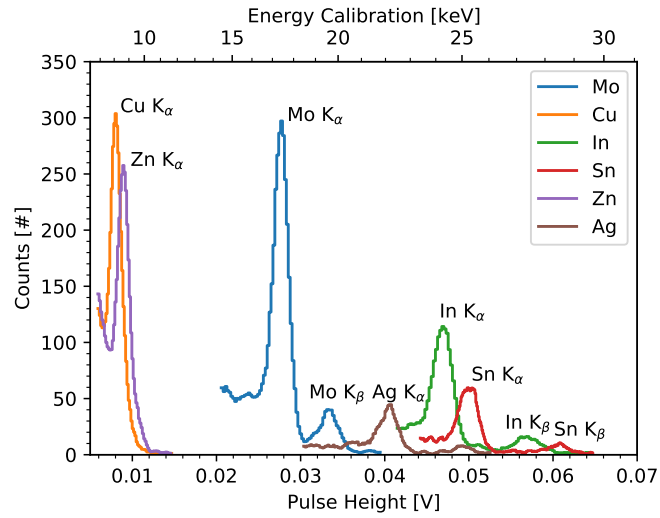


Figure 8. Measurement of the pulse height histogram for each of the elements used in the experiment. They were obtained by monitoring the output voltage of the first stage of a single pixel located at the edge of the matrix. Only the peak part is shown for clarity. The top energy axis was calculated according to the energy calibration of figure 9.

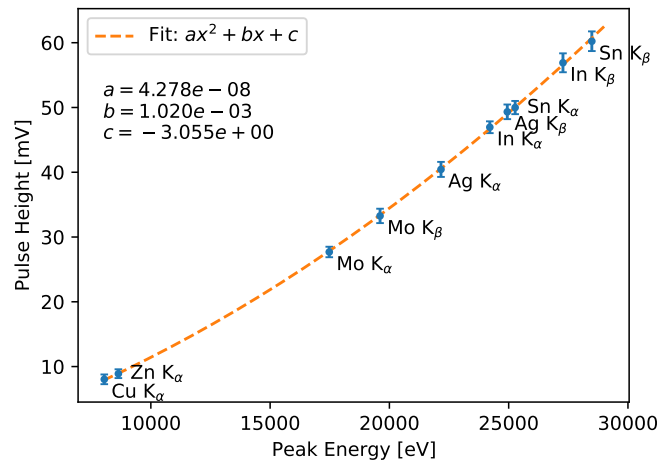


Figure 9. Pulse-height vs. energy curve. The energy of the emission lines was taken from the table 2 and its amplitude by fitting the peaks of figure 8 with a gaussian curve and taking the mean value. The error bars represent the standard deviation of the fits.

energy of the emission lines listed in table 2, obtaining in this way the energy calibration curve. The response is slightly non-linear and so it was fitted with a quadratic function. The fitting function was then used to generate the top energy axis seen in figure 8.

The standard deviation of the Molybdenum K_α peak resulted in 458 eV, which can be translated to an Equivalent Noise Charge (ENC) in silicon of 127 e⁻rms. Due to the slightly non-linear response the gain is a bit higher at higher energies, so doing the same for the Indium K_α peak gives 122 e⁻rms. These numbers are similar to the standard deviation obtained in reference [17] for a ⁵⁵Fe K_{α} peak (5.9 keV), and slightly higher than the standard deviation obtained with a hybrid detector [21, 22].

In order to measure the noise generated solely by the first stage amplifier, the X-ray source was shut off and the analog output was sampled with the oscilloscope at a rate of 5 Gs/s during a time span of 200 μ s. The obtained signal has a gaussian noise distribution with a standard deviation of 0.89 mV, that is equivalent to 100 e⁻rms of noise charge, so most of the noise is introduced by the first stage amplifier.

It can be seen in figure 8 that the peak have tails toward their left. These tails are produced by the incomplete charge collection (ICC) at the sensor diode. Photons ionizing the silicon below and outside the depletion zone produce charge that can diffuse and escape from the collection node, leading to smaller voltage pulses.

3.2 Time-over-Threshold

In this section the results of the measurements using the ToT mode are presented. The clock used for counting the ToT was set to 200 MHz, so a digital unit represents 5 ns in time. As before, the sensor junction was biased at 60 V.

In this case, instead of reading just one pixel, ToT counts are acquired from the whole matrix, one value per pixel, and these values are used to create an X-ray spectrum by generating a histogram. In this case, the calibration of the sensor's response is needed due to the pixel to pixel variation and thus the procedure described in section 2.4 was followed by using the test pulse input as stimulus. The baseline voltage was set to 900 mV and the threshold level to 885 mV, the second right below the voltage at which spurious counts are generated by noise. After calibration, triggering the sensor 4200 times with the same pulse gives a gaussian distribution of ToT with standard deviation of 4 units. Knowing that each unit represents 5 ns, this means that, for the same input, 68% of the times the measured ToT will lay in a 20 ns interval around its mean value. The baseline and threshold voltages were maintained for all measurements.

Figure 10 shows the obtained Time-over-Threshold histograms for the different target elements. The measurements were performed including ToT counts of the whole matrix after calibration. The principal emission lines are evident, although the energy resolution in this case is worse than using the pulse height of the first stage, as in figure 8. In this case the peaks have a long tail towards the left, effect that will be discussed in the next section. Also the spectrums of Cu and Sn have a notable contribution between 20 and 40 ToT counts that correspond to lead impurities. This is explained because the set of targets used in this case is different than that of section 3.1.

Again the pulses were fitted but this time using bimodal distributions in order to have a better fitting in the cases of mixed principal and secondary emissions. The mean and standard deviations along with the energy of the X-ray photons of table 2 were used to generate the calibration curve of figure 11. The figure also shows a second order polynomial line that fits the data points. The

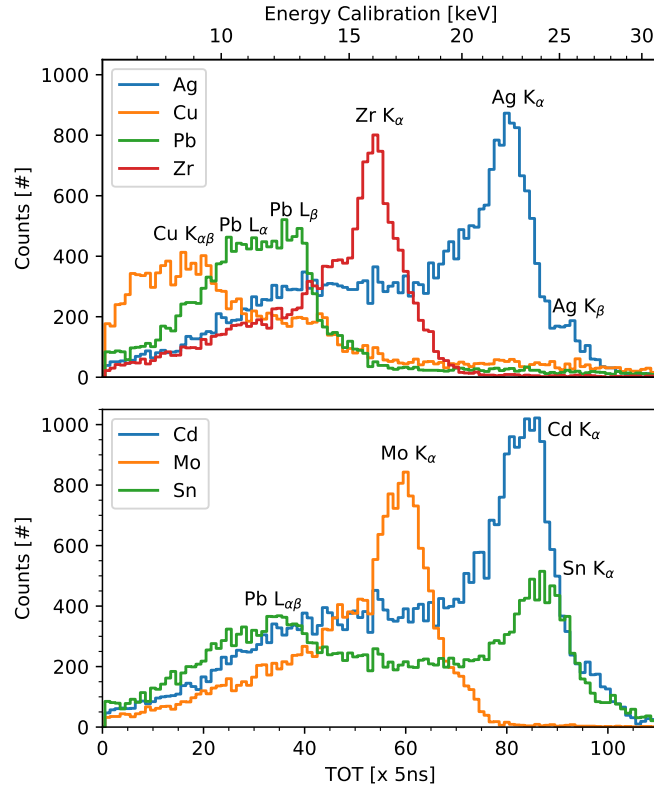


Figure 10. ToT histograms for each of the elements used in the experiment. The top energy axis was calculated according to the energy calibration of figure 11.

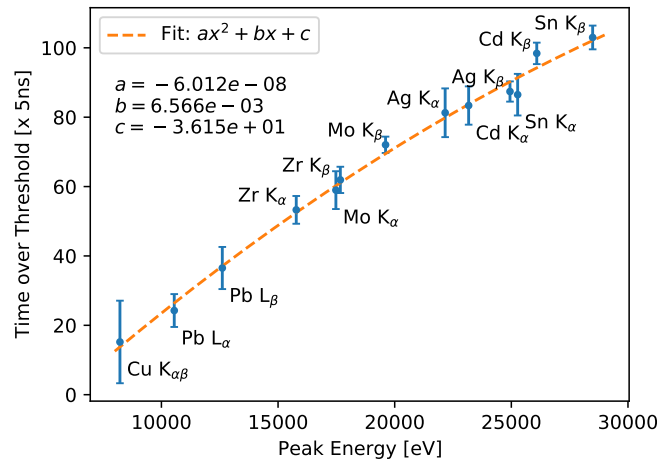


Figure 11. ToT vs. energy curve. The energy of the emission lines was taken from the table 2 and values in the y-axis were obtained by fitting the peaks of figure 10 with bimodal curves. The error bars represent the standard deviation of the gaussian model.

coefficients obtained from this fit were used to generate the energy calibration top axis in figure 10. The ToT response is slightly non-linear and spans from 8 keV to 30 keV equivalent to 15 to 103 ToT counts, with a slightly better resolution for photons of higher energies.

For the Mo peak, the standard deviation is 5.5 ToT counts, equivalent to 1 keV or 276 e^- rms of ENC. It was mentioned before that the response to the test pulse input has a standard deviation of 4 ToT counts and this can be translated to 200 e^- rms of ENC. So the pixel response calibration is the main contributor to the low energy resolution in the ToT mode.

The reason of the low number of ToT counts in figure 10 is because the detector was designed for an energy range from 8 keV to 100 keV, so a big part of the 10-bit range was not used in these experiments. A faster clock would have extended the range, but it was not possible with the current setup and LVDS I/Os.

Another thing to notice in the ToT histograms of figure 10 is that the peaks have a long tail towards the left. This is the same ICC effect that was explained in section 3.1.

4 Conclusions

With the monolithic and pixelated ionizing radiation detector presented in this work it was possible to count and measure the energy of X-ray photons. The fabrication process allows the fabrication of an n-type implant below the buried oxide that can be connected through the BOX with the active electronics. A reverse voltage of up to 110 V can be applied to the buried device, although for this work 60 V have been used. With the standard handle wafer resistance, the depletion region extends approximately 25 μm into the p substrate at 60 V and this affects the charge collection efficiency of the device. The possibility of using a high-resistivity substrate will be studied in order to increase the depth of the depletion region.

The MAPS includes both analog and digital processing. It has been shown that the analog part is comprised by two cascaded amplifiers. The first stage has been characterized by using X-ray fluorescence photons and as part of the experiments the emission lines of several materials were obtained and distinguished. The emission peak of a Molybdenum target was obtained with a standard deviation of 127 e^- of ENC and the noise introduced by the amplifier itself accounted for 100 e^- rms. These numbers are slightly better than other works using the same technology [17].

Another characteristic of the analog electronics is the addition of a second stage whose purpose is to add the charge generated in neighboring pixels, although this operation mode has not been completely tested yet and will be reported in future works.

The digital part has several operation modes that allow the counting of particles, the counting of the ToT and include the special *hit* mode in which the pixel operation gets locked after detecting a particle hit until a read cycle has been performed. The matrix readout is governed by the scan chain and this reduces the amount of data transferred outside chip. This technique would significantly reduce the access time in large arrays. X-ray fluorescence spectra of various materials were obtained using the ToT mode with an ENC as high as 276 e^- .

This ASIC has proven to be useful for the detection of X-ray photons and to perform a basic energy discrimination. Taking advantage of its energy and spatial resolution, future works will explore the possibility of using BUSARD covered with conversion layers for the detection of

thermal and epithermal neutrons, a technique that was studied by using commercial CMOS image sensors [23, 24].

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