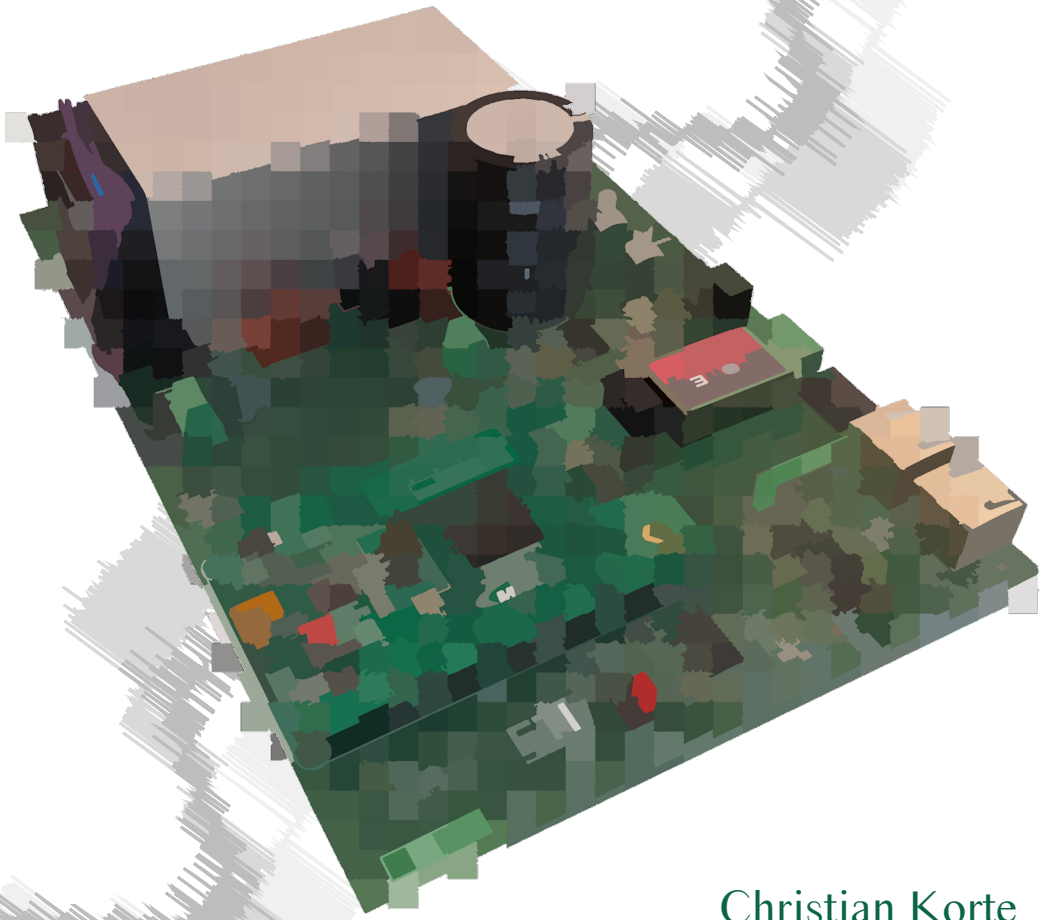
Analysis, Design, and Control of a Modular Multilevel Series-Parallel Converter (MMSPC)



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Analysis, Design, and Control of a Modular Multilevel Series-Parallel Converter (MMSPC)

Zur Erlangung des akademischen Grades eines

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Korreferent: Prof. Dr.-Ing. Dieter Gerling
(Universität der Bundeswehr München)

Vorwort

Diese Arbeit entstand während meiner Tätigkeit als wissenschaftlicher Mitarbeiter am Elektrotechnischen Institut (ETI) des Karlsruher Instituts für Technologie (KIT). Im Rahmen einer wissenschaftlichen Kooperation hatte ich die Möglichkeit einen neuartigen Ansatz zur Realisierung des elektrischen Automobil-Antriebsstrangs zu erforschen.
Dieser Ansatz, der Modular Multilevel Series-Parallel Converter (MMSPC), zieht eine umfassende Umgestaltung der elektrischen Automobil-Architektur nach sich. Aus diesem Grund habe ich mir die Aufgabe gesetzt, einen möglichst fundamentalen wissenschaftlichen Vergleich zwischen dem herkömmlichen Ansatz und dem MMSPC zu erarbeiten. Ferner habe ich mich darauf konzentriert, die Leistungsfähigkeit des MMSPC durch Regelung zu erhöhen.
Ohne die durchgehende Unterstützung aus meinem privaten und beruflichen Umfeld wäre es nicht möglich gewesen, diese Arbeit erfolgreich abzuschließen. Dafür möchte ich mich bei allen Beteiligten herzlich bedanken.
Insbesondere gilt dieser Dank meinem Doktorvater Prof. Dr.-Ing Marc Hiller, der es mir ermöglicht hat mit großer wissenschaftlicher Freiheit an meiner Arbeit zu forschen. Bei Prof. Dr.-Ing Dieter Gerling bedanke ich mich ebenfalls für die Begutachtung und die Übernahme des Korreferats. Zudem möchte ich mich bei Prof. Dr.-Ing Malte Jaensch und Prof. Dr.-Ing. Stefan Götz bedanken, für das entgegengebrachte Vertrauen und die große Unterstützung während meiner Tätigkeit bei Porsche Engineering.
Ohne die außergewöhnliche Atmosphäre und Kollegialität am ETI wäre die Entstehung dieser Arbeit mit deutlich weniger Freude und guten Erinnerungen verbunden. Dafür bedanke ich mich bei allen Kollegen und Studenten des ETI, mit denen ich das Vergnügen hatte zu Arbeiten.
Mein Dank richtet sich insbesondere an Daniel, für die viele Hilfe bei meinen Publikationen, dafür dass Du immer die Wissenschaft am ETI vorangetrieben hast und vor Allem für die ganzen unvergesslichen Erlebnisse die wir geteilt

haben. Weiterhin möchte ich mich bei Firat, Patrick, Simon, Felix, Felix und Tobi für Eure andauernde Unterstützung und die großartige Zeit bedanken.
Seit meiner Kindheit haben mir meine Eltern und (meistens) meine Schwester jederzeit den Rückhalt gegeben, den ich benötigte um erfolgreich meine Fortbildung und meine Promotion zu bestehen. Dafür bedanke ich mich herzlichst, denn ohne Euch hätte es nicht klappen können.
Während meiner Promotion hat Ravina am meisten miterlebt, wie ich mit der Arbeit gekämpft habe. Dennoch hast Du mir immer geholfen das Beste aus mir herauszuholen und immer an meinen Erfolg geglaubt. Danke dafür und dass Du eine wundervolle Freundin bist!

Kurzfassung

Seit der Einführung des Tesla Roadster in 2008 haben sich elektrische Antriebe für seriengefertigte elektrische Fahrzeuge stetig weiterentwickelt. Trotz einer Vielzahl wissenschaftlicher Publikationen über alternative Umrichtertopologien für den Automobileinsatz, kamen bisher ausschließlich Zweitpunktumrichter in signifikanter Stückzahl zum Einsatz. Diese Entwicklung ist insbesondere auf wichtige Vorteile wie eine hohe Effizienz, niedrige Kosten und technologische Reife des Zweipunktumrichters zurückzuführen.
In dieser Arbeit wird eine neuartige Multilevel-Umrichtertopologie, welche die Reihen- und Parallelschaltung von Umrichter-Submodulen erlaubt, auf ihre Anwendbarkeit als Automobilumrichter in zukünftigen Fahrzeugen untersucht. Hierbei wird die Topologie, der *Modular Multilevel Series-Parallel Converter (MMSPC)*, mit dem Zweipunktumrichter und mit dem kaskadierten H-Brücken-Umrichter (*Cascaded H-Bridge (CHB)*) verglichen. Insbesondere wird die Wechselwirkung zwischen Batterie und Umrichter betrachtet.
In Kapitel 2 wird der Stand der Technik von Leistungselektronik und Energiespeichern in elektrischen Fahrzeugantrieben dargestellt. Anschließend wird in Kapitel 3 ein neuartiger Ansatz zur Analyse der verschiedenen Umrichtertopologien und der damit verbundenen Energiespeicherkonfigurationen präsentiert. Durch geeignete Vereinfachungen werden die fundamentalen Unterschiede zwischen den Systemen mit getrenntem Zwischenkreis (MMSPC und CHB) und dem Zweipunktumrichter ersichtlich. Dieses Kapitel beschreibt und quantifiziert einen fundamentalen Nachteil der kaskadierten Umrichter: gegenüber Zweipunktumrichtern mit vergleichbaren Eigenschaften führt die Verteilung der Zwischenkreise zu einer um mehr als 20% höheren Effektivstrombelastung der Batterien.
Kapitel 4 analysiert die Schaltung des MMSPC und vergleicht diese mit der des CHB, um die Vor- und Nachteile der Submodul-Parallelschaltung zu erörtern. Ein neuartiger Modellierungsansatz zur Untersuchung der Umrichter erlaubt es,

verschiedene Modulationsverfahren auf deren Leistungsfähigkeit zum Ladezustandsausgleich (*balancing*) und hinsichtlich der erreichbaren Batterieeffizienz zu vergleichen. Es wird eine optimale Modulationsstrategie für beide Umrichter beschrieben, anhand derer die Unterschiede ersichtlich werden.
Während der MMSPC durch die Parallelschaltung die Verluste der Batterien gegenüber dem CHB deutlich reduzieren kann, verringert dies gleichzeitig die verfügbaren Freiheitsgrade für den Ausgleich der Ladezustände der Submodule. Es wird hergeleitet, warum ein Ausgleich der Ladezustände aller Submodule beim MMSPC bei effizienzoptimaler Modulation nicht möglich ist. Darüber hinaus wird eine Entwurfsmethodik für die Submodule dargestellt, welche die Strombelastungen möglichst optimal zwischen der Ladungsübertragung (*charge transfer*) der Batterie, seiner Doppelschichtkapazität und des Zwischenkreiskondensators verteilt.
In Kapitel 5 wird eine neue Regelung für den MMSPC vorgestellt. Auf Basis der vorherigen Analysen wird die Common-Mode-Spannung des Umrichters genutzt, um durch eine Optimierung der Frequenzspektren der Batterieströme die Effektivstrombelastung der Batterien zu minimieren. Durch diese Regelung kann eine höhere Effizienz des MMSPC ohne Einschränkung des Arbeitsbereichs erreicht werden. Des Weiteren wird ein nachgelagertes Verfahren beschrieben, welches die Ladezustände der Umrichterphasen ausgleicht.
In Kapitel 6 werden Analyse, Entwurf und Regelung des MMSPC anhand simulativer und experimenteller Ergebnisse validiert und die resultierenden Eigenschaften mit anderen Umrichtertopologien verglichen. Die Simulationsergebnisse heben die Vor- und Nachteile des MMSPC bezüglich Effizienz und Arbeitsbereich gegenüber den anderen Umrichtern hervor. Über einen WLTP-Fahrzyklus kann die Effizienz im Vergleich zu Zweipunktumrichtern und dem CHB gesteigert werden.
Anhand eines Labor-Prototypen wird daraufhin eine FPGA-Echtzeitimplementierung des vorgestellten Regelungsverfahrens für den MMSPC beschrieben. Die Messergebnisse zeigen, dass die eingeprägte Common-Mode-Spannung den Effektivstrom der Batterien um ca. 4% reduziert und gleichzeitig ein Angleichen der Ladezustände der Batterien zulässt.

Contents

Chapter 1

Introduction

Current research in electric vehicle (EV) technology is continuously striving for improved efficiency, weight and cost in the technologies comprising the vehicle powertrain. Despite large academic interest and numerous novel power electronic converters topologies introduced in recent years, the maturity of state-of-the-art converters is so high that improvements generally only occur incrementally. Advances in automotive converter design are often based on the advances of semiconductor materials from which the power electronics are made. For example, the silicon (Si) insulated-gate bipolar transistor (IGBT) is being replaced by silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET), increasing the switching speed and reducing the losses of the converters. In the future more advanced materials such as gallium nitride (GaN) may also be used, as well as more advanced topologies such as the three-level (3L) converter.

The Modular Multilevel Series Parallel Converter (MMSPC)—first presented in 2010—is the focus of this work, in which its characteristics are analysed and compared [F1]. Furthermore, its advantages and disadvantages are highlighted and contrasted to established technologies. There have been numerous academic publications about the MMSPC in recent years, focussing on its design and control in various applications, however there has been no comprehensive analysis of its traits in comparison to similar converters for an EV.

Here, the MMSPC is investigated in different levels of abstraction to give the reader a deep understanding of the MMSPC's qualities and limitations. In contrast to many previous works, the converter and battery are analysed together, as the choice of converter has a significant effect on the battery loading. In

chapter 3, high-level assumptions are made revealing the fundamental differences between the MMSPC and conventional powertrain architectures. A series of easy-to-use equations are derived, allowing an engineer to quickly understand and analyse the basics of the MMSPC.
Following from this, chapter 4 dives into the numerous important aspects of the design of the MMSPC, and gives guidelines for the component choice and sizing. This section highlights the effects of the parallel mode of the MMSPC through rigorous mathematical analysis, illustrating its ability to improve converter efficiency, while simultaneously impeding the balancing of sub-modules.
Chapter 5 proposes a new control scheme for the MMSPC, based on the findings presented in the Analysis, which allows the converters efficiency to be maximised by manipulation of the converter's common-mode voltage.
Finally, in chapter 6, the findings of the analysis, design, as well as the proposed control scheme, are verified in simulation and on an experimental test bench. Simulations show that the MMSPC can surpass state-of-the-art converters in terms of efficiency over an entire EV drive cycle. A dedicated, custom-built laboratory prototype validates the feasibility of the converter on a machine test bench, and shows the proposed control scheme can be implemented on a real-time system to reduce the losses of the MMSPC while ensuring stable operation.

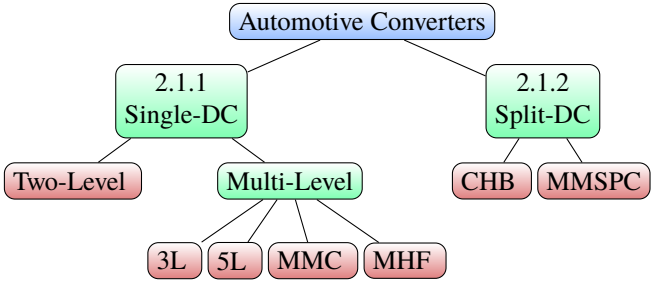
Chapter 2

Literature Review

This section examines the origins, requirements, and research of state-of-the-art automotive power electronic and energy storage systems. First, different converter types are discussed and compared. Second, the control of multilevel power converters in the context of this work is introduced. Third, the interactions of powertrain batteries and power electronics are discussed, and the battery models used are presented. At the end of the introduction, a short recapitulation of the previous works of this area is given and the objectives of this thesis are outlined.

2.1 Converters in Automotive Applications

Modern automotive powertrains require power electronic converters to convert the direct current (DC) energy of the energy storage (conventionally lithium-ion batteries) to alternating current (AC) power for the electric motor [F2]. In automotive high-volume applications, the two-level (2L) converter is the most commonly used topology. While the majority of power converters currently use Silicon IGBTs for the converter switches [F3], there is a trend towards SiC MOSFETs, for example used in the Tesla Model 3 [F4].
In this section, numerous different possible converter topologies for automotive powertrains are presented, classified and briefly discussed. The topologies are divided into converters with a single (common) DC-link and converters with multiple DC-links (henceforth called split-DC converters). It should be noted that in this work, the battery poles are defined to comprise the DC-link(s). As such, some converters that have many DC capacitors but only one monolithic



CHB	Cascaded H-Bridge
MMSPC	Modular Multilevel Series-Parallel Converter
3L	Three-Level Converter
5L	Five-Level Converter
MMC	Modular Multilevel Converter
MHF	Modular High-Frequency Converter

Figure 2.1: General classification of automotive converters

battery—such as the Modular Multilevel Converter (MMC)—are considered to be single-DC converters.
Until today, all production EVs have used a single DC-link for their converters. There has however been research into alternative battery and converter topologies, which is discussed here. First, the relevant converter and battery topologies with single DC-links are presented, followed by split-DC converter-battery topologies.
Figure 2.1 visually depicts the categorisation of the investigated converters, according to a proposed classification scheme. It should be noted that while there has been a vast amount of research into different converter types, only the three-phase 2L converter has been used in mass-production EVs.

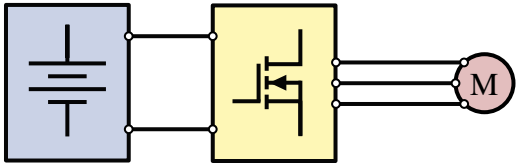
2.1.1 Single DC-Link

In the following, various single DC-link converters are presented and their advantages and disadvantages are briefly introduced. The basic structure of all single DC-link converters is shown in fig. 2.2 (a). While most automotive con-

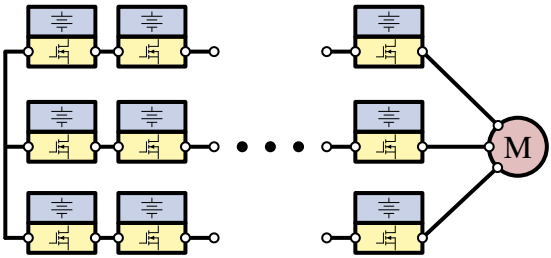
verters connect the DC-link of the converter directly to the battery poles [F5], this structure also allows a boost converter to raise the converter's DC-voltage at the expense of additional semiconductors and inductors. For the purpose of this comparison, the use of boost converters is not considered as their use in series produced EVs is diminishing. This is because the benefit of allowing the DC-link voltage to vary independently of the battery voltage is outweighed by the increased cost and complexity of the DC-to-DC (DCDC) converter, while the efficiency of the system is only marginally improved [F6].
The separation of energy storage and DC-to-AC conversion in single-DC converters has led to the ever deeper integration of the converter with its load, the AC motor. This allows a car's topology to be modular and simplifies the design of EVs with additional motors as options at an extra cost. This is significantly more complex with split-DC converters, where the power electronics is necessarily integrated with the batteries. Furthermore, the presence of a single DC-link facilitates the connection of high-power aggregates, such as air-conditioning, heating and cooling systems [F7].

2.1.1.1 Two-Level Converter

Since the introduction of the first mass-produced lithium-ion battery EV, the Tesla Roadster [F8], the 2L converter has dominated the automotive converter domain. Its most significant benefits are its simplicity, low cost, and proven track record since the introduction of the first switching semiconductors [F9].
The disadvantages of the 2L converter are the relatively low output voltage quality, as only two voltage levels are available for the synthesis of the output AC voltage, a high blocking voltage requirement of the semiconductors (maximum battery voltage), and the fact that the entire battery voltage is switched at once, causing severe electromagnetic interference (EMI). The large electromagnetic transients may also cause further issues such as isolation damage and bearing currents. While the principle design of automotive converters has remained the same since their inception, there is significant development and research of their continuous improvement, especially in the fields of integration, cooling and control [F10].
As the 2L converter is widely adopted in past and state-of-the-art EVs, it is used as the reference against which the advantages and disadvantages of the following converters are compared.



(a) Single-DC converter



(b) Split-DC converter (wye-connected)

Figure 2.2: Schematic comparison of three-phase single-DC and split-DC converters. While single-DC converters have only one battery and power electronic unit, the split-DC converter has several batteries and power electronic units in each phase. These are called sub-modules (SM).

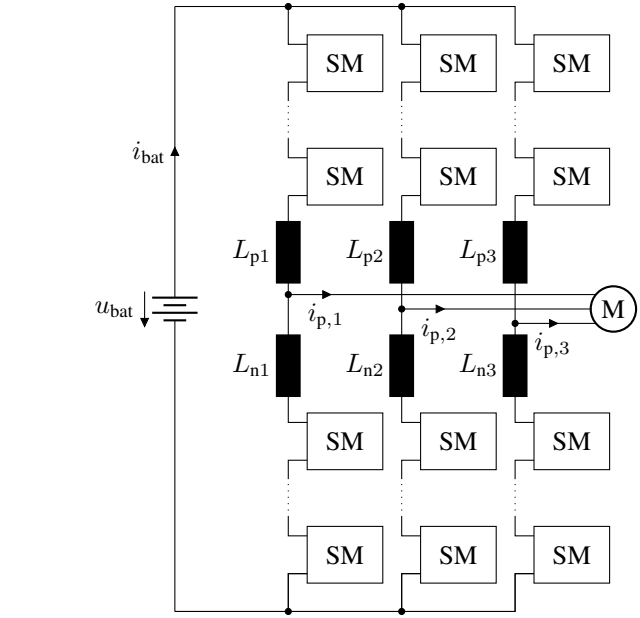
2.1.1.2 Three-Level Converter

The 3L converter is closely related to the 2L converter but provides an additional voltage level at the output of each phase. The earliest 3L converters were introduced in the 1970s [F11, F12] and have been investigated for EV applications recently (e.g. [F13]).
There are several different variations of the 3L, such as the (active) neutral point clamped ((A)NPC) 3L converter, the T-type 3L converter or the flying capacitor 3L converter [F14]. Benefits of the 3L converters include a higher quality output voltage than the 2L due to the additional output voltage level, better efficiencies at higher frequency, and reduced EMI. Furthermore, most semiconductors only require half the voltage rating of 2L converters, although more semiconductors are required. The efficiency of 3L converters can reach and surpass those of 2L converters for automotive applications [F15], while the required chip-area is dependent of the exact topology used, but can be lower than that of 2L converters [F14, F16].

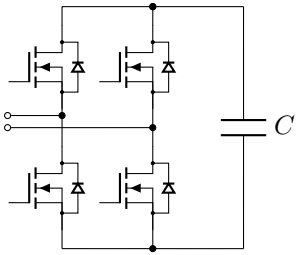
Despite these advantages, the 3L converter has not yet found use in EVs other than a few prototype applications [F17]. This is largely due to its higher cost than 2L converters as a result of the increased number of semiconductors. A further disadvantage is the significantly more complicated control, as the DC capacitors must be actively balanced by the control algorithm to allow steady-state operation.
Increasing the number of levels further, the 3L topologies can be extended to five, seven or more levels. As the number of levels increases, the number of semiconductors and complexity also greatly increase, making the application over these converters in automotive converters unlikely in the next few generations of EVs.

2.1.1.3 Modular Multilevel Converter

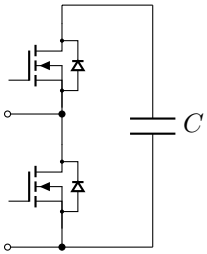
Reducing the complexity of the previously discussed multilevel converters, modular converters with multilevel output waveforms have been patented in the 1970s [F18] and studied in detail since the 1990s [F19, F20]. These converters allow modular SMs to be connected as a cascade, thereby allowing an arbitrarily high output voltage with much lower SM voltages, and therefore semiconductor voltage ratings. Modular converters with multilevel output waveforms can have both a single DC-link or numerous DC-links. In this subsection, only single DC-link multilevel converters are treated, while section 2.1.2 discusses cascaded converters with multiple batteries.
The most significant converter of this type is currently the MMC (fig. 2.3), presented for the first time in 2002 by Rainer Marquardt [F21] and studied extensively since [F22–F24]. The MMC commonly uses full-bridge (fig. 2.3 (b)) or half-bridge (fig. 2.3 (c)) SMs, depending on the application. Using full-bridge SM allows the converter to provide DC fault-blocking and a reverse polarity SM output at the expense of additional component cost. The MMC has been deployed in high voltage direct current (HVDC), static synchronous compensator (STATCOM), and large motor drive applications in the medium voltage range (>1 kV), but has not been developed in series production for low-voltage applications.
The advantages of the MMC include its high output voltage bandwidth, scalability to any desirable voltage level, redundant fault-tolerant design, reduced hardware complexity compared to non-modular multilevel converters at high level numbers, and the fact that no central DC-capacitor is needed. In automotive applications, the use of modular multilevel converters allows the use of Si MOSFETs in place of Si IGBTs, with the advantage of better low-load efficiency due to their ohmic nature. Significant disadvantages are the high control complex-



(a) Overview of the MMC

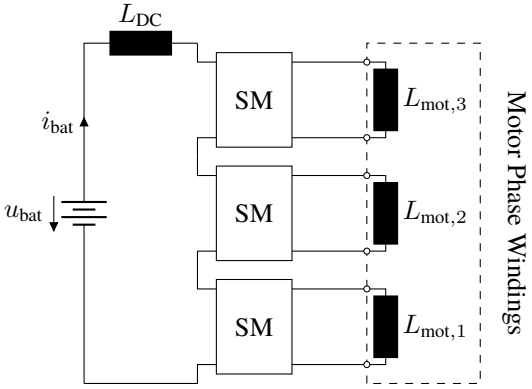


(b) Full-Bridge MMC sub-module

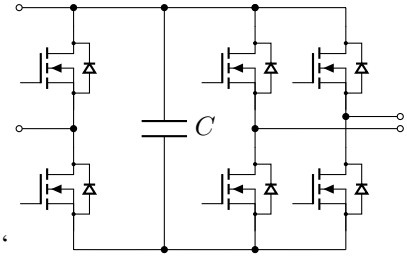


(c) Half-Bridge MMC sub-module

Figure 2.3: The MMC for an automotive application. The sub-modules (SM) can be implemented either as a full-bridge or a half-bridge SM.



(a) Overview of the Modular High-Frequency Converter (MHF)



(b) SM of the MHF

Figure 2.4: The MHF for an automotive application

ity, and in comparison to 2L converter far larger number of semiconductors and capacitors required.
As a result of the complexity and the associated cost, the MMC has not been investigated for vehicle use beyond academic research [F20, F25–F27].

2.1.1.4 Modular High-Frequency Converter

Based on the MMC, the MHF was introduced as a modular converter for applications in EVs, as shown in fig. 2.4. The MHF reduces the number of SMs required for realistic designs for the automotive voltage range (200 V to 1000 V), and reduces the size of the capacitors required [F28]. These improvements arise at the

cost of an additional inductor required in the DC-link and the need to connect each end of the stator windings of the motor separately. At the time of writing, the MHF has not found use in vehicular applications.

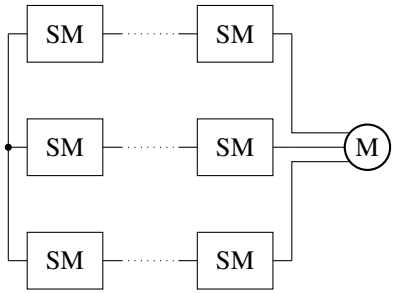
In addition to the converters mentioned, a myriad of alternative converter topologies has been introduced and investigated, primarily in academic research, to improve on the conventional 2L converter. Despite these efforts, the robustness, simplicity, and low cost of the 2L have not been overcome in the cost and reliability-driven automotive industry. Therefore, this work will use only the 2L converter as a benchmark from the single-DC converters when evaluating the benefits of the MMSPC.

2.1.2 Split-DC

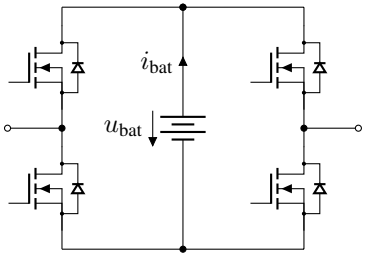
While current state-of-the-art EVs use monolithic battery packs for energy storage, there can be advantages to dividing the battery and associated power electronics into smaller modular units. These types of battery-converter systems are called split-DC converters here, of which two are analysed in detail in this work.
In general, split-DC converters divide the battery energy storage into several SMs, which are then connected in series to form a converter arm, corresponding to a converter phase. The generalised structure of a wye-configured split-DC converter is depicted in fig. 2.2 (b), in which all three phases are connected at the so-called neutral point. While there are numerous different ways to connect the modular SMs to a converter system—such as delta-configured—only the simplest form depicted in fig. 2.2 (b) is discussed here.
The split-DC SMs can have the battery directly connected to their DC-link capacitance, or indirectly linked for example with a boost converter [F29, F30]. In this work, only directly-linked batteries are considered, as the additional cost and weight of the boost converter is deemed too large for automotive applications.
Several different split-DC converters are presented, including the MMSPC, which is the focus of this work. Following this section, a generalised comparison of single DC-link converters and split-DC converters is presented.

2.1.2.1 Cascaded H-Bridge Converter

The cascaded H-bridge (CHB) with isolated energy sources was the first modular multilevel converter topology converting DC to AC current, patented in 1975 by Baker and Bannister [F18]. The topology of the CHB with integrated batteries



(a) Overview



(b) SM of the CHB

Figure 2.5: CHB Topology for automotive drives

is shown in fig. 2.5. Since then, it has been investigated in many applications, and in recent years there has been significant interest in the use of CHB converters in EVs. One of the earliest mentions of the use of a CHB for automotive applications was in 2002 by Tolbert et al. [F31].
The CHB can be seen as the simplest form of a cascaded multilevel converter for an automotive application, stringing together SMs consisting of a battery and a H-bridge in series to form a phase [F32]. While multilevel converters generally have SMs with equal voltages, it is also possible to efficiently operate the CHB with varying module voltages [F33]. Assuming that all SMs have the same rated voltage, the minimum semiconductor blocking voltage u_{SC} required is:

$$u_{\text{SC}} = \frac{\max(u_{\text{p}})}{N}, \tag{2.1}$$

where $\max(u_\mathrm{p})$ is the maximum required phase-to-neutral voltage amplitude, and N is the number of SMs.
There has been a significant amount of research published on the CHB showing that, from a technical perspective, the performance of the converter can surpass that of a 2L converter [F27, F29, F32, F34], with some work suggesting that the CHB is the cheaper solution as well [F27].

2.1.2.2 Modular Multilevel Converter

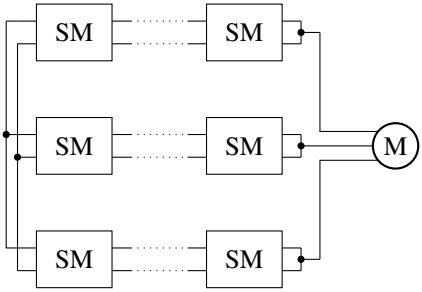
The MMC with batteries integrated into the SMs is another modular multilevel topology that has been proposed for automotive application [F35]. While the required number of SMs is four times as high as a comparable CHB (if the same SM voltage is used), it offers the advantage of a DC-link which can be used for auxiliary power consumers and charging. For the MMC with integrated batteries, the minimum semiconductor blocking voltage u_SC required is:

$$u_\mathrm{SC} = 4\frac{\max(u_\mathrm{p})}{N}, \tag{2.2}$$

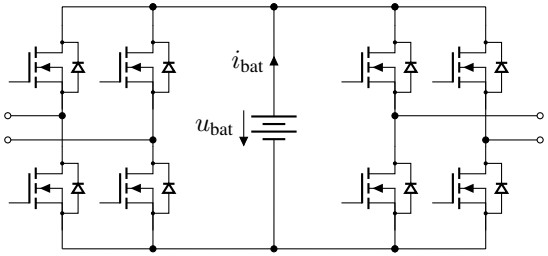
as each converter arm must be able to block the entire output phase voltage. A disadvantage of the MMC in this form is the fact that each arm needs an inductor between its output and the motor terminal [F36].
Similar to the CHB, the MMC has been shown to be promising for EV application in academia [F25, F37], but there has been no indication of the automotive industry seriously considering an application in a series production EV.

2.1.2.3 Modular Multilevel Series-Parallel Converter

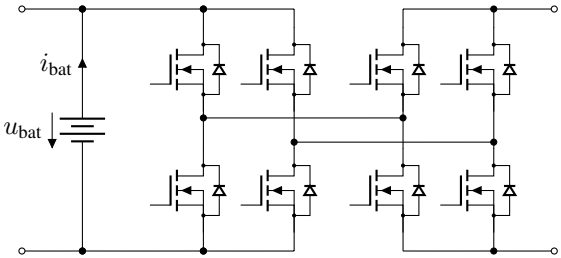
In 2010, a further development of the MMC was patented [F1], now known as the MMSPC. The advancement from the classical MMC is the fact that a SM in a phase string can be connected in series as well as in parallel to its neighbouring SMs [F38, F39]. The MMSPC exists both in the topology of the MMC, with two converter arms per phase, as well as in the topology of the CHB, as shown in fig. 2.6. Other topologies allowing the parallel connection of SMs have also been proposed, such as by Ilves et al. [F40]. In this work, only the CHB-like topology is analysed as it results in a simpler and cheaper converter more suited to EV use.
The parallel connection allows the resistance of a phase to be reduced, and facilitates the equalisation of SM voltages, especially in applications where the SMs contain only capacitors. While the MMSPC has twice the number of



(a) Overview

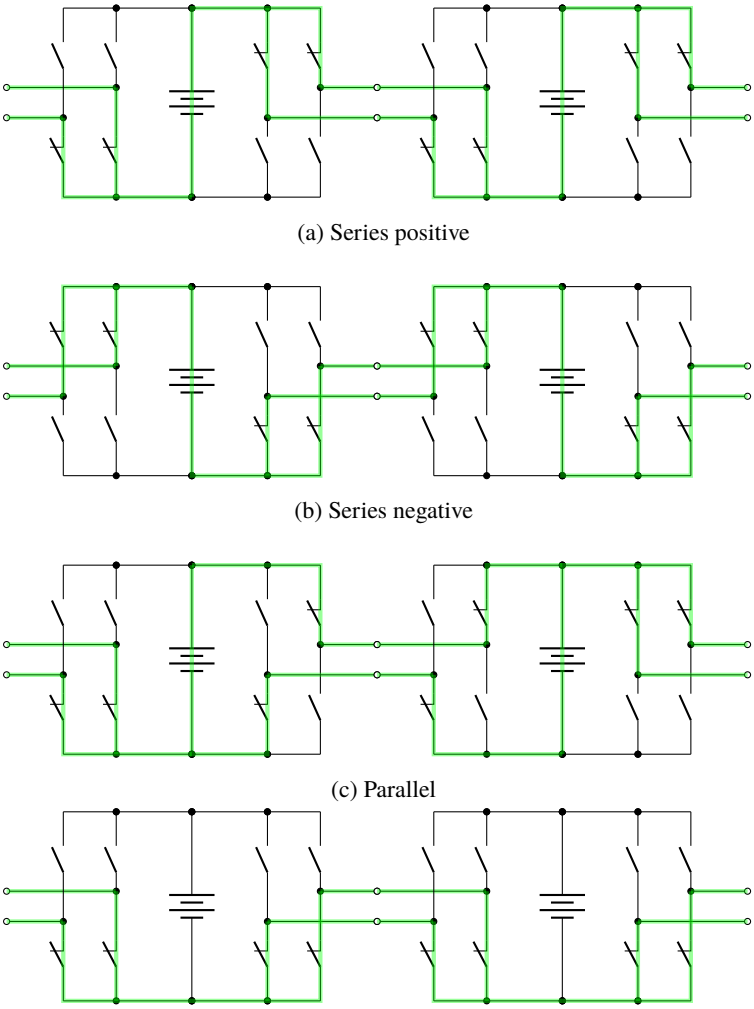


(b) Symmetrical SM



(c) Asymmetrical SM

Figure 2.6: Overview and SM topologies of the MMSPC. The SMs are shown in both the the symmetrical and asymmetrical design.



(a) Series positive

(b) Series negative

(c) Parallel

(d) Bypass negative

Figure 2.7: The different possible switching states of the MMSPC SM. In addition to the displayed bypass negative, the bypass positive is also possible, where the current flows along the positive battery terminal.

semiconductors as a CHB for the same voltage and current, the MMSPC's semiconductors only need to be rated for half the current. As a result, the total required semiconductor area of the CHB and MMSPC is the same. The required semiconductor blocking voltage is also given by eq. (2.1).
In normal operation, the MMSPC SM allows four different switching states, as shown in fig. 2.7:

1. Figure 2.7 (a): Series positive, connecting the battery in the phase with a positive polarity.
2. Figure 2.7 (b): Series negative, connecting the battery with a negative polarity.
3. Figure 2.7 (c): Parallel, connecting the battery to a neighbouring SM battery in parallel.
4. Figure 2.7 (d): Bypass negative, not connecting the battery in the phase, allowing the current to bypass it.

The detailed operating principles of the MMSPC are not discussed in detail here, as they have been presented in numerous publications. For more information on how the MMSPC enables the parallel mode, the reader is referred to [F38, F39]. Figure 2.6 shows the design of the SM of the MMSPC, which can be symmetrical or asymmetrical [E1, E2].
While the parallel mode of the MMSPC allows the phase resistance to be reduced, the symmetrical topology shown in fig. 2.6 (b) leads to the half-bridges responsible for the parallel connection being on separate SMs, and likely on separate printed circuit boards (PCB). As a result, communication errors could cause a short across the DC terminals if the two half-bridges do not switch at the same time. By placing all semiconductors responsible for a parallel connection on the same PCB, this problem can be avoided in the asymmetrical SM (see fig. 2.6 (c)).
In this work, the MMSPC is analysed in detail and compared to a conventional 2L converter in an automotive application. Based on the analysis in chapter 3, a design methodology for the MMSPC is presented. The analysis and design of the converter is verified in simulation in section 6.1, based on which an experimental prototype was built to demonstrate the capability of the MMSPC in a laboratory environment. The experimental results are shown and discussed in section 6.2.

2.1.3 Comparison of Single-DC and Split-DC Converters

In this section, the advantages and disadvantages of both single-DC and split-DC converters with regards to the automotive application are discussed. The differences between the different converters and the implications on their performance are shown. The disadvantage of battery ripple current in split-DC converters is highlighted separately in section 2.1.3.3, as it is a focus of this work.

2.1.3.1 Conceptual Advantages of Split-DC Converters

In contrast to common-DC converter systems with monolithic batteries, split-DC systems offer several advantages. A key advantage of most split-DC systems is the modularity of their design. The converter and battery system can be adapted to any voltage level depending on the design of the EV, independently of the semiconductors used. The modular SM allows the same components to be used in applications with significantly different requirements. This can save costs in the design of an EV and facilitate its repair.
Another benefit of using a modular system is the increase in output quality, analogous to multilevel converters with a single DC-link, such as those discussed in section 2.1.1.2. This occurs for two reasons: the number of levels of the output voltage is higher and the permissible switching frequency is higher. The permissible switching frequency increases because the cascaded structure of the converters allows lower-voltage semiconductors to be used—such as unipolar MOSFETs—which allow higher switching frequencies. The increase in output voltage quality can improve the torque control of the motor by reducing the current ripple, while simultaneously reducing the additional losses generated in the motor by high-frequency current components. Furthermore, the increase in number of voltage levels improves the EMI caused by the converter, as the common-mode voltage (CMV) is reduced and the output voltage steps are smaller [F41].
The performance of the EV's battery can also be improved by the use of a split-DC converter because the division of the battery enables active balancing of the SMs. While monolithic batteries generally have no ability to control how the current is divided between the cells in the battery, split-DC systems allow the SMs to be loaded differently. This allows the inherent differences in battery capacity—due to ageing or manufacturing variability—to be counteracted in operation, so that all batteries have an equal state of charge (SoC).
Lastly, the reduction of the blocking voltage of each SM of the converter compared to the overall equivalent DC voltage permits the use of MOSFETs in the

SMs instead of IGBTs. The resistive conduction characteristic of MOSFETs results in excellent low-load efficiency compared to IGBTs, which always have a forward voltage. This can be very important when considering the range of an EV, as most of the time the full drivetrain power is not required. In most standard driving cycles used to evaluate EVs, such as the Worldwide Harmonised Light-Duty Vehicles Test Procedure (WLTP), this is the case.

2.1.3.2 Conceptual Disadvantages of Split-DC Converters

Despite the aforementioned advantages, there are several severe disadvantages of the use of split-DC converters, which are discussed here.
The division of the power electronics of the drive system across all of the SMs means that a high-power PCB is required for each SM. In addition to the PCB itself, gate-drivers and safety electronics are required as well. The cost of these PCB are significant in the extremely cost sensitive automotive industry.
Another disadvantage of split-DC systems is their modularity with regards to the structure of the drivetrain. While the use of SMs allows a single converter to be scaled easily to the desired voltage level, it is not easily possible to increase the number of motors attached to the same energy source. While common-DC systems allow virtually any number of converters and motors to be connected to the DC bus, it is not possible to share the energy in one phase of a split-DC system with another system connected to a different motor without costly additional electronics providing galvanic isolation. As such, the common practice of offering the same EV with a different number of motors in different options is not feasible.
An additional issue arising from the lack of an available battery-voltage DC bus is that the incorporation of high-power auxiliary loads is difficult [E3]. Commonly, EVs use the battery DC-link to supply loads that require in the range of 1 kW to 10 kW of power, such as air conditioning, heating and the supply of the 12 V battery [F7]. The lack of a DC bus means that this equipment must be powered by a different means.
Finally, a significant disadvantage of most split-DC converters is the fact that their structure requires the embedded batteries to supply both AC and DC current. This is discussed further in section 2.1.3.3.

2.1.3.3 Ripple Current in Split-DC Converters

As mentioned previously, a prevalent disadvantage of split-DC converters is the fact that the batteries of the SM must provide both AC and DC current (analysed

in detail in section 3.2.1). This is in contrast to a battery attached to a single battery, where the idealised battery sees only DC current (in a real application, the battery will also experience small AC currents due to semiconductor switching and load changes [F42]).
As the energy delivered by a battery is a result of the potential difference between its electrodes—which is a DC value—it is only capable of delivering active power under DC load. Any additional AC power cannot deliver active power and results in reactive power, only generating losses in the battery. This makes it undesirable for any battery to be subjected to AC currents [F26, F43, F44].
The suppression of the ripple currents in the batteries (and capacitors) in modular multilevel applications has garnered interest in academic research. For converters with capacitors in their SMs, the main goal of the ripple current suppression is to reduce the voltage oscillation of the capacitors [F45, F46], as this reduces the capacitance required, keeping the costs low.
In contrast, modular multilevel converters with integrated batteries do not suffer from this issue. Since the battery acts as a voltage source, the current ripple does not increase the requirement for the installed energy storage. Instead, the ripple current causes additional loss, and with it heat generation, in the batteries. This reduces the efficiency of the converter and could lead to faster battery ageing, which is discussed in section 2.3.2.1.
Several methods have been proposed to reduce the ripple current of integrated batteries in modular multilevel converters. Kersten et al. [F47] propose the use of additional filter capacitors in parallel with the batteries, increasing the cost of the converter. Li et al. [F48] propose a control-oriented approach to reduce the ripple current without any additional hardware. This work proposes a novel control approach based on a rigorous derivation of CHB and MMSPC batteries' ripple current that minimises the root mean square (rms) current seen by the SMs' batteries.

2.2 Control of Multilevel Converters

The control of modular multilevel converters has been investigated in academic research over the past two decades [F23, F49, F50]. Especially for the MMC, the large number of independent currents and the energy stability in the converter arms are difficult to manage [F51].
This section provides a brief overview of the challenges of multilevel converter control, especially the CHB and the MMSPC. First, the balancing and energy control of multilevel converters is discussed, followed by the modulation.

The control of the multilevel converter's load (such as motor current control), is not discussed in detail here. For common loads such as a three-phase grid or an electric motor, the current of the converter is controlled over a load inductance. This can be achieved with conventional controllers, such as proportional-integral (PI) controllers [F23], but many advanced control methods have also been explored such as model predictive control (MPC) and model-based control [F22, F51].
In this work, the output control is kept simple and implemented as a standard field-oriented current controller of the load motor [F52].

2.2.1 Energy and Balancing Control

In addition to the output of the converter, the internal energy of the energy storage elements must be controlled. These can be either the capacitors or batteries. For the MMC and other topologies with multiple arms per phase, this requires the control of internal circulating currents and the control of the DC-link current to allow steady-state operation [F23].
In contrast, for wye-connected cascaded converters such as the CHB, there are no circulating or DC-link currents in the converter arms, and only the phase current of the load passes through each converter arm. Instead, the targets of the energy and balancing control are to maintain the same energy (and therefore voltage) in each SM in a phase. An additional target is to evenly distribute the total energy stored between all phases (these control targets are shared with MMCs).
For multilevel converters without parallel connection, the balancing of the SM within a phase can be achieved by sorting the SMs by their voltage and prioritising the discharge of those with a high voltage and vice versa [F53–F55]. In general, this task is performed by the modulator of the converter, as discussed in section 2.2.2.
For the MMSPC however, this task is more challenging due to the parallel connection of the modules. The parallel connection of the modules means that a module's current cannot be controlled independently of all other modules, as in this case the current is shared between at least two SMs [F39, E1, E2]. This problem is discussed in this work in section 4.2 and has been analysed in a separate doctoral thesis within the same project as this work [E4].
The balance of the energy of a phase is generally achieved by the injection of a CMV to distribute the power delivered by each converter arm [F23]. This can be done independently of the converter type to achieve a balance of energy in the converter. Other methods have also been considered, particularly for some

topologies of the MMSPC that allow power to be transferred across the neutral point of the converter [E4].

2.2.2 Modulation

In power electronics, the modulation has the responsibility of converting a continuous voltage demand to a discrete voltage level that the electronics can manifest at its terminals. For 2L converters, there is one converter switching state corresponding to each possible voltage level (except 0 V), while multilevel converters have multiple converter switching states corresponding to each possible voltage level [F56, F57]. This redundancy in switching states enables the converter to balance the energies of its SMs, as the different switching states will lead to different SMs charging or discharging. The modulation methods discussed can generally be used for any type of multilevel converter, including those with a common DC-link, such as the 3L converter.

2.2.2.1 Fundamental Frequency Switching and PWM

The simplest form of modulation for multilevel converters is fundamental frequency switching [F58]. Similar to block commutation with 2L converters, fundamental frequency switching allows each SM to change its state once per electric period. The choice of level can either occur by rounding, or at predetermined angles for optimal harmonic performance [F59–F61]. Multilevel pulse width modulation (PWM) is also commonly used, with phase-shifted or level-shifted PWM carriers [F57, F62, F63]. Similar to 2L converters, multilevel space-vector modulation (SVM) can also be used instead of PWM to directly include the CMV in the modulation algorithm [F64]. Other modulation methods include spectral control [E5–E8], which controls the spectrum of the converter directly using a model-predictive cost function.
When choosing a modulation scheme, it is important to consider the limitations of the signal-processing capabilities of the converter. For example, if the modulation is calculated on a central processing unit and distributed to the SM via a communication bus, the latency of the bus and the maximum possible transmission frequency may limit the switching frequency and modulation bandwidth of the controller systems. In such cases, it can be advantageous to have a local modulator for each SM instead of a single central modulator [F23].

2.2.2.2 Delta-Sigma Modulation

In contrast to PWM, and the aforementioned modulation methods which modulate the width of the converter pulses, delta-sigma modulation (DSM) modulates the density of the pulses. This has the advantage that the minimum time between two switching instances is much larger than for PWM for the same bandwidth of the modulator. A disadvantage is the fact that the switching frequency is not constant and can become very large for certain modulation indices. First patented in 1946 [F65] and originating from communication technology [F66, F67], DSM has also been employed in power electronics for its computational simplicity and its spectrum shaping ability [F68–F70].
The noise of a DSM is, unlike PWM, distributed across a wide frequency range, minimising the transmitted power at any given frequency. With regular reference signals, spectral tones with large energy density can occur, though these can be suppressed by dithering the input signal [F71]. DSM have been analysed for the application in multilevel converters in addition to 2L topologies, such as by Jacob and Baiju [F72]. This work uses the DSM for the modulation of the experimental prototype, with a more detailed analysis of the benefits and drawbacks given in section 5.3.

2.3 Automotive Batteries

In the context of EVs, batteries are generally thought of to be the costliest component of a vehicle and the largest hurdle preventing the widespread adoption of EVs. In contrast to power electronics and electric motors, the technology is not advanced enough to match the characteristics of internal combustion engine (ICE)-driven cars. This is due primarily to the fact that batteries cannot be charged as quickly as a fossil-fuel driven car can be refuelled. In addition, the (relatively) low energy density of lithium ion cells prevents an EV's range from significantly exceeding that of an ICE car. Furthermore, EV batteries degrade with use and time, reducing the value and performance of the vehicle [F73, F74].
As a result, there is significant research interest and development into the improvement of batteries, especially lithium-ion batteries, which EVs use almost exclusively.
As this work is focussed on the effect of a converter system on the performance and efficiency of an EV, the interaction of battery and power electronics must be considered to fairly evaluate different power electronic systems. This section

gives on overview on the aspects of lithium ion battery science relevant to this work.

2.3.1 Modelling

The modelling of a lithium-ion battery's voltage and current behaviour poses a significant challenge to engineers due to their highly-nonlinear characteristics [F75]. In general, the behaviour of lithium-ion cells is also strongly non-linearly dependent on its temperature, SoC, current and state of health (SoH) [F76]. Most models are able to recreate the behaviour of lithium-ion cells in specific operating points, but not over the entire operating range.
There are two general categories of lithium-ion cell models. The first are equivalent circuit models (ECM), which attempt to model the cells as a system of electric components (mostly resistances and RC elements of different time constants). Secondly, physics-based models are used, which aim to model the physical processes in a cell.
ECMs, introduced in 1947 [F77] can predict the behaviour of a cell to an acceptable level, but generally only for constant current charges and discharges [F78, F79]. Furthermore, they have to be parametrised of each possible SoC, temperature, and current to remain accurate when the conditions of the cell are changing [F80, F81]. Modelling only the behaviour of the cells, as opposed to the underlying physics [F82, F83], these models do not allow insight into the processes occurring inside the cell, as well as the states of the electrodes.
To improve on the drawbacks of ECMs, the physics-based Fuller-Newman-Doyle model [F84] was introduced, modelling the dynamics of the electrodes and lithium ions in order to recreate their terminal behaviour. The Fuller-Newman-Doyle model aims to reduce the empirical testing in different operating points required to develop a cell model, but itself has a large number of parameters (>20) that need to be identified to accurately model a cell. Furthermore, its complexity makes it prohibitively computationally expensive to compute in real time, and as a result, many reduced order models have been proposed in an attempt to accelerate the model [F85].
In this work, only ECMs are used to simulate the behaviour of the lithium-ion cells. This has been shown to be more accurate than a simple voltage source with an inner resistance for the pulsating currents occurring in cascaded multilevel converter [F34].

2.3.2 Degradation

Lithium ion cell degradation is, similar to their modelling, a complex non-linear process that is not fully understood [F73]. Many degradation mechanisms are known, such as solid-electrolyte interphase (SEI) layer formation, lithium plating, and electrode cracking [F74, F86], however their modelling and prediction remains a significant challenge in cell research [F87]. While the quantitative contribution to ageing is not entirely predictable, it is well known that increased temperatures and high charging currents significantly increase the degradation of lithium-ion cells [F88].

2.3.2.1 Frequency-Dependent Degradation

For batteries in power-electronic applications that are subjected to significant AC current in addition to the power-delivering DC current, there have been several empirical studies on the effect of the superimposed AC on the lifetime and degradation of the batteries.
Uno and Tanaka [F89] showed that AC currents at low frequencies $<100\,\mathrm{Hz}$ significantly increased the cells degradation, while higher frequencies did not cause additional ageing. They hypothesise that the higher frequency current bypasses the cell's charge transfer process and only passes through the double-layer capacitance (DLC) of the cell, limiting degradation. It was also shown that the low-frequency cells reached a higher temperature during the cycling which is likely to have negatively affected their degradation.
Zhao et al. [F88] show that the rms current seen by the cell is a significant factor in the cell's ageing, as it invariably increases the temperature of the cell. This is supported by other studies as well [F90, F91]. Brand et al. [F92] weakly confirmed the hypothesis of AC current increasing the degradation rate of lithium-ion cells at low frequencies, despite maintaining all cells at a constant temperature. This suggests that in addition to the increased temperature of the greater rms current, the current ripple can also cause damage in the cell.
Bessman et al. [F93] were unable to correlate superimposed AC current with cell ageing, but also indicated that low-frequency current harmonics had a larger impact on degradation than high-frequency harmonics.
In general, the literature is at this point inconclusive on the exact effect of AC current on the degradation of lithium-ion cells. It is clear however, that an increased low-frequency current will increase the temperature of the cell compared to a purely DC case, if the cooling is kept the same. Therefore, reducing the rms current, especially at low frequencies in the range of $1\,\mathrm{Hz}$ to $1000\,\mathrm{Hz}$, is likely

to be beneficial in an automotive application as cooling costs can be reduced to maintain the cells at an ideal temperature.

2.4 Objectives of this Work

As shown in this section, there has been some scientific foray into the use of modular multilevel converters in automotive applications. Individual issues of different converter topologies have been analysed and presented for different converter types based on different assumptions, requirements and components.
This work is intended to provide an implementation-independent analysis of the MMSPC and compare it to its nearest relative, the CHB, as well as the state-of-the-art automotive 2L converter. The goal of this work is not to compare multiple fully elaborated designs of different converter types, but rather to identify and understand the fundamental differences that arise when faced with the choice of energy storage and power conversion system in a modern EV. As such, emphasis in not placed on the exact selection of components and detailed finalising of the thermal management, but rather on the comparability of the different converters presented through the use of representative electronic components and a focus on the overarching correlations.
In chapter 3, a high-level analysis of all three converter types is presented with significant simplifications taken to identify the most relevant differences and similarities.
This is followed by a more detailed analysis of the design considerations specific to the MMSPC and CHB in chapter 4, and especially the differences that arise between the two technologies. A control scheme is then presented in chapter 5, to efficiently operate the MMSPC over its entire operating range.
The validation of the analysis, design and control is presented in chapter 6 using a simulative and experimental approach. A simulation of the reference design shows the differences of all converters when applied to a state-of-the-art EV, while the experimental prototype proves the feasibility of the converter design and the functionality of the proposed control system.

Chapter 3

Analysis

In this chapter, a new analytical model of the MMSPC is derived and presented. The model allows the MMSPC battery currents to be described as continuous functions of the output voltage and current of the converter. Using this model, the battery currents within the MMSPC are compared to the battery currents in conventional 2L converters and the CHB. While the analysis in this section assumes an ideal and symmetric converter, and therefore only investigates a simplification of the real systems, it allows an engineer to evaluate the trade-offs of the three converters with considerable accuracy (which is verified in section 6.1). The fundamental modelling approach presented here has been published in a previous paper of the author [E1], and in this work the previous model is expanded upon and augmented by a loss and efficiency model.

Two approaches are used to compare the battery currents of the converters. First, it is assumed that the load of the converters is identical, and the current loading of the battery of each converter is derived (section 3.2.2.2). This shows that both split-DC converters incur significantly larger battery currents than the single-DC 2L converter. Second, the converters are compared by assuming specific battery properties, and evaluating the achievable output voltage and current of each converter (section 3.2.2.2). Again, the 2L converter shows improved performance compared to the split-DC converters.

In sections 3.2.3 and 3.2.4, the losses of the converters analysed based on their origin, and the efficiency of each converter is calculated across the operating area. Despite the simplicity of the calculations presented in this section, they are reliable indicators of how the converters differ when they are used with the same load, or the same battery.

3.1 Modelling

This section briefly describes the assumptions made in the analysis of this chapter, and the modelling approaches taken to scale the properties of the converter.

3.1.1 Assumptions

Several key assumptions have to be taken in order to describe the converters analytically, which are listed here:

1. Sinusoidal output voltage and current
   The output voltages and currents are assumed to be perfectly sinusoidal, without any harmonics other than a third harmonic voltage injection. The effect of the current ripple resulting from the switching of the semiconductors is neglected. This is a reasonable assumption, since modern automotive converters control the load current accurately to approach sinusoidal waveforms.

2. In the split-DC converters, the output current is perfectly split between all SM batteries
   It is assumed that the MMSPC and CHB are operated such that the output current in one phase is always evenly distributed among the SM batteries of that phase. This means that the switching of semiconductors is assumed to be so fast that they do not affect the battery current, which becomes continuously differentiable. The derivation of this assumption is given in eq. (3.3) to eq. (3.9).

3. All battery voltages are constant
   The open-circuit voltage (OCV) of all cells are assumed to be the same and constant. While real lithium-ion cells' voltages vary with their SoC, these changes are slow compared to the power electronic time-scales relevant for this analysis. This means that these changes will affect all converters equally, and do not need to be modelled to compare the converters' performance.

These assumptions allow the model to describe the battery currents of the converters as simple analytical functions of the output voltage and current. Furthermore, the analysis is independent of the number of SMs in the split-DC converters.

3.1.2 Models and Scaling

In order to compare the different converters fairly, the active and passive components need to be scaled. This is based on empirical relationships which are discussed in this section. For all comparisons, the load is kept the same: a symmetrical three-phase load with arbitrary power factor and without a connected neutral point. This generally corresponds to an automotive electric machine.

3.1.2.1 Battery

In this section, the battery is modelled as a constant voltage source with a series resistance. In general, automotive batteries consist of a number of identical lithium-ion cells connected in series and in parallel [F7], where a parallel connection decreases the resistance and a series connection increases both the resistance and voltage u_{bat}. The energy contained in a battery pack E_{bat} is simply proportional to the number of cells. Therefore, we assume a constant battery chemistry, and a battery pack energy given by:

$$E_{\text{bat}} = c_{\text{bat}} u_{\text{bat}}, \tag{3.1}$$

where c_{bat} is the current capacity of the battery in units of electrical charge (A h). Since the overall battery's resistance is proportional to the number of cells in series (and the battery voltage u_{bat}), and inversely proportional to the number of cells in parallel (and the battery capacity c_{bat}), a battery resistance R_{inner} can be calculated with a constant of proportionality k_{R}.
The battery resistance follows the equation:

$$R_{\text{inner}} \propto \frac{u_{\text{bat}}}{c_{\text{bat}}} = k_{\text{R}} \frac{{u_{\text{bat}}}^2}{E_{\text{bat}}}. \tag{3.2}$$

The constant of proportionality is a property of the cell chemistry and will vary between different types of lithium ion cells. If a single cell chemistry is used, the relationship in eq. (3.2) can calculate the battery resistance for any size battery pack, and it is therefore used to scale the resistances between the 2L converter battery and the split-DC converters' batteries.

3.1.2.2 Semiconductors

The comparison of semiconductors across different semiconductor technologies (Si-MOSFET, SiC-MOSFET and Si-IGBT) is challenging, as their behaviour varies strongly with the type and voltage range. Due to this, simple scaling laws

such as eq. (3.2), are not sensible for semiconductors spanning different technologies. Instead, the requirements are derived first, and then state-of-the-art components are used as examples for the semiconductors.

3.2 Analytical Comparison of Split-DC and Single-DC converters

This section provides an analytical comparison of conventional (single-DC) 2L converters and split-battery multilevel converters. First, the battery currents are analysed in the different converter types. Second, the requirements, operating area, and a simple loss model are set up based on the basic parameters of the converters. While this section presents only a simplified and abstract comparison of the converters, the results are compared with detailed simulation and validated in the later sections, verifying their accuracy.

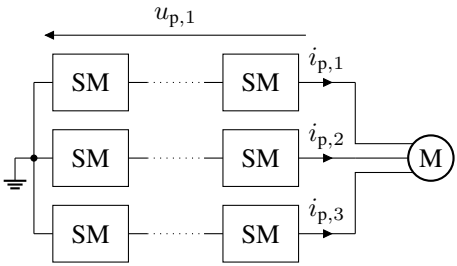
3.2.1 Battery Current Analysis

The analysis of the battery currents of the different converters is presented here, which describes how the current in the batteries changes depending on the load. Due to the split-battery nature of the multilevel converters, the battery current is very different to the conventional case of a 2L converter.

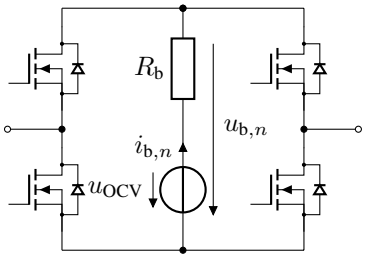
3.2.1.1 Split-DC Converters

The analysis of the battery-integrated MMSPC and CHB are shown in this section. Figures 3.1 (a) and 3.2 (a) show the topological overviews of the CHB and MMSPC, respectively, while their SMs are depicted in figs. 3.1 (b) and 3.2 (b). The relevant voltages and currents are labelled in these figures, where n corresponds the the SM number.
Based on assumption 1 in section 3.1.1, the output voltage $u_{\mathrm{p},i}$ of phase $i \in \{1,2,3\}$ of the converter is defined as:

$$u_{\mathrm{p},i}(t) = \hat{U} \sin\left(\omega t + \frac{2\pi(i-1)}{3}\right), \tag{3.3}$$



(a) Overview



(b) SM of the CHB

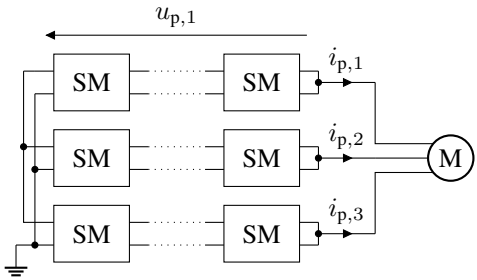
Figure 3.1: Circuit diagram of the CHB used in this section. The battery is modelled as a constant voltage source with an internal resistance, and is assumed to be identical for all SMs.

where $\hat{U}$ is the amplitude of the phase-neutral output voltage, ω is the output frequency, and t is the time. The modulation index m is given by:

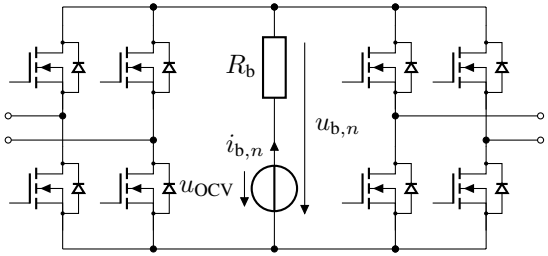
$$m = \frac{\hat{U}}{U_{\mathrm{DC,max}}}, \tag{3.4}$$

where $U_{\mathrm{DC,max}}$ is the maximum achievable (DC) output voltage of the converter. In the following analysis, only one phase will be investigated ($i = 1$), as the currents and voltages are three-phase symmetrical. The output current of phase 1, $i_{\mathrm{p},1}$, is given by:

$$i_{\mathrm{p},1}(t) = \hat{I} \sin(\omega t - \phi_c), \tag{3.5}$$



(a) Overview



(b) SM of the MMSPC

Figure 3.2: Circuit diagram of the MMSPC used in this section. The symmetric SM is used for these calculations. The battery is modelled as a constant voltage source with an internal resistance, and is assumed to be identical for all SMs.

where $\hat{I}$ is the amplitude of the output current and ϕ_c is its phase shift with respect to $u_{\mathrm{p},i}$.
The phase current is divided evenly between the N batteries of the phase, according to assumption 2, depending on the output level of the converter. The output level of the converter is $M \in \{-N, -N+1,...,N\}$, and represents the number of SMs that are in series within a phase of the converter.
To illustrate the splitting of the battery current, consider the case that u_{p} is equal to the maximum output voltage $U_{\mathrm{DC,max}}$ $(M = N)$. In this case, all of the SMs are switched in series and each battery sees the phase current, as seen in fig. 3.3 (a). If u_{p} is smaller than $U_{\mathrm{DC,max}}$, the current is split between the batteries, as SMs can be switched in parallel. In general, it is beneficial to switch the SMs in parallel whenever possible, as this allows the batteries to be parallelised and

the overall resistance of the phase to be reduced. In this analysis, the MMSPC SMs use the parallel mode whenever it is possible to reduce the overall resistance of the converter phase. For positive output levels, the number of SMs (and therefore batteries) that can be switched in parallel N_{par}, is given by:

$$N_{\text{par}} = \min\left(\frac{N}{M}, N\right) = \min\left(\left\lfloor \frac{U_{\text{DC,max}}}{u_{\text{p}}} \right\rfloor, N\right), \tag{3.6}$$

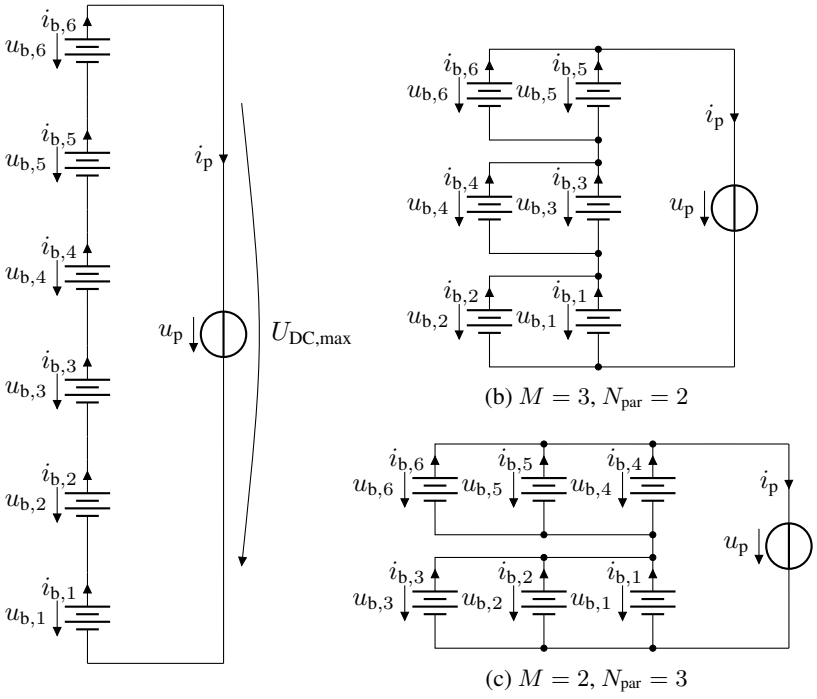
where $\lfloor\ \rfloor$ denotes the floor function, while $\lceil\ \rceil$ denotes the ceiling function.
This is shown in fig. 3.3, which shows how the MMSPC phase with six SMs can be configured with output levels $M = 6$ in fig. 3.3 (a), $M = 3$ in fig. 3.3 (b), and $M = 2$ in fig. 3.3 (c).
Equation (3.6) is true if all parallel groups contain the same number of SMs, which is however not always the case (this is analysed in more detail in section 4.2). In this section, the number of SMs is later assumed to be infinite (see eq. (3.9)), and therefore eq. (3.6) will always holds true.
It should be noted that for readability, u_{p} is assumed to be positive here, however the presented calculations are valid for both positive and negative values of u_{p}. When u_{p} is negative, eq. (3.6) becomes:

$$N_{\text{par}} = \max\left(\left\lfloor \frac{U_{\text{DC,max}}}{u_{\text{p}}} \right\rfloor, -N\right), \tag{3.7}$$

and N_{par} becomes negative. A negative value of N_{par} corresponds to $|N_{\text{par}}|$ SMs in parallel with a negative output polarity.
While eq. (3.6) intuitively holds true for the MMSPC due to the parallel mode, it also holds true for a CHB with integrated batteries. The difference is that a larger switching frequency is needed to ensure the phase current is split equally across all modules, as there is no parallel mechanism to directly share current. This is discussed and quantified in detail in section 4.2.
Using eq. (3.6), the current through a battery $i_{\text{b},n}$, in SM number $n \in \{1,2,...,N\}$ is therefore:

$$i_{\text{b},n} = \frac{i_{\text{p}}}{N_{\text{par}}} = \max\left(\left\lfloor \frac{U_{\text{DC,max}}}{u_{\text{p}}} \right\rfloor^{-1}, \frac{1}{N}\right) i_{\text{p}}. \tag{3.8}$$

Equation (3.8) describes the battery current of each SM, assuming that all parallel groups are of the same size. It is however not a convenient equation to manipulate, as it contains the rounding and max functions, and is only valid for N SMs. To extend the validity of eq. (3.8) and obtain a more general descrip-



(a) $M = 6$, $N_{par} = 1$

(b) $M = 3$, $N_{par} = 2$

(c) $M = 2$, $N_{par} = 3$

Figure 3.3: Three possible MMSPC configurations of a single phase for three values of the output level M, when the number of SMs $N = 6$. The number of SMs in parallel is given by eq. (3.6), and is only a function of the instantaneous output voltage. In the analysis of this chapter the number of SMs is extended to infinity, allowing the MMSPC to be generalised and analysed analytically. This is visualised in fig. 3.4.

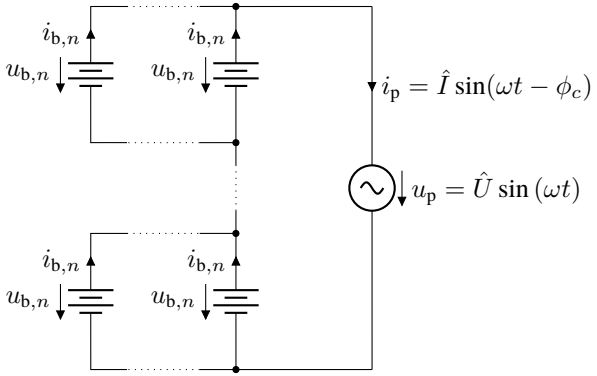


Figure 3.4: This figure visualises the generalisation of fig. 3.3, for the case where there are an infinite number of SMs. The current in all batteries is the same, and given by eq. (3.9).

tion of the SMs' batteries, it is assumed that N tends to infinity ($N \to \infty$) and therefore:

$$i_{\mathrm{b},n} = \frac{u_{\mathrm{p}}}{U_{\mathrm{DC,max}}} i_{\mathrm{p}}. \tag{3.9}$$

Now the battery current is only dependent on the output voltage and current, as well as the converter's maximum voltage. It should be noted that the battery current in eq. (3.9) is the instantaneous battery current at any point in time t, and not an average over a period.

The generalisation of eq. (3.9) is visualised in fig. 3.4, which shows a converter system with a continuous number of equally-loaded batteries. This can also be obtained by visual inspection of fig. 3.3, and the consideration of how it would look like if there were a very large number of SMs.

Section 4.3.2.2 provides design guidelines of the SMs that ensure that this analysis remains valid for a real converter with a finite number of SMs. Substituting eq. (3.3) and eq. (3.5) into eq. (3.9) nowtti gives:

$$i_{\mathrm{b},n} = \frac{\hat{U}\sin(\omega t)}{U_{\mathrm{DC,max}}} \hat{I}\sin(\omega t - \phi_c) \tag{3.10}$$

$$= \frac{\hat{I}m}{2}(\cos(\phi_c) - \cos(2\omega t - \phi_c)). \tag{3.11}$$

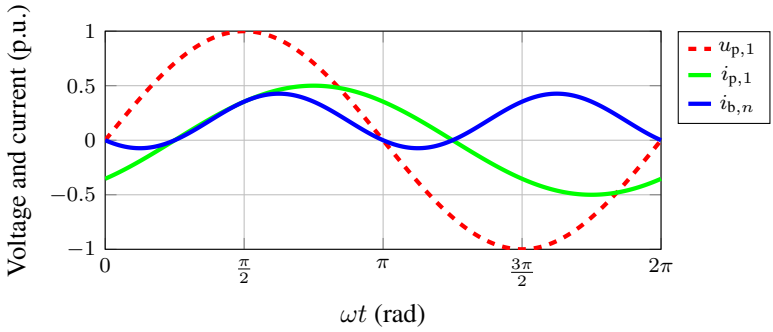


Figure 3.5: Waveforms of the MMSPC phase voltage, phase current and battery current. In this operating point, $m = 1$, $\hat{I} = 0.5$ pu, and $\phi_c = \pi/4$.

Equation (3.11) shows that the current in the batteries is proportional to m and $\hat{I}$ and consists of two terms:

- $\frac{\hat{I}m}{2} \cos \phi_c$, a constant term that corresponds to the active power delivered by the module battery
- $\frac{\hat{I}m}{2} \cos(2\omega t - \phi_c)$, an oscillating term with a frequency of twice the fundamental frequency and an amplitude independent of the power factor.

Figure 3.5 shows the waveforms of the phase voltage and current, as well as the battery current, for an example operating point.
To analyse the effect of the battery current, it is helpful to use the rms current, as the losses in the battery can be approximated to be purely resistive (section 2.3). Computing the rms current of eq. (3.11) over a fundamental period ($\omega t \in [-\pi, \pi]$) gives:

$$\breve{i}_{\mathrm{b},n}(\phi_c) = \frac{\sqrt{2}\,\hat{I}m}{4} \sqrt{\cos(2\phi_c) + 2}, \tag{3.12}$$

where $\breve{}$ indicates the rms value. It can be seen that the battery sees an rms current at every power factor. A disadvantage of the MMSPC (and CHB) becomes apparent: the battery current decreases much more slowly than the power factor, whereas for a conventional 2L converter the battery current decreases proportionally to the power factor. This causes greater battery losses of the MMSPC at

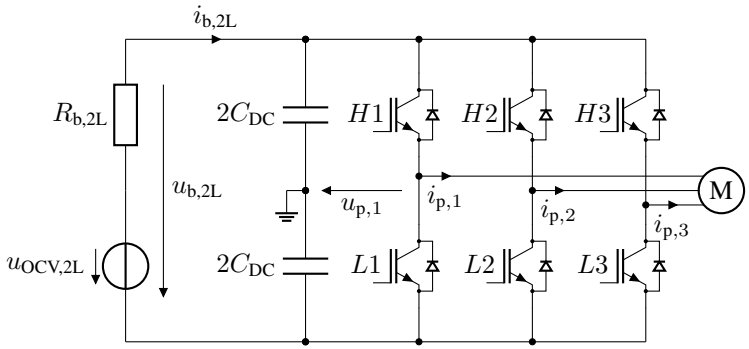


Figure 3.6: The modelled 2L converter

large phase angles. The rms battery current in the split-DC converters is compared to the battery current in 2L converters in fig. 3.7.

3.2.1.2 Single-DC Converters

In contrast to split-dc converters, the battery in conventional 2L converters is loaded with a current contribution from all three phases simultaneously, and as a result is only subject to DC-current. This holds true under the assumption that all of the oscillating current from the semiconductor switching is buffered by the DC-Link capacitor (assumption 2), and that all components are ideal.
For comparability, the output voltage and current, as well as the maximum output voltage are kept the same. This means the 2L battery voltage $u_{\mathrm{b,2L}}$ is given by:

$$u_{\mathrm{b,2L}} = 2U_{\mathrm{DC,max}}, \tag{3.13}$$

when no load is drawn, as seen in fig. 3.6. In a 2L converter, the output current of phase i will result in a battery current contribution $i_{\mathrm{b,2l},i}$ according to :

$$i_{\mathrm{b,2l},i} = i_{\mathrm{p},i}\frac{u_{\mathrm{p},i}}{\frac{u_{\mathrm{b,2L}}}{2}} = \frac{\hat{I}m}{4}\left(\cos\left(\phi_c\right) - \cos\left(2\omega t - \phi_c + \frac{2\pi(i-1)}{3}\right)\right). \tag{3.14}$$

Each output phase current results in a battery current contribution, at a different phase angle. When the battery currents due to all three phases are summed up, the expression simplifies to give the total converter battery current $i_{\mathrm{b,2L}}$:

$$i_{\mathrm{b,2L}} = \sum_{i=1}^{3} i_{\mathrm{b,2l},i} = \frac{3\,\hat{I}m}{4}\cos(\phi_c). \tag{3.15}$$

Since $i_{\mathrm{b,2L}}$ is constant for a given ϕ_c, the instantaneous value of $i_{\mathrm{b,2L}}$ is simultaneously the rms value. It is evident that in a conventional converter, the battery only sees a current proportional to the active power ($P = {}^{3}\!/_{2}\,\hat{U}\hat{I}\cos(\phi_c)$), and the battery sees no current in the case of pure reactive power ($\phi_c = \pm\pi$), unlike in split-dc converters.

The two equations for battery rms current can now be compared for the 2L and multilevel case. To allow a fair comparison and equal overall power, the multilevel battery rms current must be multiplied by 3 as there are three phases; and divided by 2 to account for the fact that the sum of the SM voltages is only half of the 2L converters battery voltage. This ensures that the total total stored energy is the same in both split-DC and single-DC converters. The equivalent module rms current $\breve{i}_{\mathrm{b,eq}}$ is thus:

$$\breve{i}_{\mathrm{b,eq}} = \frac{3}{2}\,\breve{i}_{\mathrm{b},n} = \frac{3\sqrt{2}\,\hat{I}m}{8}\sqrt{\cos(2\phi_c)+2}. \tag{3.16}$$

Comparing eq. (3.15) to eq. (3.16) shows that the multilevel converters' batteries experience a larger current compared to the 2L case, even for the best-case load, which is $\phi_c = 0$. This can be seen in fig. 3.7, which shows the 2L battery current and the equivalent rms battery current of the split-DC converters. Both battery currents are proportional to $\hat{I}m$, but at $\phi_c = 0$ the constant of proportionality is ${}^{3}\!/_{4}$ for the 2L but ${}^{3\sqrt{6}}\!/_{8} = 0.919$ for the multilevel case, which corresponds to an increase of 22.5%. The increase becomes larger as $\phi_c \to {}^{\pi}\!/_{2}$, where the increase is infinite as the battery current is 0 A and $0.53 \cdot \hat{I}m$ for the 2L and multilevel converters, respectively.

Based on this analysis of the converter's battery currents, the following section formulates the battery and power electronics requirements for both converter types, and analyses the available operating area for each converter.

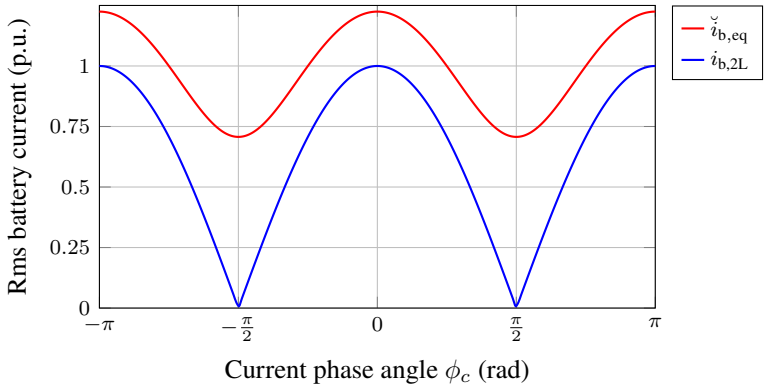


Figure 3.7: Rms battery current of the MMSPC and 2L converter as a function of phase angle. The MMSPC current is plotted as the equivalent rms battery current (see eq. (3.16)). The rms current of the 2L battery is equal to the instantaneous current, because it only contains a DC component.

3.2.2 Comparison of Requirements and Operating Area

The different converters are analysed and compared at all possible operating points in this section. Three different converters are investigated: conventional 2L converters with a central DC-Link, the CHB with integrated batteries, and the MMSPC. In section 3.2.2.1, the converters are compared from the perspective of the application, i.e. the load conditions are held constant and the power electronics and the batteries are analysed. In Section 3.2.2.2, a given battery chemistry (fixed value of k_R) and size is assumed and the impact of the power electronics on the ability of the system to provide output power is investigated. While the numerical results will vary for different values of k_R, the results for all converters will vary in the same way, which gives insight into the differences between the converters even if only a single battery chemistry is used for the numerical examples.
A given sinusoidal load of the converters is assumed, as shown in section 3.2.1, and the battery current derived in section 3.2.1 is used. Furthermore, the inner resistances of the power electronics are assumed to be negligible compared to the battery resistance and all currents are assumed to be continuous. The assumption of the power electronics' resistance being negligible is validated in section 6.1.1,

Parameter	Value	Description
$\hat{U}_{\max}$	231 V	Maximum load voltage ($\hat{U}$) amplitude (eq. (3.3))
E_{bat}	48 kW h	Energy stored in the battery
k_{R}	41.1 s^{-1}	Battery resistance constant (eq. (3.2))
$\max \hat{I}$	500 A	Maximum load current ($\hat{I}$) amplitude (eq. (3.5))
N	5	Number of SMs
$u_{\text{b,2L}}$	400 V	2L open-circuit DC-link voltage
$U_{\text{DC,max}}$	200 V	Split-DC converter maximum output voltage
$i_{\text{b,2L}}$	433 A	2L battery current

Table 3.1: Parameters of the example application. It should be noted that the AC voltages and currents are given as phase-to-neutral amplitudes.

where a representative converter is simulated, and the ratio between the SM battery and MOSFET resistances is greater than 17. In sections 3.2.3 and 3.2.4, where the converter losses and efficiencies are calculated, the semiconductor losses are not neglected.
To compare the converters with a practical example, a representative application is proposed whose parameters are given in table table 3.1. The application is chosen to represent the conditions in a mid-range EV such as the VW ID3 but are not based on a specific car model. As any change in these parameters will affect the comparative results, the purpose is solely to convey how the requirements in an automotive application differ between the converters.

3.2.2.1 Requirements for a Given Application

In order to investigate the converters from the perspective of the application, the load currents and voltages are the same for all converters, according to equations Equations (3.3) and (3.5). From the basis of this given application, the requirements of the battery and the power electronics are derived. In addition to the load, the amount of energy stored in the battery E_{bat} is held constant. This analysis provides simple equations that relate the battery current to the output current and voltage of the converters. These equations show that despite the fact that the battery parameters between all three applications are the same, the amount of rms current passed through the batteries is different between the different converters. Both split-DC converters require the batteries to be able to handle significantly more current than for 2L-converters for the same load, and this relationship is quantified here.

Two-Level Converters

The requirements of the battery and the power electronics for the 2L converter are derived in this section.

Battery The battery of an EV is generally defined by its capacity and its resistance (which determines the power that it can deliver). As shown in eq. (3.2), the resistance of a battery is related to its capacity. In this section, the required battery current is calculated in dependence of the operating point, so that a fitting battery can be chosen.
To define the maximum DC-link voltage of the 2L converter, which is equivalent to the battery voltage, it is assumed that the converter uses third harmonic injection (THI) [F94] to generate its output voltage:

$$u_{\mathrm{p},1} = \hat{U}\left(\sin(\omega t) + \frac{1}{6}\sin(3\omega t)\right). \tag{3.17}$$

For readability, only the output voltage equation for phase 1 is shown. The battery voltage is therefore given by:

$$u_{\mathrm{b,2L}} = \sqrt{3}\hat{U}_{\mathrm{max}}, \tag{3.18}$$

where $\hat{U}_{\mathrm{max}}$ is the maximum value that $\hat{U}$ can take. Now, in contrast to eq. (3.15), the internal resistance of the battery $R_{\mathrm{b,2L}}$ is not assumed to be zero. The DC-Link voltage of the converter $u_{\mathrm{b,2L}}$ is thus no longer equal to $u_{\mathrm{OCV,2L}}$, but instead:

$$u_{\mathrm{b,2L}} = u_{\mathrm{OCV,2L}} - i_{\mathrm{b,2L}} R_{\mathrm{b,2L}}, \tag{3.19}$$

giving:

$$i_{\mathrm{b,2L}} = \frac{3\,\hat{U}\,\hat{I}}{4(u_{\mathrm{b,2L}} - i_{\mathrm{b,2L}} R_{\mathrm{b,2L}})}\cos(\phi_c), \tag{3.20}$$

which is a quadratic equation of $i_{\mathrm{b,2L}}$. For realistic values of the variables, this gives a battery current of:

$$i_{\mathrm{b,2L}} = \frac{\sqrt{3}\left(\hat{U}_{\mathrm{max}} - \sqrt{{\hat{U}_{\mathrm{max}}}^2 - 2\,\hat{I}\,R_{\mathrm{b,2L}}\,\hat{U}\,\cos(\phi_c)}\right)}{2\,R_{\mathrm{b,2L}}}. \tag{3.21}$$

Using eq. (3.2), the resistance of the battery can be put in proportion to the battery pack voltage and its energy capacity, giving:

$$i_{\mathrm{b,2L}} = \frac{E_{\mathrm{bat}}\,\hat{U}_{\mathrm{max}} - \sqrt{{E_{\mathrm{bat}}}^2\,{\hat{U}_{\mathrm{max}}}^2 - 2\sqrt{3}\,E_{\mathrm{bat}}\,\hat{I}\,k_{\mathrm{R}}\,\hat{U}_{\mathrm{max}}\,\hat{U}\,\cos(\phi_c)}}{2\,k_{\mathrm{R}}\,\hat{U}_{\mathrm{max}}}. \quad (3.22)$$

This equation gives the battery current of a 2L converter in dependence on the load ($U_{\mathrm{DC,max}}$, $\hat{I}$, ϕ_c, and $\hat{U}_{\mathrm{max}}$), and the system's energy capacity E_{bat}, allowing the battery to be roughly sized with a given load profile.

Power Electronics In addition to the battery, the power electronics of the system must also be sized. This is done based on the total switching power, which is the rms current that needs to be switched by a given half-bridge multiplied by the voltage of that half-bridge. For a 2L converter with three phases, the switched voltage $u_{\mathrm{b,2L}}$ is simply the battery voltage, while the switched current $i_{\mathrm{sw,2L}}$ of each half-bridge is the rms phase current. Therefore the total switched power $P_{\mathrm{sw,2L}}$ is:

$$P_{\mathrm{sw,2L}} = u_{\mathrm{b,2L}} i_{\mathrm{sw,2L}} = \frac{3\sqrt{6}}{2}\hat{U}_{\mathrm{max}}\hat{I}, \quad (3.23)$$

Together with the previously derived battery current, these values give the two cornerstones of the design of an automotive battery and converter system. In the following section, the same is done for split-DC converters.
It should be noted that the comparison of the switched power between different converters with different semiconductors can never provide more than a point of reference to determine semiconductor effort. To compare the split-DC and single-DC converter semiconductor effort in simple analytical terms here is impossible, as the behaviour of MOSFETs and IGBTs are so different, and the voltage levels of the components are not comparable. Later in section 3.2.3 and the latter sections of this work, the converters are compared based on existing automotive semiconductor components, which allow a representative comparison for a specific application with specific components, but this not easily generalised analytically.

Split-DC Converters

In this section, the battery and power electronics requirements for the battery-integrated MMSPC and CHB are derived.

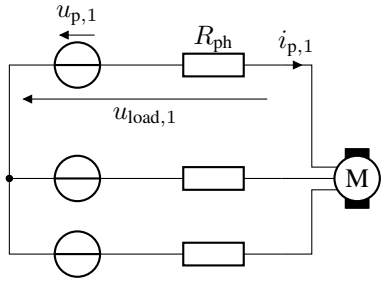


Figure 3.8: Simplified circuit diagram of a split-dc converter, where all battery resistances are grouped to one resistance R_{ph}. Only phase 1 is annotated for readability.

Battery Similarly, to the 2L converter, the maximum voltage can be defined from the maximum voltage of the load. Since multilevel converters can switch their batteries in both a positive and negative output polarity, the sum of all module battery voltages $u_{\mathrm{b},n}$ is half the voltage of the 2L converter battery:

$$N u_{\mathrm{b},n} = \frac{u_{\mathrm{b,2L}}}{2} = U_{\mathrm{DC,max}}, \tag{3.24}$$

which is equal to the converters' maximum output voltage.
The battery rms current can now be calculated with eq. (3.12). Again, the resistance of the batteries is not neglected in this section and thus affects the output voltage of the converter. For this, a multilevel converter phase is modelled as a voltage $u_{\mathrm{p},i}$ with a series resistance R_{ph}, which consists of the resistances of the SMs' batteries, and depends on the phase configuration. The voltage at the terminals of the converter is called $u_{\mathrm{load},i}$, as shown in fig. 3.8. Here, a distinction between the MMSPC and CHB has to be made. For both converters, the resistance of a phase R_{ph} is maximum when all modules, and therefore the module battery resistances R_{b}, are in series:

$$R_{\mathrm{ph}} = N R_{\mathrm{b}}. \tag{3.25}$$

When modules are not in series, they are in parallel with other modules in the MMSPC, or bypassed in the CHB. Therefore, as the output voltage decreases, the

phase resistance decreases linearly in the CHB, and quadratically in the MMSPC. Assuming a large number of modules and a fast switching rate gives:

$$R_{\text{ph}} = N R_{\text{b}} \Big(\frac{u_{\text{p}}}{\frac{U_{\text{DC,max}}}{2}} \Big)^{H}, \tag{3.26}$$

where $H \in \{1,2\}$ indicates the number of half-bridges on either side of a SM's battery ($H = 1$ for CHB and $H = 2$ for MMSPC).
This leads to the converter voltage expression:

$$u_{\text{p},i} = u_{\text{load},i} \; + i_{\text{p},i} R_{\text{ph}}. \tag{3.27}$$

In order to simplify the analysis of the battery currents, it is assumed that the phase resistance is constant over a period of the output voltage. Furthermore, as the voltage drop across the resistance is small, it is assumed that

$$\frac{u_{\text{p},i}}{U_{\text{DC,max}}} \approx \frac{u_{\text{load},i}}{\hat{U}_{\text{max}}}. \tag{3.28}$$

The constant phase resistance is defined as the mean phase resistance over a fundamental half-period:

$$\overline{R_{\text{ph}}} = \frac{N R_{\text{b}}}{\pi} \int_0^{\pi} \Big(\frac{u_{\text{load},i}}{\hat{U}_{\text{max}}} \Big)^{H} \mathrm{d}t, \tag{3.29}$$

which gives:

$$\overline{R_{\text{ph}}} = \begin{cases} \frac{19\, N\, R_{\text{b}}\, \hat{U}}{9\pi\, \hat{U}_{\text{max}}} & H = 1 \\ \frac{37\, N\, R_{\text{b}}\, \hat{U}^2}{72\, \hat{U}_{\text{max}}^{\;2}} & H = 2. \end{cases} \tag{3.30}$$

Now the estimated phase resistance can be used to calculate the output voltage of the converter. First, however, the battery current according to eq. (3.12) must be recalculated to account for the THI, giving:

$$\breve{i}_{\text{b},n}(\phi_c) = \frac{\sqrt{2}\, \hat{I}m}{4} \sqrt{\frac{2\cos(2\phi_c)}{3} + \frac{37}{18}}. \tag{3.31}$$

It is noteworthy that the THI alters the rms current of the battery (unlike for the 2L converter); in fact, the rms current of the battery is reduced. This is due to the fact that the THI decreases the phase voltage at the peak $\omega t = \pi/2$, which allows the converter to switch more SMs in parallel. This distributes the current

more equally across all of the SMs and therefore reduces each module's rms current. This is further investigated and used for the MMSPC control, as shown in chapter 5.
If, in addition to the THI, the phase resistance of the MMSPC is taken into account, the rms battery current becomes the cumbersome expression:

$$\breve{i}_{\mathrm{b},n} = \begin{cases} \dfrac{\sqrt{6}\hat{I}\,\hat{U}\sqrt{38\,\overline{R_{\mathrm{ph}}}\,\cos(\phi_c)+3\,\pi\left(\frac{2\,\cos(2\,\phi_c)}{3}+\frac{37}{18}\right)+\frac{361\,\overline{R_{\mathrm{ph}}}^{\,2}}{9\,\pi}-\frac{19\,\overline{R_{\mathrm{ph}}}\,\cos(3\,\phi_c)}{9}}}{12\,\hat{U}_{\max}\,\sqrt{\pi}} & H=1 \\ \dfrac{\sqrt{2}\hat{I}\,\hat{U}\sqrt{\frac{16\,\cos(\phi_c)^2}{3}+\frac{1369\,\overline{R_{\mathrm{ph}}}^{\,2}\,\hat{U}^2}{432\,\hat{U}_{\max}{}^2}+\frac{259\,\overline{R_{\mathrm{ph}}}\,\hat{U}\,\cos(\phi_c)}{18\,\hat{U}_{\max}}-\frac{74\,\overline{R_{\mathrm{ph}}}\,\hat{U}\cos(\phi_c)^3}{27\,\hat{U}_{\max}}+\frac{50}{9}}}{8\,\hat{U}_{\max}} & H=2. \end{cases} \tag{3.32}$$

Equation (3.32) can now be used to compare the battery load in the split-DC converters with that of conventional 2L converters, by substituting in eqs. (3.2) and (3.29). Since the resulting expression has hundreds of terms, it is not printed here but compared graphically in fig. 3.9.

Power Electronics The power electronic requirements of the split-DC converters are derived here, in terms of the switching voltage and the switching current. The switching voltage of a half-bridge $u_{\mathrm{sw,ML}}$ is the maximum DC output voltage of the converter $U_{\mathrm{DC,max}}$ divided by the number of SMs N. When THI is used, the maximum output voltage is given by:

$$U_{\mathrm{DC,max}} = \frac{\sqrt{3}\hat{U}_{\max}}{2}, \tag{3.33}$$

and therefore the switching voltage of the half-bridges is:

$$u_{\mathrm{sw,ML}} = \frac{\sqrt{3}\hat{U}_{\max}}{2N}. \tag{3.34}$$

The switching current of a split-DC converter half-bridge $i_{\mathrm{sw,ML}}$ is equal to the rms phase current ($\hat{I}/\sqrt{2}$) for the CHB and MMSPC. Since a CHB cell has two half-bridges per SM, this gives:

$$i_{\mathrm{sw,ML}} = 2\frac{\hat{I}}{\sqrt{2}}. \tag{3.35}$$

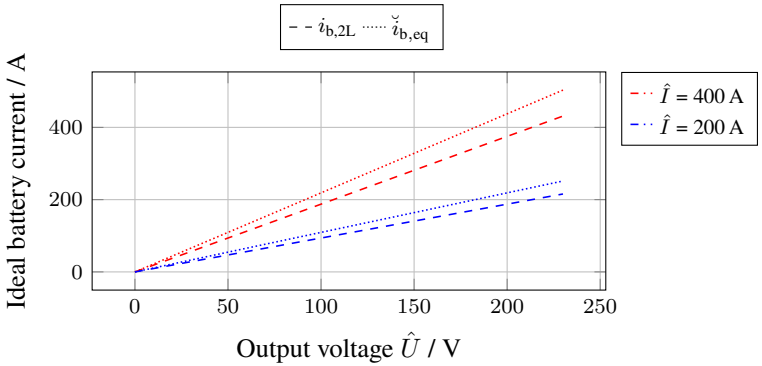
Even though the MMSPC has twice as many half-bridges as the CHB, each only conducts half of the current, and is rated at half the power. Therefore the switching current is the same per SM in the MMSPC as the CHB.
From eqs. (3.34) and (3.35), the total switching power of the split-DC converters can be calculated as:

$$P_{\text{sw,ML}} = 3N \cdot u_{\text{sw,ML}} i_{\text{sw,ML}} = \frac{3\sqrt{6}\,\hat{I}\,\hat{U}_{\text{max}}}{2}, \tag{3.36}$$

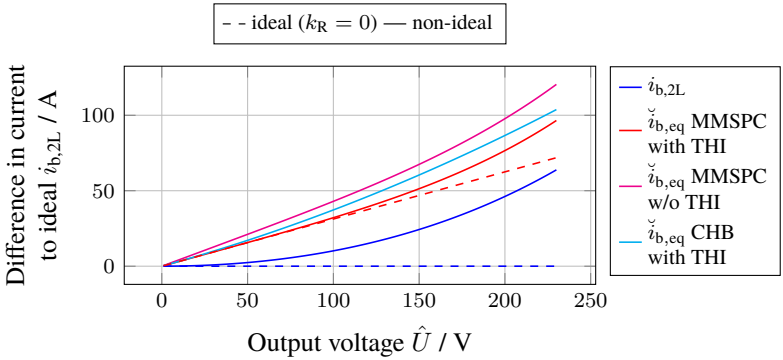
which is the same value as for the 2L converter eq. (3.23). This shows that while the different converter types generally use different semiconductor technologies, the overall requirement in terms of the power that has to be switched is the same.

Comparison

Figure 3.9 shows the battery currents of the 2L converter according to eq. (3.22) and MMSPC according to eq. (3.32), whose parameters are those given in table 3.1. In order to compare the MMSPC converter's battery current with that of the 2L converter, $\breve{i}_{\text{b,eq}}$ is again used, which means the MMSPC current is multiplied by $3/2$ (see eq. (3.16)).
In fig. 3.9 (a), the current of the idealised converters are plotted, i.e. all resistances are assumed to be $0\,\Omega$. Three different values of $\hat{I}$ show how the battery current changes with the output voltage and output current. It can be seen that the ideal battery current scales linearly with the output voltage and the output current, however the current in the MMSPC is consistently higher than the current in the 2L converter.
Figure 3.9 (b) now shows the battery currents for the operating point $\hat{I} = 400\,\text{A};\ \phi_c = 0$ of non-ideal converters with a battery resistance, while including the ideal currents as a reference. Furthermore, the battery current when THI is not used, as well as the battery in a CHB, are shown. The currents are plotted as the difference to the ideal 2L converter current.
Figure 3.9 (b) shows that the real MMSPC battery current is close to the ideal battery current, especially for low output voltages. This is because the MMSPC can use the parallel mode to significantly decrease the phase resistance. As the output voltage increases, however, the parallel mode can be used less frequently and the battery current diverges quickly from the ideal current. In contrast, the CHB battery current does not increase as quickly at high output voltages, but is always higher than in the MMSPC. At the maximum output voltage, the two converters almost have the same battery current.



(a) Ideal (no battery resistance) battery current at different output current amplitudes



(b) Difference between non-ideal current and ideal 2L converter battery current

Figure 3.9: Ideal (a) and non-ideal (b) battery current for the 2L converter and MMSPC, at $\phi_c = 0$. The battery current of the MMSPC is plotted as the equivalent battery current (see eq. (3.16)). The bottom graph shows the difference between the non-ideal battery currents for the two converters and the ideal current for a 2L converter. In addition, the difference in current for the MMSPC without THI and the CHB (with THI) are shown.

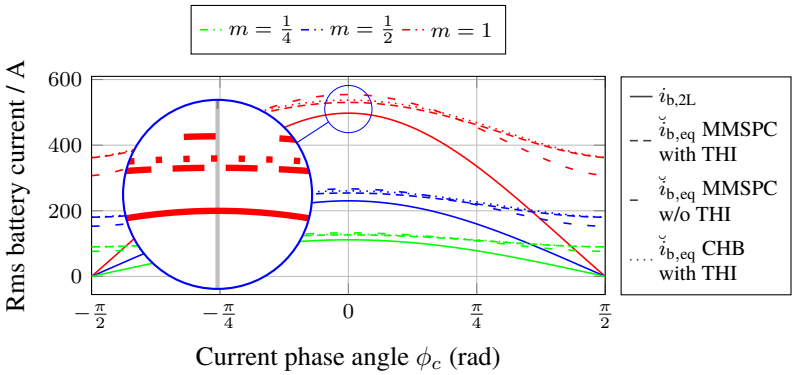


Figure 3.10: Rms battery current vs. phase angle for the 2L, MMSPC, MMSPC without THI, and CHB. The values are plotted for three different output voltages.

When no THI is used, the battery current is even higher in the MMSPC than in the CHB, showing that THI plays a significant role in determining the converters' battery current. It should be noted that while fig. 3.9 shows the battery currents at output voltages up to $\hat{U} = \hat{U}_{\max}$, these operating points cannot be achieved as a resistive voltage drop over the battery's resistance will prevent the maximum voltage from being reached when a current is flowing. This occurs at $\hat{U} = 217\,\mathrm{V}$ for the MMSPC and $\hat{U} = 221\,\mathrm{V}$ for the 2L converter.
Figure 3.10 shows how the battery currents change with the power factor for three different output voltages and a current of $\hat{I} = 400\,\mathrm{A}$. As predicted by fig. 3.7, the multilevel converter currents decrease much more slowly with increasing phase angle compared to the 2L converter. Furthermore, while THI decreases the battery current at low ϕ_c, the battery current is smaller without THI at phase angles above ca. $\pi/4$ rad, showing that THI does not always reduce the battery current. This is due to the fact that as the output current is out of phase with the output voltage, the voltage reduction caused by the THI no longer reduces the output voltage when the current is high, but increases the output voltage when the current is high. This is investigated further in chapter 5, where it is shown that THI can always be used to reduce the battery current, but must be shifted depending on the power factor. It can also be seen that the current distribution is relatively independent of the output voltage.

The comparison in this section has analysed how the rms battery current for the three converters changes depending on the load. The following section assumes that the battery for all converters is the same, and analyses the operating area that is available to the converters, which is defined by their maximum output voltage and current.

3.2.2.2 Operating Area for a Given Battery

While section 3.2.2.1 investigates the use of split-DC converters given a specific application, defined by the output voltage and current of the converter, this section investigates the same converters using the battery as the input variable. The total energy of the battery E_{bat}, the battery constant k_{R}, and the maximum voltage $U_{\text{DC,max}}$ are held constant across the investigated converters.
The maximum battery current is defined as $i_{\text{b,2L}}$ for the 2L converter, and scaled by a factor of $2/3$ (see eq. (3.16)) for the split-DC converters. Using this analysis, it is possible to see the effect that the converter choice has on the output characteristics of each specific converter if the battery behaves according to eq. (3.2). Specifically, the analysis reveals the maximum output voltage and current that is achievable with each converter, assuming the same battery is used.
In this analysis it is assumed that the current is only limited by the batteries, whereas in a real application the power electronics also limit the maximum AC current. As a result of this assumption, the maximum possible AC currents are unrealistically high for very low output voltages.

Two-Level Converter For the two level converter, the battery has a voltage of $u_{\text{OCV,2L}}$, which corresponds to $2U_{\text{DC,max}}$. Therefore, eq. (3.22) can be rearranged for $\hat{I}$ to give the maximum AC current that the converter can deliver, $\hat{I}_{\text{max,2L}}$:

$$\hat{I}_{\text{max,2L}} = \frac{2\, i_{\text{b,2L}} \left(u_{\text{OCV,2L}} - \frac{k_{\text{R}}\, i_{\text{b,2L}}\, {u_{\text{OCV,2L}}}^2}{E_{\text{bat}}} \right)}{3\, \hat{U} \cos\left(\phi_c\right)}. \tag{3.37}$$

Split-DC Converters Similarly, the maximum AC current of the cascaded converters $\hat{I}_{\text{max,ML}}$ can be determined by rearranging eq. (3.32), and holding $U_{\text{DC,max}}$ constant to the case with the 2L converters (see eq. (3.24)), giving:

$$\hat{I}_{\text{max,ML}} = \frac{4\, i_{\text{b,2L}}\, u_{\text{OCV,2L}}}{\hat{U} \sqrt{24 \cos\left(\phi_c\right)^2 + 25}}, \tag{3.38}$$

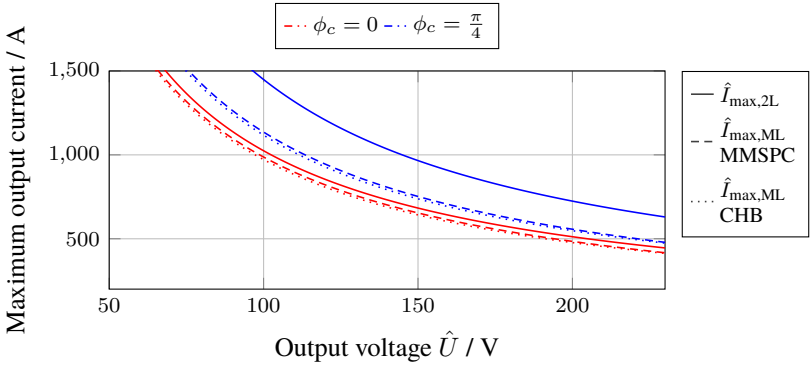


Figure 3.11: Maximum output current of the compared converters for the case where only the battery limits the output current

for the case when $k_{\text{R}} = 0$. The expression when $k_{\text{R}} \neq 0$ is complex, dependent on H, and not given here due to its extreme length; the result is plotted in fig. 3.11.
From eq. (3.38) the disadvantage of the multilevel converters compared to the 2L converter can be seen. While all converters' maximum currents exhibit the same proportionality to $i_{\text{b,2L}}$, $u_{\text{OCV,2L}}$, and $\hat{U}$ (when $k_{\text{R}} = 0$), the constant of proportionality is different. For the 2L converter the constant is $2/3$, while it is $4/7 = 0.571$ for the multilevel converters at $\phi_c = 0$, and less as ϕ_c increases. This shows that—ignoring semiconductor losses and battery losses—the multilevel converters always have a smaller maximum AC output current than a comparable 2L converter with the same battery parameters.
Figure 3.11 shows the maximum output current of the 2L converter and the split-DC converters. As expected, the 2L converter allows a higher output current for all output voltages, with the difference increasing as ϕ_c increases.

The analysis of the operating area of the cascaded and single-DC link converter has shown that the use of cascaded converters always results in higher battery rms currents compared to conventional converters. This is the result of the property of these converters that the batteries are subjected to AC as well as DC currents. It is also shown that the split-DC converter batteries can benefit from a third harmonic injection into the output voltage to reduce the rms current, but this effect is dependent on the load power factor. In all operating conditions, the

MMSPC is shown to have lower battery currents than the CHB due to its ability to put SMs in parallel, which can reduce the phase resistance.
In the following section, the converters losses are calculated based on these analyses.

3.2.3 Losses

While section 3.2.2 has shown that the split-DC converter's batteries suffer from larger rms currents than comparable 2L converters, the power electronics has not been taken into account. In this section, the losses of the three presented converters are calculated, using the previous calculations. Three different losses are investigated, depending on the operating point of the converter: the ohmic losses in the batteries, the conduction losses of the semiconductors, and the switching losses of the semiconductors.
The ohmic losses in the battery $P_{\text{bat,loss}}$ are calculated according to:

$$P_{\text{bat,loss}} = {i_{\text{bat}}}^2 R_{\text{inner}}, \tag{3.39}$$

where i_{bat} is the current flowing through a battery and R_{inner} is its inner resistance. For periodic currents, the instantaneous current is substituted by the rms current. The sum of the conduction losses and switching losses of the semiconductors are equal to the power dissipated by the semiconductor. Depending on whether they are MOSFETs or IGBTs, the semiconductors are modelled differently. MOSFETs are modelled as resistances R_{DS} when switched on, while IGBTs and diodes are modelled as a voltage source U_{f} opposing the current flow in series with a resistance R_{on}. Therefore the conduction losses of semiconductors $P_{\text{cond,loss}}$ are given by:

$$P_{\text{cond,loss}} = u_{\text{SC}} i_{\text{SC}} = \begin{cases} {i_{\text{SC}}}^2 R_{\text{DS}} & \text{MOSFET} \\ {i_{\text{SC}}}^2 R_{\text{on}} + i_{\text{SC}} U_{\text{f}} & \text{IGBT or diode,} \end{cases} \tag{3.40}$$

where i_{SC} and u_{SC} are the current and voltage of a semiconductor, respectively. Again, for the resistive terms the rms current can be used to infer the losses for periodic currents while the mean current is used for the term proportional to the current.
Finally, switching losses are calculated based on the simplifying assumption that they are proportional to the switching voltage and current. As the voltage of all switching actions is the same in the presented converters, the losses only change

with the current. For a sinusoidal output current of amplitude $\hat{I}$, the switching losses $P_{\text{sw,loss}}$ (for all converters) are given by:

$$P_{\text{sw,loss}} = \frac{f_{\text{SC}}\hat{I}}{i_{\text{SC,nom}}\pi} E_{\text{sw,nom}}, \tag{3.41}$$

where, f_{SC} is the switching frequency of the half-bridge, $i_{\text{SC,nom}}$ is the nominal semiconductor current, and $E_{\text{sw,nom}}$ is the nominal switching energy of the half-bridge [F95]. The nominal switching energy is the sum of the turn-on and turn-off energies of the half-bridge semiconductors:

$$E_{\text{sw,nom}} = E_{\text{on,sc}} + E_{\text{off,sc}} + E_{\text{on,D}} + E_{\text{off,D}}. \tag{3.42}$$

where $E_{\text{on,sc}}$, $E_{\text{off,sc}}$, $E_{\text{on,D}}$, and $E_{\text{off,D}}$ are the turn-on and turn-off energies of a transistor and a diode, respectively. All other losses are assumed to be negligible. The energies are obtained from the datasheets for the IGBTs and diode, and calculated according to [D1] for the MOSFETs.

In order to calculate the losses based on these formulae, the characteristics of the semiconductors and batteries have to be chosen. For this analysis, the 300 A, 80 V MOSFET IAUT300N08S5N012 of Infineon was chosen for the split-DC converters, with two MOSFETs per semiconductor for the CHB, and one per semiconductor for the MMSPC [D2]. The IGBTs and diode from the 820 A, 750 V converter module FS820R08A6P2B of Infineon are chosen as the reference semiconductors for the 2L converter [D3]. The parameters of eqs. (3.40) and (3.41) are fitted to the curves in the data sheet at 150 °C and are shown in tables 3.2 and 3.3.

These semiconductors are chosen because they represent state-of-the-art automotive transistors from the respective voltage ranges of the multilevel and 2L converters. The MOSFET is chosen as it has the lowest R_{DS} of all available automotive MOSFETs by Infineon, at the time of writing. Similarly the IGBT is chosen as it has the lowest forward voltage and inner resistance of the available IGBTs from Infineon. Choosing two semiconductors from the same manufacturer means that their datasheet values are likely to be obtained by similar methods, making the comparison more fair compared to the comparison of semiconductors from multiple manufacturers.

It should be noted that the effective switching rate of the cascaded converters ($f_{\text{ML}} \cdot N$) could be significantly higher than for the 2L converter, since low-voltage MOSFETs can inherently switch much faster than the IGBTs while resulting in far less power loss. However, due to the computational complexity

Table 3.2: Semiconductor parameters for the 2L converter according to the datasheet, at 150 °C

Parameter	Value	Description
f_{2L}	10 kHz	Switching frequency
$u_{2L,nom}$	400 V	Nominal semiconductor voltage
$i_{2L,nom}$	450 A	Continuous DC collector current
$E_{sw,2L}$	53.5 mJ	Switching energy at nominal current and voltage
$U_{f,IGBT}$	0.85 V	IGBT Forward voltage
$R_{on,IGBT}$	1.9 mΩ	Conduction resistance of IGBT
$U_{f,D}$	1.03 V	Diode Forward voltage
$R_{on,D}$	1.1 mΩ	Conduction resistance of diode

Table 3.3: Semiconductor parameters for the split-DC converters according to the datasheet, at 150 °C

Parameter	Value	Description
f_{ML}	4 kHz	Switching frequency
$u_{ML,nom}$	40 V	Nominal semiconductor voltage
$i_{ML,nom}$	300 A	Continuous drain current (100 °C)
$E_{sw,ML}$	2.2 mJ	Switching energy at nominal current and voltage
$R_{on,FET}$	1.8 mΩ	Drain-source on-state resistance

of the control algorithm, an overall switching frequency of 20 kHz was achieved in the experimental prototype, and this value is used here for consistency.
Despite this relatively low multilevel converter switching frequency, the harmonic distortion of the cascaded converters greatly surpasses the 2L converter due to the multilevel output waveform. If the harmonic distortion were held constant across the converters it would not be possible to provide a realistic comparison, as either the MOSFETs' switching rate would be unreasonably low or the IGBTs' would be unreasonably high. Instead, the switching frequencies reflect common applications at these voltages and currents [F5].

Two-Level Converter For the 2L converter, the battery losses can be directly calculated from eq. (3.22), which gives the rms current of the battery. The mean and rms current of the semiconductors are calculated according to [F95]:

$$\bar{i}_{\mathrm{D}} = \frac{\hat{I}}{2}\left(\frac{1}{\pi} - \frac{m\cos\left(\phi_c\right)}{4}\right), \tag{3.43}$$

$$\bar{i}_{\mathrm{IGBT}} = \frac{\hat{I}}{2}\left(\frac{1}{\pi} + \frac{m\cos\left(\phi_c\right)}{4}\right), \tag{3.44}$$

$$\breve{i}_{\mathrm{IGBT}} = \hat{I}\sqrt{\frac{1}{8} - \frac{m\cos\left(\phi_c\right)}{3\,\pi}}, \tag{3.45}$$

and,

$$\breve{i}_{\mathrm{IGBT}} = \hat{I}\sqrt{\frac{1}{8} + \frac{m\cos\left(\phi_c\right)}{3\,\pi}}. \tag{3.46}$$

where i_{D} and i_{IGBT} denote the currents through each diode and IGBT of the 2L converter, respectively. The switching losses are then calculated according to eq. (3.41).

Split-DC Converters The battery losses of the split-DC converter are calculated using the battery rms current according to eq. (3.32), and multiplied by the number of modules in the converter ($3N$). In contrast to the 2L converter, the phase current is always conducted by the same number of identical semiconductors (4 per SM for the MMSPC and 2 per SM for the CHB), and therefore the split-DC converter semiconductor conduction losses $P_{\mathrm{cond,loss,MMC}}$ can be calculated directly from the phase rms current according to:

$$P_{\mathrm{cond,loss,MMC}} = 3\left(\frac{\hat{I}}{\sqrt{2}}\right)^2 N\,R_{\mathrm{on,FET}}, \tag{3.47}$$

where $R_{\mathrm{on,FET}}$ is the R_{DS} of an equivalent MOSFET in the SM half-bridge of the CHB. In this context, an equivalent MOSFET can consist of several parallel MOSFETs being switched together as a single half-bridge. Since the MMSPC has twice as many half-bridges as the CHB, but each half-bridge is composed of half as many parallel MOSFETs, the result is the same for both split-DC converters. The switching losses are calculated according to eq. (3.41) multiplied by the number of modules.

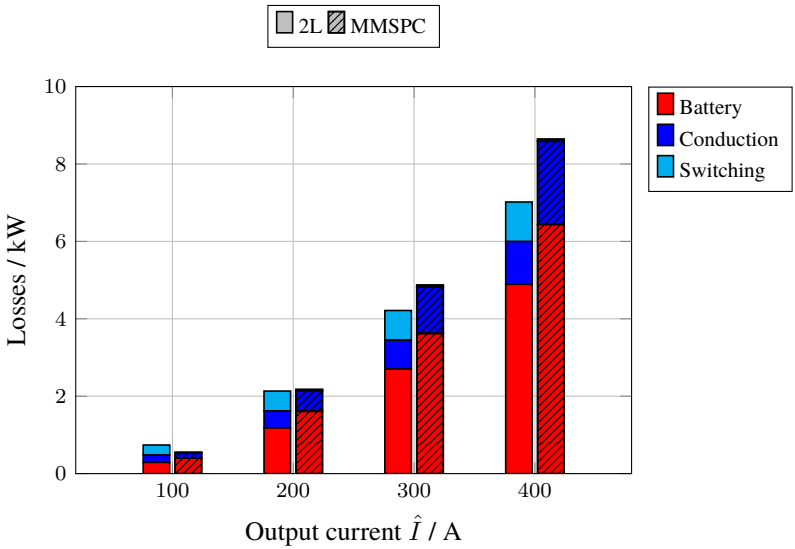
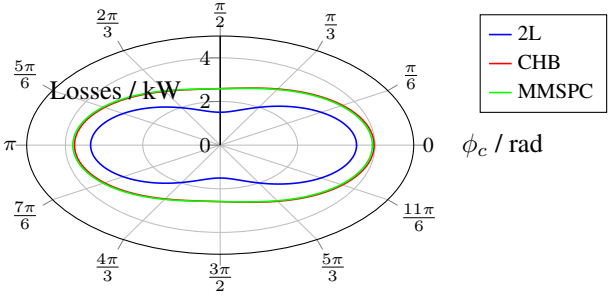


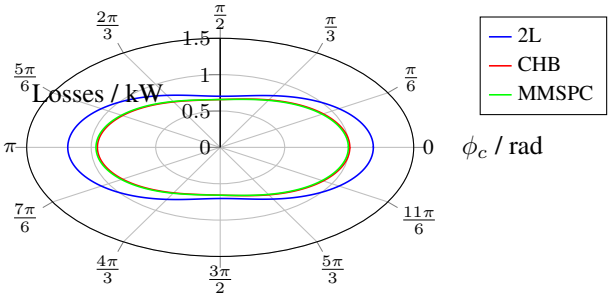
Figure 3.12: Battery, conduction and switching losses of the 2L converter and MMSPC at the maximum output voltage as a function of current. For these operating points, $\phi_c = 0$.

Comparison To compare the three investigated converters, the example application described in table 3.1 is again used, with the semiconductor parameters given in tables 3.2 and 3.3.
Figure 3.12 shows the losses of the 2L converter and MMSPC for different output currents at an output voltage $\hat{U} = \hat{U}_{\max}$. The losses for both converters are dominated by the batteries' ohmic losses for all output currents while the semiconductor losses play a subordinate role. It is noteworthy that the conduction losses of the MMSPC are significantly higher than those of the 2L converter, despite the fact that the nominal current of the semiconductors is higher. This is due to the characteristics of MOSFETs: they are better suited for low-load operation due to their purely ohmic behaviour, while IGBTs are more efficient at higher loads.
For the switching losses, the MMSPC significantly outperforms the 2L converter by a factor of more than eight over the entire current range. This shows the significant advantage in output voltage quality that is achieved by using multilevel converters. The higher output voltage quality can also decrease the losses in the

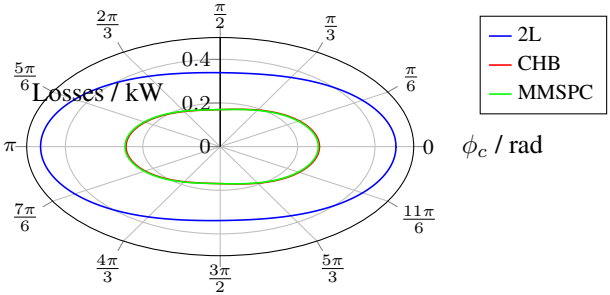
load in the case of e.g. electric motors, as additional losses are reduced [F96]. However, this is not investigated here as the load is assumed to behave the same for all converter types.
Figure 3.13 shows the total losses of the converters at three different output currents ($\hat{I} = 300\,\text{A}$, $\hat{I} = 150\,\text{A}$, $\hat{I} = 75\,\text{A}$), and an output voltage of $\hat{U} = 200\,\text{V}$. The inspection of fig. 3.13 (a) underlines the advantage in losses of 2L converters compared to split-DC converters at high output voltages and currents. The difference is substantial ($>10\%$) at unity power factor when comparing the MMSPC and the 2L converter, and increases as the power factor decreases. As the losses in these cases are dominated by the battery losses, the advantage remains independently of the chosen semiconductors, which are difficult to compare for such different technologies.
It can be seen that at negative power factors, the CHB's losses are lower than the MMSPC's despite the topology being inherently less efficient (in this modelling framework). This is due to the fact that the output current and current are held constant for all converters, but the power entering the batteries varies. The only reason the CHB has lower losses is that the CHB batteries' charging current is lower than for the MMSPC; the efficiency of the CHB is nonetheless worse (see section 3.2.3).
As the output current deceases, the losses of the MMSPC decrease more quickly than in the 2L converter, which can be seen in figs. 3.13 (b) and 3.13 (c), where the output current is reduced to $\hat{I} = 150\,\text{A}$ and 75 A. In addition to the reduction of the losses, the converter losses are significantly less dependent on the power factor compared to at high loads, as the battery losses no longer dominate as strongly.
To investigate the losses over the entire output power capability of the converters, fig. 3.14 shows the losses of the 2L converter over the output current and voltage. Analysis of the figure shows the losses increasing strongly at high output currents and voltages, while the majority of the lower left operating area has low losses.
To compare the 2L losses to the split-DC converters, fig. 3.15 shows the ratio of MMSPC losses to 2L converter losses (fig. 3.14) at $\phi_c = 0$. It shows that the MMSPC system outperforms the 2L at low currents, while the 2L has significantly lower losses at high currents. Especially at operation with high output voltages and high output currents, the MMSPC is worse, as in these points the semiconductor losses are more dominant than in the other operating areas.
The reason that the MMSPC losses are lower than the 2L converter's at low output voltages is that in these operating regions the MMSPC reduces the battery losses by switching its batteries' in parallel, reducing the effective resistance of



(a) $\hat{I} = 300\,\text{A}$ and $\hat{U} = 200\,\text{V}$



(b) $\hat{I} = 150\,\text{A}$ and $\hat{U} = 200\,\text{V}$



(c) $\hat{I} = 75\,\text{A}$ and $\hat{U} = 200\,\text{V}$

Figure 3.13: Losses of the converters at decreasing output voltage. The 2L converter has lower losses at high output voltages, and higher losses at low voltages. The CHB and MMSPC are closely matched, however the MMSPC always has lower losses.

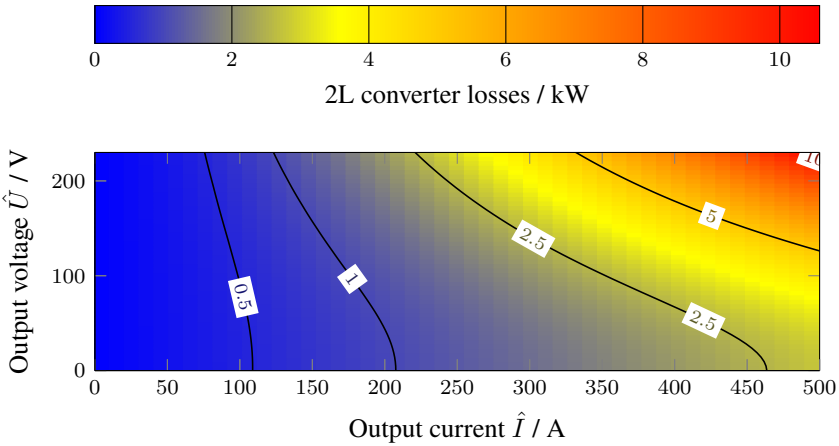


Figure 3.14: Losses of the 2L converter ($\phi_c = 0$) over the operating area

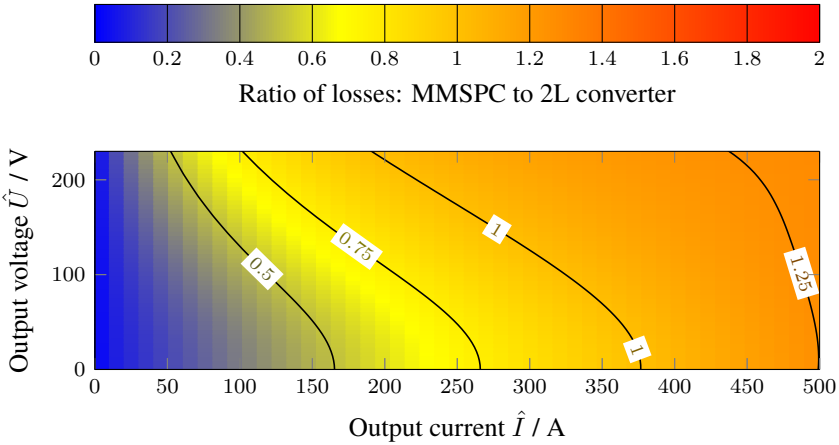


Figure 3.15: Ratio of 2L converter and MMSPC losses over the operating area

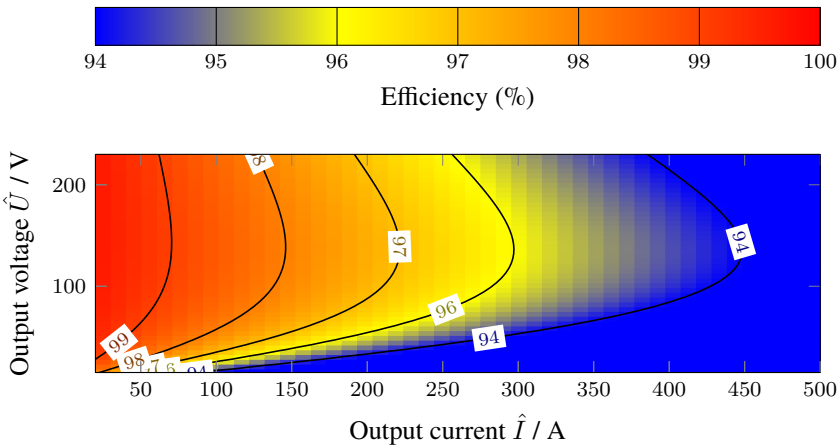


Figure 3.16: Efficiency of the MMSPC over the operating range

the phase. This is especially significant at low output voltages, where more batteries can be switched parallel.

3.2.4 Efficiency

By relating the losses of the converter to their output power, the efficiency of the converter systems can be investigated. This is an important metric, as it determines the amount of usable energy a converter can extract from a fixed amount of energy in a battery.
Figure 3.16 shows the efficiency of the analysed MMSPC at $\phi_c = 0$, according to the equations given in this section. The efficiency is defined as the ratio of the output power to the sum of output power and losses. At low currents, the efficiency of the MMSPC is shown to be excellent, and above 99% below an output current amplitude of 50 A. As the current increases, the efficiency becomes worse, as both the battery and MOSFET losses are proportional to the current squared.
When compared to the efficiency of a state-of-the-art 2L converter, the benefits of the MMSPC become clear. The percentage increase in efficiency of a 2L converter compared to an MMSPC is shown in fig. 3.17, where negative numbers indicate the MMSPC is more efficient and vice versa. The 2L is up to $2\Delta\%$ more

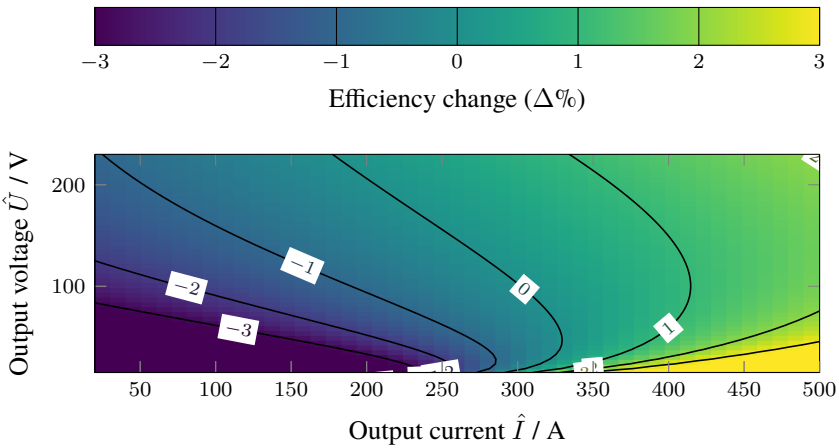


Figure 3.17: Increase in efficiency from MMSPC to 2L converter. Negative numbers indicate that the MMSPC is more efficient.

efficient than the MMSPC at high output currents, as the losses in the converter semiconductors only scale with the first power of the current. Here, Δ% is used to denote a difference in percentage points. Simultaneously, the battery losses are consistently lower than for an MMSPC due to their DC loading.
Nonetheless, the MMSPC performs significantly better at low currents, where vehicles often spend a majority of their operating life. This shows that despite the increase in battery rms current, and therefore battery losses, the MMSPC can provide a viable alternative to conventional converters.
Figure 3.18 shows the same comparison of the MMSPC with the CHB. While the MMSPC is more efficient over the entire operating region, this difference is almost negligible. This arises since the battery losses are the same in both cases, and the only efficiency improvement provided by the MMSPC is the slight reduction in phase resistance, as shown by eq. (3.30). However, the validation in section 6.1 shows that the simplified analysis presented here does not account for the unequal distribution of current in the CHB compared to the MMSPC, which is analysed in detail in chapter 4. The ability of the MMSPC to significantly improve the current distribution in the SMs allows it to reach far higher efficiencies than the CHB for realistic operation points. In contrast, the efficiency difference

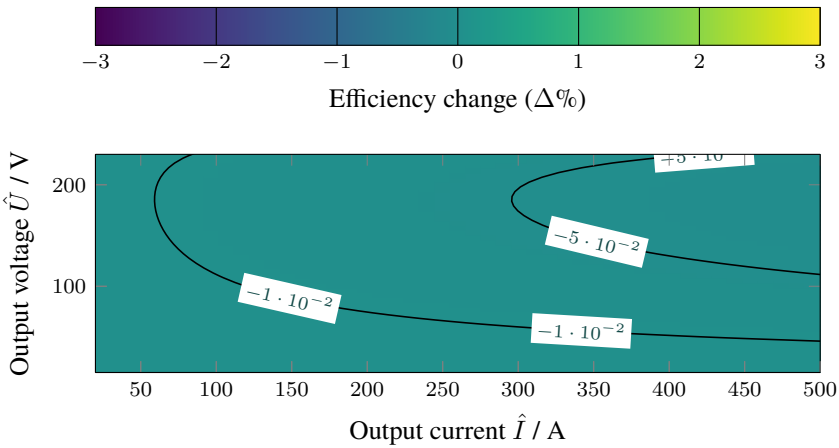


Figure 3.18: Increase in efficiency from MMSPC to CHB. Negative numbers indicate that the MMSPC is more efficient.

between the MMSPC and 2L corresponds very well to the results of the detailed simulation in section 6.1.
Section 6.1 provides a more comprehensive analysis of the converter's efficiencies, and shows which components affect the efficiency in different operating points. Furthermore, the efficiency of the converters is analysed over load profiles based on common automotive drive cycles. The comparison of figs. 3.16 and 3.17 with figs. 6.12 (a) and 6.12 (b) the shows that the simplified equations presented here enable a basic analysis and design of the converter to be performed without necessitating a semiconductor-level simulation. The caveat is, however, that for the results to correspond to real values the battery current must be distributed well within the multilevel converters' SMs, which is not the case for the CHB here.

3.3 Discussion

This section has provided an analytical introduction to the MMSPC, including a comparison with the CHB and conventional 2L converters. The analysis, which assumes an equal current distribution in all batteries—simplifying the ana-

lytical relationships between the output values and battery values—shows the fundamental differences between the single-DC 2L converter and the split-DC converters. The results in the validation of chapter 6 corroborate the analysis here, which provides the tools for engineers to compare these converter architectures at system level.
The following chapter 4 dives deeper into the analysis of the MMSPC, and highlights the differences between the MMSPC and CHB by analysing the impact of the battery current distribution on the batteries' performance. Chapter 4 shows why the discrepancy between the MMSPC and CHB is so large in the verification while being very similar in the simplified analysis presented in this section.

Chapter 4

Design

This chapter highlights several central aspects to the design of an MMSPC, and compares them to the CHB. The aim of the chapter is to help the reader understand the design differences between the two converters, and choose the suitable one for a specific application. As the converter systems contains power electronics and batteries, both aspects are investigated and considered here.
First, a simple converter design for both systems is proposed based on a small number of requirements in section 4.1. The resulting design serves as a reference for the remainder of the chapter, as well as for the simulative validation in section 6.1. This design provides only an outline to determine the parameters of the system. For the full design of a series produced converter system, several other aspects have to be taken into account, such as cost, volume, weight, EMI, and many others that are not handled here.
This is followed by an analysis of the impact of the number of SMs on the converter performance, which considers how well the phase current can be divided between the SM batteries in order to minimise converter losses. Section 4.3 then provides a guide for the most relevant considerations to ensure a good SM design, focussing in particular on how to design the frequency response of the different components of the SM. The provided SM design guide provides a method to ensure that the assumptions used in chapter 3 are reasonable, which enables the system to achieve high efficiencies.
Finally, section 4.4 analyses the impact of the number of SMs and the balancing method on the ability of the converter to maintain the same SoC across all SMs. A novel methodology is presented, which allows any balancing algorithm

to be analysed and shows that high converter efficiency and SoC balancing are competing targets in split-DC converters' performance.
Throughout the chapter, the key performance metrics of the CHB and MMSPC are compared and contrasted, to highlight the differences in their operation and their merits.

4.1 Converter Design

Here, the requirements for an MMSPC application are presented, based on which a converter system can be designed. In the following, the requirements are given, which result in the converter sizing that is used in the simulation to verify the analyses.

4.1.1 Requirements

The basis of any power electronic system design are the requirements describing the application in which the system is used. For this design an automotive application is considered, in which the requirements are given in the form of the current and voltage demands of an electric motor. Furthermore, the range of the example EV is considered, in terms of the energy that must be provided by the converter to the load. The properties of the load, including its losses, are not considered to be within the scope of this work.
In an EV, the electric motor is generally operated in the base frequency region and in field-weakening, with common field weakening factors of up to $2-3$ [F7]. This corresponds to an approximately constant voltage and current above the nominal speed when the motor is operated at maximum torque. As a result, the maximum current requirement is assumed to be constant across the demanded output voltage range. For simplicity, the required maximum torque and current values are considered to be steady-state, without overloading. While this does not correspond to the real-life operation of automotive converters, this simplification allows the converters to be compared against each other fairly, and it is assumed that the relative differences between the converters remain the same when features such as overloading are considered.
The requirements used are general and not extensive or detailed enough to be used for the design of a real-world battery-converter system. The purpose of the general design is to provide a feasible example of the sizing of an MMSPC, which is used to compare its performance in simulation with other converters. The comparison is presented in section 6.1.

Parameter	Value	Description
$\hat{U}_{\text{max}}$	230 V	Maximum load voltage amplitude at maximum current
E_{mot}	48 kW h	Energy delivered to load for the investigated drive cycle
$\hat{I}_{\text{max}}$	400 A	Maximum load current amplitude (available at all voltages)
F_{Sa}	1.05	Voltage control margin

Table 4.1: Converter design requirements. The voltage and currents are phase-to-neutral amplitudes.

A number of other requirements for mass-produced EVs are mentioned here, which are not included in this design. The converter system must be able to provide an output voltage at a high enough frequency to control the motor currents at high speeds. Charging operation must also be considered, as it greatly impacts how automotive converters are designed, due to the difficulty of charging lithium-ion batteries at rates comparable to the re-fuelling of conventional ICE vehicles. Additionally, the power losses generated by the converter and batteries need to be considered, as an EV has limited cooling power available and excessive cooling can significantly reduce its range.
The example requirements of the converter used in this section are given in table 4.1. Section 4.1.2 provides a simple sizing of the converter batteries, which is also used for the simulation in section 6.1.

4.1.2 Battery Sizing

The first step of the basic converter system design is the sizing of the batteries that determine the output voltage and output power of the converter. Based on these values, the batteries can be scaled to change the stored energy and battery resistance. In this section, the number of SM is irrelevant, as only the total battery size is considered. Section 4.2 and the following chapters consider the effects of the number of SMs. For the battery sizing, the battery is again modelled as a constant voltage source with a series resistance, as shown in fig. 4.1. In section 4.3.1.1, a more detailed model of the battery is used to analyse the current distribution within the SM.
Sizing the MMSPC battery begins with the choice of the systems maximum output voltage $U_{\text{DC,max}}$. The voltage must be large enough to supply and control the

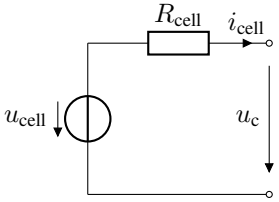


Figure 4.1: Simplified battery equivalent circuit diagram

Table 4.2: Parameters of the battery used

Parameter	Value	Description
R_{cell}	1.3 mΩ	Cell DC resistance
u_{cell}	3.7 V	Nominal cell voltage
i_{cell}	100 A	Nominal cell current
C_{cell}	30 A h	Cell current capacity

output current at all times. This maximum voltage can be calculated by adding the voltage drop over the cells' resistances to the output voltage of the converter. Furthermore, a control margin (or safety factor) F_{Sa} is used to ensure that the current can be controlled at the maximum voltage. This gives the maximum voltage:

$$U_{\text{DC,max}} = F_{\text{Sa}} \left(\hat{U}_{\text{max}} + R_{\text{ph}} \, \hat{I}_{\text{max}} \right), \tag{4.1}$$

where the only variable is the phase resistance R_{ph}. The variable R_{ph} is not defined by the requirements as it is dependent on the chosen battery. As in section 3.2.2, the semiconductor resistances are assumed to be negligible relative to the battery resistances. R_{ph} is calculated as the product of a cell's resistance and the number of cells in series that are needed to reach the desired voltage $U_{\text{DC,max}}$:

$$R_{\text{ph}} = \frac{U_{\text{DC,max}}}{u_{\text{cell}}} \, R_{\text{cell,par}}, \tag{4.2}$$

where u_{cell} is the nominal voltage of the cell and $R_{\text{cell,par}}$ is the resistance of a parallel group of cells (calculated by eq. (4.3)). In general, the number of cells used in an EV must naturally be an integer. Despite this, it is assumed here that non-integer numbers of cells are possible. This is an acceptable assumption as a reference cell is used to represent the behaviour of a representative vehicle

cell, and EV manufacturers generally can vary the capacity of the battery cells to ideally suit a specific application. $R_{\text{cell,par}}$ is calculated based on the estimated required current capacity of a phase C_{ph}, according to:

$$R_{\text{cell,par}} = \frac{C_{\text{cell}}\, R_{\text{cell}}}{C_{\text{ph}}}, \tag{4.3}$$

where C_{cell} and R_{cell} are the current capacity and DC resistance of the cell, respectively. C_{ph} itself can only be estimated as it depends on the calculated series voltage of a phase, and is calculated by:

$$C_{\text{ph}} = \frac{E_{\text{mot}}}{3\,\hat{U}_{\text{max}}}. \tag{4.4}$$

Since the voltage drop over R_{ph} is small, the error incurred by this estimation is negligible.
This allows the converter to deliver the required current at the nominal cell voltage. It should be noted that, in a real application, the cells' voltage is not constant and the power delivered will decrease as the SoC decreases [F80]. In this section, the battery cell voltage is assumed to be constant for simplicity. Substituting eqs. (4.2) to (4.4) into eq. (4.1) and rearranging, gives:

$$U_{\text{DC,max}} = \frac{\sqrt{3}\, E_{\text{mot}}\, F_{\text{Sa}}\, u_{\text{cell}}\, \hat{U}_{\text{max}}}{2\, E_{\text{bat}}\, u_{\text{cell}} - 6\, C_{\text{cell}}\, \hat{I}_{\text{max}}\, R_{\text{cell}}\, F_{\text{Sa}}\, \hat{U}_{\text{max}}}. \tag{4.5}$$

Now the cell resistance must be determined, by evaluating the current and energy requirements that determine the current capacity or number of parallel cells in the converter. Here it is assumed that doubling the number of cells in parallel is the same as doubling the capacity of each cell.
Substituting eq. (4.2) into eq. (3.32) for the MMSPC gives the required rms battery current for the application:

$$\breve{i}_{\text{b},n} = \frac{\hat{I}_{\text{max}}}{36}\left(\frac{23273\, C_{\text{cell}}\, R_{\text{cell}}\, F_{\text{Sa}}\, {\hat{U}_{\text{max}}}^2}{9\left(2\, E_{\text{mot}}\, u_{\text{cell}} - 6\, C_{\text{cell}}\, \hat{I}_{\text{max}}\, R_{\text{cell}}\, F_{\text{Sa}}\, \hat{U}_{\text{max}}\right)} + \frac{1874161\, {C_{\text{cell}}}^2\, {R_{\text{cell}}}^2\, {F_{\text{Sa}}}^2\, {\hat{U}_{\text{max}}}^4}{2592\left(E_{\text{mot}}\, u_{\text{cell}} - 3\, C_{\text{cell}}\, \hat{I}_{\text{max}}\, R_{\text{cell}}\, F_{\text{Sa}}\, \hat{U}_{\text{max}}\right)^2} + 588\right)^{\frac{1}{2}}, \tag{4.6}$$

as a function of the requirements and the battery resistance R_{cell}. Here, $\breve{i}_{\text{b},n}$ is the current that the converter battery must be able to deliver. Since it is an

rms current, it can be compared to the rated DC current of a battery according to its specification. Simplifying eq. (4.6), where the first two fractions in the exponentiated brackets are more than an order of magnitude smaller than 588 for the example design, gives:

$$\breve{i}_{\mathrm{b},n} \approx \frac{\hat{I}_{\mathrm{max}}\sqrt{588}}{36} = 0.674\,\hat{I}_{\mathrm{max}}. \tag{4.7}$$

In general, $\breve{i}_{\mathrm{b},n}$ is likely to be higher than the current that a single cell can deliver, and therefore a certain number of cells $n_{\mathrm{b,par}}$ may be needed in parallel for each SM:

$$n_{\mathrm{b,par}} = \frac{\breve{i}_{\mathrm{b},n}}{i_{\mathrm{cell}}}, \tag{4.8}$$

where i_{cell} is the maximum current of a battery cell. Given $n_{\mathrm{b,par}}$, the total energy that the converter E_{bat} can provide can now be calculated, if the load-cycle efficiency of the converter system η_{load} is known. Assuming that the energy capacity of a cell E_{cell} is given by $E_{\mathrm{cell}} = C_{\mathrm{cell}}u_{\mathrm{cell}}$, where C_{cell} is the current capacity, the total energy in the converter is simply a summation of the energy of all of the cells:

$$E_{\mathrm{bat}} = \eta_{\mathrm{load}}\,3\frac{U_{\mathrm{DC,max}}}{u_{\mathrm{cell}}}\,n_{\mathrm{b,par}}\,E_{\mathrm{cell}}. \tag{4.9}$$

η_{load} can now be calculated based on section 3.2.3 and the given load profile of the converter application (in this case WLTP). For the optimal cell in the given application, the energy delivered by the battery should be equal to the energy required by the load:

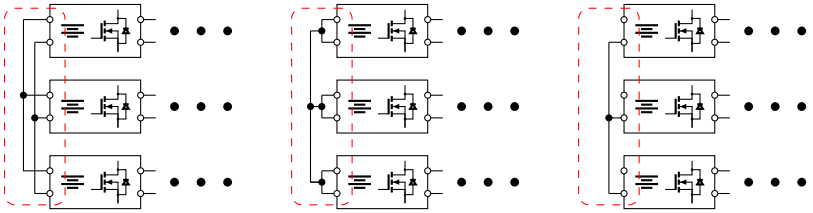
$$E_{\mathrm{bat}} \stackrel{!}{=} E_{\mathrm{mot}}, \tag{4.10}$$

and the optimal cell is the cell whose parameters fulfil this optimisation objective. Since both E_{cell} and $n_{\mathrm{b,par}}$ (through i_{cell}) are dependent on the chosen cell, the solution to eq. (4.10) to find the optimal cell must be calculated iteratively. Based on the chosen cell, the further detailed design of the converter can be done.
The Samsung CM0280R0001C is used for this converter design, as detailed parameters are provided and its suitability for use with AC currents is shown in [F93]. The parameters of the battery are extracted from the electrochemical impedance spectroscopy (EIS) of the paper, and given in table 4.2. Using this cell, and assuming an overall converter efficiency of 95% (see section 6.1.3.2), the converter

is sized according to the equations presented in this section, giving a design with 52 cells in series and 2.73 cells in parallel. While a real application can clearly not have non-integer numbers of cells in parallel, this design and the subsequent validation assumes it is possible, as cells are made to a capacity specification in real applications, and the capacity can be varied to meet a specific demand of the EV manufacturer.
The presented analysis shows how a first general design of the converter can be performed, before the division of a phase into SMs must be considered. Due to the assumptions taken (temperature-independent battery performance, no battery ageing, no auxiliary loads, etc.) the design shown here is simple and only given to serve as a reference for the following sections. A full production EV system design would require a far more detailed approach. Section 6.1 uses the battery design presented here for a comparison of the MMSPC, CHB and 2L converter.

4.1.3 Neutral Point

Since the MMSPC's SMs have two electrical connections to neighbouring SMs, an additional degree of freedom in how the neutral point SMs are connected arises, as discussed in section 2.1.2.3. The different connections of the neutral point can have various benefits and drawbacks for the converter system.
For a symmetrical build-up of the SMs, two possibilities exist to connect the neutral point: connect all upper and lower connection points of the SMs in parallel (fig. 4.2 (a)), or connect all connection points together in a shorted configuration (fig. 4.2 (b)).
In the parallel configuration, the neutral point batteries can be connected in parallel and thus energy can be transferred directly between the phases of the converter, and auxiliary loads can be connected to their poles. The shorted configuration is simpler electrically and for the balancing algorithm, but does not allow energy transfer between the phases. Furthermore, it is not possible to use the neutral point SMs as a source for auxiliary loads in the EV directly, because there is no DC connection available. The single connection is not relevant for the symmetrical SM, as it offers no advantage over the shorted configuration.
As discussed in section 2.1.2.3, the SM may be built asymmetrically onto a PCB in order to ensure the synchronicity of the switching signals for the transistors. This option has been chosen for the experimental validation, as the risk of non-synchronous switching in the symmetric build-up is considered too large. In this case, the battery's electrodes are directly connected to the SM connections without any semiconductors to disconnect them. As a result, the neutral point of the converter can be connected in three different ways: the parallel configuration



(a) Parallel configuration (b) Shorted configuration (c) Single connection

Figure 4.2: Possibilities for realising the MMSPC neutral point. The neutral point of the wye connection is circled in red. The ellipses indicate the connection to the other SMs. It is noteworthy that the shorted configuration in (b) cannot be used with the asymmetrical SM architecture, as it would result in the battery poles being shorted.

or the single connection configuration (with either lower or upper connection points connected), as shown in fig. 4.2.
In all cases, the number of available voltage levels compared to the symmetric SM is reduced by 1. As a result, the maximum output voltage $U_{\mathrm{DC,max}}$ is reduced by half of a SM voltage. The output voltage is symmetrical around the voltage midpoint between the positive and negative battery voltage of the first SM.
The difference between the parallel connection and the unipolar connections of the neutral point are that the parallel connection again allows energy transfer between the phases, as well as the connection of auxiliary loads to the neutral point SMs of the converter. A disadvantage is the increased complexity of the cabling and the fact that the neutral point SMs are now loaded differently to the other SMs in the phase.
Considering the only way to connect auxiliary loads to the MMSPC with asymmetrical SMs is the use of a parallel-connected neutral point, this topology is chosen for the laboratory prototype (section 6.2.1).
This results in two changes on the analysis presented in chapter 3. First, the maximum voltage $U_{\mathrm{DC,max}}$ is reduced by $u_{\mathrm{b},n}/2$. Second, the current loading of the batteries in neutral point is different to the loading of the other batteries in the phase.
Since the neutral point batteries are now connected in parallel, each battery sees the load of the current in its own phase in addition to the current loading of the other two phases. The configuration of the batteries and SMs in this case is shown in fig. 4.3. In the case with zero resistance, summation of the currents for

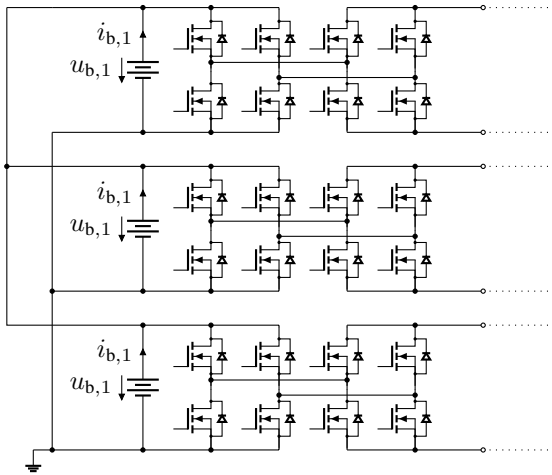


Figure 4.3: The electrical arrangement of the batteries when the asymmetrical SM is connected in the parallel configuration (fig. 4.2 (a)). Because the batteries are connected in parallel, they are all loaded by the same current, as derived in eq. (4.11).

all phases in eq. (3.9) divided by three gives the current in the neutral point SM batteries ($n = 1$):

$$i_{\mathrm{b},1} = \frac{1}{3}\sum_{i=1}^{3} m \sin\left(\omega t + \frac{2\pi(i-1)}{3}\right)\hat{I} \cdot \sin\left(\omega t + \frac{2\pi(i-1)}{3} - \phi_c\right). \quad (4.11)$$

This expression simplifies to a DC current (and therefore the rms-current):

$$i_{\mathrm{b},1} = \breve{i}_{\mathrm{b},1} = \frac{\hat{I} m \cos\phi_c}{2}, \quad (4.12)$$

which gives the same result if THI is included in the voltage term of eq. (4.11), unlike the currents in the other SMs' batteries. Due to the fact that these batteries only see a DC current, their rms current is lower than that of the other batteries even though the mean value is the same.
The ratio of neutral point's rms current to the other batteries' rms current $\breve{i}_{\mathrm{b},1}/\breve{i}_{\mathrm{b},n}$ is $^6/_7 = 0.857$ with THI and $\sqrt{^6/_3} = 0.817$ without, independently of the output

voltage and at $\phi_c = 0$. This analysis assumes the resistances within the SM is negligible.
Even though the neutral point batteries see a slightly lower rms current than the other phase batteries, their use for auxiliary loads will increase the effective current they see. Therefore, in the further analysis presented, the current load on all batteries is assumed to be equal.

4.2 Number of Sub-Modules: Efficiency Considerations

After the general sizing of the converter, including the number of batteries in series and in parallel, the number of SMs can be decided. There are several advantages and disadvantages of increasing the number of SMs, which will be evaluated here. Of course, the complexity and resulting cost may be a significant factor in the decision of the number of SMs, but it is not treated explicitly here.
The choice of the number of SMs has a significant impact on the output voltage quality and the battery current distribution and is largely affected by the choice of semiconductors available.
Analysis of the current distribution in the MMSPC and CHB SMs is a significant aspect of this work, and it is important for two reasons, which are elucidated here. The two reasons for the significance of the current distribution are relevant in vastly different time scales, from the time scale of the power electronic switching to the time scale of a discharge cycle of the batteries. In this section, the short-term current distribution is analysed, which impacts the efficiency of the converter.
In section 4.4, the long-term current distribution is treated, which affects the ability of the converter to balance the SoCs of the SMs. It is evident that—especially for the MMSPC with extensive use of the parallel mode—these two goals are contradictory.
The short-term current distribution is affected by the number of SMs and the switching frequency of the semiconductors. In order to investigate the current distribution within a phase of the MMSPC, the vector $\vec{S}_\mathrm{p}$ is introduced, which is a vector that encodes the switching states of an MMSPC phase.
The length of the vector gives the number of SMs that are switched in series of a particular phase, while each element in the vector indicates how many SMs are in parallel for this parallel group $p \in \{1,...,N\}$. In addition, the sign indicates the

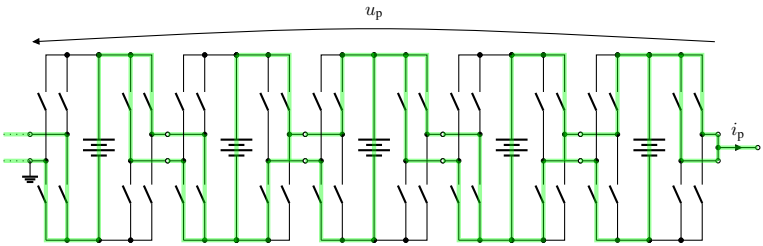


Figure 4.4: An example configuration of an MMSPC phase corresponding to $\vec{S}_\mathrm{p} = \begin{pmatrix}1 & 2 & 2\end{pmatrix}^\mathrm{T}$. The green highlight indicates the current path. For this example, $N = 5$.

polarity of the SMs ($+$ is series positive, $-$ is series negative). The sum of the absolute values of the entries of $\vec{S}_\mathrm{p}$ must be equal to N if no SMs are bypassed. For example, if:

$$\vec{S}_\mathrm{p} = \begin{pmatrix}1\\2\\2\end{pmatrix}, \tag{4.13}$$

the output voltage of the phase is $3u_\mathrm{b}$. In the first, second and third parallel groups $p = 1$, $p = 2$, and $p = 2$, respectively. For consistency, a single SM in series is considered a parallel group with $p = 1$, even though there are technically no SMs in parallel.
As more SMs are used, the chance that the SMs can be configured in such a way that the current can be split equally is increased. For example, if $N = 8$, the current can be split equally at the following output voltages:

- $u_\mathrm{p} = U_\mathrm{DC,max} \rightarrow M = 8 \rightarrow \vec{S}_\mathrm{p} = \begin{pmatrix}1 & \cdots & 1\end{pmatrix}^\mathrm{T}$
- $u_\mathrm{p} = {}^{U_\mathrm{DC,max}}/_{2} \rightarrow M = 4 \rightarrow \vec{S}_\mathrm{p} = \begin{pmatrix}2 & 2 & 2 & 2\end{pmatrix}^\mathrm{T}$
- $u_\mathrm{p} = {}^{U_\mathrm{DC,max}}/_{4} \rightarrow M = 2 \rightarrow \vec{S}_\mathrm{p} = \begin{pmatrix}4 & 4\end{pmatrix}^\mathrm{T}$
- $u_\mathrm{p} = {}^{U_\mathrm{DC,max}}/_{8} \rightarrow M = 1 \rightarrow \vec{S}_\mathrm{p} = \begin{pmatrix}8\end{pmatrix}^\mathrm{T}$

This is because for each of these output voltages the number of parallel SMs is the same in each group of parallel SMs. An increase in the switching frequency also allows the current to be distributed better in time, as in cases where the

distribution is not equal, the SMs can be rotated between different configurations more quickly.
This analysis assumes that the current is always split evenly between parallel SMs, which is an assumption that is not always valid (see section 4.3.2). For the calculations presented here, the non-even split of current is neglected, because it only occurs when three or more SMs are in parallel. This is only the case when the modulation index is low, in which cases the current is generally well distributed compared to higher modulation indices (see fig. 4.9), and as a result this assumption does not significantly alter the results here.
In order to investigate the current distribution as a function of the switching frequency and number of SMs, it is assumed that the SM switching is so fast that the batteries are not subjected to switching currents. This is ensured by the sizing of the SM power electronics and decoupling capacitors, given in section 4.3.2.2.
Since the current distribution is dependent on the way in which the SMs of a phase are switched ($\vec{S}_\mathrm{p}$), the balancing strategy must always be taken into account. In this context, the balancing strategy describes the choice of $\vec{S}_\mathrm{p}$ in dependence of the desired output level $M \in \{0,...,N\}$ (which is an output of the superordinate motor control scheme). Here, M is the number of SMs switched in series in a phase.
The balancing strategy that underlies the analysis in this section is the so-called 'efficiency-optimal balancing' that is optimal with regards to the short-term current distribution of the SMs. When the batteries are modelled as voltage sources with inner resistances, and the converter (including the semiconductors) is free of parasitic elements, this is the balancing strategy that achieves the highest efficiency. In this idealised case, the only losses that occur are within the batteries, due to their inner resistance.
This idealisation is an accurate approximation to determine the losses incurred due to the balancing strategy, as the conduction losses in the semiconductors depend only on the phase current (since the same number of MOSFETs are always conducting the same current). The switching losses are similarly independent of the balancing strategy, and in general far lower than the conduction losses for MOSFETs in the $<$100 V range.
The optimal balancing uses the parallel mode of the SMs as often as possible and also tries to distribute the current in all batteries in a phase as evenly as possible. The reason that a an even distribution is optimal for losses is that the battery losses are proportional to the battery current squared, and the sum of all battery currents in a phase is always equal and independent of the chosen $\vec{S}_\mathrm{p}$. Thus the

lowest losses will be achieved when the current is equally distributed across all batteries.
Since the parallel state provides a more equal current distribution than the bypass state, it is always preferred. To distribute the battery current evenly, there will always be at most two different widths of parallel groups in a phase for a given output level of a phase. Here the width of a parallel group means the number of SMs in parallel (p). This ensures that the current in all batteries of a phase is as close to the mean battery current as possible.
As an example, an MMSPC with five SMs per phase is considered ($N = 5$). This number of SMs will be used throughout the rest of this chapter to exemplify the calculations.
When $M \leq {}^{N}/_{2}$, it is possible to have at least two SMs in parallel in each group, for example when $M = 2$ in the configuration $\vec{S}_{\mathrm{p}} = \begin{pmatrix} 2 & 3 \end{pmatrix}^{\mathrm{T}}$.
When $M > {}^{N}/_{2}$, groups with single SMs must be used to achieve the output level, e.g. at $M = 4$, $\vec{S}_{\mathrm{p}} = \begin{pmatrix} 2 & 1 & 1 & 1 \end{pmatrix}^{\mathrm{T}}$.
Of course, sometimes only one width of parallel group is needed as described above (when ${}^{N}/_{M} \in \mathbb{Z}$), which results in the ideal current distribution.
Generalising this rule, the two possible values that the width of a parallel group p takes is given by:

$$p_1(M) = \left\lceil \frac{N}{M} \right\rceil \qquad \text{and} \qquad p_2(M) = p_1 - 1, \tag{4.14}$$

where $\lceil\ \rceil$ denotes the ceiling function.
In the above example, where $N = 5$, $M = 2$ and $\vec{S}_{\mathrm{p}} = \begin{pmatrix} 2 & 3 \end{pmatrix}^{\mathrm{T}}$:

$$p_1 = \left\lceil \frac{N}{M} \right\rceil = \left\lceil \frac{5}{2} \right\rceil = 3, \tag{4.15}$$

and

$$p_2 = p_1 - 1 = 2. \tag{4.16}$$

The number of parallel groups in a phase with widths p_1 and p_2, is $n_{\mathrm{p},1}$ and $n_{\mathrm{p},2}$, respectively. These can be calculated according to:

$$n_{\mathrm{p},1} = N - Mp_2 \qquad \text{and} \qquad n_{\mathrm{p},2} = p_1 M - N. \tag{4.17}$$

Using the same example of eqs. (4.15) and (4.16):

$$n_{\mathrm{p},1} = N - Mp_2 = 5 - 2 \cdot 2 = 1, \tag{4.18}$$

and

$$n_{\mathrm{p},2} = p_1 M - N = 3 \cdot 2 - 5 = 1. \tag{4.19}$$

For the readability of these equations it has again been assumed that the output voltage is always positive, even though this analysis also applies for negative output voltages. In this case, M and p both switch sign and the result stays the same, except that series positive is switched with series negative.
While p_1, p_2, $n_{\mathrm{p},1}$, and $n_{\mathrm{p},2}$ give the number of parallel and series SMs in a phase, they do not give any information about which specific SMs are switched in parallel and which are switched in series. In the case of efficiency-optimal balancing, the exact SMs that are switched in series and parallel are rotated to ensure that the current is distributed evenly in the batteries. For example, for the case that $M = 2$ and $N = 5$ as above, the phase state $\vec{S}_{\mathrm{p}}$ switches between $\vec{S}_{\mathrm{p}} = \begin{pmatrix} 2 & 3 \end{pmatrix}^{\mathrm{T}}$ and $\vec{S}_{\mathrm{p}} = \begin{pmatrix} 3 & 2 \end{pmatrix}^{\mathrm{T}}$.
If the switching between all possible values of $\vec{S}_{\mathrm{p}}$ for each M is fast, the current of the batteries is considered to be ideally distributed between the SMs for this M. In normal operation, M will also vary with the modulation index m. In the following, the degree to which the current is distributed is derived.
Considering the earlier case $M = 2$ and $N = 5$, the battery current is distributed unevenly, with $i_{\mathrm{p}}/2$ flowing through the SMs where $p = 2$, and $i_{\mathrm{p}}/3$ through the SMs where $p = 3$. More generally,

$$i_{\mathrm{b},n} = \frac{i_{\mathrm{p}}}{p}, \tag{4.20}$$

while the mean current through all SMs $\bar{i}_{\mathrm{b}}$ is given by:

$$\bar{i}_{\mathrm{b}} = \frac{1}{N} \sum_{n=1}^{N} i_{\mathrm{b},n} = \frac{1}{N} \left(n_{\mathrm{p},1} \frac{i_{\mathrm{p}}}{p_1} + n_{\mathrm{p},2} \frac{i_{\mathrm{p}}}{p_2} \right) = i_{\mathrm{p}} \frac{M}{N}, \tag{4.21}$$

which is the expected result, as it is the discretised form of eq. (3.9) obtained by the ideal analysis.
From this result, the deviation from the mean current in each SM $\delta i_{\mathrm{b},n}$ can be calculated to determine how evenly the current is distributed. For each SM, the relative deviation from the mean current is:

$$\delta i_{\mathrm{b},n} = \frac{i_{\mathrm{b},n} - \bar{i}_{\mathrm{b}}}{i_{\mathrm{p}}}, \tag{4.22}$$

and the average absolute deviation within the phase δi_p is:

$$\delta i_\mathrm{p}(M) = \frac{1}{N}\sum_{n=1}^{N}|\delta i_{\mathrm{b},n}|. \tag{4.23}$$

The value of δi_p provides a measure of how unbalanced the battery currents in the MMSPC are for each output level M under efficiency-optimal balancing. The larger the average deviation δi_p is, the more unevenly the currents are distributed within a phase of the converter. This uneven distribution leads to increased losses as the total rms current of the batteries is always minimal when all currents are equal. In addition to δi_p, the number of available different switching states per M also plays a large role in the distribution of the currents, which is explored below.

Figure 4.5 shows the total current deviation of a phase for different values of M and N, for both the MMSPC and CHB. The current distribution with $N = 500$ indicates the distribution as $N \to \infty$. For the MMSPC, it can be seen that the shape of the distribution over the output levels is the same regardless of the number of SMs, but is more smooth the larger the number of SMs is. The deviation is highest between $M/N = 1/2$ and $M/N = 1$ and decreases as the output level decreases. In the cases where N/M is an integer, the current distribution is ideal and the deviation is zero.

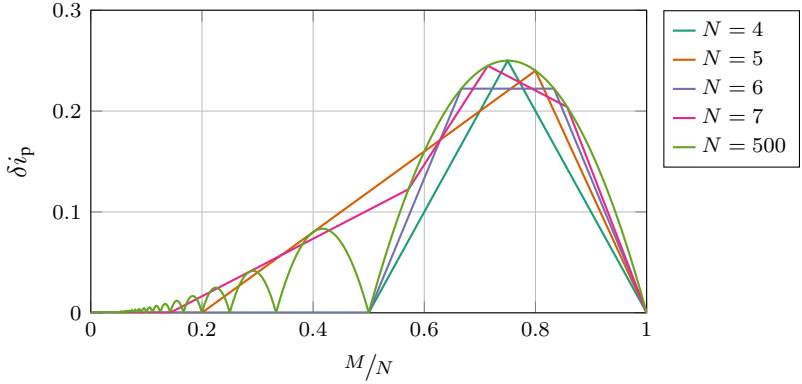
From fig. 4.5, it can be seen that increasing the number of SMs does not improve the distribution of the currents. In fact, a SM number of four or six has an ideal current distribution below $M/N = 1/2$, as here $n_{\mathrm{p},2} = 0$.

Compared to the CHB, the current distribution of the MMSPC is far more equal due to the ability to switch the SMs in parallel. For the CHB, the expression for $\delta i_\mathrm{p}(M)$ is:

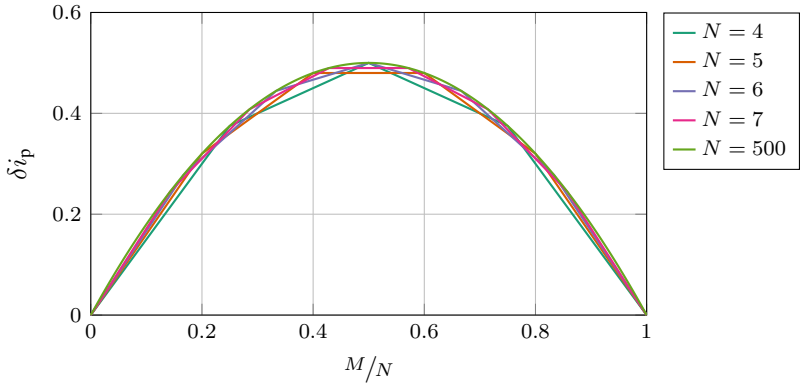
$$\delta i_\mathrm{p}(M) = 2 - 2\frac{M}{N}, \tag{4.24}$$

which is always significantly higher than the value for the MMSPC, especially below $M/N = 1/2$, where the deviation for the MMSPC decreases towards zero but is large for the CHB.

While δi_p shows how unevenly the current is distributed, it does not take the switching between states into account. For this, the number of different states that need to be applied before the current is on average ideally distributed needs to be determined.



(a) MMSPC



(b) CHB

Figure 4.5: Current deviation within a phase for different output levels and different numbers of SMs. These distributions are representative for the efficiency-optimal balancing methodology, and are a function of the balancing methodology used. Note the different y axes.

Considering the previous case, where $\vec{S}_\mathrm{p} = \begin{pmatrix}2 & 3\end{pmatrix}^\mathrm{T}$ or $\vec{S}_\mathrm{p} = \begin{pmatrix}3 & 2\end{pmatrix}^\mathrm{T}$, two different states are necessary to distribute the current ideally. Similarly, for $M = 3$ and $\vec{S}_\mathrm{p} = \begin{pmatrix}2 & 2 & 1\end{pmatrix}^\mathrm{T} | \begin{pmatrix}2 & 1 & 2\end{pmatrix}^\mathrm{T} | \begin{pmatrix}1 & 2 & 2\end{pmatrix}^\mathrm{T}$, three different states are necessary.
Figure 4.6 shows the battery current over two cycles of each possible $\vec{S}_\mathrm{p}$ in this case. Due to the limitations of the discrete number of output levels, it is not possible to distribute the current more evenly (i.e. to reduce $\delta i_{\mathrm{b},n}$) than as shown, but this does not mean that each battery will deliver the same amount of charge over a cycle. It can be seen that the average current in batteries 2 and 4 is lower than in the other batteries. Hence, efficiency is optimised due to good distribution of currents, but over time the SoCs of the batteries will drift.
The number of necessary states can be determined by finding the number of unique permutations of $\vec{S}_\mathrm{p}$. Before the permutations are calculated, the vector $\vec{S}_\mathrm{p}$ can be simplified if it is symmetrical.
$\vec{S}_\mathrm{p}$ can be simplified if the greatest common divisor (gcd) of $n_{\mathrm{p},1}$ and $n_{\mathrm{p},2}$ is larger than one. For example, when $N = 6$ and $M = 4$:

$$p_1 = \left\lceil \frac{N}{M} \right\rceil = 2 \qquad \text{and} \qquad p_2(M) = p_1 - 1 = 1, \tag{4.25}$$

and

$$n_{\mathrm{p},1} = N - Mp_2 = 2 \qquad \text{and} \qquad n_{\mathrm{p},2} = p_1 M - N = 2. \tag{4.26}$$

Since there are two parallel groups of width 2 and two parallel groups of width 1, it is not necessary to use all possible permutations of $\vec{S}_\mathrm{p}$ to distribute the current ideally. Instead, the ideal distribution can be found by dividing the phase by $\gcd(n_{\mathrm{p},1}; n_{\mathrm{p},2}) = 2$, and only analysing half of the SMs, because the other half can switch between the states identically.
Considering this, the number of necessary permutations n_σ can be mathematically expressed as:

$$n_\sigma = \frac{\left(\frac{n_{\mathrm{p},1}+n_{\mathrm{p},2}}{\gcd(n_{\mathrm{p},1};n_{\mathrm{p},2})}\right)!}{\frac{n_{\mathrm{p},1}}{\gcd(n_{\mathrm{p},1};n_{\mathrm{p},2})}! \cdot \frac{n_{\mathrm{p},2}}{\gcd(n_{\mathrm{p},1};n_{\mathrm{p},2})}!}. \tag{4.27}$$

In the ideal case, n_σ would always be 1, and therefore no switching would be necessary to ideally distribute the currents. However, this is not the case for many output levels, where a significant number of switching state permutations are

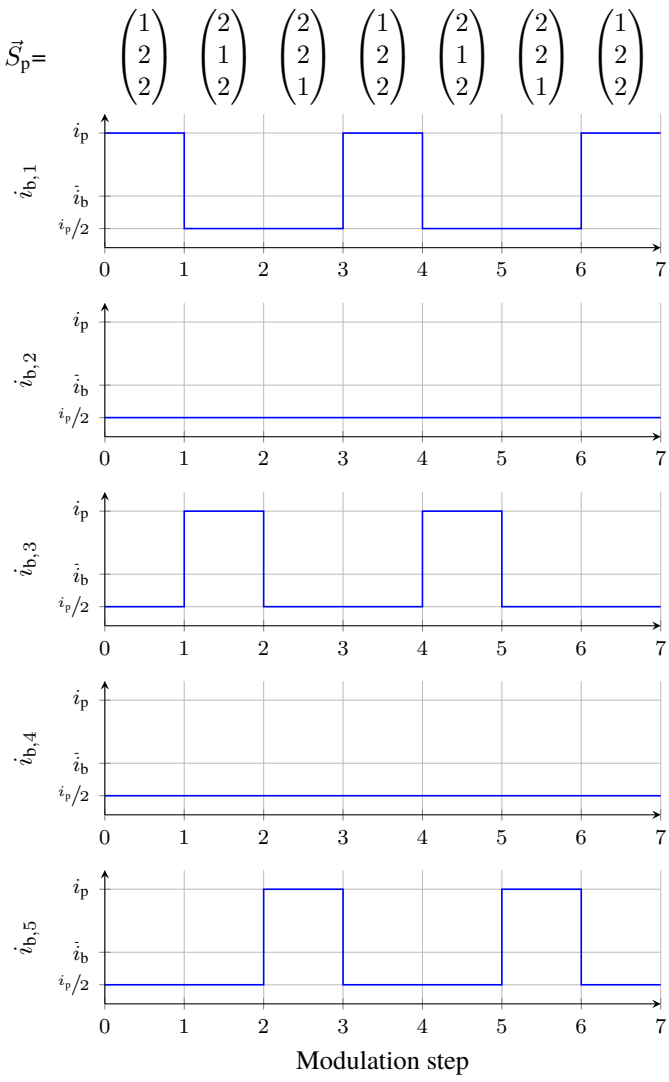


Figure 4.6: Current in each SM battery over the cycle of each possible phase switching state for the case $N = 5$ and $M = 3$. In total, there are three permutations of phase vector $\vec{S}_{\mathrm{p}}$ for this output level and therefore $n_\sigma = 3$.

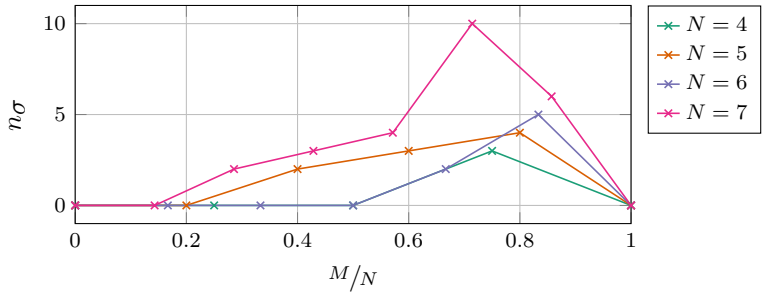


Figure 4.7: Number of permutations of $\vec{S}_\mathrm{p}$ for different output levels and numbers of SMs for the MMSPC

necessary to use all available switching states at an output level. As n_σ increases, the required switching rate to distribute the battery currents well increases. Calculating n_σ for the previous case where $N = 6$ and $M = 4$, gives:

$$n_\sigma = \frac{(1+1)!}{1! \cdot 1!} = 2. \tag{4.28}$$

Now an example with five SMs is considered, where $N = 5$ and $M = 3$, giving:

$$p_1 = \left\lceil \frac{N}{M} \right\rceil = 2 \qquad \text{and} \qquad p_2(M) = p_1 - 1 = 1, \tag{4.29}$$

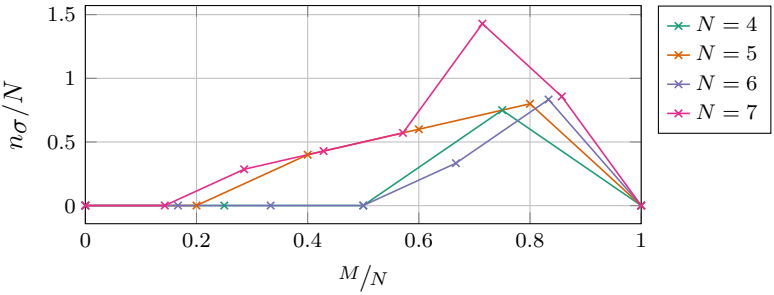
and

$$n_{\mathrm{p},1} = N - Mp_2 = 2 \qquad \text{and} \qquad n_{\mathrm{p},2} = p_1 M - N = 1. \tag{4.30}$$

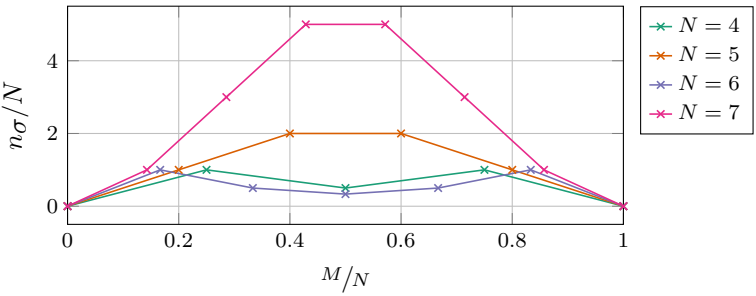
In this example, the gcd of $n_{\mathrm{p},1}$ and $n_{\mathrm{p},2}$ is 1, and therefore the number of permutations are:

$$n_\sigma = \frac{(2+1)!}{2! \cdot 1!} = 3, \tag{4.31}$$

as shown previously.
Figure 4.7 shows the number of necessary phase state permutations n_σ, to ensure that the current is ideally distributed for different values of M and N(for the MMSPC). The number of states increases considerably as the number of SMs of the converter is increased, indicating that a greater number of SMs does not make it easier to distribute the battery currents. Even if it is considered that



(a) MMSPC



(b) CHB

Figure 4.8: Number of state permutations n_σ, weighted by the number of SMs. The values are shown for different output levels and different numbers of SMs. Note the different y axes.

with more SMs the phase switching rate can increase without increasing the SM switching rate, the effort of ensuring balanced current distribution still greatly increases with the number of SMs. This is shown in fig. 4.8, which shows the number of permutations divided by the number of SMs N. It can also be seen that the MMSPC requires far fewer cycles to use all available phase states.
Investigating figs. 4.5 and 4.8, it can be seen that higher modulation indices make it more difficult to distribute the current for two reasons: the number of 'optimal' ways to switch the SMs increases and the current is less well distributed because there are fewer SMs in parallel.

Performance Metric for Current Distribution Based on the calculations of the previous section, this section derives a performance metric for the current distribution across the phase batteries. The performance metric describes how well the current is distributed, which reduces the overall losses in the batteries. There are two factors that determine how well the battery current is distributed: the current imbalance δi_p, and the number of switching cycles before a phase state $\vec{S}_\mathrm{p}$ is repeated (given by the number of $\vec{S}_\mathrm{p}$ permutations n_σ).
To quantify the effect of these factors for a particular output level, a performance function J_N is defined:

$$J_N = \delta i_\mathrm{p}(M,N) \cdot \frac{n_\sigma(M,N)}{N}, \tag{4.32}$$

which evaluates the optimality of an output level M and a number of SMs $N$with regards to the current distribution. Since J_N captures the imbalancing battery currents as well as the number of switching cycles required to evenly load all of the SMs, it provides a quantitative measure of how well currents are distributed for a particular balancing algorithm and number of SMs. As such, it provides a measure of the efficiency of a particular balancing algorithm. It should be noted that J_N is a function of the output level.
The value of J_N for each output level and for several different numbers of SMs is shown in fig. 4.9. Figure 4.9 shows that the MMSPC greatly outperforms the CHB with regards to its ability to distribute the current between SMs. This is due to the fact that the parallel mode allows it to inherently distribute current well (see fig. 4.5), and the fact that far fewer rotations of the SMs are necessary to use all available phase states (see fig. 4.8).
The sum of all J_N for a specific number of SMs, ΣJ_N, evaluates how well a certain number of SMs distributes the current, according to:

$$\Sigma J_N = \sum_{M=1}^{N} J_N(M). \tag{4.33}$$

ΣJ_N therefore quantifies how well a balancing method distributes the currents for all output levels, on average. The larger the value, the more unequal the current distribution is, leading to higher losses.
Figure 4.10 shows ΣJ_N for each output level from three to seven. It shows that there is a huge gap in the current distribution between the CHB and MMSPC with efficiency-optimal balancing, with the MMSPC having an advantage of almost an order of magnitude for each N. Furthermore, the addition of SMs decreases the ability of the converters to distribute the current well, mainly due to the fact

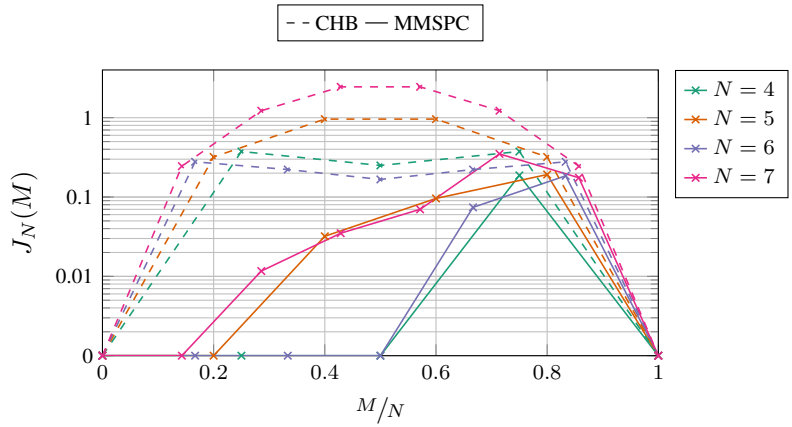


Figure 4.9: Value of the battery current distribution performance function J_N for the MMSPC and CHB for several different numbers of SM. The MMSPC performs far better than the CHB for all output levels. In order to show where J_N is zero, the y axis is modified and not strictly logarithmic.

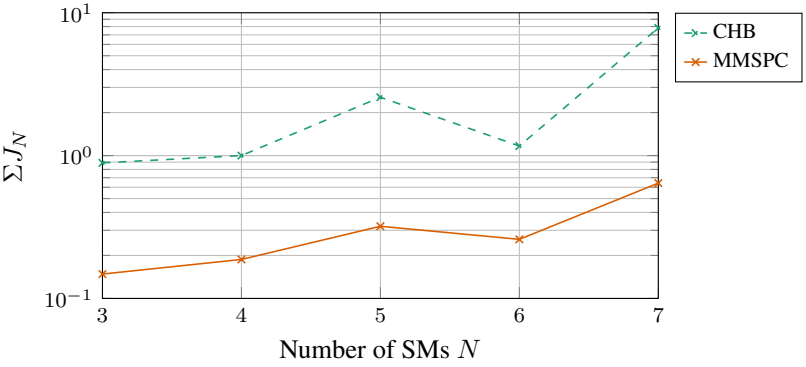


Figure 4.10: Sum of J_N over all output levels as a function of the number of SMs

that there are far more permutations of possible phase state vectors $\vec{S}_\mathrm{p}$ that need to be iterated.
This analysis has shown how well-distributed the SM currents in the MMSPC and CHB are when balancing optimally for efficiency. This correlates with the losses in the batteries, as evenly distributed currents result in lower rms currents and lower losses (as validated in section 6.1.2.2). However, even when the current is distributed *ideally* in the short term with regards to the efficiency, the current cannot always be distributed perfectly *equally* across all SMs in the long term (see fig. 4.6). If the current cannot be distributed equally, individual SMs' SoCs will drift over time, in the time frame of several minutes to hours. This is analysed in detail for the CHB and MMSPC in section 4.4. In order for this to be done, the detailed distribution of currents within a parallel group must first be analysed, which is presented in section 4.3.

4.3 Sub-Module Design

While previous sections provide a process to follow for the design of the system, including the number of SMs, this section details the design of the SM. Starting from the equivalent circuit (EC) of the SM, the design of the power electronics and the switching cell are presented. The principal aim of the SM design is to allow the system to perform as expected in the analysis of chapter 3. This means that the switching currents due to the the semiconductors do not flow through the battery.

4.3.1 Sub-Module Equivalent Circuit

In order to design the SM of the converter, it must be modelled in an EC to allow requirements to be formulated. The model of the battery and power electronics of the SM is presented here.

4.3.1.1 Battery Modelling

The electrical modelling of lithium-ion batteries generally relies on equivalent circuits with passive components whose behaviours mimic that of a real cell. Conventionally, batteries are modelled as voltage sources with a series resistance and a number of RC elements, as described in section 2.3.1. The time constants of the RC elements ranges from $<$1 s to $>$100 s, and in the most common methods the time-dependent behaviour is split into two RC elements, each affecting a

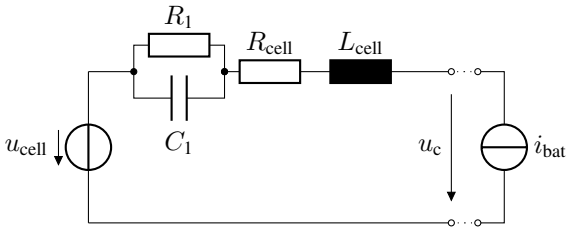


Figure 4.11: Equivalent circuit of the lithium ion cell in the Foster form

different frequency range. In the analysis of power electronic processes such as in this work, only the behaviour of the RC element with the small time constant is of interest, and as a result the battery is modelled with a single RC element here.
The RC elements are used to model the cells' behaviour in response to time-dependent current loads at frequencies well below the common switching frequencies of MOSFETs (5 kHz to 100 kHz), as these frequencies are not generally of interest for battery analysis. In order to determine the effect of the power electronics on the battery, and vice versa, these frequencies do however need to be considered. The behaviour of the cell at these frequencies is captured through a stray inductance of the cell L_{cell}, which is in series to the SM stray inductance. L_{cell} is dependent on the cell and the way in which the cells are connected together.
Figure 4.11 shows how the battery is modelled with a single RC element and a stay inductance in the common Foster form. In the presence of only a single RC element and a constant open circuit voltage u_{cell}, this circuit can be rearranged to an equivalent circuit in the Cauer form as shown in fig. 4.12, which behaves identically at the terminals. It is assumed that u_{cell} is constant in the time frames relevant to the power electronics, as it varies with the SoC of the modelled cell. As C_1 represents the double-layer capacitance of the cell [F89], the Cauer model can be used to intuitively describe how the load current can be filtered from the charge-transfer process of the lithium ion cell, which is represented by the current i_{OCV} flowing through u_{cell}.
To model the battery of a SM, which consists of a string of cells in series and/or in parallel, the same EC can be used with adjusted parameters. The resistances, inductances, and u_{cell} are multiplied by $n_{\text{b,ser}}/n_{\text{b,par}}$, while the capacitance is multiplied by $n_{\text{b,par}}/n_{\text{b,ser}}$. $n_{\text{b,ser}}$ gives the number of cells in series in a SM, while $n_{\text{b,par}}$ gives the number of cells in parallel. As a result, the time constant of the

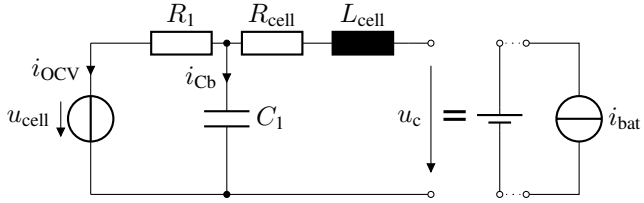


Figure 4.12: Equivalent circuit of the lithium ion cell in the Cauer form

RC element stays the same independently of how the cells are arranged in the battery.
The SM battery parameters equivalent to cell parameters R_{cell}, u_{cell}, u_{c}, L_{cell}, C_1, and R_1 are R_{b}, u_{OCV}, u_{b}, L_{b}, $C_{\text{b,RC}}$, and $R_{\text{b,RC}}$, respectively. This is also shown in fig. 6.5.

4.3.1.2 Power Electronics

The power electronics of the SM are modelled as shown in fig. 4.13, where the MOSFETs are modelled as their on-resistance R_{DS} when turned on and an open circuit when turned off. The resistance R_{Cm} models the equivalent series resistance (ESR) of the SM bypass capacitor C_{m}. The turn-on and turn-off time are both 0 s. The battery voltage source $u_{\text{b},n}$ represents the equivalent circuit of the battery corresponding to fig. 4.12.
Other parasitic elements, such as the stray inductance in the battery wiring are assumed to be negligible for the time scales of interest. The inductance of the half-bridge commutation loops—while of significant importance to the SM design—are not relevant to the considerations described here. Another inductance that is significant but not shown here is the inductance seen by the sum of the currents $i_{p,\text{H}}$ and $i_{p,\text{L}}$, which equals the phase current. This is assumed to be negligible compared to the motor inductance, through which the same current flows. For the context of this analysis, the motor inductance is so large that it behaves like a current source for the phase current.

4.3.2 Detailed Current Distribution

In the design of the MMSPC SMs, the current distribution within a parallel group is an important factor that has to be considered. In the previous analyses, it has

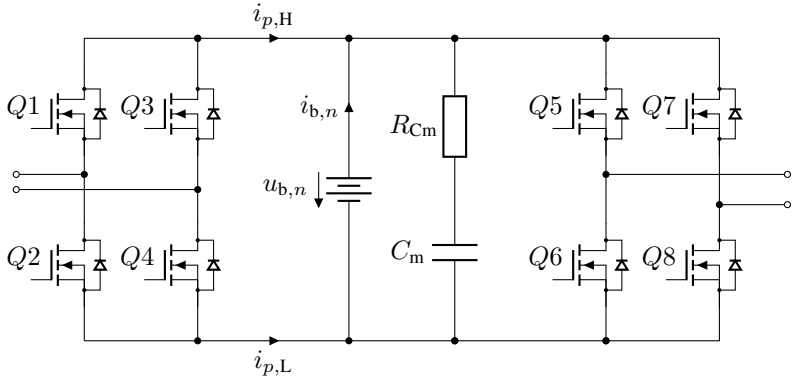
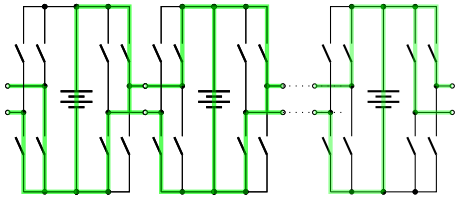


Figure 4.13: Model of the SM of the MMSPC for transient current analysis

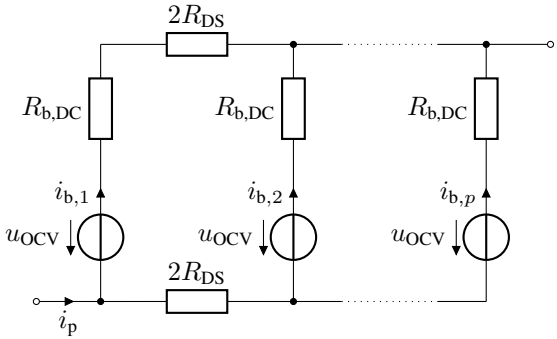
always been assumed that the current is evenly distributed in parallel groups, however this does not hold in reality.
During transient processes, the time-dependent behaviour of L_{b} and $C_{\mathrm{b,RC}}$ causes the current to be unevenly distributed, and even in steady-state processes the current is unequally distributed due to the mismatch of the MOSFET and battery resistances. Furthermore, different battery voltages of SMs before they are parallelised will result in equalisation currents between SMs until both batteries are at the same voltage. The three effects are analysed separately in the sections below.

4.3.2.1 Steady-State Current Distribution

In the ideal modelling of the MMSPC, the current shared in groups of parallel SMs is shared perfectly equally when the SM has reached steady-state. This is not the case when realistic values for the battery and MOSFET resistances are used, resulting in unequal battery current distributions that worsen as SMs are added to a parallel group.
To analyse the distribution of current in steady-state, a group of parallel-connected SMs are modelled according to fig. 4.14, where all time-dependant components are removed and $R_{\mathrm{b,DC}} = R_{\mathrm{b,RC}} + R_{\mathrm{b}}$.
When all voltage sources are equal, they can be replaced by short circuits to calculate how much current flows through each battery using the Kirchhoff voltage and current laws as well as the superposition theorem.



(a) Schematic of p SMs connected in parallel, used to derive the equivalent circuit model below.



(b) Equivalent circuit model of n_{p} SMs connected in parallel, derived from the schematic above. This model can be used to determine how the phase current is split up between the SMs.

Figure 4.14: Model of multiple parallel SMs in steady-state. The parallel group itself is connected in series positive to neighbouring groups.

In general, the current is distributed symmetrically within the parallel groups, and for a parallel group where $p = 3$, the current in the middle SM is given by:

$$i_{\mathrm{b},2} = i_{\mathrm{p}} \frac{R_{\mathrm{b,DC}}}{3R_{\mathrm{b,DC}} + 4R_{\mathrm{DS}}}, \tag{4.34}$$

while the current in the outer SMs is given by [S1]:

$$i_{\mathrm{b},1} = i_{\mathrm{b},3} = i_{\mathrm{p}} \frac{R_{\mathrm{b,DC}} + 2R_{\mathrm{DS}}}{3R_{\mathrm{b,DC}} + 4R_{\mathrm{DS}}}. \tag{4.35}$$

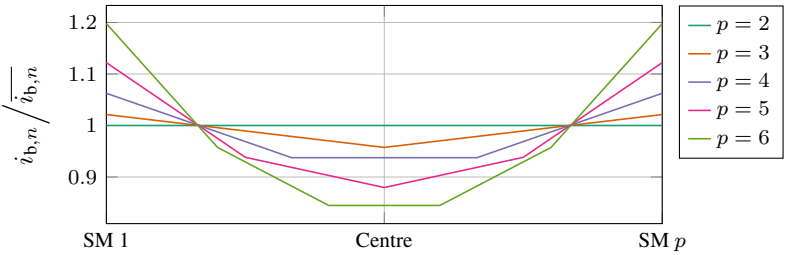


Figure 4.15: Distribution of currents within a parallel group when $R_{b,DC}/R_{DS} = 15$, for parallel groups of width two to six. The x axis denotes the position of the battery in a parallel group from 1 to p, as shown in fig. 4.14.

Equations (4.34) and (4.35) show that the current is distributed differently due to the fact that the resistance of the MOSFETs is non-zero, and the imbalance is amplified as R_{DS} increases or $R_{b,DC}$ decreases.
The imbalance increases the larger the parallel group is, as shown in fig. 4.15, which shows the current distribution through the parallel group in relation to the mean current, for the case when $R_{b,DC}/R_{DS} = 15$. This value of the ratio is close to the value used in the analysis and simulation (17.3), and is representative of the semiconductor and battery technology used in modern EVs.
It can be seen that the current can differ by a factor of greater than two for large parallel groups, even for a large ratio of battery resistance to R_{DS}. As a result, it is disadvantageous to have a large number of SMs within a phase as this necessitates large parallel groups to keep the resistance low.
The extent to which the current is unequally distributed depending on the ratio of battery resistances is shown in fig. 4.16. Here, the current of the first SM $i_{b,1}$ is shown in relation to the mean current through the parallel group. The first SM (and the last SM) is always the SM with the highest current in a parallel group. Figure 4.16 shows that even for very high ratios of battery to MOSFET resistance, a high number of parallel modes results in a very unequal distribution of currents.
In order to minimise the difference in battery currents, the number of parallel SMs should not exceed five or six, as the unevenness in the distribution directly leads to higher losses within the converter.

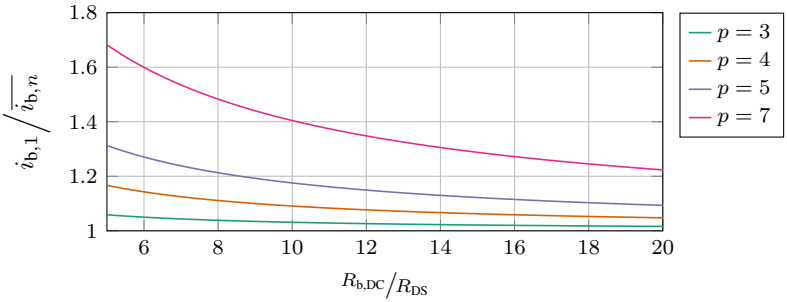


Figure 4.16: Distribution of currents within a parallel group as a function of the ratio of battery to MOSFET resistance

4.3.2.2 Transient Current Distribution

In addition to the unequal current distribution due to the non-negligible on resistance of the MOSFETs, transient processes of the converter also cause unbalanced currents. This occurs because the switching semiconductors and a changing load current alter the current through a SM's battery.
In general, there are three processes that are time-dependant that can cause a transient imbalance of the current through the batteries in addition to the steady-state imbalances discussed in section 4.3.2.1. These are listed here in order of increasing frequency:

1. Changes in the operating point ($\tau > 0.1$ s).
   For an automotive application, the operating point changes depending on the speed of the car and the inputs by the driver. These changes occur in time-scales that are generally far greater than the time constants of the power electronics and the associated passive components and are therefore not handled here.

2. Change in the output current ($\tau \sim 100$ ms to 1 ms).
   These changes occur due to the changes in the load current and occur on the time-scales of the output current frequency, which can be up to 5 kHz for automotive motors. The SM's AC current frequency is generally at twice and four times the output frequency (see eq. (3.11)).

3. Change of SM switching state ($\tau \sim 10$ µs to 1 µs).
   The switching rate of silicon MOSFETs is commonly larger than 10 kHz for

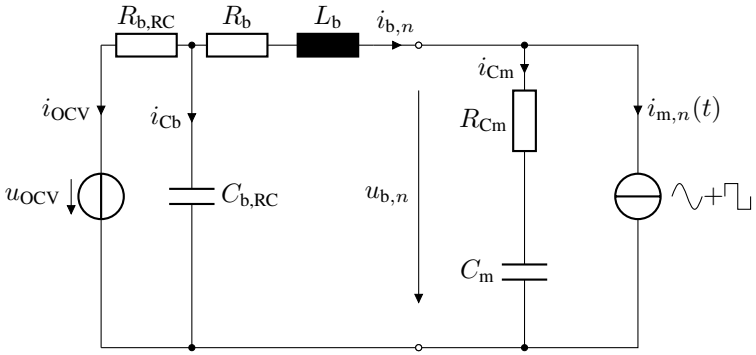


Figure 4.17: Model of the SM and battery used to analyse the effect of current perturbations on the battery current. The SM current $i_{\mathrm{m},n}$ comprises the current due to the load (sinusoidal) and the current due to the MOSFET switching (rectangular).

100 V components, which causes current ripples at the switching frequency and its odd harmonics.

In order to design the SM to account for the transient processes, a more detailed model must be used with time-dependent components. Figure 4.17 shows how the SM is modelled to consider transient processes when the SM is switched between the parallel (or bypass) and the series positive state, and $i_{\mathrm{m},n}$ is the current which is composed of the varying load current and the current ripple induced by the semiconductors i_{sw}. To model the SM's other transitions, from parallel (or bypass minus) to series negative, the direction of the current source is reversed. The transition from series minus and series positive is not discussed here as it results in a larger change in output voltage, but can be analysed in a similar fashion. Furthermore, the transition from series minus to series positive is not used in the balancing in this work.
In this model, the time-variable current through the SMs sees the three different possible paths with different impedances, and the total load current $i_{\mathrm{m},n}$ is the sum of i_{OCV}, i_{Cb}, and i_{Cm}. Each of these current paths has a different impedance and, as a result, the current is distributed between these paths depending on the load current frequency.
The most high frequency components of the SM current $i_{\mathrm{m},n}$ are low-pass filtered by the SM capacity C_{m}. The remaining current of lower frequency is divided

between i_{Cb} and i_{OCV}. Here, i_{OCV} is low-pass filtered by L_{b} and $C_{\mathrm{b,RC}}$, which act as a second-order low-pass filter with a resonance frequency of:

$$\frac{1}{2\pi\sqrt{L_{\mathrm{b}}C_{\mathrm{b,RC}}}}, \tag{4.36}$$

and a damping factor of:

$$\frac{R_{\mathrm{b,RC}}}{2}\sqrt{\frac{C_{\mathrm{b,RC}}}{L_{\mathrm{b}}}}. \tag{4.37}$$

Furthermore, the inductance L_{b} and the capacitances form a resonance circuit which can result in oscillations between $C_{\mathrm{b,RC}}$ and C_{m}. The resonance frequency should be significantly lower than the components of current $i_{\mathrm{m},n}$.
For the design of the SM, it is important to consider and tune these three circuits so that the SM current is divided ideally between the three paths. In this analysis it is assumed that the time constants of the three current loops are significantly different so that each current loop is assumed not to interact with the others, and is modelled separately.
As in all common power electronic applications with half-bridges, the current ripple of a switching half-bridge must be passed through a decoupling capacitor to avoid commutation loops with a high inductance, and here this function is provided by the capacitance C_{m}. If this capacitance is too small, this can lead to over-voltages at the semiconductors as well as EMI.
It is noteworthy that the decoupling capacitor shown in the asymmetrical SM, such as in fig. 4.13, is responsible for decoupling the current of the half-brides $[Q1 + Q2]$ and $[Q3 + Q4]$ on the SM as well as the half-bridges $[Q5 + Q6]$ and $[Q7 + Q8]$ on the previous SM. In a real design however, the decoupling capacitors of the half-bridges $[Q5 + Q6]$ and $[Q7 + Q8]$ are on the same PCB as the half-bridges to keep the inductance in the decoupling loop low.
In addition to the switching ripple current, the output load current causes a current ripple in the batteries which causes additional losses while not providing active power. However, its frequency is in general too low to be buffered with capacitors in the SM, as it is in the region of $<$10 kHz. Alternatively to discrete capacitors, the DLC $C_{\mathrm{b,RC}}$ of the lithium-ion battery can be used to filter this current from the batteries' charge transfer process (modelled by u_{OCV}) to reduce the losses in the batteries and increase their lifetime. If this can be ensured by the choice of lithium-ion cell, the voltage source representing the charge transfer process in the cell sees only very low frequency and DC current.

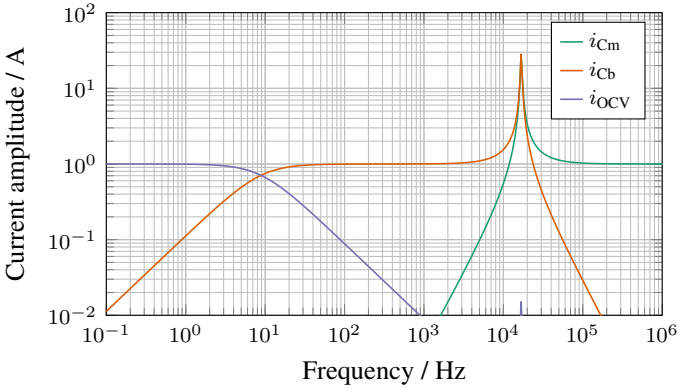


Figure 4.18: Frequency distribution of a SM's load current across the decoupling capacitor, the DLC, and the battery's charge-transfer voltage source. In this model, the battery and SM properties are the same as those used in the analysis and simulation.

Figure 4.18 shows the frequency distribution of a current $i_{\mathrm{m},n}$ with amplitude 1 A, of the three possible current paths. All frequency-domain simulations are performed in LTspice XVII. The parameters for the SM that are used for the simulation are the same as in the simulative validation in section 6.1. From the frequency response it can be seen that the SM capacitor is able to absorb the current ripple of the switching above the corner frequency of ca. 10 kHz. Below this frequency, the current flows through the battery double-layer capacitance until the frequency is lower than 10 Hz, when the current flows through the charge transfer of the battery.
Due to the low parasitic resistance of the capacitor, however, the battery inductance L_{b} forms a resonant circuit with the SM capacitance (due to its size the DLC's effect is negligible), which can cause current oscillations of high magnitude. Since this current path is also the main path for power delivery, it is not sensible to dampen the current with additional resistance, and the excitation of these oscillations should be avoided by an appropriate choice of switching frequency.
It is evident that a large DLC is important to ensure that the ripple of the output current can be buffered effectively. Care must be taken when designing the battery to ensure that the filtering effect is used throughout the operating region.

As the capacitance can change with temperature and SoC, different battery conditions will result in different distributions of SM current.
Despite the filtering effect of the DLC, there is still a significant amount of current flowing through the voltage source at low frequencies. This shows that it is difficult to completely filter the AC current from the battery's charge-transfer process.

Sub-Module Load Current Modelling In order to design the SM based on the modelled frequency response, the current load must be determined. The analysis highlights the differences between the CHB and MMSPC and describes the SM current $i_{\mathrm{m},n}$ as a function of the operating point and semiconductor characteristics. For the derivation of the current, the internal resistances are neglected as they result in negligible changes to the current shape.
Based on eq. (3.10), the SM current due to the output current $i_{\mathrm{p},i}$ (ignoring semiconductor switching) is given by:

$$i_{\mathrm{m},n} = \frac{\hat{I}m}{2}\big(\cos(\phi_c) - \cos(2\omega t - \phi_c)\big). \tag{4.38}$$

This equation is valid both for the CHB and MMSPC, assuming that the switching frequency is high enough to evenly distribute the battery currents within a phase.
The current induced by the switching semiconductors, is however different for the two topologies. For CHB, the SM current switches between the phase current $i_{\mathrm{p},1}$ and 0 A, which in the worst case scenario is a rectangular current with amplitude $\hat{I}$, at the peak of the output current sinusoid. The magnitude of i_{sw} is independent of the output voltage and its fundamental frequency is f_{ML}.
In contrast, i_{sw} for the MMSPC switches between different fractions of $i_{\mathrm{p},i}$ and its amplitude is proportional to the output voltage. The worst-case scenario for i_{sw} is when the converter is transitioning from the maximum output level N to $N-1$, and here the amplitude of this pulsed current is $i_{\mathrm{p},i}/2$. The switching frequency is the same as for the CHB.
For the design of the SM capacitor, the worst case scenario must always be taken into account, as the performance of the system must be guaranteed for all operation points. To filter the rectangular pulse signal generated by the semiconductor switching (such as PWM), the fundamental frequency must be considered as well as the harmonics.

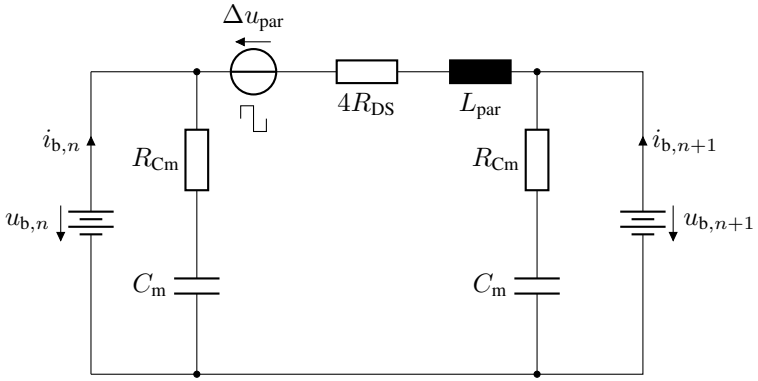


Figure 4.19: Model of two parallel SMs used to analyse the impact of balancing on the SM

Parallel Equalisation The switching of SMs from a series state to a parallel state can cause significant equalisation currents, which are analysed in this section. If a current flows through a series SM during operation, it will cause a voltage change at the terminals of the battery ($u_{\text{b},n}$), due to its inner resistance. When this SM is then switched in parallel with another SM with a different terminal voltage, an equalisation current will flow from one SM to the other until the terminal voltages are equal.
This process causes circular current through the SMs and does not deliver any power to the load; as such it is detrimental to the operation of the converter and should be minimised to increase the efficiency. It should be noted that these circular currents do not flow in state-of-the-art, non-parallelisable multilevel converters such as the CHB. To model the equalisation current, two parallel SMs are connected via a pulsed voltage source as shown in fig. 4.19.
The voltage source Δu_{par} models the step voltage change at the SM terminals as the result of the aforementioned parallelisation. The inductance L_{par} is the inductance of the SM connections that connect SMs when they are in the parallel state.
The magnitude of Δu_{par} is dependent on the load current and the resistance of the cells, and the current induced by it is superimposed onto the SMs battery current described in the previous paragraph. In the worst case, the voltage is equal to

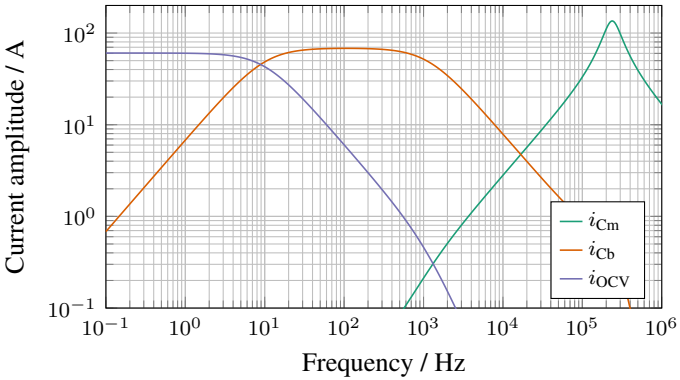


Figure 4.20: Frequency distribution of a SM's current as the result of a voltage disturbance Δu_{par}, from the parallelisation of SMs with different capacitor voltages. The battery and SM properties are the same as those used in the analysis and simulation.

the difference between a SM voltage that is seeing the whole current and a SM voltage that is seeing half the current:

$$\Delta u_{\mathrm{par}} = R_{\mathrm{b}} i_{\mathrm{p},i} - R_{\mathrm{b}} \frac{i_{\mathrm{p},i}}{2} = R_{\mathrm{b}} \frac{i_{\mathrm{p},i}}{2}. \tag{4.39}$$

This worst case arises when a SM is switched from a parallel group of two SMs to a series positive state.
Figure 4.20 shows the current frequency response to the parallelisation voltage $|\Delta u_{\mathrm{par}}| = 1\,\mathrm{V}$. Similar to fig. 4.18, the current divides between the three paths depending on its frequency. A new resonance is created between the L_{par} and C_{m}, at around 240 kHz, but this time it mainly affects the SM capacitors, which are required to sustain the switching currents, and therefore are not negatively impacted by this current from the parallelisation.
It is far more important to avoid this current entering the battery as i_{Cb}, which could generate significant losses. To achieve this, the switching frequency should be chosen to be beyond the corner frequency the low-pass filter formed by $C_{\mathrm{b,RC}}$ and $R_{\mathrm{b,RC}}$, which is around 1 kHz for the parameters chosen in this analysis, and used in the validation.
In the ideal case, the parallelisation current flows entirely through the SM capacitance to reduce the load on the battery. As the frequency of the disturbance

Δu_{par} is the same as that of the switching current i_{sw}, the SM will have the same frequency reponse to the voltage disturbance Δu_{par} and the current distribution will be analogous to fig. 4.18. The loss due to parallelisation E_{par} is given by:

$$E_{\text{par}} = \frac{C_{\text{m}}}{4} \Delta {u_{\text{par}}}^2, \tag{4.40}$$

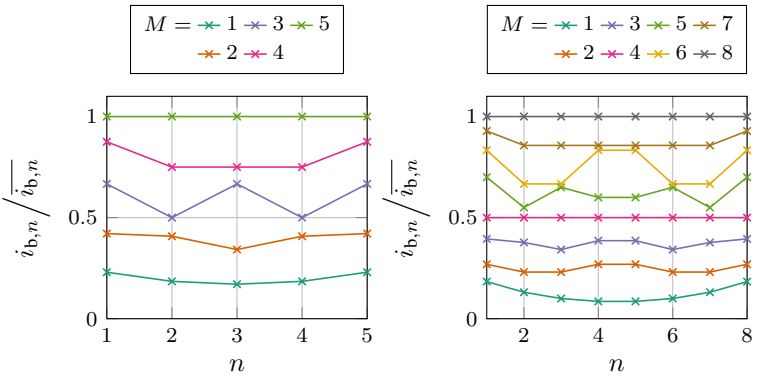
which is notably independent of the capacitor's resistance [F38]. For a converter design, it should be ensured that the loss due to parallelisation is negligible compared to the other losses.
While the parallelisation current can cause an increasing current load, it is not a viable method to balance the SoCs of adjacent SMs. From fig. 4.18, it can be seen that a significant charge-transferring current only occurs at low frequencies, below 100 Hz. This means that SMs would have to be in parallel for several milliseconds to observe a meaningful balancing effect, which is not realistic in automotive applications with switching frequencies in the kHz range.

4.4 Number of Sub-Modules: SoC-Balancing Considerations

Based on the analysis of section 4.2, this section investigates the SoC balancing of the converter's SM batteries. As discussed in section 2.1.2.3, this can be a problem in the MMSPC, where the SMs' currents cannot be individually manipulated due to the parallel interconnection of neighbouring SMs. Here, it is shown that it is impossible to balance the currents across all SMs of the converter when the parallel connection is always used when available (as in efficiency-optimal balancing).
Unlike section 4.2, this section analyses the current distribution from the perspective of ensuring that all of the SMs' SoCs are balanced. This is in contrast to the previous section, which aims to minimise the short-term fluctuations in the SMs' batteries to reduce their rms current and maximise the converter efficiency. The analysis in this section shows that these aims are at odds with each other.

4.4.1 Efficiency-Optimal Balancing

To analyse the SoC-balancing abilities of the MMSPC, an example analysis is presented using the efficiency-optimal balancing derived in section 4.2. This means that SMs are always in parallel when they are not in series, and the parallel groups are always divided as equally as possible across the phase. Furthermore,



(a) $N = 5$ (b) $N = 8$

Figure 4.21: Battery currents for each SM n relative to the phase current for all output levels. It is assumed that efficiency-optimal balancing is used and all available phase states are used equally. The results are independent of switching frequency.

the number of parallel group permutations n_σ is minimised to distribute the SM current.

Under these assumptions, fig. 4.21 shows the average current seen by a SM for all output levels M for an MMSPC with five and eight SMs. Each available phase state $\vec{S}_\mathrm{p}$ is used equally for each output level, according to eq. (4.27). Figure 4.21 shows that the distribution of the batteries' currents is not equal at most output levels.

The batteries closer to the centre of the phase, or the centre of a symmetrical group within the phase, see a lower current than the batteries far away from the centre. This occurs because the SMs in the centre are in parallel groups more often than the outside SMs. In a parallel group, the current of a battery is lower than in series, and the larger the parallel group is, the lower the current eq. (4.20). Figure 4.21 shows that for most M, it is not possible to balance the current—and therefore SoC—of all batteries when simply rotating the proposed most efficient states $\vec{S}_\mathrm{p}$.

This is in contrast to the CHB, where the current is equally distributed for every output level. For the MMSPC, only few output levels allow equal current distribution, such as $M = 4$ when $N = 8$.

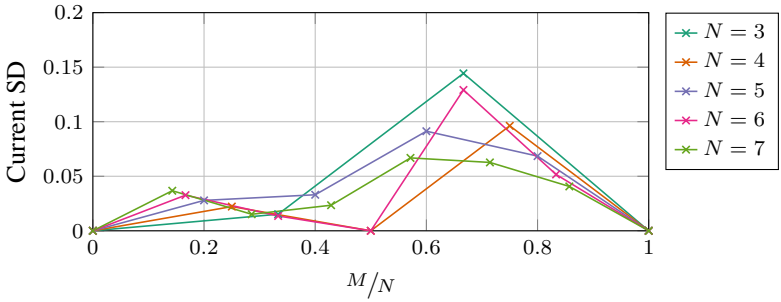


Figure 4.22: Standard deviation (SD) of current in the batteries for different output levels, when using efficiency-optimal balancing. These values are calculated directly from the current distributions shown in fig. 4.21.

Figure 4.22 summarises the information shown in fig. 4.22 for $N \in \{3,4,...,7\}$. The average standard deviation (SD) of the batteries' currents for each output level and number of SMs is shown. It can be seen that under the proposed efficiency-optimal balancing a significant imbalance of battery current occurs for all output levels and numbers of SMs.
Understanding that the MMSPC does not allow the battery currents to be balanced when being operated in the most efficient manner, the next section analyses the reason for this and proposes a systematic methodology to show when the batteries' SoCs can be balanced.

4.4.2 Improving Balancing

In this section, a novel approach to the analysis of the balancing problem of the MMSPC is introduced. Using this approach, the conditions for the possibility of SoC balancing can be derived and analysed. The analysis investigates every possible state of imbalance of a converter phase, and shows which states $\vec{S}_\mathrm{p}$ are needed to balance the batteries' SoCs.
For this analysis, the imbalance vector $\vec{B}_{N\times 1}$ is introduced, which represents the 'direction' a phase is imbalanced. We define that each battery may have one of two possible states of balance. Either it has a higher SoC than the mean of all SMs in a phase, or a lower SoC. These states correspond to values of 1 and -1 in $\vec{B}$, respectively.

For example, the states of charge z_n comprising vector $\vec{z}$ in a phase of five SMs can be:

$$\vec{z} = \begin{pmatrix} 40\% & 80\% & 70\% & 40\% & 30\% \end{pmatrix}^{\mathrm{T}}, \tag{4.41}$$

giving a mean SoC of 62%. The corresponding imbalance vector $\vec{B}$ is:

$$\vec{B}(M) = \begin{pmatrix} -1 & 1 & 1 & -1 & -1 \end{pmatrix}^{\mathrm{T}}. \tag{4.42}$$

For the case where an SoC (or a current in eq. (4.43)) corresponds to exactly the mean of the vector, it is rounded to $+1$. Using $\vec{B}$, we can now analyse whether a particular current distribution within the phase will lead to a balancing or un-balancing of the phase. Similar to $\vec{B}$, a current 'direction' vector $\vec{C}_{N\times 1}$ is defined, indicating whether the current of a battery is greater or less than the mean current.
For example, if the battery currents for a particular $\vec{S}_{\mathrm{p}}$ are:

$$\vec{i}_{\mathrm{b}} = \begin{pmatrix} 6\,\mathrm{A} & 5\,\mathrm{A} & 8\,\mathrm{A} & 5\,\mathrm{A} & 3\,\mathrm{A} \end{pmatrix}^{\mathrm{T}}, \tag{4.43}$$

where a positive current denotes discharging, giving a mean current of 5.4 A. The current direction vector is therefore:

$$\vec{C}(\vec{S}_{\mathrm{p}}) = \begin{pmatrix} 1 & -1 & 1 & -1 & -1 \end{pmatrix}^{\mathrm{T}}. \tag{4.44}$$

Assuming that a specific state is active for a short amount of time compared to the time it takes for the SoCs of the batteries to change, a $\vec{C}$ vector that is equal to $\vec{B}$ will always lead to the imbalance the phase being reduced. Henceforth, this will be considered the 'matching' of imbalance vector $\vec{B}$ and current vector $\vec{C}$. There are 2^N possible arrangements of $\vec{C}$ and $\vec{B}$, in total. $\vec{B}_q$ is used to represent each possible value that $\vec{B}$ can take, where $q \in \{1,2,...,2^N\}$.
Not all possible values of $\vec{B}_q$ can be matched with the current distributions achievable for the efficiency-optimal balancing. This is shown in fig. 4.23, which shows the fraction of vectors $\vec{B}_q$ matched by possible vectors $\vec{C}$. In this figure, the number of available $\vec{C}$ vectors is equal to the number of phase state permutations $\vec{S}_{\mathrm{p}}$. It is evident that across the output level range, the optimal balancing can never counteract more than half of the possible imbalances that can be encountered. Furthermore, the MMSPC can match far fewer imbalances than the CHB, especially for converters with more than three SMs.
While a majority of possible imbalances $\vec{B}_q$ cannot be balanced using a single $\vec{C}$, different combinations of $\vec{C}$ can be combined to increase the number of $\vec{C}$

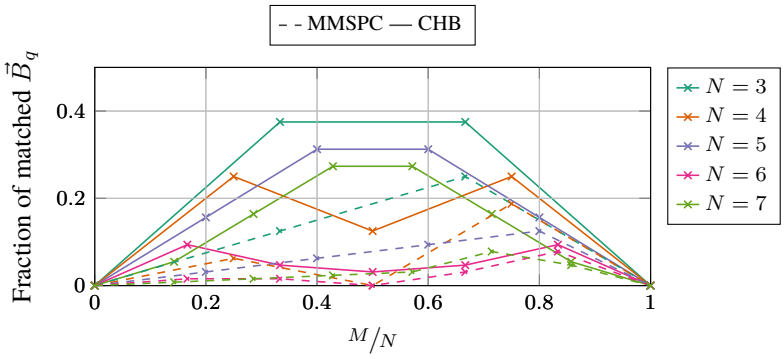


Figure 4.23: Fraction of possible values of $\vec{B}_q$ that can be matched by the current vectors $\vec{C}$ occurring in efficiency-optimal balancing. The fraction of matched $\vec{B}_q$ is shown for each output level.

vectors available. Limiting the choice of $\vec{S}_\mathrm{p}$ to those presented in section 4.2, the number of available $\vec{S}_\mathrm{p}$ to combine per output level is n_σ.
To asses the ability to balance converter imbalances using a combination of phase states $\vec{S}_\mathrm{p}$ and corresponding $\vec{C}$, an optimisation problem can be solved, which is presented here.
First, the equivalent current vector $\vec{C}_\epsilon$ (size $N \times 1$) is introduced, which is a current vector that can be achieved by combining different $\vec{C}$ vectors. It is defined as:

$$\vec{C}_\epsilon = \vec{D}\vec{\Theta}, \tag{4.45}$$

where $\vec{D}_{N \times n_\sigma}$ is a matrix of the possible values that $\vec{C}$ can take for a specific output level, according to:

$$\vec{D}(M) = \begin{pmatrix} \vec{C}_1 & \vec{C}_2 & \cdots & \vec{C}_{n_\sigma} \end{pmatrix}, \tag{4.46}$$

where $\vec{C}_k$ ($k \in \{1,2,...,n_\sigma\}$) indicates the k^{th} possible value that $\vec{C}$ can take for a specific output level. $\vec{\Theta}_{n_\sigma \times 1}$ is a vector of the relative period for which each vector $\vec{C}$ is active.
Now, by altering the values taken by $\vec{\Theta}$, different equivalent current vectors $\vec{C}_\epsilon$ can be generated in addition to the vectors $\vec{C}$ that are already available. For each

value of $\vec{B}_q$, the vector $\vec{\Theta}$ can be optimised to give the current vector $\vec{C}_\epsilon$ that optimally balances the batteries.
The optimal solution is found using the cost function:

$$J_{\mathrm{B},q} = \frac{\left(\vec{B}_q - \vec{C}_\epsilon\right)}{N}, \tag{4.47}$$

where $J_{\mathrm{B},q}$ is the balancing cost associated with the equivalent current vector $\vec{C}_\epsilon$. The optimum $\vec{C}_\epsilon{}^*$ is found according to:

$$\vec{C}_\epsilon{}^* = \arg\min\left(J_{\mathrm{B},q}\right). \tag{4.48}$$

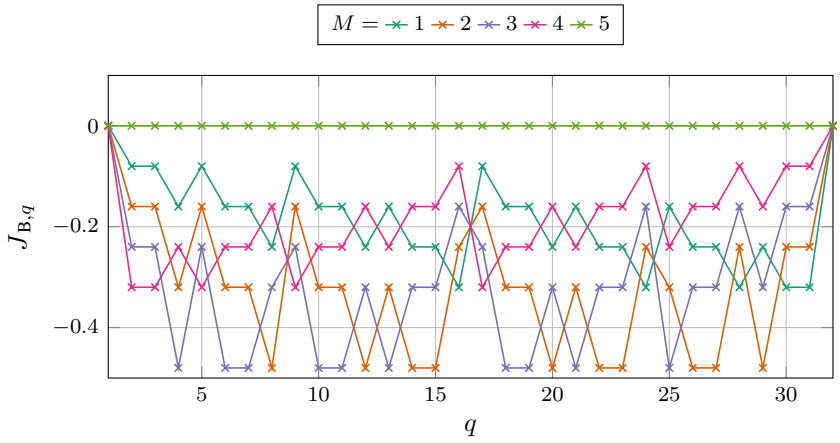
The right-hand side (rhs) of eq. (4.47) is divided by the number of SMs N to allow comparisons between converters with different numbers of SM. The optimisation is subject to the inequality constraint:

$$0_{N\times 1} \leq \vec{I}\vec{\Theta} \leq 1_{N\times 1}, \tag{4.49}$$

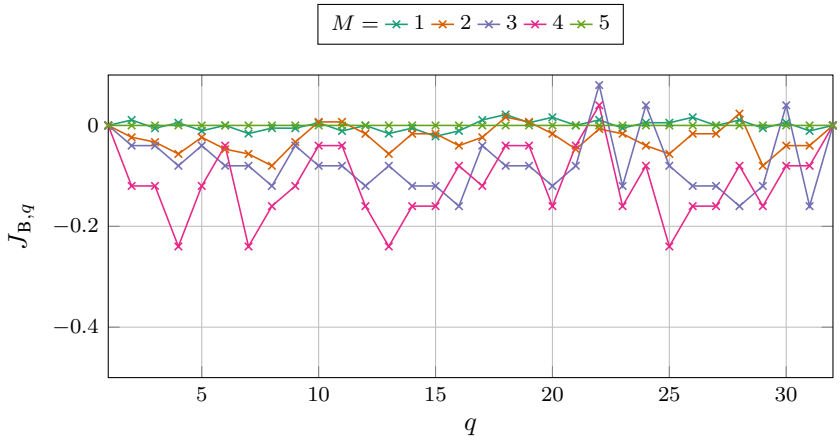
where $\vec{I}$ denotes the identity matrix. Equation (4.49) encapsulates the fact that each element of $\vec{\Theta}$ must be between zero and one (where zero indicates a state is never used, and 1 indicates it is always used). In addition to eq. (4.49), the sum of all elements of $\vec{\Theta}$ must equal one, which is ensured by the equality constraint:

$$\left\|\vec{\Theta}\right\|_1 = 1, \tag{4.50}$$

Due to the linearity of the optimisation problem, a global minimum can always be found. If the optimal value of $J_{\mathrm{B},q}$ is negative, the phase imbalance is reduced, while a positive value indicates that the phase cannot be balanced.
Figure 4.24 shows the optimal value of $J_{\mathrm{B},q}$ for each q for both the CHB and MMSPC converters with five SMs using MATLAB's *fmincon*. As expected, the CHB is able to balance the converter much better than the MMSPC as it can control the SM currents independently.
For the CHB, every imbalance vector can be balanced at every output level, while for the MMSPC there are no output levels at which every imbalance vector can be balanced. Some values of $\vec{B}_q$, such as $\vec{B}_{22}$, can only be balanced at specific output levels, in this case $M = 2$. Even though $\vec{B}_{22}$ can theoretically be balanced, the value of $J_{\mathrm{B},q}$ is very small, meaning that the converter would need to remain at this output level for a long period of time to achieve balanced SoCs.
Figure 4.25 shows the ratio of imbalance vectors that cannot be balanced when combining phase states $\vec{S}_\mathrm{p}$ to increase the number of achievable current vectors



(a) CHB



(b) MMSPC

Figure 4.24: Optimal value of cost function $J_{\mathrm{B},q}$ for each imbalance vector $\vec{B}_q$ for the CHB and MMSPC with $N = 5$.

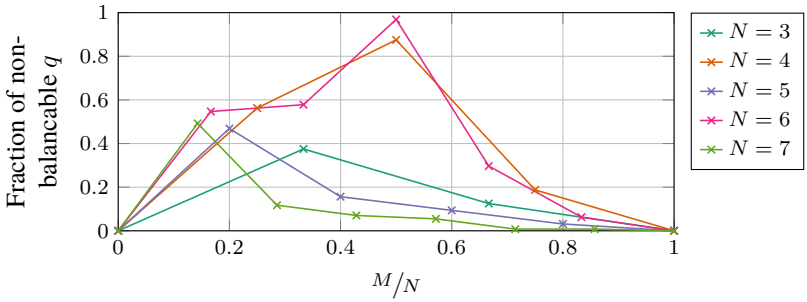


Figure 4.25: Ratio of imbalance vectors $\vec{B}_q$ that cannot be balanced in the MMSPC. Irrespective of the number of SM, there are always imbalances that cannot be balanced.

$\vec{C}$. For all investigated N, every output level has some imbalances that cannot be balanced. In total, an odd number of SMs has a significantly lower number of non-balancable states than even numbers. This is because they have fewer symmetric output states $\vec{S}_\mathrm{p}$ allowing more combinations of $\vec{C}$ to be achieved.

Discussion of SoC Balancing As shown in this section, the MMSPC cannot be balanced when the SMs are used in the efficiency-optimal methodology shown in section 4.2. In contrast, the CHB can be balanced in the efficiency-optimal strategy, although its attainable efficiency is lower than that of the MMSPC. Therefore, additional phase states $\vec{S}_\mathrm{p}$ must be allowed for the MMSPC to balance. Since an MMSPC can always operate as a CHB, albeit with reduced efficiency, balancing is always possible. Finding which values of $\vec{S}_\mathrm{p}$ allow balancing to be achieved is a non-trivial task and is discussed in this work in section 5.4.
This section provides a tool for the analysis of different converters and different balancing mechanisms. In order to achieve SM balancing, a control algorithm must evaluate the SoC imbalance and generate a resulting control action that reduces the imbalance.
It should be noted that the analysis here only proves the ability to balance for static output voltage levels and does not mean that all imbalances can be eradicated in a non-ideal converter operating under sinusoidal load. The fact that $J_{\mathrm{B},q}$ is negative is only a necessary, but not a sufficient condition for stable operation. This is because the model that is presented here is idealised and assumes that all components are identical and there are no parasitic elements. Whether the

balancing is stable depends strongly on the load cycles and asymmetries of the real-life system. Nonetheless, the analysis presented can allow an engineer to determine whether a particular balancing method can theoretically balance the converter at all, by giving an upper bound for the balancing performance.

4.5 Discussion

In this section, various aspects of the design of the MMSPC have been highlighted, with a focus on the comparison between MMSPC and CHB.
A rule-of-thumb sizing of the converter and battery components is given at first, including a consideration of the possibilities offered by the parallel mode in the construction of the neutral point. This is followed by the detailed analysis of the effect of the number of SMs in a converter phase, investigated from various perspectives.
First, the ability of the MMSPC and CHB to distribute the current is derived. In section 6.1.2.2, this is shown to be an important indicator of the battery efficiency of a converter, as an equal distribution of current leads to lower battery rms currents and therefore lower losses. Based on this analysis, the ability of the converters to balance the SoCs of their batteries is analysed, for which the time-scales are much larger than for the efficiency considerations.
It is shown that the requirements of equal current distribution for high efficiency and the ability of a converter to balance SoCs are opposite: while the CHB requires more switching states to distribute the currents evenly between its SMs, this allows it to balance the SoCs better. The opposite holds true for the MMSPC, which can only balance the SM SoCs using efficiency-nonoptimal balancing.
In practice this means that while the MMSPC has a significant efficiency benefit due to its ability to distribute the battery currents in the short term, this benefit cannot always be realised, as some SoC imbalance may occur. To operate the MMSPC stably, its efficiency may have to be reduced from its maximum theoretically achievable efficiency. Whether this is the case or not depends heavily on the type of driving cycle, as some states of the MMSPC allow better SoC balancing than others.
Second, the electronic modelling of the SM is presented to provide a means for its design. Considering the different loading cases of the SM as a result of semiconductor switching, motor current, and balancing parallelisation, a framework for the sizing of the components is given to minimise the degradation of the SM battery.

The design of the converter and SM, including the effect of the choice of SM number, is verified in simulation and experiment in chapter 6.

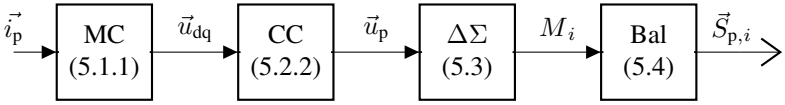
Chapter 5

Control

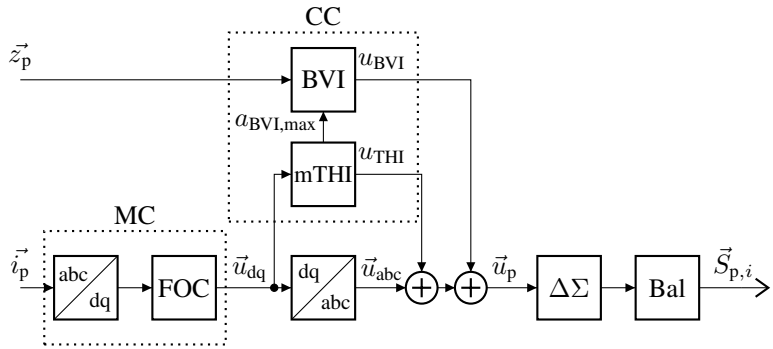
A significant challenge of the deployment of a cascaded multilevel converter such as the MMSPC is the converter control. This is a result of the numerous degrees of freedom that arise due to the many different switching states that can be achieved. In this section, a novel control strategy for the MMSPC is presented, analysed, and discussed. The verification of its effectiveness in simulation and experiments is then given in chapter 6.
The control is split into three sections: the converter control (section 5.2), the delta-sigma modulation (section 5.3) and the balancing (section 5.4). The input of the converter control is the measured current and the desired operating current while the output is the continuous converter voltage. The input of the modulation is the continuous converter voltage while the output is the discrete voltage level M of the converter in SMs. The input of the balancing is the discrete voltage level M and the output is the exact switching state of each converter SM $\vec{S}_{\mathrm{p}}$. Figure 5.1 (a) shows an overview of the converter's control scheme. Section 6.2 gives the details of the real-time implementation of the proposed control scheme on a field-programmable gate array (FPGA).

5.1 Control Targets

The control of an electric drive system with a battery-integrated MMSPC is divided in to the external control, which is the control of the MMSPC load, and the internal control, which is the control of the MMSPC. The aim of the external control is to attain the desired operating point (in the case of a permanent magnet synchronous machine (PMSM) this is the desired torque), while the aim of



(a) General overview of the MMSPC control. The motor control (MC) uses the phase currents $\vec{i}_\mathrm{p}$ to control the dq-voltage $\vec{u}_\mathrm{dq}$. This is the input to the presented converter control (CC), which implements a common-mode voltage and returns the phase voltages $\vec{u}_\mathrm{p}$. These voltages are the modulated by the DSM ($\Delta\Sigma$) to determine the output levels M of each phase. The output level serves as the input to the balancing algorithm (Bal), which determines the phase switching states $\vec{S}_\mathrm{p}$ and sends these to the SMs.



(b) Detailed overview of the proposed MMSPC control. The dq-voltages of the field-oriented control (FOC) are used for the modified THI (modified third harmonic injection (mTHI)), which reduces the batteries rms current. In addition, the balancing voltage injection (BVI) injects an additional common-mode voltage to balance the phase SoCs $\vec{z}_\mathrm{p}$.

Figure 5.1: Overview of the proposed control structure of the MMSPC. The novel presented control scheme comprises BVI and mTHI, which are detailed in this section.

the internal control is to balance the SoCs of the batteries and to incur minimal losses. This work focusses on the internal control of the MMSPC, as there is abundant research available on the control of three-phase loads such as electrical motors controlled with voltage source converters (VSC).

5.1.1 External

The aim of the load control is to ensure that the target operating point is reached and that the load can be operated safely, and in the required dynamics. To ensure this, the controller should be stable and non-oscillatory over the entire operating range. For this work, the external control is only briefly discussed (section 5.2.1) as it is not the focus. Control of the load is only used to generate a representative operating point to investigate the application and validity of the proposed control scheme, which is an internal converter control.

5.1.2 Internal

In contrast to conventional battery-powered converters, there are several relevant control objectives for the MMSPC. Primarily, the SoCs of the batteries should always be within a narrow band to ensure the maximum availability of the converter system. This is important since once a single cell has reached its minimum SoC the system must shut down to avoid damage, and cannot function any more. Ideally, all cells would reach the minimum SoC at the same time. At the same time, the losses should be uniformly distributed over all SMs to minimise the required cooling power. This is achieved by ensuring that all batteries as well as all semiconductors have the same rms current.
Furthermore, the efficiency of the converter should be maximised. As shown in chapter 3, the efficiency can be significantly influenced by the batteries' current loading, and a purely DC-load on the battery ensures the minimum possible battery losses. The internal converter control must also not impact or be influenced by the external control, which ensures the load is maintained in the desired operating point.

5.2 Converter Control

This section details the control of the MMSPC with a PMSM load, which is representative of the use-case in an EV. As the behaviour of the MMSPC is similar to other VSCs for the load, the motor control of conventional two-level converters is

used. The motor control's output is a dq-frame space vector voltage $\vec{u}_{\mathrm{dq}}$ without zero-sequence voltage which then serves as the input to the internal converter control. The internal converter control implements a CMV injection, composed of a third harmonic voltage injection, henceforth called mTHI, and a voltage injection at the fundamental frequency, called BVI, which together optimise the operating point of the converter without affecting the current in the load.
Thus the internal converter adds two voltage components to the motor control output voltage, according to:

$$\vec{u}_{\mathrm{p}} = \vec{u}_{\mathrm{abc}} + u_{\mathrm{THI}} + u_{\mathrm{BVI}}, \tag{5.1}$$

where u_{THI} is the mTHI voltage, u_{BVI} is the BVI voltage, and $\vec{u}_{\mathrm{abc}}$ is the motor control output voltage in abc-coordinates. These two components comprise the CMV of the converter u_{cmv}, which is defined as:

$$u_{\mathrm{cmv}} = \frac{1}{3}(u_{\mathrm{p},1} + u_{\mathrm{p},2} + u_{\mathrm{p},3}). \tag{5.2}$$

Figure 5.1 (b) gives an overview of the different components of the proposed control scheme, and how they fit into the overall converter control.

5.2.1 Motor Control

To ensure that the reference currents generate the demanded torque in the electric load, FOC is used, as described in section 2.2. The origin of the reference currents can be generated by control strategies such as the maximum torque per ampere (MTPA) algorithm or a d-current controller.
The FOC uses two independent PI-controllers for the d and q current control, which are controlled using the independent d and q voltage. Since the dynamic performance of the motor control is not significantly affected by the type of converter used and not a significant interest in this work, the controller is tuned to favour stability and not dynamics. The layout and tuning of the motor controller itself is not a focus of this work, as it is state-of-the-art [F52]. The controller is only used to control the load's currents to be sinusoidally steady-state.

5.2.2 Internal Converter Control

This work proposes an internal control of the MMSPC that uses a modified third harmonic voltage injection to reduce the battery losses as well as an additional

zero-voltage injection BVI to balance the SoCs of the converter phases. Conventionally, converters use third harmonic injection to increase the fundamental to peak output voltage ratio of the converter. Conventional third harmonic injection is denoted as THI, to distinguish it from the proposed modified third harmonic injection mTHI. These methods use the degree of freedom in the converters voltages that remains in three-phase systems when the other two voltages are used to control the motor currents in wye-connected motors. The balancing of the SM batteries within a phase is discussed in section 5.4, which uses the numerous degrees of freedom in the choice on how the semiconductors of the SMs can be switched to achieve the desired output voltage level.

5.2.2.1 Modified Third Harmonic Injection

In the MMSPC, a third harmonic voltage can be injected to reduce the rms battery current seen by the SM's batteries, as shown in section 3.2.2.1. This property of the MMSPC is investigated in this section and used to minimise the battery currents and therefore minimise the battery losses. This control scheme has been introduced in a previous publication of the author [E1], and in this work a more rigorous derivation and a more detailed analysis and discussion are presented.
As shown in eq. (3.12), the rms battery current $\breve{i}_{\mathrm{b},n}$ is proportional to $\sqrt{\cos(2\phi_c)+2}$ when all voltages and currents are sinusoidal (where ϕ_c is the phase angle of the current). It can also be seen from eq. (3.31) that the rms current is reduced when THI is used to increase the achievable phase-to-phase output voltage.
Starting from this observation, the ideal voltage injection to reduce the batteries' rms currents is derived here. The converter output voltage with a generalised injection at the third harmonic of the output frequency is defined as:

$$u_{\mathrm{p},i} = \hat{U}\left(\sin(\omega t) + a_3 \sin(3\,\omega t - \phi_3)\right), \tag{5.3}$$

where a_3 is the amplitude of the injection relative to the fundamental, and ϕ_3 is its phase shift. Using eq. (3.9) and assuming a sinusoidal current load according to eq. (3.5), the battery current is:

$$i_{\mathrm{b},n} = \frac{\hat{I}m}{2}\Big(\cos(\phi_c) - \cos(2\,\omega t - \phi_c) + a_3\,\cos(2\,\omega t + \phi_c - \phi_3) - a_3\,\cos(4\,\omega t - \phi_c - \phi_3)\Big). \tag{5.4}$$

Equation (5.4) shows that the battery current is composed of four different contributions at three different frequencies (including frequency zero). The zero-frequency term is proportional to the power factor and determines the active power that is drawn from the batteries.
There are two currents at twice the fundamental frequency. The current «$\cos(2\,\omega t - \phi_c)$» is independent of the mTHI while the current «$a_3 \cos(2\,\omega t + \phi_c - \phi_3)$» depends on the amplitude and phase of the injected voltage. It can be seen that if $\phi_3 = 2\phi_c$, the two currents are in phase and the third harmonic injection can be used to reduce or eliminate the current at this frequency.
At the same time, this results in a current at four times the fundamental frequency, given by the final term «$a_3 \cos(4\,\omega t - \phi_c - \phi_3)$». When $\phi_3 = 2\phi_c$, the reduction in the second harmonic current is counteracted by an equal increase in the fourth harmonic.
This can be exploited to reduce the rms battery currents as the rms of a value x is proportional to the root of the sum of the magnitude at each frequency squared, where ${}^k x$ is the kth term in the Fourier Series of x:

$$\breve{x} = \sqrt{\frac{{}^0x^2}{4} + \sum_{k=1}^{\infty} \frac{\left|{}^k x\right|^2}{2}}. \tag{5.5}$$

Therefore, if the sum of the amplitudes of the harmonics of x are constant, according to:

$$\left(\sum_{k=1}^{\infty} \left|{}^k x\right| = \text{const.}\right), \tag{5.6}$$

distributing the amplitude of x over all frequencies will reduce the rms value of x. The minimum rms of the battery current $i_{\mathrm{b},n}$ according to eq. (5.4) is therefore achieved when the currents at the second and fourth harmonic are of equal amplitude.
This minimum can be found by calculating the rms current of the battery directly, analogous to eq. (3.12):

$$\breve{i}_{\mathrm{b},n} = \frac{\sqrt{2}\,\hat{I}m}{4} \sqrt{2\Big({a_3}^2 - a_3 \cos\left(2\,\phi_c - \phi_3\right)\Big) + \cos\left(2\,\phi_c\right) + 2}. \tag{5.7}$$

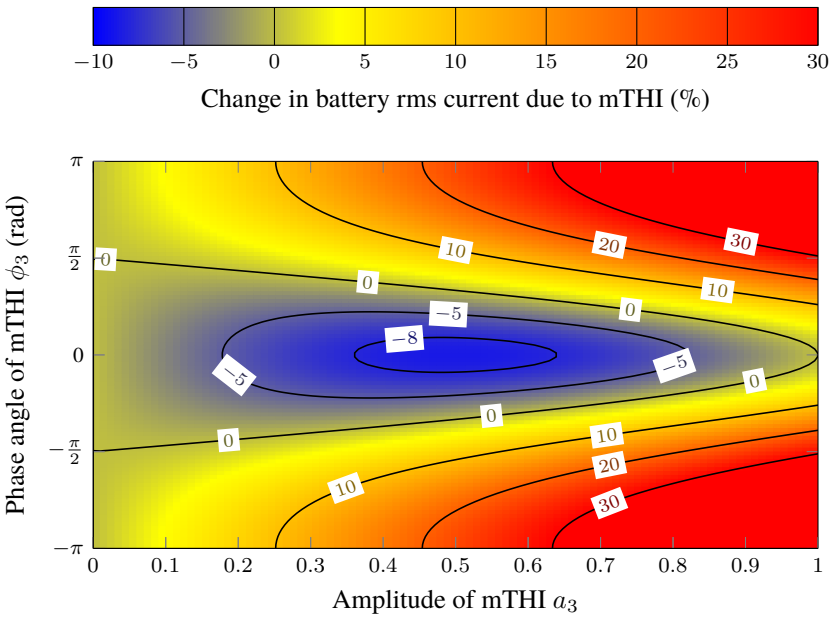
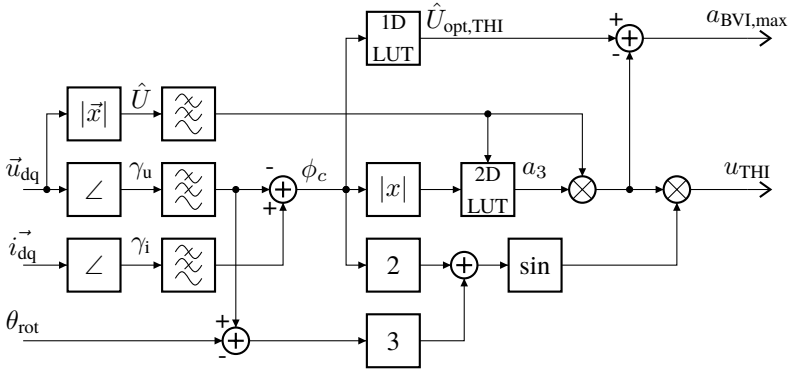


Figure 5.2: Reduction of rms battery current with mTHI, for different values of a_3 and ϕ_3 when $\phi_c = 0$

The minimum of eq. (5.7) occurs under the following conditions:

$$a_3 = 0.5 \text{ and } \phi_3 = 2\phi_c, \tag{5.8}$$

which are notably independent of the output voltage u_p and only depend on the phase of the output current. This is the minimum in the domain $a_3 \in [0, 1] \ \vee \ \phi_3 \in [-\pi, \pi]$, which can also be seen in fig. 5.2, which plots the rms current as a function of a_3 and ϕ_3 when $\phi_c = 0$.
Figure 5.3 shows the block diagram of the implementation of the mTHI algorithm to generate the injected third harmonic voltage u_THI. The second output of the control scheme in the block diagram, $a_\text{BVI,max}$, gives the maximum amplitude of the BVI voltage, which decreases as the amplitude of mTHI increases. As shown in fig. 5.3, the measured current and controller voltage in dq coordinates are used to estimate the current and voltage of the converter. A 2D lookup table (LUT)



where:

1D LUT = LUT of maximum $\hat{U}$ for which $a_3 = 1/2$; function of ϕ_c

2D LUT = LUT of optimal a_3; function of $\hat{U}$ and $|\phi_c|$

Figure 5.3: Block diagram of mTHI control to reduce the batteries' rms current

uses the voltage magnitude and current phase angle to determine the optimal relative magnitude of the mTHI, a_3. Figure 5.8 shows the values stored in the LUT. The absolute value of the phase angle can be used, as the optimum value is symmetric around $\phi_c = 0$. The optimal value of a_3 is then multiplied by a sinusoid of three times the output frequency, derived from the electric rotor angle θ_{rot}.

Figure 5.4 shows the current and voltage waveforms of the phase and the batteries with and without the proposed mTHI according to eq. (5.8). In this exemplary operating point, $m = 0.7, \hat{I} = 1$ p.u. and $\phi_c = \pi/4$.

Observation shows that the battery current with the injected mTHI has an additional frequency component compared to the case without injection, which reduces the battery rms current. Furthermore, the maximum value of the phase voltage u_{p} is significantly increased by the injection, showing that this method is not available at the limits of the modulation index and requires separate handling, which is discussed in section 5.2.2.1.

Analysis of the terms of the Fourier series shows how the reduction in battery current works by spreading the current across different harmonics. Figure 5.5

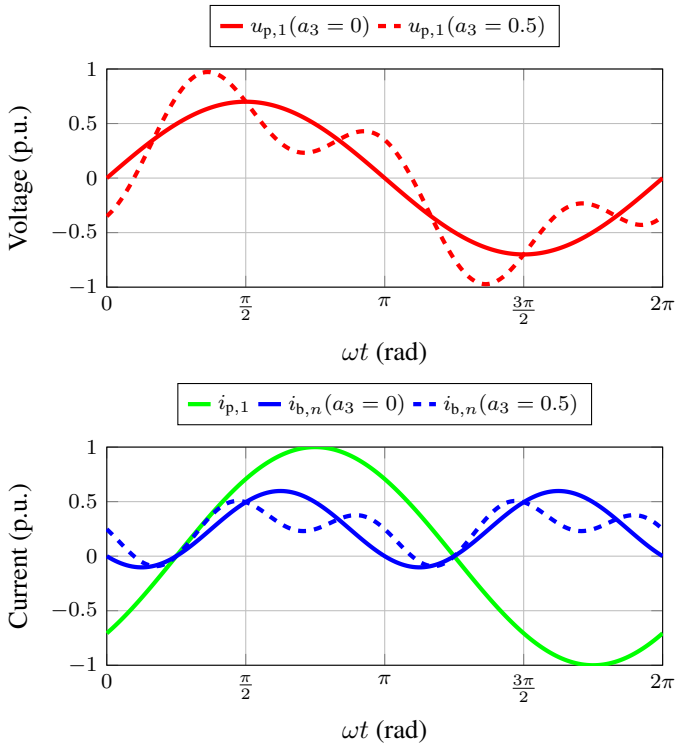


Figure 5.4: Current and voltage waveforms under optimal mTHI to reduce the battery rms current. At this operating point $\phi_c = \pi/4$.

shows the first two harmonics of the battery current with and without the optimal injection for all power factors, according to eq. (5.4). The 0^{th} term of the Fourier series is divided by two according to the general definition of the Fourier series, and is the same for both cases.
It is noteworthy that all harmonics are constant regardless of the power factor and that the amplitude of the first harmonic without injection is split exactly in two when the injection is added. The reduction in rms due to the control scheme is shown in fig. 5.6, showing a minimum rms reduction of 8.7% at $\phi_c = \{0, \pi\}$ and 29.3% at $\phi_c = \pm\pi/2$.

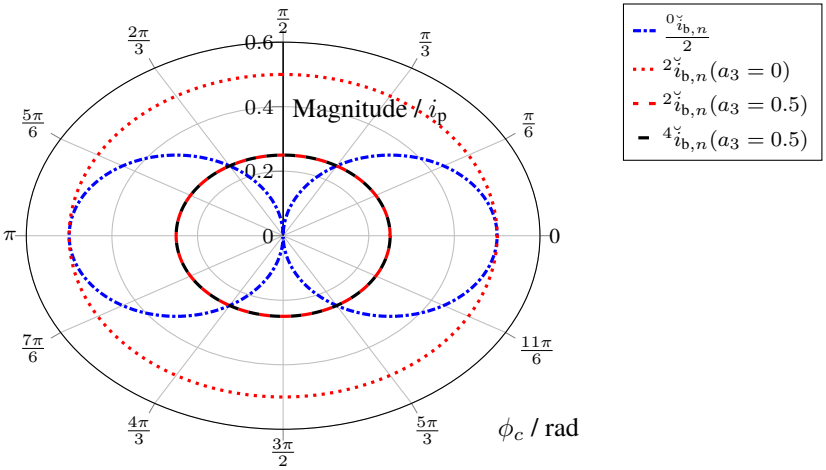


Figure 5.5: Battery current harmonics with and without mTHI over the load phase angle. The magnitude of the harmonics is given relative to the magnitude of the phase current fundamental magnitude.

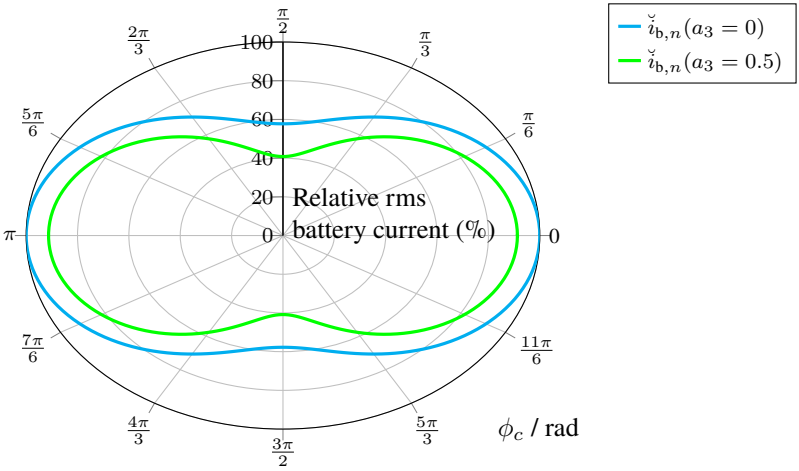


Figure 5.6: Relative rms battery current with and without mTHI over the load phase angle

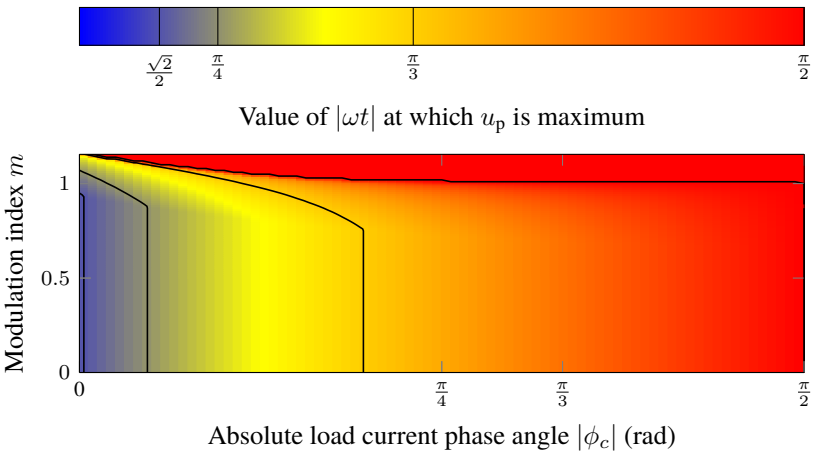


Figure 5.7: Maximum point of $u_{\mathrm{p},1}$ with optimal injection

Voltage Limiting While conventional THI with the amplitude of $1/6\,\hat{U}$ maximises the ratio of the fundamental to peak output voltage, the proposed injection decreases the fundamental to peak output voltage in all cases when $a_3 = 0.5$. As a result, the injection must be reduced when the peak of the output voltage waveform exceeds $U_{\mathrm{DC,max}}$.

To determine the reduction of the injected voltage, the ratio of the maximum to peak voltage output voltage must be known for all values of ϕ_c and m. To find this ratio, the location of the maximum is determined for all combinations of ϕ_c and m that yield solutions where the modulation index does not exceed its maximum ($2/\sqrt{3}$). This is a strongly nonlinear function of ϕ_c and m, but can be easily calculated by a brute-force search.

Figure 5.7 shows at which point the converter phase voltage is maximum in the period depending on the current phase angle and the amplitude of the fundamental output voltage. The location of the maximum output voltage can be seen to vary strongly and nonlinearly with the current phase angle and modulation index. In the top right-hand side of the graph the maximum is at $\pi/2$ and therefore at the peak of the fundamental. In these operating points, it is not possible to inject a third harmonic voltage where $\phi_3 = 2\phi_c$ to reduce the batteries rms current.

This is shown in fig. 5.8, which shows the maximum permissible amplitude of a_3 over the entire operating area without exceeding $U_{\mathrm{DC,max}}$. It can be seen from

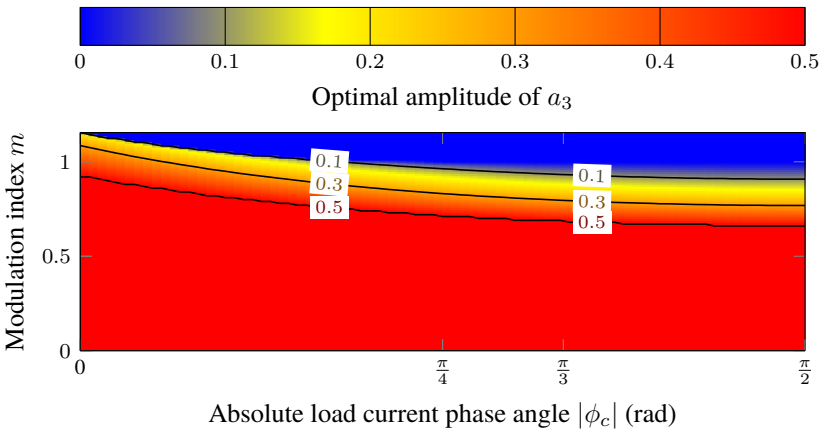


Figure 5.8: Optimal amplitude of a_3 to minimise the SMs' rms current

eqs. (5.4) and (5.7) that any positive value of a_3 will decrease the battery rms current. The benefits are greatest at low phase angles and output voltages, while no rms reduction can be achieved when the output voltage is close to the maximum. Figure 5.8 shows the maximum value of a_3 for all values of m that can be achieved without distortion of the fundamental ($2/\sqrt{3}$). In the scope of this work, no higher modulation indices are considered, such as those that can be achieved with flat-top modulation or six step modulation.
In order to allow the MMSPC control to inject the optimal voltage, the information shown in fig. 5.8 is stored in a a 2D LUT, as shown in fig. 5.1. Figure 5.9 shows the summary of the amount by which the rms battery current can be reduced in the MMSPC, according to the ideal analysis. While the rms current can be reduced substantially at lower voltages, especially when the current phase angle is high, the reduction reduces as the modulation index approaches its maximum.

Higher Order Harmonics Conventional converters commonly use THI together with multiples of the 3rd harmonic in order to simplify the implementation of the injection, such as in SVM [F97]. While these harmonics do not affect the ratio of the maximum to peak output voltage, they also do not affect the three-phase current, similar to the 3rd harmonic.

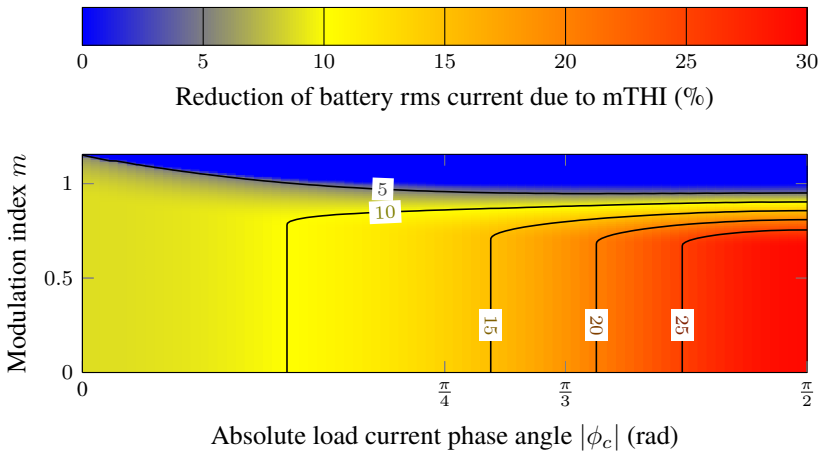


Figure 5.9: Reduction in rms battery current due to mTHI over the operating area of the MMSPC. The rms current reduction at reactive loads is substantially larger than at active loads, and the reduction approaches zero as the modulation index approaches 1. This is due to the fact that the amplitude of the mTHI has to be reduced to allow the desired fundamental output voltage to be achieved.

In the case of the MMSPC however, higher order harmonics increase the battery rms currents and therefore do not provide an additional benefit. This becomes evident when calculating the battery current when the output voltage includes higher-order harmonics (6^{th}, 9^{th}, 12^{th}, 15^{th}, etc.):

$$i_{\mathrm{b},n} = \frac{\hat{I}m}{2}\Big(\cos(\phi_c) - \cos(2\,\omega t - \phi_c) + a_3\,\cos(2\,\omega t + \phi_c - \phi_3) \\ - a_3\,\cos(4\,\omega t - \phi_c - \phi_3) - \sum_{n\in T} a_n\,\cos\big((n-1)\,\omega t + \phi_c + \phi_n\big)\Big). \quad (5.9)$$

where a_n is the amplitude of the n^{th} harmonic, ϕ_n is its phase, and T is the set of the higher multiples of the third harmonic, defined as: $T = \{6,9,12,...\}$. The rms of eq. (5.9) is:

$$\breve{i}_{\mathrm{b},n} = \frac{\sqrt{2}\,\hat{I}m}{4}\sqrt{2a_3\left(a_3 - \cos\left(2\phi_c - \phi_3\right)\right) + \cos\left(2\phi_c\right) + 2\sum_{n\in T} {a_n}^2 + 2}, \tag{5.10}$$

and therefore any non-zero values of a_n will increase the batteries' rms current. This also shows that for the MMSPC and CHB with integrated batteries, SVM will increase the batteries' currents compared to THI. The effect is small however, as the magnitude of the harmonics decreases with increasing frequency.

5.2.2.2 Balancing Voltage Injection

In addition to the voltage injection presented in section 5.2.2.1 that reduces the rms current seen by the battery, the CMV is also used to balance the SoCs of the phases $z_{\mathrm{p},i}$. This is a state-of-art-technique that can reduce the power of individual phases in order to balance the energy stored in each phase, which is proportional to the mean of all battery SoCs in that phase [F23].
In theory, the converter and the load will be balanced in the three phase system and therefore imbalances in phase SoCs only occur due to fabrication tolerances in the batteries, power electronics or load. These fabrication tolerances are controlled accurately in modern automotive production processes and as a result the imbalances are small. This fact, in conjunction with the fact that the time constant of the SoCs decreasing from 100% to 0% is given in hours, mean that the time constant of this control is large and dynamic response is not critical.
Increasing the CMV generally reduces the voltage amplitude of a phase while increasing the voltage amplitude of the other phases (or vice versa). Since the current amplitudes in all phases are the same, the power of a phase whose voltage amplitude has been increased increases, and its phase SoC changes more quickly than the others. This effect is used to balance the SoCs of all phases.
The control system is modelled as an ideal current integrator with the integration time constant of $1/C_{\text{cell}}$. As a result the SoC can be controlled using a simple proportional controller, and given the large time constants of the SoC compared to the converter control, all delays and dead-times can be ignored. This gives a closed-loop transfer function of a PT1 element and allows the phase SoC to be controlled simply and little steady-state error.

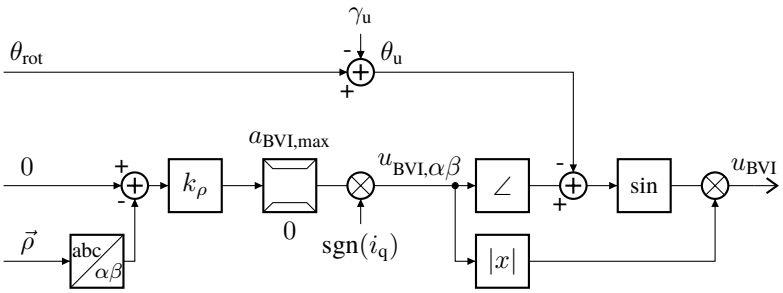


Figure 5.10: Block diagram of BVI control used to balance the converter phases

The three phase SoCs, denoted by $z_{p,i}$ are independent of each other and create a three Degree of Freedom (DoF) system. The deviation of each $z_{p,i}$ from the mean value of $\vec{z_p}$ is denoted as $\vec{\rho}$, and calculated according to:

$$\vec{\rho} = \vec{z_p} - \overline{\vec{z_p}}. \tag{5.11}$$

$\vec{\rho}$ can be expressed as a space vector in $\alpha\beta$ components, where the amplitude is proportional to the magnitude of the total SoC deviation and the angle describes the direction of the deviation. The space vector $\vec{\rho}$ has no zero-component and therefore only two degrees of freedom; the subtraction of the mean in eq. (5.11) eliminates any mean component.
Figure 5.10 shows the block diagram of the BVI algorithm. Since the goal of the BVI is to have no difference in phase SoCs, the setpoint is 0. Multiplying the controller error by k_ρ gives the voltage vector that is added to the output voltage to achieve balance in the phase SoCs.
This vector is first limited by the available voltage after mTHI has been applied, $a_{BVI,max}$, and then multiplied by the sign of the q current. The sign of the q current is the simplest indicator of whether the batteries are currently charging or discharging. Since the control achieves balance by reducing the power of the phase with the lowest SoC when the batteries are charging, and vice versa, the direction of power flow is required to ensure the correct polarity of the injected voltage.
Subsequently, the injected voltage in the $\alpha\beta$-frame $u_{BVI,\alpha\beta}$ is synchronised to the output voltage angle of the converter, θ_u. It should be noted that the $\alpha\beta$-

frame of $\vec{\rho}$ has no relation to the $\alpha\beta$-frame of the motor control. The angle and magnitude of $u_{\text{BVI},\alpha\beta}$ are extracted, and used to calculate u_{BVI} according to:

$$u_{\text{BVI}} = \left| u_{\text{BVI},\alpha\beta} \right| \sin\Big(\angle u_{\text{BVI},\alpha\beta} - \theta_{\text{u}} \Big), \tag{5.12}$$

which is added to the phase voltage of all phases (as seen in eq. (5.1)).

Voltage Limiting Similar to the third-harmonic injection described in section 5.2.2.1, the zero voltage injection also increases the required voltage at the converter phases and is thus limited in magnitude. As the imbalance of SoC in an automotive application is in general small and changes in time constants far greater than the time constants of the output voltage, the BVI has a lower priority than the mTHI.
The BVI is limited to the maximum available CMV after the mTHI has been applied. As only proportional control is used, no anti wind-up is necessary. An example of the use of BVI can be seen in fig. 6.29.

5.3 Modulation

Subsequently to the controller, a modulator discretises the demanded output voltage to an integer number of the output levels available to the converter. Power electronic converters commonly use PWM, for example with phase or level-shifted carriers for multilevel converters, as discussed in section 2.2.2. In this work, first-order delta-sigma modulation (DSM) is used in place of conventional PWM and the advantages and disadvantages of doing so are presented here. The main benefit of DSM is shown to be the fact that the minimum time between switching events is increased compared to PWM, enabling the implementation of computationally expensive balancing algorithms for each transition in switching state.
Due to the difficulty of balancing the SoCs of the SM batteries in the MMSPC, complex calculations are performed at every control step before each switching event to calculate the optimum switching state for the next control step. These calculations are significantly more complex than comparable calculations in CHB converters, since the addition of the parallel state adds another possibility for each SM. Furthermore, the switching state of a SM may also affect other SMs adjacent to it, if its neighbours or itself are in the parallel state. This complexity requires the calculation of the switching states to be performed centrally on the main control unit. In this work, the calculation of the optimal switching state

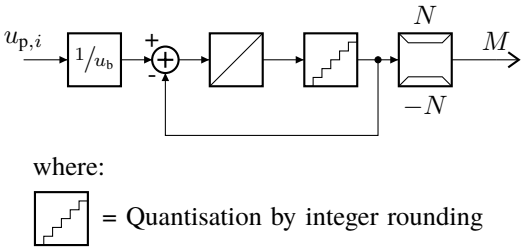


Figure 5.11: Block diagram of the multilevel DSM algorithm for a single phase

for the next control step requires more computation time than all other control calculations combined, and is described in section 5.4.
The DSM allows the switching state control to have fixed intervals for its computation time, as the switching actions are always spaced in integer multiples of the modulation time. The switching frequency, however, is not constant and can vary depending on the modulation index.
In contrast, the switching frequency of PWM is constant, but the time between two switching actions can be arbitrarily short (limited only by the minimum possible duty cycle achievable with the semiconductors and gate-drive circuitry). Since the time between two switching actions can be extremely short, it is impossible to always calculate the next switching state between each switching state. Alternatively, the minimum duty cycle could be increased to such a value that would allow calculation of the balancing algorithm, however this would greatly deteriorate the temporal resolution at low duty cycles.
This results in a significant advantage of using DSM instead of PWM for converters such as the MMSPC, if the optimal converter state is calculated at every modulation step. If the modulation and balancing algorithm is simple and not computationally intensive, such as SVM for 2L converters, or even the simple balance-by-sorting algorithms used in MMCs, the advantage is often negligible. In contrast, the computational complexity of the balancing algorithm used in the experimental verification means that it would not be possible to operate the converter at representative frequencies by using PWM instead of DSM.
Figure 5.11 shows the block diagram of the multilevel DSM used in this work. After the scaling of the controller voltage by the SM voltage, the result is integrated and quantised before it is limited to the number of SMs in the converter (both in positive and negative). The output of the quantisation is subtracted from

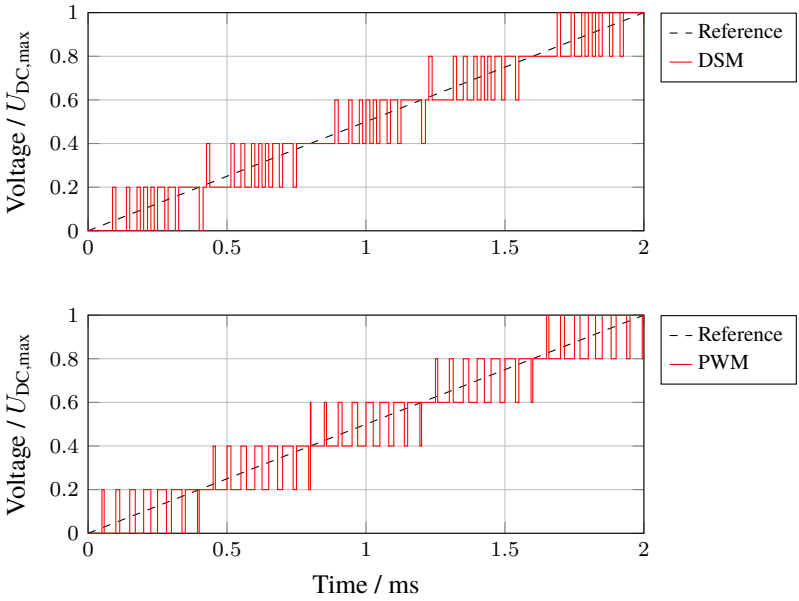


Figure 5.12: Comparison of DSM and phase-shifted PWM waveforms. The frequency of the DSM is 80 kHz, resulting in an average switching frequency of 21 kHz. The PWM switching frequency is 20 kHz.

the input voltage, eliminating the error of the output voltage with closed-loop feedback.
Figure 5.12 compares the output waveform of both phase-shifted PWM and DSM, with switching rates of circa 20 kHz. It can be seen that the switching transitions occur more regularly for PWM than for DSM, and the DSM switching actions are concentrated around the periods when the reference signal is exactly between two output levels.
In the following, the significant differences of the modulation techniques are discussed.

Switching Frequency One of the disadvantages of DSM is that the switching frequency is not constant and varies significantly with the modulation index. This can cause the switching losses of the semiconductors and the effect on the load to be difficult to predict. While this can be a disadvantage in very precisely

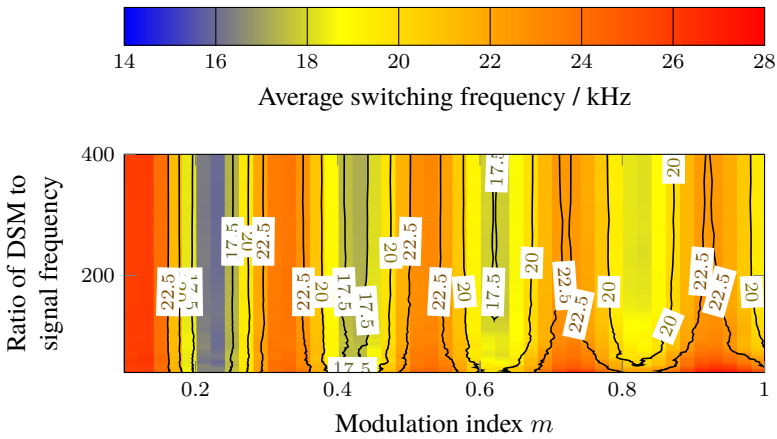


Figure 5.13: Switching frequency of a five-level DSM over a range of modulation indices and signal to modulation frequency ratios. For this analysis, the frequency of the DSM is 80 kHz, and the input signal is a pure sinusoid of varying frequency and amplitude.

controlled DC systems, the relatively high output frequency of the load ensures that switching events are regular and therefore the switching frequency does not vary strongly. Moreover, in multilevel systems such as the MMSPC, the switching losses are very low in comparison to the conduction losses.

For sinusoidal signals, the switching frequency of DSM is on average approximately ¼ of the modulation frequency, as shown in fig. 5.13, which shows the average output switching frequency of DSM over a wide range of fundamental to modulation frequency ratios, and output modulation indices. When used for converter control, the input to the modulator contains many different frequencies and varies over time, resulting in an overall switching frequency that is almost constant over the operating range of the converter.

Because the switching frequency of the DSM is significantly lower than the modulation frequency, the modulation must run significantly faster than the desired switching frequency. While this constrains the calculation time of the balancing algorithm, the shortest time to the next switching instance is always known and far greater than when using PWM.

Noise As a result of the variable switching frequency of DSM, the spectrum of the quantisation noise generated is significantly different to that generated by PWM. While the spectrum of PWM concentrates the distortion at the switching frequency and its harmonics, DSM results in a relatively flat noise spectrum up to the modulation frequency. The switching energy, and therefore the EMI, is not concentrated around specific frequencies but evenly spread across the spectrum, which can be beneficial for the electromagnetic compatibility (EMC).
With DC or purely sinusoidal inputs, DSM commonly creates tones (peaks) in its output spectrum, which can be counteracted by dithering the input signal by adding white noise at low amplitude [F72]. In a power electronic application—such as motor control—the noise of the input current and rotor angle signals is large enough to prevent tones in the output, and therefore additional dithering is not required.

Frequency Response Both conventional PWM and DSM can be modelled as a PT1 element to describe their frequency response, where the time constant is the modulation period or PWM period. Here, only the response of the modulation itself is considered, ignoring the controller. As a result, the frequency response of a PWM is only dependent on the switching frequency and the PWM resolution, and not on the type of sampling (e.g. symmetric or asymmetric).
For the DSM, the time constant of its representative PT1 element is equal to the modulation period, which is four times smaller than the average switching period. In contrast, the switching period of a PWM is equal to the time constant of the PT1 used to model it. As a result, for an identical switching frequency the DSM will show superior frequency response to the PWM, and the modulation algorithm is required to be executed four times faster. Using DSM therefore makes the output voltage of the converter follow the controller output voltage more accurately. It should be noted however, that the frequency response of the modulation generally only has a small impact on the converters overall frequency response, which is dominated by the controller and sensors.

5.4 Balancing

After the modulator of the control scheme discretises the output voltage, the subsequent balancing algorithm decides which SMs to switch in series and parallel to achieve the desired output voltage level. Due to the nature of cascaded multilevel converters, each voltage level M, apart from the highest and lowest, has multiple possibilities to be generated. The balancing algorithm chooses how to

generate the output voltage level based on several criteria. In general, the efficiency of the converter and the balancing of SM SoCs are the most important goals [E4]. As shown by the analysis in section 4.4.2, a balancing using only the most efficient switching states cannot work. This is because the efficiency is maximised when the use of the parallel SM state is always forced, but this leads to SMs being unable to be balanced at high modulation indices since the battery currents cannot be controlled independently within a phase.

5.4.1 Simulation

In the simulative validation in this work in section 6.1, a balancing scheme is chosen that does not guarantee balancing of the SM SoCs, but maximises the efficiency of the converter. For each output level, the optimal phase switching states are used, according to the analysis of section 4.2. The converter then alternates between all of the available switching states for each output level, to allow for the best possible current distribution across the batteries.
This balancing scheme is chosen because it is not affected by the SoCs of the batteries, which results in the same performance independent of the current SM SoCs. As shown in chapter 4 and verified by the results of section 6.1, the type of balancing has an impact on the efficiency, which would skew the results depending on the initial condition of the SM SoCs. Since the balance and imbalance of the SMs depends strongly on the drive cycle used and the duration during which the modulation index is high or low, evaluating the efficiency of the MMSPC while considering SM imbalance can never be comparable for different use cases of the converter. For example, an imbalance occurring during aggressive discharging could in many cases be compensated in drive cycle phases with a moderate load, meaning that the most efficient overall operation always needs to consider the SoCs throughout the whole drive cycle.
Such an optimisation however makes it impossible to evaluate and compare the converters at specific operating points to compare their advantages and disadvantages, which is the aim of this work. For this reason, the balance of battery SoCs is not considered in the simulative verification of the converters, and instead the efficiency-optimal balancing is used. It should therefore be noted that the performance shown provides an upper bound for the achievable efficiency of the converters, and the efficiency of the converter may (or may not) be reduced in real-world usage, depending on the drive cycle.

5.4.2 Experimental Validation

In the experimental validation, a balancing algorithm is used that was developed in the Master's thesis of Merz [S1], proving the ability of the MMSPC to remain balanced in real operation. A current distribution in the SMs is predicted based on a simplified model of the converter, which models the batteries as a voltage source with an internal resistance and neglects the semiconductor resistances. At each modulation step, the current distribution is calculated for all allowed switching states and the optimal current distribution is chosen depending on the control objectives. The two objectives are: reducing converter losses and balancing of the SoCs.
In the development of the balancing algorithm, it became evident that the efficiency-optimal converter states alone (as predicted in section 4.4) could not provide balanced SoCs. Therefore the number of allowed states was heuristically expanded [S1] until converter balancing was achieved, as shown in section 6.2.2.2. It is shown that balancing is achievable when using the control algorithm proposed here, but this is not the emphasis of this work. The optimisation of the balancing problem of the MMSPC is discussed in a dissertation written in collaboration with this work on the same project [E9].

Chapter 6

Validation

In this chapter, the previously presented analysis, design and control are verified in simulation and with experiments. First, simulation of the MMSPC, CHB and conventional 2L converter confirms that the behaviour of these converters corresponds to their modelling in chapters 3 and 4. Second, an experimental verification of an MMSPC prototype is presented and discussed, showing the real-time implementation of the control scheme and its ability to reduce the SM's battery currents.

6.1 Simulation

Simulation of the MMSPC as well as the other converters is performed in Matlab/Simulink 2019b using PLECS Blockset 4.4.1 for the simulation of the power electronic components. For all converter types, the electric loads and the current control are identical, whereas the modulation is different for the multilevel and two-level converters. The MMSPC is simulated with the symmetric SM (fig. 2.6 (b)), which allows a direct comparison to the CHB. First, the analysis of the multilevel converters' battery currents from section 3.2.1 is verified and compared for the MMSPC and CHB. The achievable operating area is then compared for all investigated converters in simulation, analogous to section 3.2.2, as well as the efficiency of the converters. Finally, the design of the MMSPC is verified to show the effect of the SM design and number of SMs on the performance of the MMSPC.

6.1.1 Parameters and Modelling

To make the comparison of different converters as fair as possible, the parameters are held constant where possible across the different converter types. This section discusses the parameters of the simulation and uses the values from chapters 3 and 4 where possible.

Semiconductors The semiconductors are modelled as in section 3.2.3, where MOSFETs are modelled as a resistance while IGBTs and diodes are modelled as voltage sources with a series resistance (in the conducting state). For both semiconductors, the parameters are extracted from the datasheets. The switching losses are calculated based on a LUT with datasheet values and scale linearly with the current for the MOSFETs, and to the power of 0.6 for the diode voltage and current, and to the power of 1.3 for the IGBT voltage and linearly for the IGBT current, according to [D4]. Again, the MOSFET IAUT300N08S5N012 is chosen for the multilevel converter, while the IGBT module FS820R08A6P2B is used for the two-level converter [D2, D3]. The semiconductor parameters are given in tables 3.2 and 3.3, and are extracted at 150 °C. The semiconductors are simulated to be cooled so that they remain at a constant temperature of 150 ° °Cthroughout the simulation.

Battery The batteries used in the simulation are sized according to section 4.1.2 for the MMSPC. The CHB uses the same battery configuration as the MMSPC, and between the multilevel and two-level converters, the battery parameters are scaled as described in section 3.1.2.1, to improve comparability across the different converter types. The total stored energy and maximum achievable open-circuit output voltage is identical for all converters.
The battery is modelled according to fig. 4.12, with a stray inductance of 0.1 µH for the multilevel converters and 1 µH for the 2L converter. For the results with a varying number of SMs, the battery is also scaled according to section 3.1.2. In the simulations, the battery OCVs are assumed to be constant to increase the comparability of the measurements, which is a valid assumption as lithium-ion cell voltages only change slowly compared to power-electronic time scales.

Capacitors In addition to the converter batteries, the DC-link components play a significant role in the behaviour of the converter and are an important cost driver. The 2L converter has a DC-link capacitance of 500 µF, which correponds closely to other reported capacitance values for EVs in the simulated power range [F27, F98].

Table 6.1: Motor parameters used in the simulation. All AC values are phase-to-neutral amplitudes.

Parameter	Value
Pole pairs	16
Permanent magnet flux linkage	37 mV s
d-axis inductance	44 µH
q-axis inductance	44 µH
Stator winding resistance	15 mΩ
Nominal power	150 kW
Maximum torque	400 N m
Maximum mechanical speed	7000 min^{-1}
Maximum current	500 A
Nominal voltage	230 V

The capacitors are scaled down for the multilevel converters such that the total stored energy of the converter is the same between the MMSPC and 2L converter, which results in the current in the MMSPC SMs being distributed between the battery and the SM capacitor as described in section 4.3.2. This ensures that the volume and cost incurred due to the capacitors is comparable. As the stored energy of a capacitor scales with the square of the voltage, this gives a module capacitance of 3.3 mF for the MMSPC with five levels.

Load For the simulation of the converter behaviour in dependence of the load voltage and current, the load is modelled as a three-phase current source. This modelling allows the converter to be investigated at all output voltages and current phase angles.
In an EV application, the load is generally a three-phase electric motor such as a PMSM which can be modelled as a three-phase voltage source with series inductances and resistances in each phase. For the drive cycle simulations, the motor used in the measurement results is therefore modelled as a linear PMSM, whose parameters are listed in table 6.1.

Balancing In these simulations, the balancing algorithm that is simulated uses all of the possible permutations of phase states $\vec{S}_\text{p}$ for each output level in equal proportion. This leads to the SoCs not being perfectly balanced due to the resulting unequal current distribution, as shown in section 4.4. As a result, the

Table 6.2: Operating point for the battery current verification

Parameter	Value
Output current amplitude $\hat{I}$	150 A
Modulation index m	0.7
Phase angle ϕ_c	0 rad
Output frequency f	250 Hz

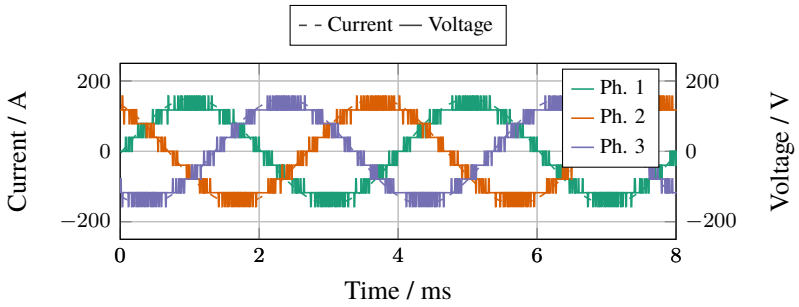
presented analysis is a best-case investigation that may slightly overestimate the efficiency of the MMSPC. The detailed analysis of the balancing problem and the trade-off between efficiency and SoC balance is investigated in the same project in a different thesis [E9].

6.1.2 Validation of Analysis and Design

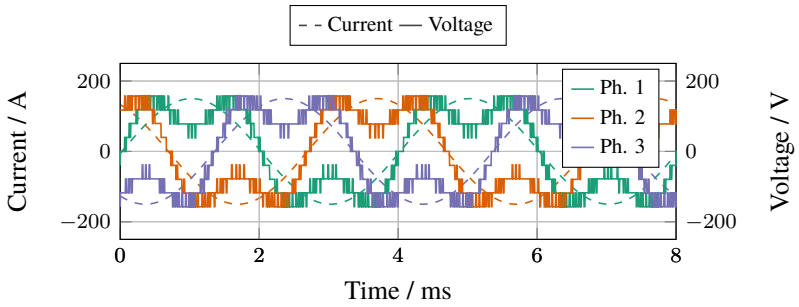
This section validates the analysis and design of chapters 3 and 4 by comparing the behaviour of ideal converters with that of the simulated converters with all relevant parasitic components. First, the battery current is shown in good approximation to behave as described in section 3.2.1, and the different frequency components of the SMs are analysed analogous to section 4.3.2. Second, the losses and operating areas of the converters are compared, with reference to the theoretical investigations of section 3.2.2. Finally, the efficiency of the converters is compared to the analysis of section 3.2.3.

6.1.2.1 Battery Current

In order to validate the analysis of the multilevel converter currents in section 3.2.1, the CHB and MMSPC are simulated in a representative operating point, the details of which are given in table 6.2. The operating point is chosen such that the output voltage is low enough to allow the maximum and optimum mTHI of $a_3 = 0.5$ to reduce the battery rms current, while the current is ca. 30% of the maximum current. As shown in the drive cycle analysis in section 6.1.3.2, this is a relevant operating point since a significant proportion of converter operation is not at maximum voltage and power. The influence of the mTHI over the operating area of the converters driving a PMSM is shown later in section 6.1.3.2. Figure 6.1 shows the output voltage and current of the three phases of the MMSPC with and without mTHI in the analysed operating point. It can be seen



(a) $a_3 = 0$



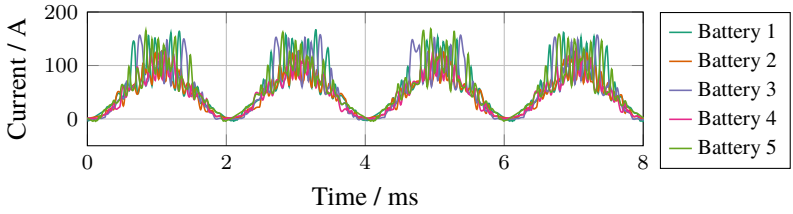
(b) $a_3 = 0.5$

Figure 6.1: Output voltage and current of all three phases of the simulated MMSPC with and without mTHI

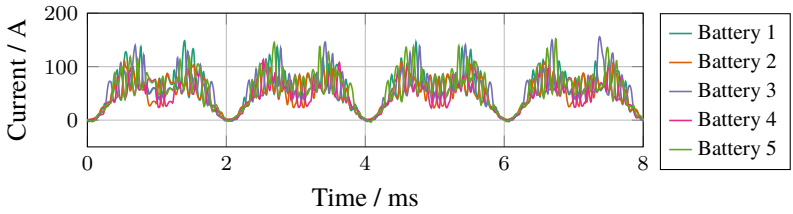
that the output voltage is reduced when the current is near its peak value, which reduces the rms current seen by the batteries.

Figure 6.2 gives the battery currents of all five SMs in phase 1 for the operating point depicted in fig. 6.1, for the MMSPC and the CHB with and without mTHI. The figs. 6.2 (a) and 6.2 (b) show the current of the MMSPC batteries while figs. 6.2 (c) and 6.2 (d) show the current in the CHB batteries. In this comparison, all components of the two multilevel converters are the same and the only difference is that the CHB does not use the parallel mode.

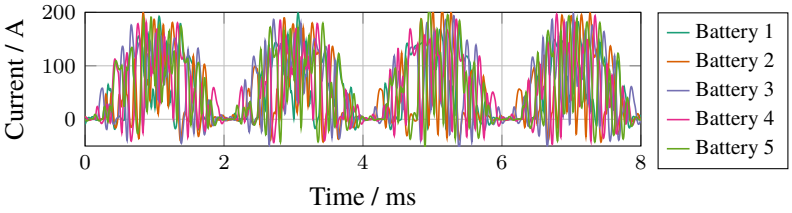
Figure 6.2 shows that the oscillations due to the SM switching are significantly greater for the CHB compared to the MMSPC. This is because of the fact that the high-frequency excitation of the resonant circuit created by the batteries' DLC and stray inductance L_b is much greater than for the MMSPC. As discussed in



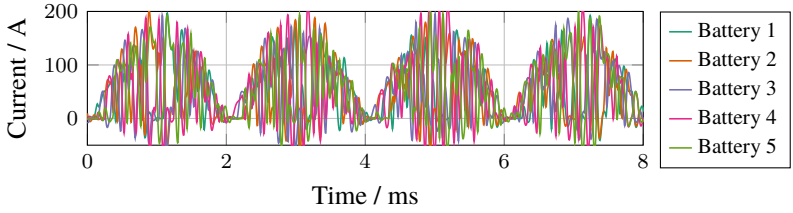
(a) MMSPC, $a_3 = 0$



(b) MMSPC, $a_3 = 0.5$



(c) CHB, $a_3 = 0$



(d) CHB, $a_3 = 0.5$

Figure 6.2: Battery currents of the SMs in phase 1, corresponding to fig. 6.1

section 4.3.2.2, the parallel mode of the MMSPC means that the changes in the SM current are smaller, because parallel SMs share the current almost equally, while in the CHB the current is zero when a module is not in series. As a result, the SM capacitance for a CHB must be far greater to reduce the amplitude of the batteries' current ripple, which significantly increases the resistive losses of the battery. For this reason, in the simulations of the converters' efficiencies in section 6.1.3.2, the SM capacitance of the CHB has been doubled compared to the MMSPC as otherwise the battery losses are unreasonably high. This doubling results in battery losses that are comparable to the MMSPC and more realistic, but comes at an additional component cost in a production environment. This showcases an advantage of the MMSPC over the CHB, that smaller SM capacitors can be used to obtain the same efficiency as the CHBs.

To analyse the battery current compared to the ideal analysis without switching in section 3.2.1, fig. 6.3 shows the same battery currents as in fig. 6.2 with the higher-order harmonics removed. All frequencies above ten times the fundamental frequency (2.5 kHz) are removed to visualise the battery currents without the impact of the semiconductor switching. The ideal battery current at this operating point, according to the analysis in section 3.2.1, is plotted as the dotted red line for comparison.

Observation shows how the mTHI changes the shape of the battery current from a single frequency of twice the output's fundamental frequency to two sinusoidal components, as described by eq. (5.4). This shows that despite the fact that the SM switching is ignored in the continuous analysis of chapter 3, it can accurately predict the shape of the battery current according to eq. (3.10).

Comparison of the MMSPC (figs. 6.3 (a) and 6.3 (b)) to the CHB (figs. 6.3 (c) and 6.3 (d)) of fig. 6.3 again shows how the parallel connections of the MMSPC provide significant advantages over the bypass connection. While it is evident that the current shape of the CHB is similar to the MMSPC, it contains far more harmonics and varies more between the batteries when compared to the MMSPC. Both of these result in increased losses in the CHB: the harmonics increase the batteries' rms current directly, and an uneven current distribution increases the sum of all battery rms currents. In the MMSPC the addition of the parallel connection allows the current to be distributed more evenly, as the number of switching state permutations n_σ needed to distribute the current equally is far lower than without the parallel connection, as analysed in section 4.2. This is further investigated in section 6.1.2.2, where the effect of the number of SMs is shown.

The benefit of the mTHI as well as the converter type can be seen from the data in table 6.3. Injecting the third harmonic voltage reduces the mean of all batteries'

Table 6.3: Mean battery rms currents for fig. 6.2

Converter	$a_3 = 0$	$a_3 = 0.5$
MMSPC	76.2 A	69.7 A
CHB	88.3 A	85.3 A

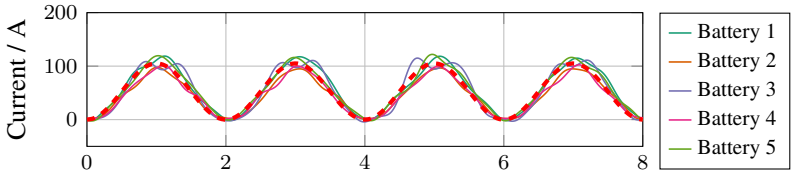
rms currents by 8.5% for the MMSPC and 3.5% for the CHB. The reason that the value for the CHB is significantly lower than for the MMSPC is that the CHB does not distribute the battery current as well as the MMSPC. This means that the CHB battery current is not as sinusoidal as the MMSPC's, and it contains far more oscillations at higher frequencies.

Figure 6.4 shows the spectrum of the battery currents in fig. 6.2, calculated using the discrete Fourier Transform (DFT). Both the MMSPC and CHB currents are in the frequency range below 2 kHz, validating the assumption of continuous battery currents in chapter 3, even at the relatively low switching frequency of the MOSFETs.

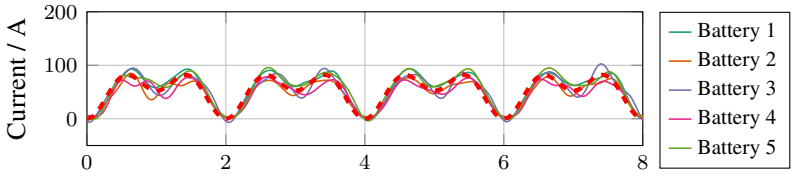
One significant difference in the spectrum of the battery currents between the MMSPC and CHB is the level of the noise floor. For the MMSPC, the noise floor is barely visible in figs. 6.4 (a) and 6.4 (b), while there is significant spurious noise in the spectra of the CHB in figs. 6.4 (c) and 6.4 (d). This is because the current is not distributed well across the SM batteries in the CHB, and results in additional losses because these currents cannot contribute to the power delivered by the converter.

As discussed in section 4.3.1.1, the DLC of the integrated battery can be used to prevent the load currents generating additional losses and degradation in the cells, by causing charge transfer to occur. This is analysed in fig. 6.6, which shows how the SM's current is divided based on the model from section 4.3.1 (see battery equivalent circuit in fig. 6.5). Figure 6.6 (a) shows that the SM capacitors absorb only the high frequency of the semiconductor switching but none of the harmonic current of the load oscillations, as predicted. This is the case despite the relatively high output frequency of 250 Hz.

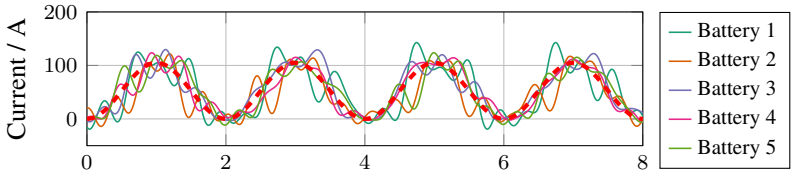
The remaining SM current is divided by the battery's RC capacitor (fig. 6.6 (b)) and the open-circuit voltage source (fig. 6.6 (c)). The voltage source only sees currents below 1 Hz and the entire oscillating energy is absorbed by the DLC. This shows that it is important to choose a battery with a DLC large enough to provide the necessary current filtering to avoid the battery experiencing high-frequency charge transfer. It must also be taken into account that the DLC of lithium-ion batteries varies with temperature, SoC and degradation.



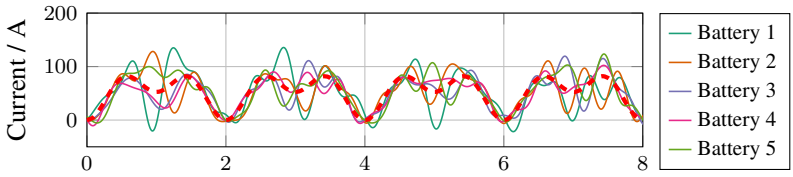
(a) MMSPC, $a_3 = 0$



(b) MMSPC, $a_3 = 0.5$

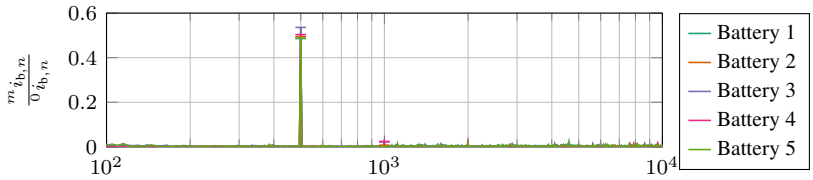


(c) CHB, $a_3 = 0$

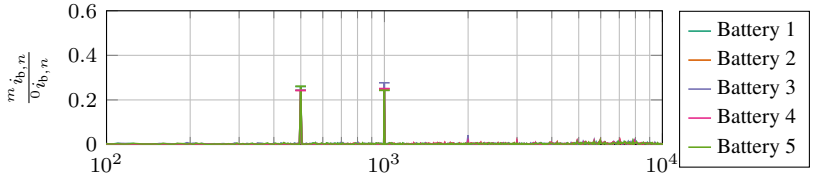


(d) CHB, $a_3 = 0.5$

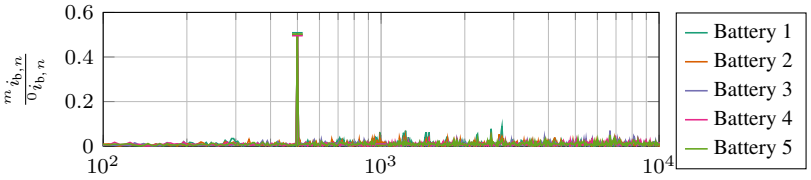
Figure 6.3: Battery current in phase 1, filtered to remove all frequencies higher than ten times the output frequency. The dotted red line indicates the current profile according to the ideal analysis presented in section 3.2.1. It can be seen that the MMSPC current corresponds much more closely to the ideal analysis than the CHB.



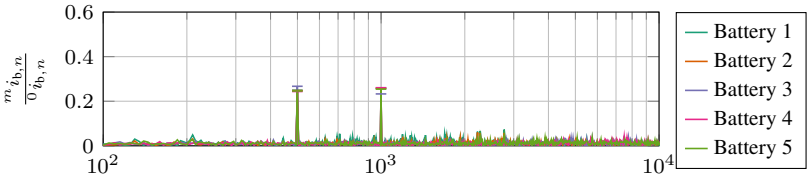
(a) MMSPC, $a_3 = 0$



(b) MMSPC, $a_3 = 0.5$



(c) CHB, $a_3 = 0$



(d) CHB, $a_3 = 0.5$

Figure 6.4: DFT of fig. 6.2, normalised to the zero frequency value. The horizontal markers indicate the 2nd and 4th harmonic of the output current, showing that the spectrum of all SMs is very similar.

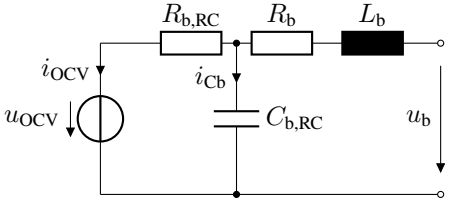


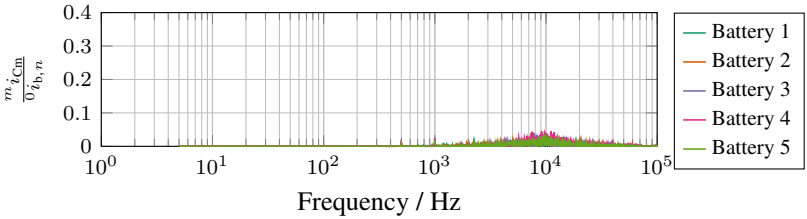
Figure 6.5: Equivalent circuit of the SM battery

Currently, the DLC of the battery does not play a large role in the design of automotive batteries, but the move toward more advanced converters such as the MMSPC may require design engineers to consider is as an element of their design. This may significantly increase the complexity of the battery design process, as the DLC properties of lithium-ion batteries are not generally provided in their specification, and must be measured at a large number of battery states.

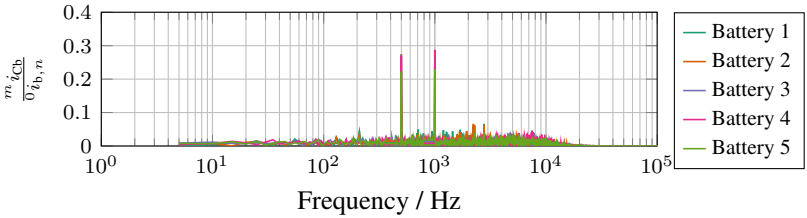
In summary, the simulation data shows that the MMSPC rms battery currents are significantly lower than for a comparable CHB. This is due to the fact that the parallel state of the SM allows the MMSPC to distribute the current between all SMs far more evenly than the CHB over several switching periods, as predicted in section 4.2. Furthermore, the proposed mTHI control scheme is able to significantly reduce the rms battery current by injecting a CMV, for both converters. A reduction in rms battery current leads to a lower heat generation, which can benefit the battery lifetime if it allows the battery to avoid temperatures at which excessive degradation takes place. Nonetheless, the battery currents will always be significantly lower in single-DC converters, as these batteries are not subjected to AC currents from the motor.

6.1.2.2 Number of Sub-Modules

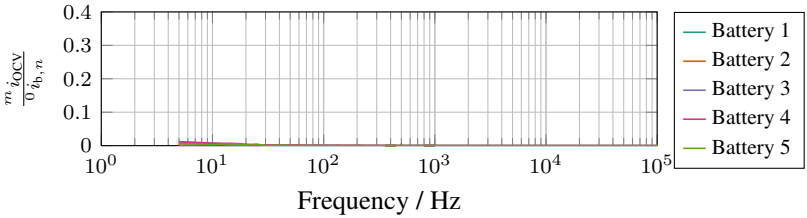
While section 6.1.2.1 shows that the simulated current of the SMs corresponds well to the presented analysis, it only shows the case for five SMs per phase. This section investigates how the number of SMs affects the ability of the converter to ideally share the current, as well as its effect on the battery losses.
Figure 6.7 (a) shows the SD of the battery currents for all SMs in the same operating point as fig. 6.2, for a varying number of SMs per phase. It can be seen that the SD depends strongly on the number of SMs and the converter type. An even number of SMs reduces the SD of the currents, as the available switching



(a) Module capacitor

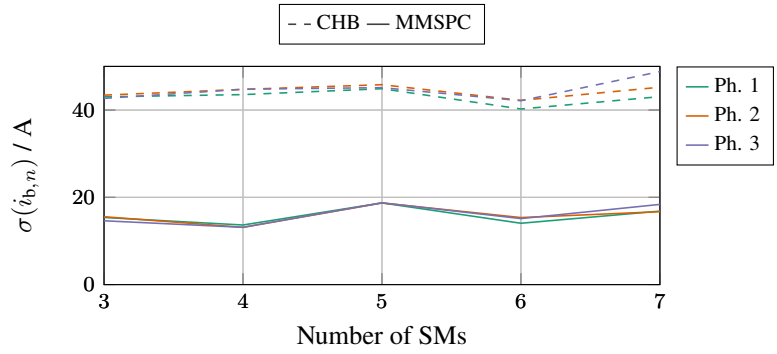


(b) DLC

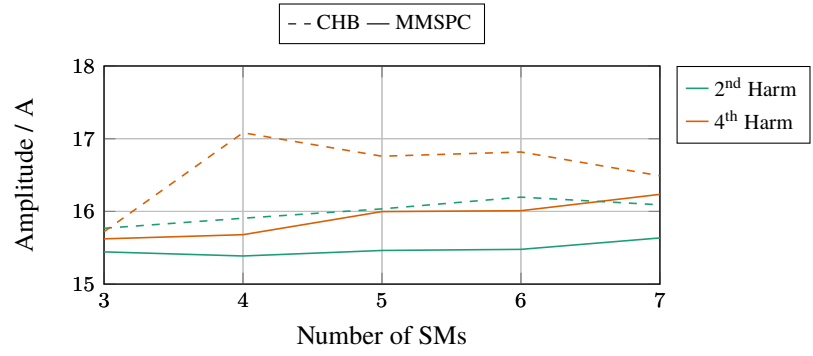


(c) Charge-transfer voltage source

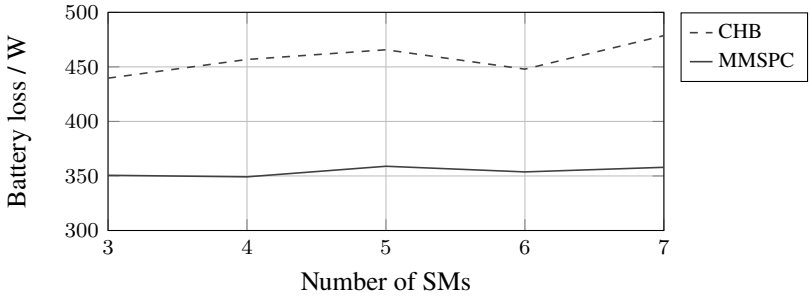
Figure 6.6: DFT of the distribution of the SM's current between the decoupling capacitor, DLC, and battery charge-transfer voltage. The decoupling capacitor filters the majority of the switching currents from the DSM, while the DLC absorbs the two 2$^{\text{nd}}$ and 4$^{\text{th}}$ harmonic peaks almost entirely. The charge-transfer voltage source sees a quasi-DC current, which does not appear on the logarithmic plot.



(a) SD of the battery current in all SMs of a phase



(b) Amplitude of the batteries' 2nd and 4th current harmonics



(c) Battery loss

Figure 6.7: Various performance metrics of the MMSPC and CHB when varying the number of SMs between three and seven

Table 6.4: Parameters for the simulated 2L converter

Parameter	Value
Battery voltage	400 V
Battery capacity	120 A h
Semiconductors	FS820R08A6P2B Drive Module
Switching rate	10 kHz
DC-Link capacitance	500 µF
Modulation	SVM

states of a phase have a better distribution of current, as predicted in chapter 4. In general, the variation of current distribution closely resembles the shape predicted by the performance function J_N in fig. 4.9. At the same time, the CHB is far inferior to the MMSPC due to its inability to share current via the parallel mode.
The amplitude of the batteries' current harmonics are also closer to the ideal for the MMSPC, as shown in fig. 6.7 (b), where the ideal case is that both harmonics have equal amplitude. The effect of the non-ideal current distribution becomes evident in fig. 6.7 (c), which shows the battery loss as a function of the number of SMs. The shape is almost identical to the SD of battery current in the SMs shown in fig. 6.7 (a), showing that this is a reliable indicator of balancing scheme's losses.
The reason that the current distribution is not ideal is that the switching rate of the MOSFETs and the number of SMs is finite, unlike the assumptions made for the analysis in chapter 3. For example, assumption 2 in section 3.1.1 is not perfectly valid, especially for the CHB. Furthermore, the modulation adds distortion to the output and results in non-sinusoidal output voltages and currents, which contradicts assumption 1. Despite this, the simple analytical equations of section 3.2.1 can predict the battery currents accurately enough for a first design analysis.

6.1.3 Converter Comparison

In this section, the multilevel converters are compared to the 2L. A converter's achievable operating area plays a significant role in the benefits and drawbacks of the converter, and is analysed here for the MMSPC, CHB, and conventional 2L converter. The scaling is as discussed in section 6.1.1, and the converter parameters are summarised in tables 6.4 and 6.5. From this point forward, all

Table 6.5: Parameters for the simulated multilevel converters

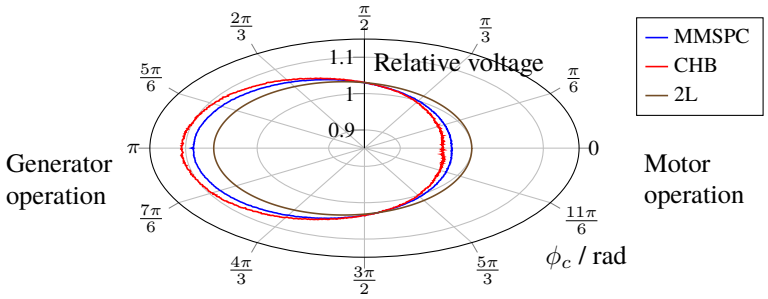
Parameter	Value
SM battery voltage	40 V
SM battery capacity	80 A h
Semiconductors (CHB HB)	4×IAUT300N08S5N012
Semiconductors (MMSPC HB)	2×IAUT300N08S5N012
Average SM switching rate	4 kHz
SM capacitance	3.3 mF
Number of SMs	5
Modulation	DSM (see section 5.3)

simulations with the multilevel converters are done using the proposed control scheme of optimal mTHI to reduce the battery rms current. All phase SoCs are balanced, so BVI is not used to balance the mean phase SoCs. This is because in realistic operation, where the SoCs of the phases are generally close together, the impact of BVI on the converter operation is marginal.
Due to the sensitivity of the results to the component parameters such as the chosen semiconductor, the quantitative comparison between the converters can vary significantly based on a specific design. These analyses are meant to provide a qualitative comparison of the difference between the converters and lead to an understanding of which effects lead to the difference on an architectural level.

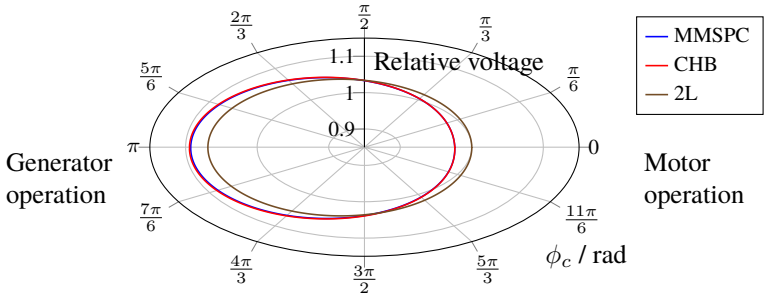
6.1.3.1 Operating Area

For automotive converters, two main aspects of their performances limit their operating area, both of which are investigated here. First, the maximum magnitude of fundamental output voltage as a function of phase angle and modulation index is analysed. Secondly, the boundaries of the operating area resulting from the losses of the battery and semiconductors are shown. All simulations occur at an output frequency of 250 Hz.

Achievable Fundamental Magnitude As shown in chapter 3, the maximum output voltage of a converter is reduced at high currents due to the voltage drop across the resistances in the system. Here, the magnitude of the fundamental component of the output voltage is used to determine the maximum output voltage, calculated using the DFT. It can be used as an indicator of the maximum power a converter can deliver.



(a) $m = {}^{1}/\sqrt{3}$



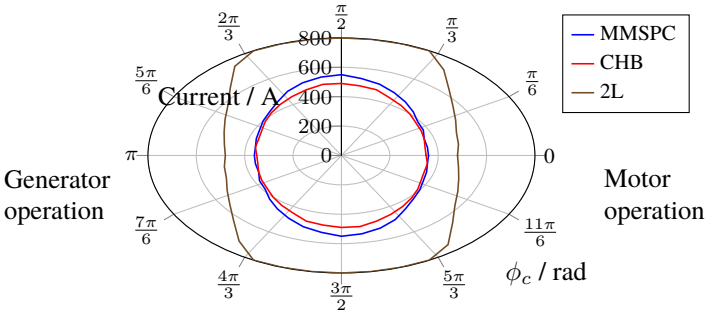
(b) $m = {}^{2}/\sqrt{3}$

Figure 6.8: Maximum achievable fundamental output voltage magnitude of the investigated converters at maximum current over the load current phase angle. The values are normalised to the fundamental magnitude of the 2L converter at $\phi_c = 0$.

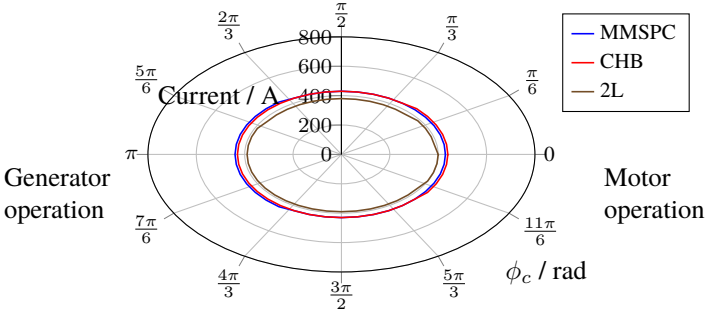
To determine the achievable fundamental magnitude, the converters are simulated at the converter's maximum current—500 A here—over all phase angles and two modulation indices, $m = {}^{2}/\sqrt{3}$ and $m = {}^{1}/\sqrt{3}$. The current is identical for all converters and simulated as a sinusoidal current source. For an ideal converter without resistances, the output fundamental magnitude would depend only on the modulation index.
Figure 6.8 (a) shows the normalised output voltage magnitude for all converters, normalised to the output voltage of the 2L converter at $\phi_c = 0$, when $m = {}^{1}/\sqrt{3}$. At this modulation index, the multilevel converters can fully utilise the mTHI to reduce their batteries' currents. It can be seen that at positive active powers, the

2L converter always has a higher fundamental voltage, indicating its ability to deliver more power than the multilevel converters. This is due to the fact that the multilevel converters' batteries must sustain a larger rms current than for the 2L, and therefore the voltage drop incurred is higher.
For the right-hand side half-plane, the fundamental output voltage of the 2L is on average 1.8% greater than of the MMSPC. In contrast, the output voltage of the CHB is -0.69% smaller as a result of the larger resistance in the converter phase.
At $\phi_c = \pi/2$ all converters have the same output voltage since there is no DC current flowing in the batteries and therefore no DC voltage drop. At negative active powers, the ratios of fundamental magnitude are inverted, as the voltage drop over the batteries' resistances now increases their voltage. Figure 6.8 (b) shows that the gap between the 2L converter and the MMSPC remains the same even at the limit of modulation. However, the difference between the MMSPC and the CHB becomes negligible. This occurs because at very high output voltages the MMSPC can no longer use the parallel mode frequently, and it's benefit compared to the CHB cannot be used.

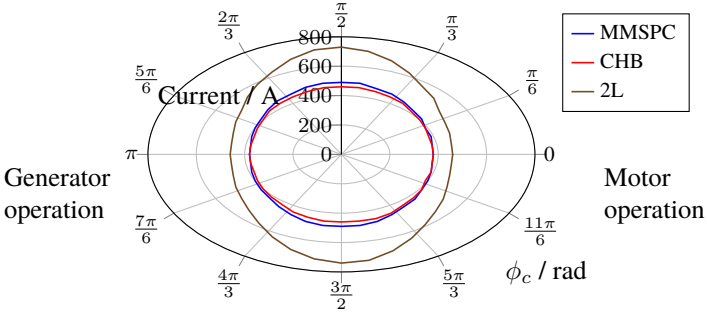
Limitations due to Losses In addition to the modulation limits of the converter, the losses generated during operation impose limits on the operating area of power converters. This is because the capacity of the cooling system is limited. If more heat is generated than can be cooled by the cooling system, continuous safe operation is not possible. In this section, the operating area limits due to the semiconductor and battery losses are examined at maximum modulation index. The losses are divided into two contributions, as in EVs the power electronics and batteries often have separate cooling loops with different temperature and cooling requirements.
In this analysis the output current is increased until a loss threshold is reached, at a constant phase angle and maximum modulation index. The current at which the loss threshold is reached is plotted over the phase angle, showing the operating area of the converters.
Figure 6.9 (a) shows at which currents the battery losses exceed 4.0 kW for all three investigated converters. As predicted in chapter 3, the split-DC converters show a very different behaviour to the 2L converter. While the maximum current of the 2L converter is almost solely dependent on the converters active power and therefore follows an almost straight vertical line, the increase in maximum current for the multilevel converters is significantly smaller as the phase angle goes to $\pm\frac{\pi}{2}$ and the active power is reduced. This is a direct result of the fact



(a) Battery losses $< 4\,\mathrm{kW}$



(b) Semiconductor losses $< 2.5\,\mathrm{kW}$. The lines for the CHB and MMSPC overlap.



(c) Total losses $< 6.5\,\mathrm{kW}$

Figure 6.9: Boundaries of the converter operating area for battery, semiconductor and total losses over the load current phase angle. For all plots, $m = {}^{2}/\sqrt{3}$.

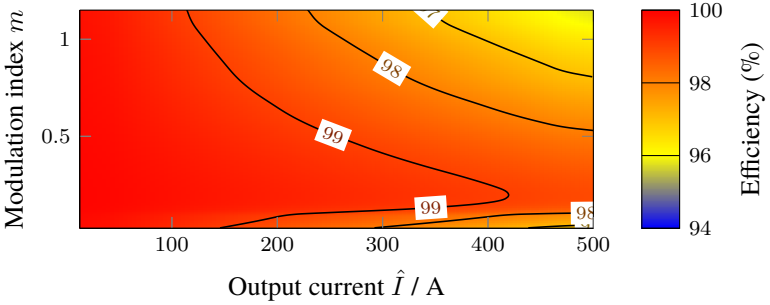
that the multilevel batteries see a significant AC current independent of the load phase angle, while the 2L battery's current is approximately proportional to the active power.
When comparing the MMSPC with the CHB, the current limit is almost identical at pure active power, while the MMSPC performs better at reactive power. This is due to the fact that the MMSPC's benefits are greatest at low output voltages, and when operating reactively the loss-generating current is largest when the voltage is low. At high voltages, the MMSPC cannot use the parallel as much and behaves very similar to the CHB.
The behaviour of the semiconductor losses is different, and the maximum current is in good approximation only dependent on the output current magnitude, as seen in fig. 6.9 (b). This is true for all converters, and the difference between the two multilevel converters is negligible. The 2L converter has a slightly smaller operating area however, showing that the multilevel converter MOSFETs are competitive to IGBTs even at high loads.
Figure 6.9 (c) shows the operating area when both losses do not exceed 6.5 kW and show that overall, the 2L converter allows a significantly larger operating area than the multilevel converter for comparable parameters. For fig. 6.9 (c), the previous limits of the semiconductors and batteries individually are ignored, and the highest output current is shown for which the total losses do not exceed 6.5 kW.
The investigation of the loss boundaries of the different converters show how all converters are limited similarly with regards to the power electronics, but the battery loss boundary is significantly different depending on whether the battery is subjected to reactive current. Furthermore, the MMSPC always achieves a slightly larger operating area than the CHB due to the lower battery losses; the semiconductor losses are identical.
It should be noted here that the comparison between the split-DC converters and the single-DC converter should only be assumed to be valid for these design parameters. The difference between the behaviour of the semiconductor types means that it is impossible to compare these converters in a general manner, and a change in either semiconductor choice could result in significantly different results. The comparison between MMSPC and CHB has a general validity however, as these converters share the same semiconductor type and number, and vary only in their interconnection.

6.1.3.2 Efficiency

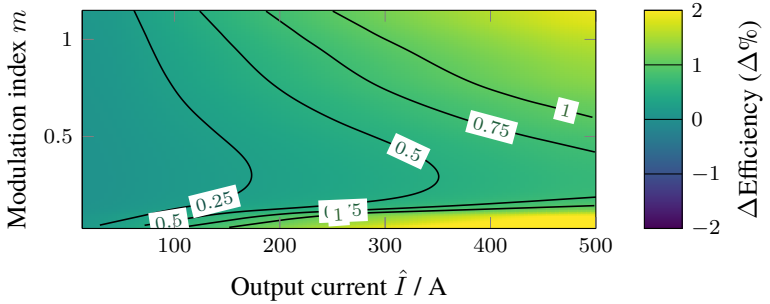
In this section, the simulations of the converter performance are used to provide a detailed understanding of the differences in the efficiency of all three converter types. The efficiency is divided into the battery efficiency, semiconductor efficiency and total efficiency, and each efficiency is defined as the one-way efficiency, i.e. for the energy transfer from battery to load.
The converters are first analysed using an ideal current source as a load, followed by a comparison in an example motor application.

Ideal Load For these plots, the load of the converters is an ideal sinusoidal current source with an output frequency of 250 Hz. The other parameters are kept constant from the previous simulations. All simulations are performed at a power factor of 1, which is the power factor at which the split-DC converters perform best compared to the 2L converter. They should therefore be considered a best-case comparison, while the comparison for an entire operating area profile is shown later.
In order to compare the MMSPC and CHB realistically, the SM capacitance of the CHB's SMs is doubled compared to the MMSPC. This allows the CHB to better compensate the suboptimal current distribution within its SMs—as shown in fig. 6.7 (c)—at the expense of an increased hardware cost. Without this adaptation of the CHB, its losses would be significantly higher and not realistic in an automotive application, highlighting the advantage of the MMSPC being able to reduce the filtering necessary to distribute the battery currents evenly.

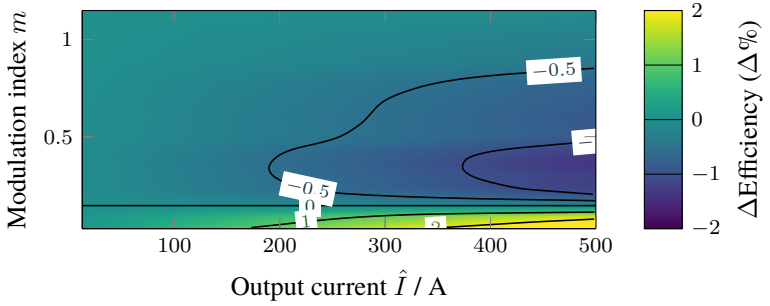
Battery Figure 6.10 shows and compares the battery efficiency of the three converter types. The battery efficiency is defined as the ratio of the delivered battery power to the sum of delivered battery power and battery loss.
Figure 6.10 (a) shows how the battery efficiency of the MMSPC varies with the output voltage and current. The battery efficiency is over 99% for the majority of the operating area, and decreases strongly as the current increases. At low output voltages, the effect is less severe, which is due to the fact that at low modulation indices the converter can distribute the current across the SMs more easily.
The comparison to the 2L converter in fig. 6.10 (b) shows that the MMSPC's battery efficiency is lower in the entire operating area, and substantially lower at higher currents and voltages. This validates the analysis presented in chapter 3, which shows that the rms battery current, and therefore the battery losses, are always higher in the MMSPC, which is a result of the need of the converter arms



(a) Battery efficiency of the simulated MMSPC



(b) Increase in battery efficiency from MMSPC to 2L

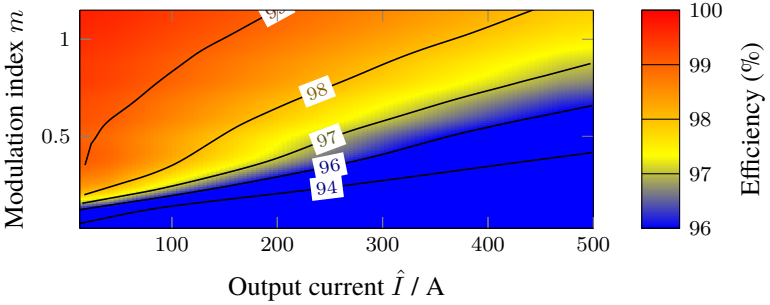


(c) Increase in battery efficiency from MMSPC to CHB

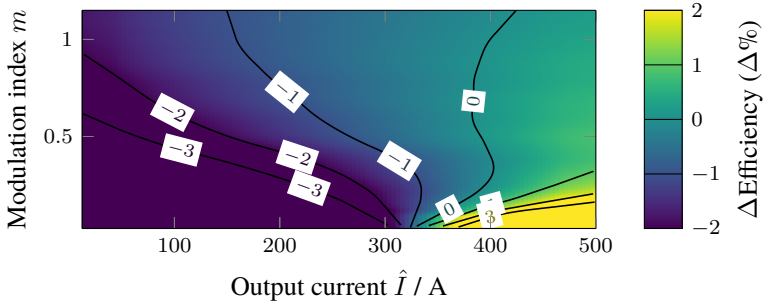
Figure 6.10: Absolute battery efficiency of the MMSPC and difference in efficiency to the 2L converter and CHB. For the comparative plots, negative numbers indicate that the MMSPC is more efficient.

to buffer the oscillating power of the phase. Despite the use of mTHI to reduce the MMSPC's rms current, the effect is significant.
The difference in battery efficiency is far smaller when comparing the CHB to the MMSPC, as shown in fig. 6.10 (c). While the MMSPC is slightly more efficient, the difference is less than 0.5% over the majority of the operating area. This is remarkable considering the simulated CHB has twice as much capacitance in its SMs compared to the MMSPC. At high output currents and low output voltages, the difference between the two converters is especially high, as the effect of the parallel mode of the MMSPC is the highest here, due to the low modulation index. In contrast, at high modulation indices the difference in battery is significantly smaller, although the MMSPC is always better.

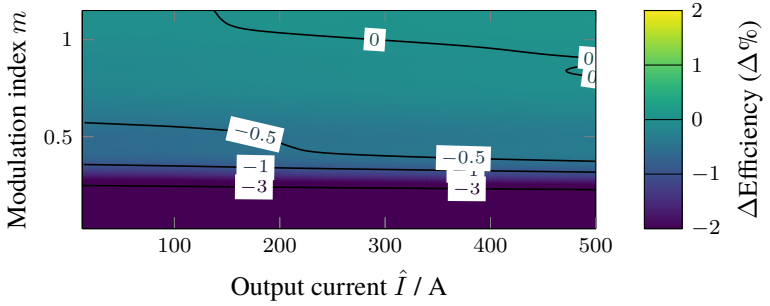
Semiconductors Figure 6.11 shows and compares the power electronic efficiency of the three converter types. The power electronic efficiency is defined as the ratio of the output power of the converter to the power delivered by the batteries. It captures the losses generated by the conduction and switching losses of the semiconductors, while lesser losses such as gate-driving losses are assumed to be negligible.
For the MMSPC, the semiconductor efficiency shows a similar trend to the battery efficiency, where the efficiency is significantly higher at lower currents than at higher currents, as both batteries and semiconductors (MOSFETs) have a resistive characteristic. Unlike the battery losses, however, the semiconductor losses do not decrease as the output voltage decreases and only depend on the conducted current, resulting in low semiconductor efficiencies at low output voltages.
Figure 6.11 (b) shows the very different semiconductor characteristic of the IGBT. While at high voltages the conduction losses only increase slowly due to the voltage drop of the forward voltage, the low current efficiency is significantly worse than the MMSPC. Over the majority of the operating area, the MMSPC is more efficient, which is also due to the significantly lower switching losses of the MOSFETs compared to the IGBTs.
The use of a CHB in the place of the MMSPC reduces the semiconductor efficiency over almost the entire operating range of the converter. This has two reasons; first, the CHB always switches every half-bridge when switching from a series state to a bypass state, while the MMSPC only switches half of the semiconductors, leading to lower switching losses. Secondly, due to the significantly larger changes in battery current (see fig. 6.2), there are large current oscillations at the semiconductor which generate significant losses. This effect is especially strong at low output voltages, where the changes in current in the CHB SM are



(a) MMSPC



(b) Increase in semiconductor efficiency from MMSPC to 2L



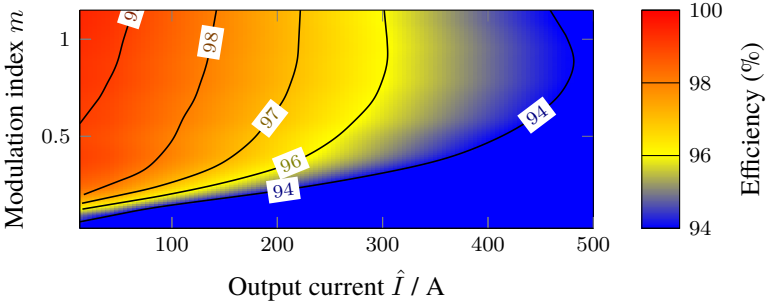
(c) Increase in semiconductor efficiency from MMSPC to CHB

Figure 6.11: Absolute semiconductor efficiency of the MMSPC and difference in efficiency to the 2L converter and CHB. For the comparative plots, negative numbers indicate that the MMSPC is more efficient.

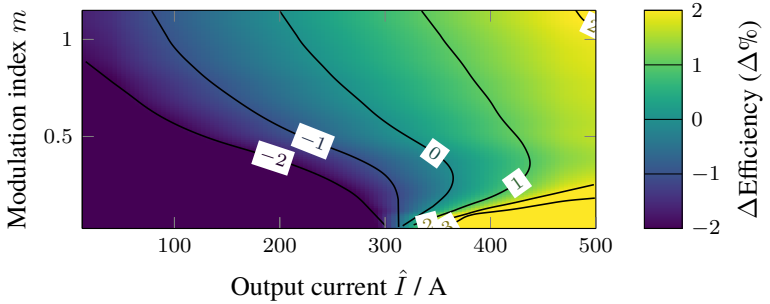
very large compared to the MMSPC, which can use the parallel mode to distribute the current, as shown by fig. 4.9.

Overall Efficiency Combining the efficiencies of the battery and semiconductors, fig. 6.12 shows the overall efficiency of the MMSPC and the increase of efficiency for the other converters. As expected by the simple calculations made in chapter 3, the MMSPC is especially efficient at low currents, achieving an overall efficiency in excess of 99%.
Comparing the simulated efficiency of the converters to the predictions made in section 3.2.3, it can be seen that despite the simplifications made in the model, the predicted efficiencies are very close together, for both the MMSPC and the 2L converter. This shows that the assumptions made in chapter 3 are valid, such as the assumptions that the battery current is split equally across all SMs in the MMSPC.
In contrast, the predicted efficiency of the CHB is widely different to the simulative results presented here, meaning that some of the assumptions that are valid for the MMSPC are not valid for the CHB. The assumption that is invalid for the CHB is the assumption that the SM currents are sinusoidal according to eq. (3.10). As shown in fig. 6.2, the battery current of the CHB has many more higher-order harmonics than the MMSPC, and the current is not divided as evenly between the SMs in the short term. This remains the case despite the fact that the capacity of the CHB SMs is twice as big as for the MMSPC. Thus the equal distribution of the SM currents is proven to be a significant advantage of the MMSPC, as predicted in section 4.3.2.
Figure 6.12 shows that the MMSPC is more efficient than the CHB over the entire operating range, but especially at lower voltages, where the ability to switch SMs in parallel greatly improves their current distribution. Following the analysis of the converters' efficiency dependent on modulation index and output current, the following section extends the analysis to realistic drive cycles, as they would be encountered by real-world vehicles.

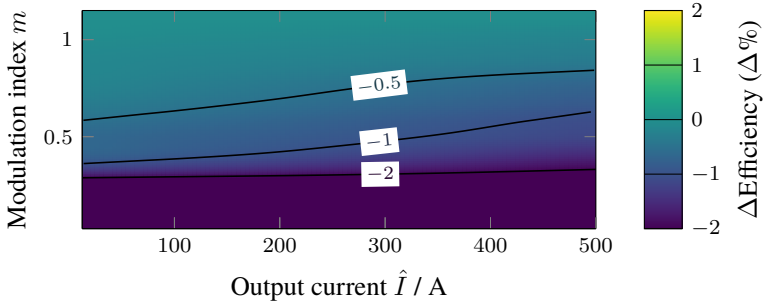
Example Motor Application With the same simulation model used for the efficiency analyses with an ideal current load, the efficiency of the analysed converters was evaluated for a model of a motor used in an automotive drivetrain. The vehicle is modelled using a simple longitudinal model with acceleration (longitudinal and rotational), friction proportional to speed, and drag proportional to the speed squared. Table 6.6 gives the relevant vehicle parameters.



(a) MMSPC



(b) Increase in overall efficiency from MMSPC to 2L



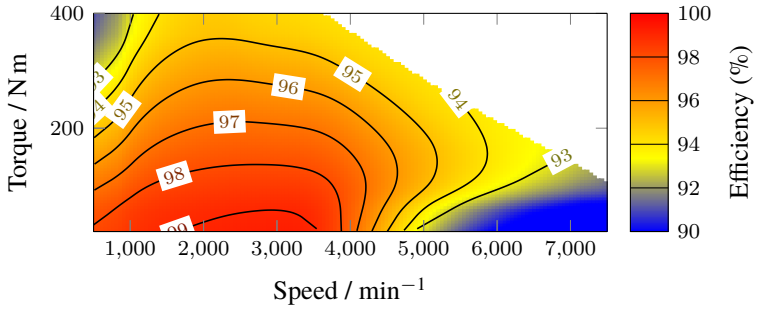
(c) Increase in overall efficiency from MMSPC to CHB

Figure 6.12: Absolute overall efficiency of the MMSPC and difference in efficiency to the 2L converter and CHB. For the comparative plots, negative numbers indicate that the MMSPC is more efficient.

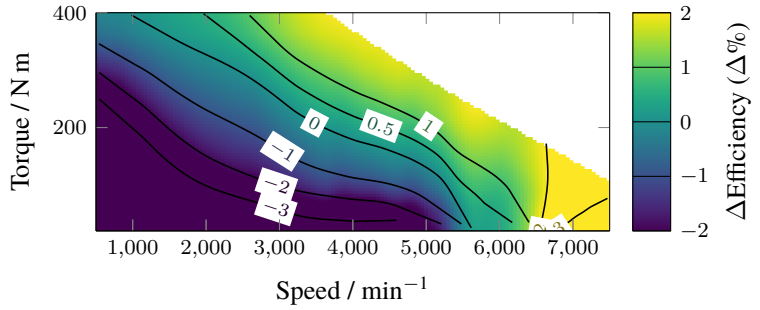
Table 6.6: Parameters of the vehicle used in the simulation

Parameter	Value
Car mass	1650 kg
Frontal area	2.36 m^2
Drag coefficient	0.27
Coefficient of friction	0.011
Total moment of inertia	1.6 kg m^2
Effective wheel radius	0.3 m
Gearbox ratio	4.95

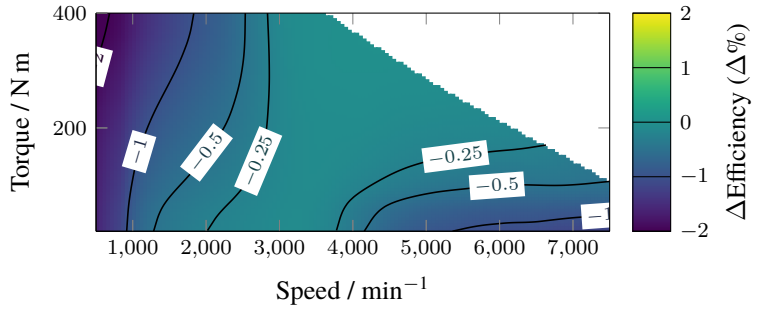
The electric load motor is modelled as a linear PMSM (see table 6.1), where the motor currents are calculated using the MTPA algorithm [F7] with a 90% control margin on the converter output voltage. The parameters are those of a linearised model of the motor used for the experimental verification section 6.2.1.3.
The efficiency of the MMSPC and the other converters in the EV application is shown in fig. 6.13. As expected, the MMSPC shows excellent low-load efficiency, and surpasses the efficiency of the 2L in approximately half of the operating points. Due to the resistive nature of the MOSFET semiconductors, the MMSPC is more than $3\Delta\%$ more efficient than the 2L converter below $2000\,\mathrm{min}^{-1}$ and 200 N m.
Compared to the CHB, the MMSPC is more efficient over the entire operating range. The advantage is especially prevalent at low speeds and high torques—due to the benefit of the parallel mode when the modulation index is low—and at high speed and low torques, because here the power factor is low. At low power factor, the advantage of the parallel mode of the MMSPC is larger as the current is high when the voltage is low, which is when the MMSPC can use the parallel mode more.
In order to determine the suitability of a converter for a specific automotive application, the drive-cycle of the target vehicle must be analysed in order to know which operating points of the motor will be used most frequently. From this information, the overall efficiency of the converter and battery for a specific application can be determined, allowing a direct comparison of two different converter types. Three different drive cycles are analysed in this work. The New European Drive Cycle (NEDC), a drive cycle used in the European Union since the turn of the 21st century, which has mainly low-speed and low-power driving, the WLTP, the successor to the NEDC with more balanced driving requirements,



(a) MMSPC

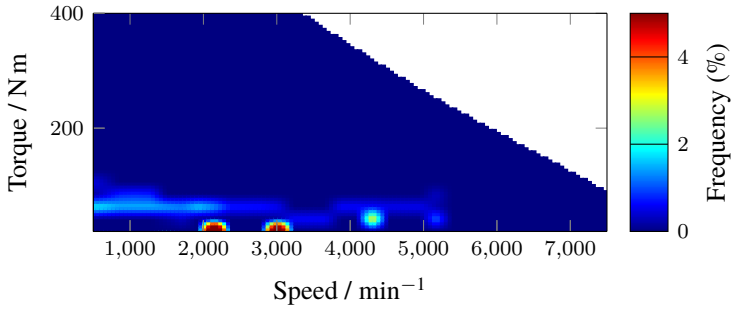


(b) Increase in efficiency from MMSPC to 2L

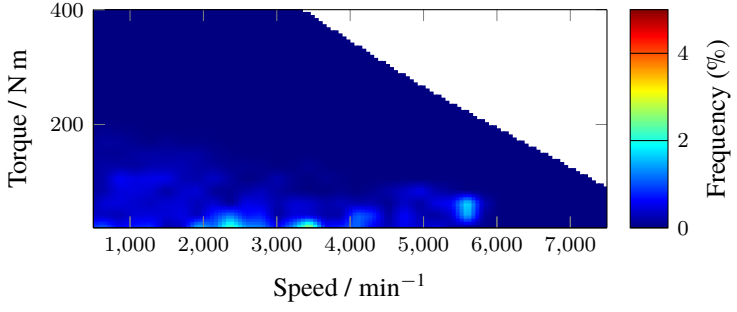


(c) Increase in efficiency from MMSPC to CHB

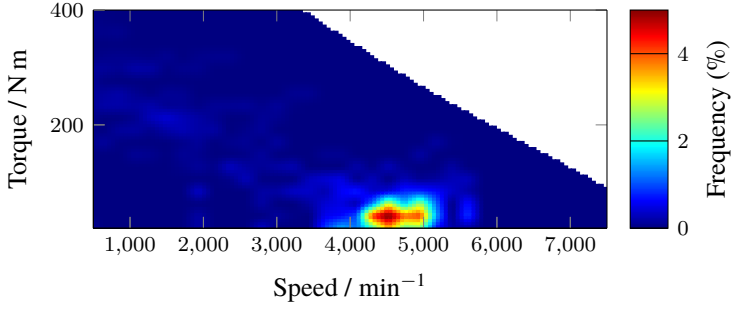
Figure 6.13: Overall efficiency of the investigated converters over the operating range of the investigated PMSM. For the comparative plots, negative numbers indicate that the MMSPC is more efficient.



(a) NEDC



(b) WLTP



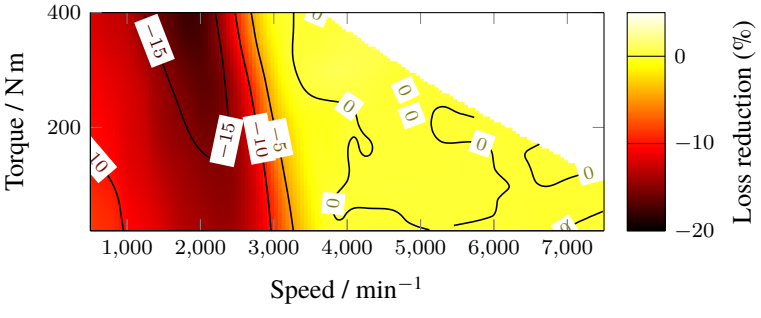
(c) US06

Figure 6.14: Frequency of occurrence of the motor operating points for the three investigated automotive drive cycles

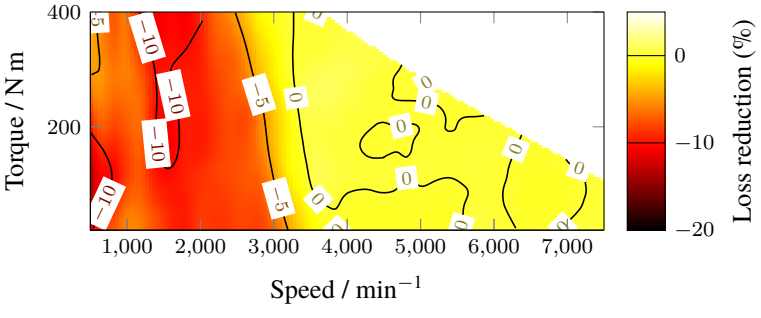
Table 6.7: Efficiency of the converters for each driving cycle

	Efficiency (%)		
Converter	NEDC	WLTP	US06
MMSPC	97.4	96.5	95.9
2L	96.0	96.1	96.2
CHB	97.0	96.1	95.5

and the United States Environmental Protection Agency FTP-75 US06 supplemental driving cycle, which emphasises high-speed driving on motorways.
Each point in the driving cycle is mapped to the motor's operating point are using the aforementioned vehicle model, at a temporal resolution of 0.1 s. Figure 6.14 shows the frequency that each operating point appears in the three driving cycles for the motor used in the experimental validation.
Table 6.7 shows the total efficiency of all analysed converters for the three driving cycles investigated here. The MMSPC is most efficient compared to the other converters for the NEDC, which is expected due to its superior efficiency at low-power operating points. It is however less efficient at the highway-focused US06 drive cycle than the 2L converter, due to its increased losses at higher powers. The CHB is less efficient than the MMSPC for all drive cycles, despite using larger capacitors in the SMs. This shows that, in general, both the 2L and MMSPC can offer similar performances, with benefits and drawbacks in different use cases.
The use of the presented control scheme's mTHI is analysed in fig. 6.15, which shows the decrease in battery losses without mTHI. For this comparison, state-of-the-art THI with an amplitude $a_3 = 1/6$ is used above a modulation index of 0.9 to increase the available voltage of the converter for the case without optimal mTHI (as presented in chapter 5).
Figure 6.15 (a) shows that the proposed control method can significantly reduce the battery losses by up to 18% at high torques and low speeds. While the CHB also allows the battery losses to be reduced, the effect is not as strong, due to the non-ideal current distribution in the CHB's SMs. At speeds above the motors nominal speed of $3000\,\mathrm{min}^{-1}$, both converters battery losses are identical to those without optimal mTHI, as here the optimal mTHI corresponds to state-of-the-art THI since the common mode voltage needs to be used to increase the modulation index.
In the base speed region, the average battery loss reductions achieved are 10.2% and 6.6% for the MMSPC and CHB, respectively, while the equivalent values



(a) MMSPC



(b) CHB

Figure 6.15: Reduction in battery loss due to mTHI for the MMSPC and CHB, for the operating area of the PMSM

for the entire operating range are 5.9% and 3.8%. Figure 6.15 shows that the proposed control method is well-suited to significantly reduce the battery losses in cascaded wye-configured multilevel converters, especially for the MMSPC, as its parallel mode allows the currents to be better balanced across all SMs.

The simulative verification has shown that the analysis presented in the chapters chapters 3 and 4 can accurately predict the behaviour of the cascaded multilevel converters, as well as the differences between the MMSPC and CHB. The proposed control scheme is verified to significantly reduce the battery losses of the multilevel converters, without impeding on the operating range of the converter. Following the simulative results, the experimental verification shows that the MMSPC functions as expected in a lab-scale prototype.

6.2 Experimental Verification

This section discusses the experimental prototype of the MMSPC that was designed, developed and tested in order to verify the analyses and simulations presented in this work. First, the power electronics and signal processing of the prototype are discussed, followed by the discussion of the real-time implementation of the control scheme on an FPGA. Second, experimental results are presented, showing the successful implementation of the control scheme.

6.2.1 Set-up

To investigate and analyse the MMSPC with the proposed control scheme, a lab-scale prototype was developed, with the help of several students' theses [S1–S5]. The prototype consists of the MMSPC—including the energy source—controlling a load motor on a dynamometer. Three phases consisting of five SMs each comprise the power system of the converter, which is controlled by a centralised control system based on the Elektrotechnisches Institut (ETI)-DSP-System [F99].
Figure 6.16 shows the experimental prototype, including the load dynamometer. The details of the testing set-up are presented in this section.

6.2.1.1 MMSPC

Due to the novelty of the MMSPC topology, custom electronic hardware and software was designed and built to investigate the MMSPC in detail. The prototype was designed for rapid prototyping of control algorithms in a realistic application environment. To allow for flexible testing of hardware and software, the energy density was not in the focus of the design.

System Overview Figure 6.16 shows a block diagram overview of the MMSPC system. The central control system controls the three phases consisting of five SMs each via three independent buses realised by four twisted wire pair CAT5e cables. One twisted pair is used unidirectionally to send the switching commands for the SMs over a RS485-derived bus, while another twisted pair is used for bidirectional Controller Area Network (CAN) communication between the SMs and the control system. Both buses have six nodes in total, one for each SM in addition to the central control system.

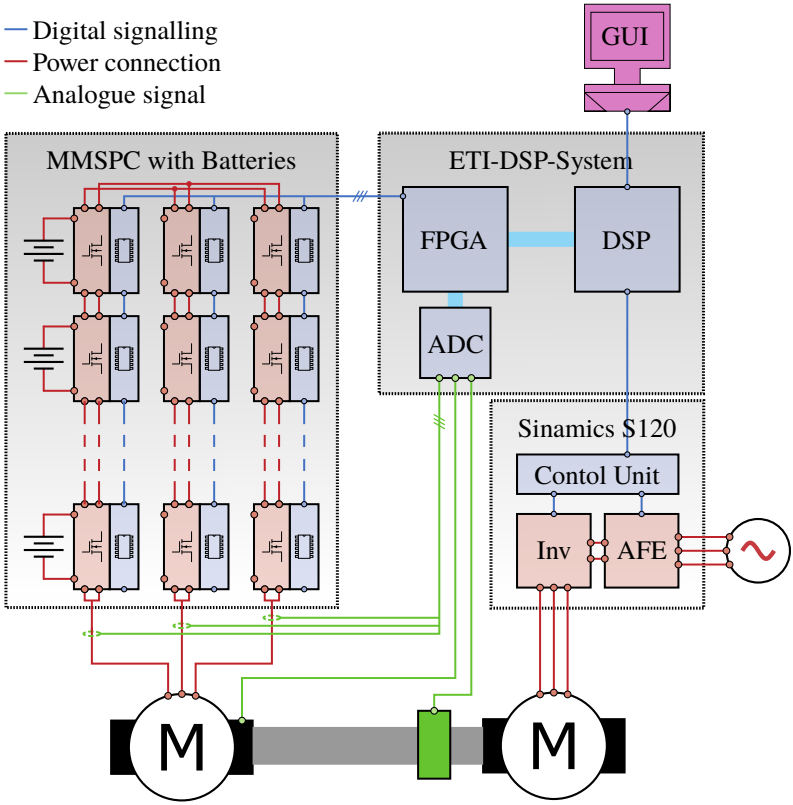


Figure 6.16: Block diagram of test-bench set-up

Control System A dedicated hybrid control system, consisting of a Altera Cyclone IV FPGA and C2000 digital signal processor (DSP) provide the computing power to control and monitor the prototype MMSPC. The hardware of the control system uses the customisable ETI-DSP-System as the basis, including the standard components DSP II, *Hochleistungsmodulatorkarte* (high-performance modulator card) (HMK), and the HMK-analogue-to-digital converter (ADC) [F99] as well as dedicated PCBs built for the MMSPC prototype.
The main control algorithm of the MMSPC is computed on the FPGA, while the DSP provides high-level safety functionality, the control of the dynamometer, and the human-machine interface (HMI). The implementation of the control al-

gorithms is presented in section 6.2.2.1. In addition to the control, the FPGA controls the motor contactors and interfaces the sensor ADCs and the emergency stop signals. The DSP and the FPGA communicate via the 16-bit ETI-Bus [F99].

Sensors The automotive load motor is controlled using three LF 510-S [D5] closed-loop hall effect current sensors with a nominial current of 500 A. An LTC2325-16 on the HMK-ADC measures the secondary current of the sensor via a shunt.
The motor's rotor position is measured by a dedicated rotor-position-sensor based on eddy-current losses. Carrier-free analogue sine and cosine output signals provide the electrical position of the rotor. These analogue signals are also sampled by the LTC2325-16 [D6] and processed by the FPGA which calculates the rotor angle from the four-quadrant arctangent of the sine and cosine signals.

Power System The centralised control system is used to control the SMs which use Infineon 150 V IPB044N15N5 power MOSFETs [D7] and an Altera MAX10 10M08DC F256 FPGA [D8] to receive the switching command and control the MOSFETs. The MOSFETs are driven by UCC21520DWR [D9] gate drivers. In addition to the semiconductors, the SMs have a ACS759 [D10] closed-loop hall-effect current sensor to measure the battery current and a voltage sensor to measure the battery voltage.
The MOSFETs are cooled through thermal vias in the PCB and an axial fan-blown heat sink isolated by a thermally conductive isolator sheet. In parallel with the battery there is a 3.9 mF electrolytic capacitor, while each half-bridge has ceramic and film bypass capacitors (19 times 220 nF ceramic and one 1 µF film). Figure 6.20 shows the SM PCB of the MMSPC prototype.
As in the example design of chapter 4, the neutral point SMs of all phases are connected together in parallel to provide a means of supplying auxiliary power. The results show that, with the parallel neutral point, the analysis of the converter remains valid and the behaviour of the converter is as predicted in section 4.1.3.

6.2.1.2 Battery

Due to the difficulty of sourcing several lithium-ion battery packs in the voltage range of 70 V to 100 V, 12 V FGC 21803 absorbent glass mat (AGM) lead-acid batteries [D11] were used in the prototype. The batteries have an inner resistance of 9.8 mΩ.
As a result of the battery choice, the output voltage of the MMSPC and the resistance of the batteries are not representative of the automotive application from

Figure 6.17: The prototype MMSPC, including the motor test-bench, control cabinet and HMI

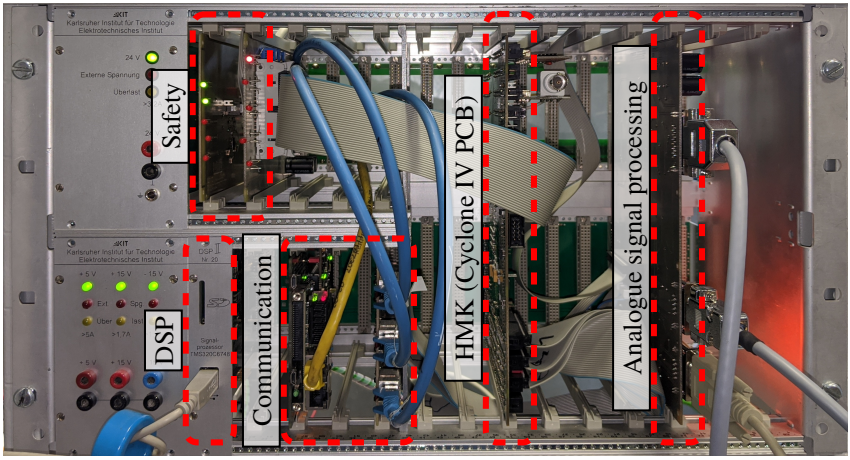
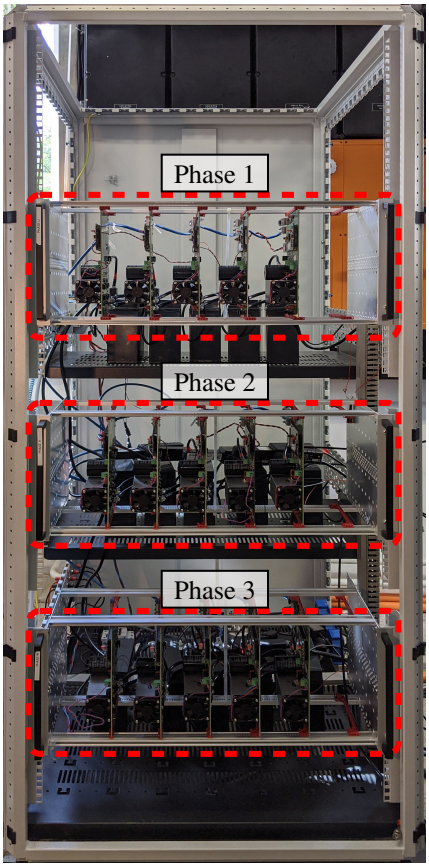
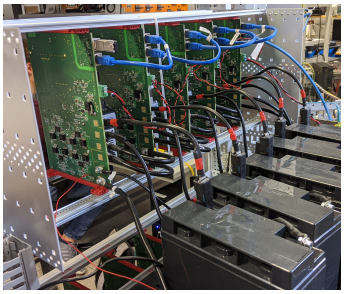


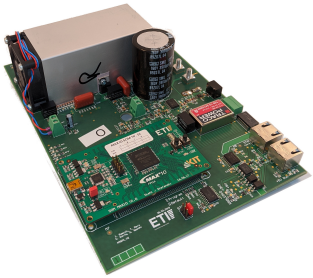
Figure 6.18: The ETI-DSP-System used to control the prototype converter using a DSP in conjunction with a Cyclone IV FPGA



(a) The power electrics of the MMSPC prototype, with three horizontal phases comprising power electronics and batteries

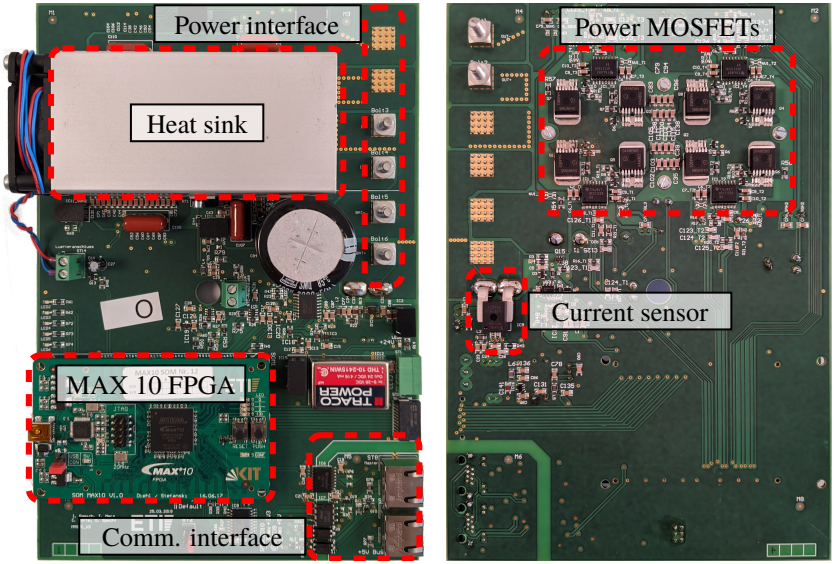


(b) A single phase of the converter viewed from the back, showing the lead-acid batteries



(c) A single SM of the MMSPC. The prototype has five SMs per phase.

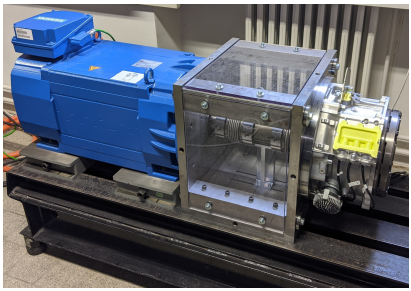
Figure 6.19: Power electronics and batteries of the prototype MMSPC



(a) Top (b) Bottom

Figure 6.20: Top and bottom side of the SM PCB

(a) The motor controller of the load dynamometer, consisting of an active front-end (AFE) with a line filter, a control unit and a converter



(b) The load PMSM (right), and the dynamometer (left), connected via a torque transducer

Figure 6.21: The load PMSM and dynamometer motor (blue), as well as the motor controller of the dynamometer

the previous chapters. Nonetheless, the prototype allows the concept of the converter and its control to be verified and tested compared to the simulations.

6.2.1.3 Load

An automotive PMSM from a modern series-production plug-in hybrid electric vehicle (PHEV) serves as the load of the MMSPC. The motor is designed for converter operation with a DC-link voltage of 320 V and a maximum current of 450 A rms. At the maximum speed of 7000 min^{-1} the PMSM can deliver 100 kW of power and has a maximum torque of 400 N m. The dynamometer braking torque is provided by a water-cooled industry induction motor (IM) from the Siemens S120 product family.
The offset angle between the rotor magnet's flux linkage is calibrated by subjecting the motor to a d-current while varying the angle of the park transform. When the torque is minimal, the calculated rotor position is in line with the permanent magnet flux linkage.

6.2.2 Prototype Results

In this section, the real-time implementation of the presented control scheme in chapter 5 and its experimental results are presented.

6.2.2.1 Implementation

The entire control of the MMSPC, including the motor control and the converter control as well as the modulation and balancing, is implemented on the Cyclone FPGA and programmed using Intel DSP Builder 18.1. Intel DSP Builder is a Matlab Simulink add-on which allows Very High Speed Integrated Circuit Hardware Description Language (VHDL) code to be generated from a Simulink model and simulates the model in exactly the same precision as the generated VHDL code.
As the control scheme—including the sensor data processing and the sending of the commands to the SMs—is done sequentially in fixed-point arithmetic, each sub-functionality is performed in a dedicated calculation block, which triggers the next block upon completion.
In order to avoid measuring the sensor values during a converter switching event, the timing of the sensor measurements is exactly in the middle of two possible switching events of the DSM. The DSM frequency of 80 kHz—giving a period of 12.5 µs—means that the control algorithm including the sensor reading has a

total time of 6.25 µs to execute. This timing was used since the complexity of the balancing algorithm required at least 5 µs on the available hardware, despite the MOSFETs being able to switch at much higher frequencies. As the Intel DSP Builder allows the latency of each block to be determined exactly in clock cycles, real-time execution of the control algorithm is guaranteed.

Internal Converter Control As shown in fig. 5.3, the internal converter control described in section 5.2.2 requires the magnitude of the output voltage and the current phase angle of the output current to calculate the injection required by the mTHI. In addition, the phase SoCs are needed to calculate the injected voltage for the BVI.
Using the Coordinate Rotation Digital Computer (CORDIC) algorithm [F100], the magnitude and angle of the output voltage in the dq-frame are calculated directly from the d and q values of the output voltage of the motor controller. Similarly, the angle of the output current is calculated from the measured current values, and the difference between the voltage and current angles gives the current phase angle of the output current to the output voltage. For the proposed mTHI method, the output voltage magnitude and current are assumed to be steady-state, but both the measured current and output voltage are distorted due to noise and the controller action. To counteract this, a first order digital low-pass filter (LPF) with a cutoff frequency of 300 Hz is used to smooth the calculated voltage magnitude and phase value.

6.2.2.2 Results

This section presents the experimental results of the prototype converter described in section 6.2.1. It is shown that the presented analysis accurately predicts the converter's behaviour and the presented control scheme is able to balance the SMs and phases while minimising the batteries' rms current. The stability of the control scheme in a real-life application at the limits of the modulation index are also shown. First, the operation of mTHI without BVI is shown and analysed to verify the ability of the control to reduce losses. Secondly, the balancing of the converter is demonstrated, including the use of BVI, without mTHI. Finally, results are presented with both mTHI and BVI active, showing that the two components of the control do not interfere with each other.
Figure 6.22 shows the measured converter phase voltage and current in operation with the proposed mTHI used to minimise the rms current of the batteries. At this operating point, the load motor is rotating at 500 min^{-1} and developing a torque of 20 N m. The BVI is not used to balance the energies between the phases.

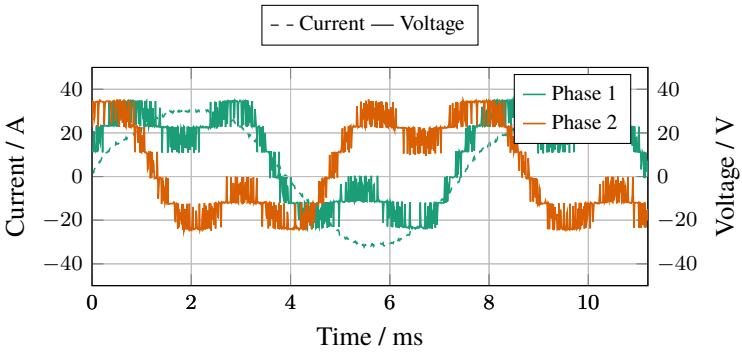


Figure 6.22: Output voltage and current of the prototype converter at a motor speed of 500 min^{-1}

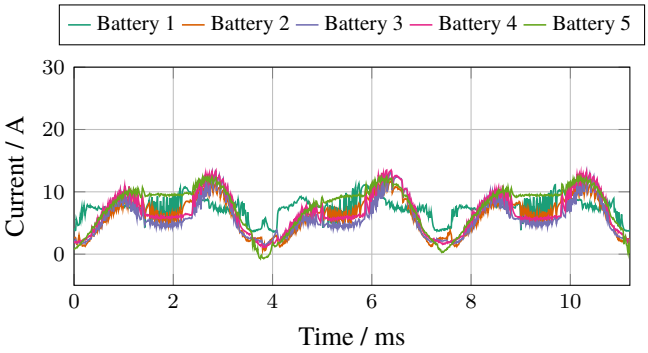
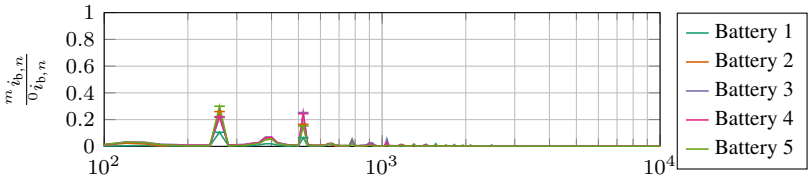
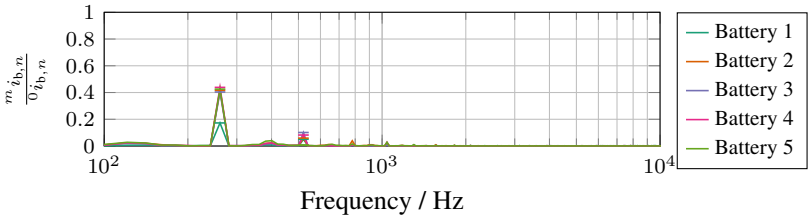


Figure 6.23: Battery currents of the batteries in phase 1 for the operating point in fig. 6.22



(a) $a_3 = 0.5$



(b) $a_3 = 0$

Figure 6.24: DFT of the battery currents shown in fig. 6.23 with and without the use of mTHI to optimise the rms current

Figure 6.22 shows that the proposed control scheme works similar to the simulation in a real-time implementation. The output voltage is reduced by the mTHI at the times when the output current is high, allowing the converter to reduce the current load of individual batteries by switching them in parallel.
Figure 6.23 shows the measured battery currents of phase 1 for the same measurement, showing the effect of the mTHI. In addition to the second harmonic current the batteries are subjected to, as analysed in section 3.2.1, a fourth harmonic is superimposed, depressing the batteries' currents at the peak of the phases' output current. This reduces the rms current of the batteries by making the current load more evenly distributed in time. The mean rms current of the measurement shown in fig. 6.23 is 7.29 A, which corresponds to a decrease of 3.85% compared to the same load point without mTHI. This is significantly less that the predicted reduction of 8.7%, which is due to the fact that the converter is operating at a lower voltage and current than originally designed for, decreasing the accuracy of the control scheme.
This can be seen in fig. 6.24, which shows the DFT of the currents in fig. 6.23. As predicted, the harmonic energy of the battery currents is shared between

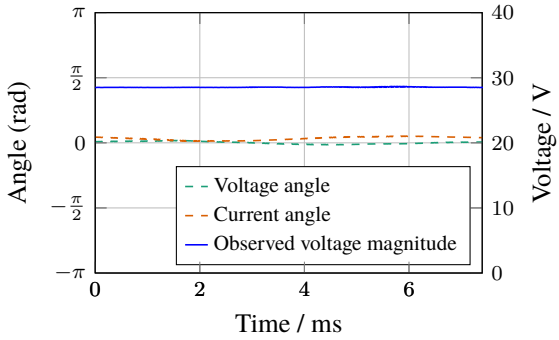


Figure 6.25: Internally observed voltage magnitude, and voltage and current angles of the presented controller

the second and fourth harmonic of the output current. The distribution of the currents is however not ideal, for the reasons stated above. It is also evident that while the harmonic current is significantly smaller in battery 1 than in the others—due to the shared neutral point design—it is not zero as predicted (according to eq. (4.12)). This is likely due to the fact that the impedance to the adjacent batteries in the same phase is significantly smaller than the impedance to the other batteries in the neutral point, as a result of the large mechanical dimensions.

The comparison to the DFT of the same currents without mTHI, shown in fig. 6.24 (b), validates the improvement caused by the mTHI at this operating point. While the spreading of the oscillating energy over two frequencies reduces the rms current of the batteries, the fact that more battery current now has a higher frequency also reduces the heat generation in the cells as more current passes through the DLC and less current causes charge-transfer.

To validate the performance of the observation of the controllers parameters, fig. 6.25 shows the observed voltage and current phase angle as well the voltage magnitude. Despite the fact that the sensors are only used in a small fraction of their measurement range, the controller is able to track the necessary parameters well. It should be noted that because these values were recorded with a serial logging tool in the FPGA, only a smaller time frame can be recorded than in the previous measurements performed using an oscilloscope.

Figure 6.26 shows the output voltage and measured current, as it is calculated by the control scheme on the FPGA. The output voltage reference closely follows the

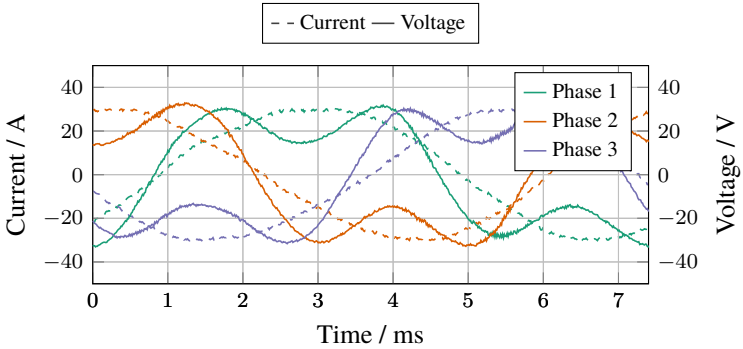


Figure 6.26: Internal controller values for the output voltage and current of all three phases. The high-frequency noise in the voltage is the result of the relatively low accuracy of the CORDIC algorithm.

idealised shape shown in fig. 5.4. Due to the limited size of the FPGA, the accuracy of the angles calculated with the CORDIC algorithm were chosen to be 10 bit. This causes some jitter in the output voltage, resulting in non-smooth waveforms. Since the output voltage is used as the input to the subsequent DSM—acting as a noisy low-pass filter—these high-frequency oscillations are not present in the voltage of the converter and do not impact it's performance.
Figure 6.27 shows the functionality of the proposed control scheme at high output voltages close to the modulation limit. Due to the high output voltage at a speed of 800 min^{-1} the amplitude of the injected voltage is decreased, as presented in section 5.2.2.1. The current remains well controlled since the mTHI does not affect the current control or reduce its available modulation range.
In addition to the control of the converter to minimise the SM batteries' rms current, this section demonstrates how the internal converter control allows the SoCs to remain balanced across the converter. Using the model-predictive balancing scheme developed by Merz [S1] in their Master's thesis, fig. 6.28 shows the SoCs of all converter SMs over a period of 250 s. The balancing scheme is implemented in succession of the DSM and chooses the module states based on the desired voltage level. Figure 6.28 (a) shows the absolute SoCs while fig. 6.28 (b) shows the deviation of each SM's SoC from the mean SoC of all SMs.
The experiment is started so that the SoCs have an unrealistically high SoC variation at $t = 0\,\mathrm{s}$, verifying that balancing is ensured even in extreme cases. The operating point is identical to fig. 6.22. It can be clearly seen that the controller

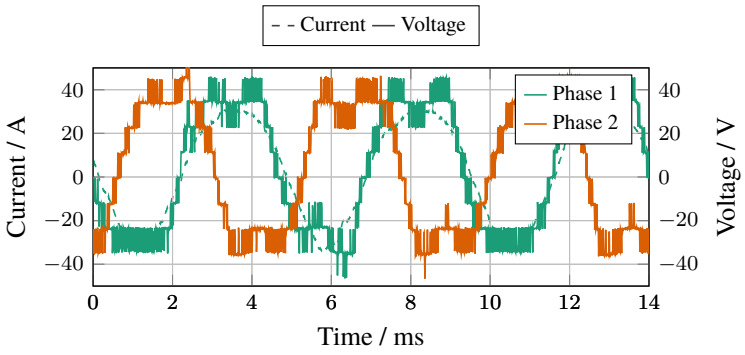
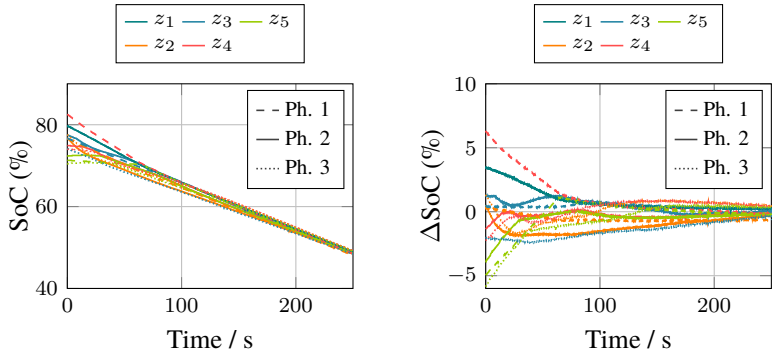


Figure 6.27: Output voltage and current of the presented controller at high output voltage and a motor speed of 800 min^{-1}



(a) Absolute SoC

(b) Difference to mean SoC

Figure 6.28: Absolute SoC and SoC difference for all SMs when starting from a state of severe imbalance. The control scheme is able to reduce the imbalance to within the resolution of the SoC measurement.

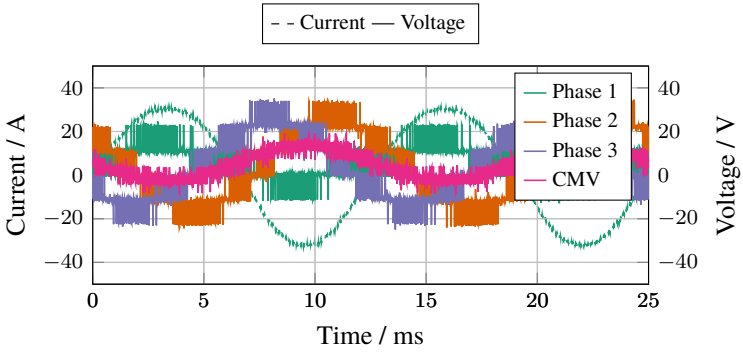


Figure 6.29: Output voltage and current using BVI to balance the average SoC of the phases. For this simulation, phase 1 has a significantly lower SoC than the others.

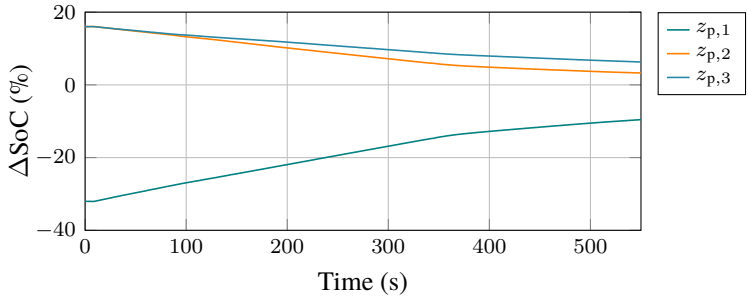


Figure 6.30: Average phase SoC when the BVI is used to balance the phase SoCs

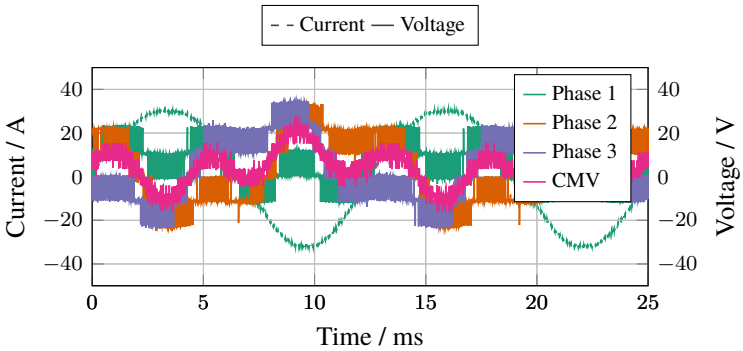


Figure 6.31: Output voltage of the converter simultaneously using mTHI to minimise the batteries' rms current and BVI to balance the average phase SoCs.

controls the SoCs well and reduces the imbalance to the resolution at which the SoCs are transmitted. This is achieved without using any of the available CMV for balancing, as the CMV is dictated by the mTHI.

In addition to balancing the SMs' SoCs within a phase using the model-predictive balancing control by Merz, the phase SoCs are balanced using the proposed BVI. This functionality is presented in fig. 6.29 and fig. 6.30, which show the converter outputs and the mean SoC of each phase, respectively. Both recordings were made at the same operating point, at $300\,\mathrm{min}^{-1}$ and a torque of $20\,\mathrm{N\,m}$. To demonstrate the phase-balancing, the SMs of phases 1, 2, and 3 have an SoC of 30%, 90%, and 90%, respectively. There is no mTHI implemented for this measurement.

Figure 6.29 shows how a CMV injected in the opposite phase of the voltage in phase 1. This reduces the power delivered by this phase while increasing the power delivered by the other phases allowing the SoCs of the phases to equalise, as shown in fig. 6.30.

Combining the previously presented control mechanisms, fig. 6.31 shows the outputs of the converter while both BVI and mTHI are active. The operating point is the same as in fig. 6.29, except that mTHI is used to reduce the cells' rms current.

It can be seen that both the mTHI and the BVI can be used concurrently to manipulate the output voltage of the converter, without impacting the current control's ability to control the currents to their setpoints. At this operating point, the amp-

litude of the mTHI is $a_3 = 0.5$, while the BVI fully utilises the remainder of the available modulation range to balance the phases. If the output voltage of the converter is increased, the amplitude of the BVI decreases. At no point is the available modulation range of the converter reduced by either injected CMV.

The experimental validation has presented the verification of the converter analysis in chapter 3 and proven the performance of the control scheme derived and introduced in chapter 5. On a lab-scale prototype, the control scheme was implemented at a sampling rate of 80 kHz on an FPGA and validated in the operating range of the test bench. It was shown that a common voltage injection at the frequency of the third harmonic of the output voltage (mTHI) can significantly reduce the batteries' rms current in operation without affecting the performance of the converter. Furthermore, a subsequent injection at the output fundamental frequency is generated and injected to balance the energy stored in each phase of the converter.

6.3 Discussion

In this validation, the various analyses and control methods presented in this work have been verified in both simulation and experiment. Due to restrictions in the test hardware, the majority of the validation of the operating characteristics of the MMSPC are presented in simulation.
First, the basic validation of the analysis was presented, in which the battery currents are analysed both for the MMSPC and CHB.
The general form of the currents corresponds well to the theory of chapter 3, which declares that two sinusoids at twice and four times the output frequency comprise the battery currents, depending on the amplitude of the third harmonic of the output voltage. Verifying the considerations of how well the current can be distributed in section 4.2, the MMSPC is shown to be far superior in ensuring the currents are distributed evenly when all other parameters are held equal.
Frequency analysis of the SM currents then confirms the distribution of currents depending on their frequency, and shows that the DLC of the lithium-ion battery is well suited to buffer the AC content of the SM current from the batteries' charge transfer processes. While it has not been proven conclusively in scientific literature, using this effect may reduce the degradation rate of lithium-ion batteries.
The impact of the number of SMs on the distribution of the current as well as the battery losses is then verified against the analysis of the MMSPC design consid-

erations presented in section 4.2. It is shown that the presented analysis reliably predicts the effect of the balancing method and it's performance function J_N on the battery current distribution, and that this is a predictor of battery losses.
While the aforementioned results have a general validity for the behaviour of the MMSPC and do not vary greatly with the chosen semiconductors or battery parameters, the analysis of the following results must always consider that they are specific for the chosen semiconductors and batteries and can vary strongly as a result of these choices. While the 2L and multilevel converters are more difficult to directly compare quantitatively due to the different type of semiconductor used in both, the multilevel converters use the same semiconductors and batteries, making their direct comparison valid.
By investigating the limits of the operating area of the converters over the output power factor, the analysis of the differences in the converters' boundaries is confirmed. It is shown that the 2L converter is far superior to the cascaded alternatives, especially at low power factors.
The investigation of the efficiencies of the converters confirms the analysis of chapter 3, and shows that the converters can be approximated well with the assumptions discussed in chapter 3, with the exception of the CHB. The CHB is shown to perform significantly worse than the MMSPC for otherwise similar conditions, as it cannot distribute the current between the SMs well in the short term. The improved distribution in the MMSPC is enabled by the use of the parallel mode, leading to lower losses overall, as the losses are proportional to the battery current squared. Drive cycle analysis corroborates the observation that the cascaded converters are especially suited to applications where frequent low-load operation is possible, and the ability of the presented control scheme to significantly reduce the battery losses of the multilevel converters is shown.
Following the validation of the analysis through simulation, the experimental verification focusses on the implementation of the converter and the control scheme to prove their feasibility in a laboratory prototype. For this investigation, an MMSPC converter was designed and built to drive an automotive PMSM from a modern series-production EV. The prototype allows the converter and the presented control scheme to be implemented, and provides necessary safety and debugging features to investigate any aspect of the system.
The experimental results show that the analysis and the simulation results correspond well to the real-life prototype. Control of the converter, based on the control scheme analysed in chapter 5, is performed on an FPGA in real time at a control frequency of 80 kHz. The control scheme is able to use the mTHI to reduce the batteries' rms currents, while using a second injected voltage to balance imbalances of the phase SoCs. It is also shown that the SoCs are balanced

well within the phases based on a model-predictive control framework, and that all aspects of the control scheme work simultaneously to control the converter.
In summary, this chapter validates the tools provided by the analyses presented earlier in this work, which allow the MMSPC to be analysed and compared to conventional converters, without the need to perform detailed simulations. Furthermore, the novel control scheme based on two simultaneous, cascaded CMV injections, is shown to work as predicted to improve the MMSPC's efficiency and allow balancing.
While this validation provides the groundwork for the investigation of the MMSPC and its comparison to state-of-the-art multilevel and 2L converters, an abundance of possible further investigations exist. For example, the trade-off between efficiency and converter SoC balancing can be investigated analytically or empirically, to determine where the optimum is for a specific use case. This work has been continued at the ETI by Merz et alia in recent publications [E4]. Furthermore, the interaction of mTHI and BVI has not been fully analysed and provides an interesting topic of further investigation. In particular, the extent to which the battery current reduction is effective when BVI is introduced is unclear.

Chapter 7

Conclusion

In this thesis, the MMSPC has been analysed from various viewpoints in an EV application, and compared to the conventional solution of a 2L converter, as well as the similar CHB. Throughout the analysis, the power electronics and the EV battery were treated together, to break down their effectiveness in providing power for an electric load, the PMSM. Simulative and experimental results are shown, which validate the analyses presented in the chapters 3 and 4, as well as the proposed controller in chapter 5.

While the MMSPC provides high output voltage quality and modularity in design, its most fundamental flaw in the EV application is the fact that its use results in higher battery rms current than in a comparable 2L converter. This difference has been quantified based on the application parameters, showing the MMSPC batteries' rms current is over 22% larger. Significantly, this drawback of the MMSPC becomes more severe as the load power factor decreases.

As a result of this, the battery efficiency of the MMSPC is lower than the 2L, as is its achievable output voltage. Nonetheless, due to the lower semiconductor losses, the efficiency over a modern EV drive cycle can be higher than for the reference 2L converter. The efficiency is significantly improved by the new proposed control scheme, which uses the CMV of the converter to reduce the batteries' currents. A third harmonic voltage induces an additional oscillating current in the batteries, at four times the output frequency, while reducing the oscillating current at twice the output frequency. This reduces the total rms current seen by the battery, by ca. 9% at unity power factor, and up to ca. 30% at a power factor of 0.

In comparison to the CHB, it was shown that the MMSPC allows significantly greater efficiency due to the parallel mode. The parallel mode distributes the load current almost equally across the SMs, reducing the overall rms current. At the same time, the parallel mode limits the flexibility of the converter to choose which SMs are loaded more heavily, and impedes the ability of the converter to balance the SMs.
In summary, the MMSPC can provide an alternative to conventional converters for applications such as EV powertrains, despite some disadvantages. It may however be more suited in applications where there are no auxiliary loads and there is no requirement for the control of multiple three-phase loads, such as battery energy storage system (BESS).

Glossary

Abbreviations

2L	two-level
3L	three-level
AC	alternating current
ADC	analogue-to-digital converter
AFE	active front-end
AGM	absorbent glass mat
BESS	battery energy storage system
BVI	balancing voltage injection
CAN	Controller Area Network
CHB	cascaded H-bridge
CMV	common-mode voltage
CORDIC	Coordinate Rotation Digital Computer
DC	direct current
DCDC	DC-to-DC
DFT	discrete Fourier Transform
DLC	double-layer capacitance
DoF	Degree of Freedom
DSM	delta-sigma modulation
DSP	digital signal processor
EC	equivalent circuit
ECM	equivalent circuit model
EIS	electrochemical impedance spectroscopy
EMC	electromagnetic compatibility
EMI	electromagnetic interference

ESR	equivalent series resistance
ETI	Elektrotechnisches Institut
EV	electric vehicle
FOC	field-oriented control
FPGA	field-programmable gate array
GaN	gallium nitride
gcd	greatest common divisor
HMI	human-machine interface
HMK	*Hochleistungsmodulatorkarte* (high-performance modulator card)
HVDC	high voltage direct current
ICE	internal combustion engine
IGBT	insulated-gate bipolar transistor
IM	induction motor
LPF	low-pass filter
LUT	lookup table
MHF	Modular High-Frequency Converter
MMC	Modular Multilevel Converter
MMSPC	Modular Multilevel Series Parallel Converter
MOSFET	metal-oxide-semiconductor field-effect transistor
MPC	model predictive control
mTHI	modified third harmonic injection
MTPA	maximum torque per ampere
NEDC	New European Drive Cycle
OCV	open-circuit voltage
PCB	printed circuit board
PHEV	plug-in hybrid electric vehicle
PI	proportional-integral
PMSM	permanent magnet synchronous machine
PWM	pulse width modulation
rhs	right-hand side
rms	root mean square
SD	standard deviation
SEI	solid-electrolyte interphase
Si	silicon
SiC	silicon carbide
SM	sub-module

SoC	state of charge
SoH	state of health
STAT-COM	static synchronous compensator
SVM	space-vector modulation
THI	third harmonic injection
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VSC	voltage source converters
WLTP	Worldwide Harmonised Light-Duty Vehicles Test Procedure

Symbols

$\vec{B_q}$	Imbalance vector of a phase indicating which SMs are charged higher and lower than the mean, for each imbalance possibility q
$\vec{C}$	Current vector analogous to $\vec{B}$ showing how the current is distributed in a phase
$C_{\text{b,RC}}$	Capcitance of an RC element of a SM battery
C_{cell}	Current capacity of a battery cell
$\vec{C_\epsilon}$	Equivalent current vector
C_{m}	Module Capacitance
C_{ph}	Required current capacity of an MMSPC phase
$\vec{D}$	Matrix consisting of all available current vectors $\vec{C}$ for a specific output level
E_{bat}	Energy capacity of a battery
E_{cell}	Energy capacity of a battery cell
E_{mot}	Required energy delivered to the electric motor for a specific drive cycle
$E_{\text{off,D}}$	Turn off energy of a diode at nominal voltage and current
$E_{\text{off,sc}}$	Turn off energy of a transistor at nominal voltage and current
$E_{\text{on,D}}$	Turn on energy of a diode at nominal voltage and current

$E_{\text{on,sc}}$	Turn on energy of a transistor at nominal voltage and current
E_{par}	Loss due to parallelisation
$E_{\text{sw,nom}}$	Energy of switching loss of a semiconductor at nominal voltage and current
$E_{\text{sw,2L}}$	Energy of switching loss of a 2L semiconductor at nominal voltage and current
$E_{\text{sw,ML}}$	Energy of switching loss of a split-DC half-bridge at nominal voltage and current
F_{Sa}	Voltage safety factor for converter design
H	Number of half-bridges on either SM side
$\hat{I}$	Magnitude of the output current
$\hat{I}_{\text{max}}$	Maximum magnitude of the output current
$\hat{I}_{\text{max,2L}}$	Maximum magnitude of the output current for a 2L converter
$\hat{I}_{\text{max,ML}}$	Maximum magnitude of the output current for the split-DC converters
$J_{\text{B},q}$	Cost function of the balancing performance of equivalent current vector $\vec{C}_{\epsilon}$, for each imbalance possibility q
J_N	Performance function of the number of sub-modules
L_{b}	Inductance of a SM battery
L_{cell}	Inductance of a battery cell
L_{par}	Inductance of two parallel=connected SMs
M	Number of modules in series in a phase
N	Number of SM per phase.
N_{par}	Number of SM that can be switched in parallel
P	Acitve power
$P_{\text{bat,loss}}$	Loss power of a battery
$P_{\text{cond,loss}}$	Conduction losses of a semiconductor
$P_{\text{cond,loss,MMC}}$	Semiconductor conduction loss of the split-DC converters
$P_{\text{sw,2L}}$	Switching power of a 2L converter
$P_{\text{sw,loss}}$	Switching losses of a semiconductor
$P_{\text{sw,ML}}$	Switching power of a multilevel converter

R_{b}	Resistance of a SM battery
$R_{\mathrm{b,2L}}$	Battery resistance a 2L converter
$R_{\mathrm{b,DC}}$	DC resistance of a SM battery
$R_{\mathrm{b,RC}}$	Capcitance of an RC element of a SM battery
R_{cell}	Series DC-resistance of a battery cell
$R_{\mathrm{cell,par}}$	Equivalent series DC-resistance of a parallel group of cells
R_{Cm}	ESRof module Capacitance
R_{DS}	Drain-source on-resistance
R_{inner}	Inner resistance of a battery
R_{on}	IGBT or diode on-resistance
$R_{\mathrm{on,D}}$	2L converter diode on-resistance
$R_{\mathrm{on,FET}}$	Split-DC converter MOSFET drain-source on-resistance
$R_{\mathrm{on,IGBT}}$	2L converter IGBT on-resistance
R_{ph}	Resistance of a converter phase, assuming negligible semiconductor on-state resistances
$\vec{S}_{\mathrm{p}}$	Variable to encode the switching state of the phase's SMs
T	The set of multiples of 3 greater than 3 (6,9,12,...)
$\hat{U}$	Magnitude of the output voltage
$U_{\mathrm{DC,max}}$	Maximum output voltage of a converter phase
U_{f}	IGBT or diode forward voltage
$U_{\mathrm{f,D}}$	2L converter diode forward voltage
$U_{\mathrm{f,IGBT}}$	2L converter IGBT forward voltage
$\hat{U}_{\mathrm{max}}$	Maxiumum magnit maximum modulation indexe of the output voltage
a_3	Amplitude of the modified third harmonic injection
$a_{\mathrm{BVI,max}}$	Maximum amplitude of BVI
a_n	Amplitude of an n^{th} harmonic voltage injection
c_{bat}	Current capacity of a battery (in units of charge)
f	Frequency of the load
f_{2L}	Switching frequency of the 2L converter
f_{ML}	Switching frequency of a split-DC converter half-bridge

f_{SC}	Switching frequency of a semiconductor
$i_{\mathrm{2L,nom}}$	Nominal DC current of the 2L converter semiconductors
$i_{\mathrm{b},n}$	Battery current of module n
$i_{\mathrm{b,2L}}$	Total battery current of a 2L converter
i_{bat}	Current of a battery
$\breve{i}_{\mathrm{b,eq}}$	Equivalent rms battery current of module n, when comparing to single-DC converters
i_{Cb}	Current through modelled battery double-layer capacitance
i_{cell}	Maximum current of a battery cell
i_{Cm}	Current through SM capacitance
i_{D}	2L converter diode current
i_{IGBT}	2L converter IGBT current
$i_{\mathrm{m},n}$	Module current of module n
$i_{\mathrm{ML,nom}}$	Nominal DC current of the split-DC converter semiconductors
i_{OCV}	Current through the modelled batteries open-circuit voltage
$i_{\mathrm{p},i}$	Current of phase i
$i_{\mathrm{SC,nom}}$	Nominal current of a semiconductor
i_{SC}	Current through a semiconductor
i_{sw}	Module switching current ripple
$i_{\mathrm{sw,2L}}$	Switching current of a 2L converter half-bridge
$i_{\mathrm{sw,ML}}$	Switching current of a multilevel converter half-bridge
k_{R}	Proportionality constant of battery resistance
k_{ρ}	Proportional gain of phase SoC control
m	Modulation index
$n_{\mathrm{b,par}}$	Number of cells in parallel per SM
$n_{\mathrm{b,ser}}$	Number of cells in series per SM
$n_{\mathrm{p},r}$	Number of parallel groups r in a phase
n_{σ}	Number of unique permutations of the largest symmetric group in $\vec{S}_{\mathrm{p}}$
p_r	Number of parallel SMs (width) of parallel group r, where $r \in \{1,2\}$

q	Numeric index of a possible imbalance vector $\vec{B}$
t	Time
$u_{\text{2L,nom}}$	Nominal voltage of the 2L converter semiconductors
$\vec{u}_{\text{abc}}$	Motor control output voltage in abc-coordinates
$u_{\text{b},n}$	Battery voltage of an SM
$u_{\text{b,2L}}$	Battery voltage of a 2L converter
u_{bat}	Voltage of a battery
u_{BVI}	The voltage injected by the BVI
$u_{\text{BVI},\alpha\beta}$	The voltage injected by the BVI in the $\alpha\beta$-frame of the phase SoCs
u_{c}	Terminal voltage of a cell
u_{cell}	Nominal voltage of a battery cell
u_{cmv}	Common-mode voltage
$\vec{u}_{\text{dq}}$	Motor control output voltage in abc-coordinates
u_{load}	Load voltage
$u_{\text{ML,nom}}$	Nominal voltage of the split-DC converter semiconductors
$u_{\text{OCV,2L}}$	Open-circuit battery voltage of a 2L converter
u_{OCV}	Open-circuit battery voltage of a SM
$u_{\text{p},i}$	Voltage of phase i
u_{SC}	Voltage over a semiconductor
$u_{\text{sw,ML}}$	Switching voltage of a multilevel converter half-bridge
u_{THI}	The voltage injected by the optimal mTHI control
z_n	SoC of the SM n
$z_{\text{p},i}$	SoC of phase i (mean of the SMs' SoCs)
$\Delta\%$	Percentage point
Δu_{par}	Voltage perturbation due to parallelisation
$\vec{\Theta}$	Vector of the ratios at which different current vectors $\vec{C}$ are used to generate an equivalent current vector $\vec{C}_\epsilon$
$\delta i_{\text{b},n}$	Relative deviation of battery current of SM n
δi_{p}	Average relative deviation of the battery currents in a phase

η_{load}	Efficiency of the converter system over the load cycle
θ_{rot}	Angle of rotor permanent magnet flux linkage
θ_{u}	Angle of converter voltage
$\vec{\rho}$	Space vector of phase SoC deviation
ϕ_3	Phase of the modified third harmonic injection
ϕ_c	Phase of output current
ϕ_n	Phase of an n^{th} harmonic voltage injection
ω	Angular frequency of the load

List of Figures

List of Tables

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