Surface-Supported Metal-Organic Framework as Low-Dielectric-Constant Thin Films for Novel Hybrid Electronics

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The miniaturization of electronic devices highlights the need for robust low-κ materials as an alternative to prevent losses in the performance of integrated circuits. For it, surface-supported metal-organic frameworks (SURMOFs), a class of porous-hybrid materials, may cover such a demand. However, the high-intrinsic porosity makes determining the dielectric properties difficult and promotes the integration of SURMOF thin films. Here, the integration of ultrathin HKUST-1 SURMOF films into a 3D functional device architecture using soft-top electrical contacts is addressed. In this novel approach, the device structure assumes an ultracompact capacitor structure allowing determine the dielectric properties of porous thin films with considerable accuracy. A low-κ value of 2.0 ± 0.5 and robust breakdown strength of 2.8 MV cm^{-1} are obtained for films below 80 nm. The spontaneous self-encapsulated structure provides a footprint-area reduction of up to 90% and yields good protection for the SURMOF toward different hazardous exposure. Finite-element calculations compare the HKUST-1 performance as dielectric layer with well-established insulators applied in electronics (SiO_2 and Al_2O_3). The possibility of integration and miniaturization of HKUST-1, combined with their interesting insulating properties, place this hybrid material as a robust low-*k* dielectric for novel electronics.

1. Introduction

The continuous development of electronics pushes the need for novel materials, fabrication processes, and architectures. For instance, the device's parallelism and the fabrication process scalability have enabled the fabrication of highly dense sets of transistors into small areas, enhancing the performance and complexity of integrated circuits (ICs).[1,2] In modern ICs, the complexity becomes visible as the distance between interconnect structures get smaller.[3] Currently, the multilevel interconnect systems employed in CMOS have inter distances below 50 nm,[4] which might compromises the performance of the ICs. The impact rises from the nonzero resistance (*R*) and the inherent parasitic capacitance (C_p) between neighboring interconnects separated by interlayer dielectrics (ILDs), inducing cross-talk noise, affecting the switching speed and the power consumption of ICs.[5,6] Both *R* and C_p depend on the distance between interconnects and ILD used as an insulating layer.[3] Thus, to continue electronics scaling-down, state-of-the-art strategies have been proposed, focusing on the metals with enhancement conductance (e.g., Cu, Co, and Ru)[7–12] and the replacement of traditional dielectrics for different organic materials and porous oxides with low-dielectric-constant ($\kappa < 2.4$).[3] While organic materials present low-κ owing to their limited polarizability, the oxide layers have their low-κ caused by large free volumes.[3,13] In both cases, intrinsic disorder and high porosity lead to poor thermal properties,[14–16] where heat management is critical. Recently, advances in boron nitride placed 2D materials as a promising class of materials to be considered for low-κ dielectrics.[17,18] However, the

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current lack of suitable 2D insulators and integration difficulties into silicon (Si) technology limit new advances.[19]

According to the 2020 International Roadmap for Devices and Systems,[20] porous-hybrid materials, specifically metal-organic frameworks (MOFs), rise as promising candidates for low-κ dielectrics. These hybrid structures, composed of metal ions connected by organic linkers, enable a huge number of possible combinations, with more than 100 000 compounds already characterized experimentally.[21] These reticular compounds have been applied to a wide range of strategic applications, including supercapacitors,[22] biosensors,[23] catalysis,[24] drug delivery,[25] and photocatalytic water splitting,[26] to mention a few. Furthermore, MOFs possess many intrinsic properties highly sought-after for use in interconnects, such as low-κ,[27] good mechanical flexibility,[21] and tunable porosity.[28] For low-κ dielectrics, the potential of MOFs was first premeditated by theoretical calculations.[29] Experimentally, strategies mostly involving pellet structures have been used to prepare devices aiming to investigate the dielectric properties of MOFs.[30–37] For example, Scatena et al. reported an experimental study correlated with theoretical results on the HKUST-1 (Hong Kong University of Science and Technology) dielectric constant (κ) for potential electronic applications.[36] It was observed good accordance between the κ of the guest-free HKUST-1 pellet (1.72) and the density functional theory (DFT) calculated (1.74). Babal et al. also described the fabrication of pellet structures with HKUST-1 powder as the dielectric by performing impedance spectroscopy in different temperatures and pressure conditions.[37] The pressure applied to the pellet electrodes produced a considerable variation on the κ, varying from 2.42 at 0.5 t to 4.88 at 10 t pressure, evidencing that MOF powders are difficult to shape for device integration. Recently, zeolitic imidazolate framework (ZIF) structures were employed as gap-filling low-κ dielectrics for 45 nm half-pitch fork-fork capacitors. Such devices exhibit competitive performance with the state-of-the-art porous organosilica dielectrics.[38]

Although these advances demonstrate the potential of MOFs for applications in low-*k* dielectrics, a significant obstacle is the fabrication of monolithic, high-quality MOF thin films. In this context, Surface-Supported Metal-Organic Frameworks (SURMOFs) prepared using layer-by-layer methods offer unique opportunities.[39] This approach provides MOF films with well-controlled features, including thickness, homogeneity, morphology, and defect density, with improved adhesion onto desired substrates.[40] In addition, the crystallinity can be deterministically tailored on both metallic and insulating surfaces by selecting the self-assembled monolayer (SAM) chain length.[41] These unique properties project exciting new possibilities for integrating and developing novel electronic devices.[42–44] Nevertheless, their potential as low-κ dielectrics has not been entirely lifted yet. In this context, Redel et al. report a systematic spectroscopic ellipsometry study on Cu-BDC and HKUST-1 SURMOFs epitaxially grown on functionalized Si substrates and using the obtained refractive index (n), they predicted low-κ values of 1.13 and 1.7, respectively.[45] Also, as low-κ dielectrics, the HKUST-1 SURMOF has been integrated into organic-field effect transistors for modifying the dielectric layer, returning good performances.[46] However, a detailed investigation of SURMOFs dielectric properties has not been reported to date. Several limitations on measurement techniques and device architectures hinder determining their κ values accurately. Among the main difficulties, the reliable fabrication of electrically conducting top contacts and the full integration in a suitable manufacturing platform are the most significant challenges owing to their high intrinsic porosity and ultrathin thicknesses. Simple evaporation of metallic patches using, e.g., physical vapor deposition must be abandoned due to the possibility of interdiffusion of metal atoms into the film during the deposition process. As regards top contact formation suitable for dielectric investigation, to the best of our knowledge, the only set of reliable data on electrical properties was obtained using the mercury drop method,[47] an approach not suited for SURMOF device integration.

In this sense, we report the integration of ultrathin HKUST-1 SURMOF heterojunctions in a 3D ultracompact capacitor structure using soft-top electrical contacts to investigate the dielectric properties. Such a device architecture is based on self-wound metallic nanomembranes (viz. rolled-up nanomembranes, r-NMs),[48] providing a damage-free, reliable, and soft-top electrical contacts onto SURMOF surfaces. The low-κ value of 2.0 ± 0.5 is accessible for different integrated SURMOF thicknesses (from 20 to 80 nm) by modeling the impedance characteristics as a function of frequency using electrical equivalent circuit models. The potential of the HKUST-1 SURMOF as ILDs is demonstrated by performing finite-element modeling (FEM) simulations and compared with traditional dielectrics widely used in the semiconductor industry (i.e., SiO_2 and Al_2O_3).

The primary motivations of this work are the promising prospects SURMOFs may offer for new electronics and the lack of experimental reports regarding their dielectric properties at the nanoscale thicknesses. The results obtained herein provide a step forward to the fundamental characterization of ultrathin SURMOFs heterojunctions as potential low-κ dielectrics. The implemented approach circumvents the inherent artifacts from conventional metal deposition methods (e.g., thermal evaporation) and substantially reduces the device footprint area (as mentioned in the abstract) by up to 90%. Furthermore, this is the first time SURMOF films are integrated into a 3D functional device architecture.

2. Results and Discussion

Figures 1a,b illustrates the device concept used to investigate the dielectric properties of the HKUST-1 SURMOF heterojunctions. Before the rolling-up process, the equivalent circuit that better represents the architecture corresponds to a conventional parallel-plate capacitor (p-Cap), having top and bottom electrodes sandwiching a 10 nm thick Al_2O_3 film. By the selective removal of a sacrificial layer based on germanium oxide (GeO_x), the capacitor heterostructure curls up. The outmost layer of the strained tri-metallic layer touches the HKUST-1 film from the top, creating a hybrid r-NM-based capacitor (h-Cap). Figure 1c shows the layer sequence for each architecture. A detailed description of device fabrication can be found in the Experimental Section and Figure S1 (Supporting Information). Also, examples can be found in previously reported works.[48–50] This rolled-up architecture allows a damage-free, reliable, and soft-top electrical contacts on the SURMOF layer. Furthermore, as the number of windings

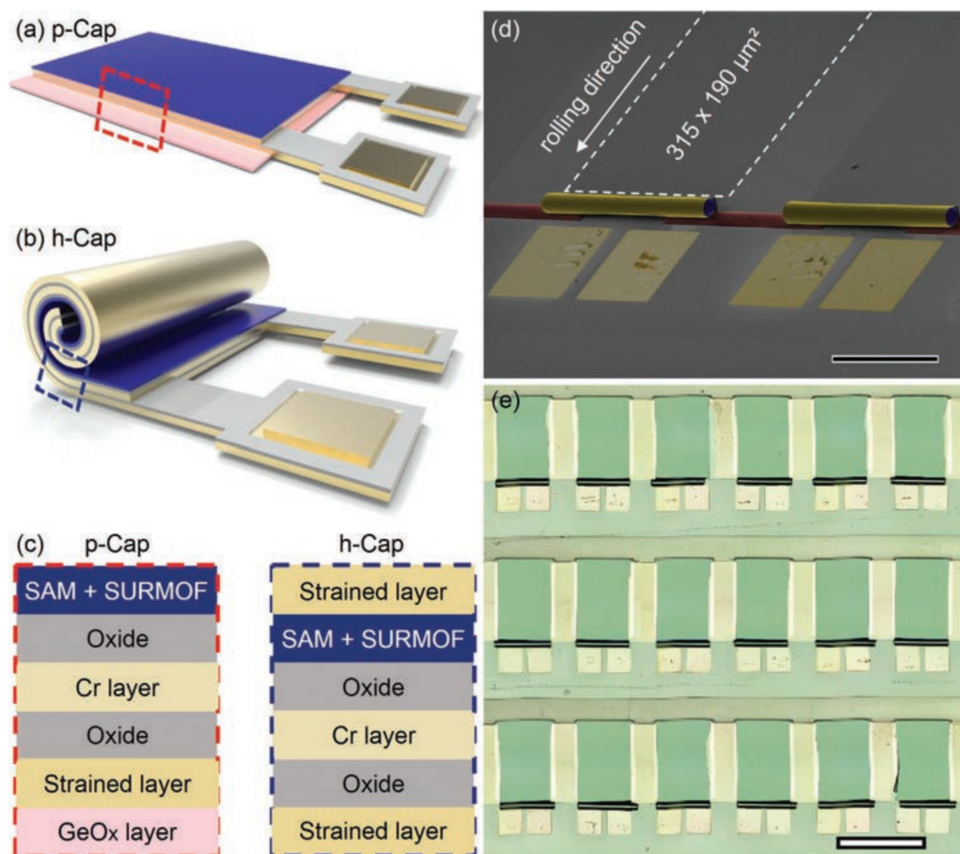

Figure 1. Device's layout and layer composition. a,b) Illustration of the p-Cap and h-Cap device structures. The roll-up process starts after the GeO_x dissolution; the soft and self-adjusted top electrical contact on the SURMOF layer is accomplished as the outermost surface of the strained tri-metallic layer curls. c) Respective layer sequence for the regions indicated in the dotted rectangles for p-Cap and h-Cap. d) SEM image for h-Cap devices after rolled-up. e) LSCM image from an array of 18 devices, showing the reproducibility and scalability of the fabrication process. Scale bars correspond to 100 and 300 µm, respectively.

increases through the roll-up process, the SURMOF layer is compacted into the tubular structure, enabling additional protection against hazardous agents that can eventually damage its integrity.[51] The number of windings can be controlled by accessing the capacitor dimensions, the strain configuration during the thin film deposition, and the SURMOF thickness.

Figure 1d shows the SEM (scanning electron microscopy) image of two h-Caps. The device footprint-area of 6×10^{-8} m^2 was reduced to 4×10^{-9} m^2 after five windings. The external tubular diameter is ≈20 µm, reducing ca. 90% of the occupied area. These values are similar to those reported for semiconducting molecular ensembles integrated into r-NM-based capacitors.[48,49] In Figure 1e,a 3D laser scanning confocal microscopy (LSCM) image shows an array of 18 fabricated devices. All devices were successfully rolled-up, evidencing the reproducibility and scalability of the fabrication processes based on conventional photolithographic methods. The high yield demonstrated here attests to a reliable and robust fabrication process, allowing profitable statistics of the obtained electrical data.[52]

Figure 2a shows the Grazing Incidence X-Ray Diffraction (GIXRD) pattern of the HKUST-1 SURMOF for different quasi-Liquid Phase Epitaxy (LPE) deposition cycles. The HKUST-1 was grown on top of the 10 nm thick Al_2O_3 film functionalized with a phosphonohexadecanoic acid (PHDA) SAM.[53,54] The diffraction patterns were obtained using a synchrotron radiation source. The step-by-step HKUST-1 SURMOF growth was performed using pre-established protocols (details in the Experimental Section and Figure S2, Supporting Information).[41–43] The principal (200) and (222) crystalline planes reflect a dynamic growth of the HKUST-1 SURMOF, with preferential orientation corresponding to [100] and [111] directions. As the SURMOF thicknesses increase, i.e., the number of deposition cycles, the film crystallinity increases, favoring the [111] direction. This behavior is consistent with previously reported,[41] where the preferential orientation changes could be controlled by either increasing the film thickness or changing the SAM chain length. Furthermore, the reduction in peak intensity observed for the 10-cycles grown samples is mainly attributed to the low film thickness (≈20 nm, Figure S3a,b, Supporting Information), making the diffraction patterning hard to detect.

The Atomic Force Microscopy (AFM) topography images for the thinner (10-cycles samples) and the thicker (40-cycles samples) HKUST-1 SURMOF films are shown in Figures 2b,c. The films have a homogenous surface without pinholes and significant agglomerates for 5 µm × 5 µm area. The surface roughness, corresponding to the root-mean-square (*Rq*), was found 10.4 ± 0.3 nm and 41.2 ± 8.3 nm, respectively. These values are

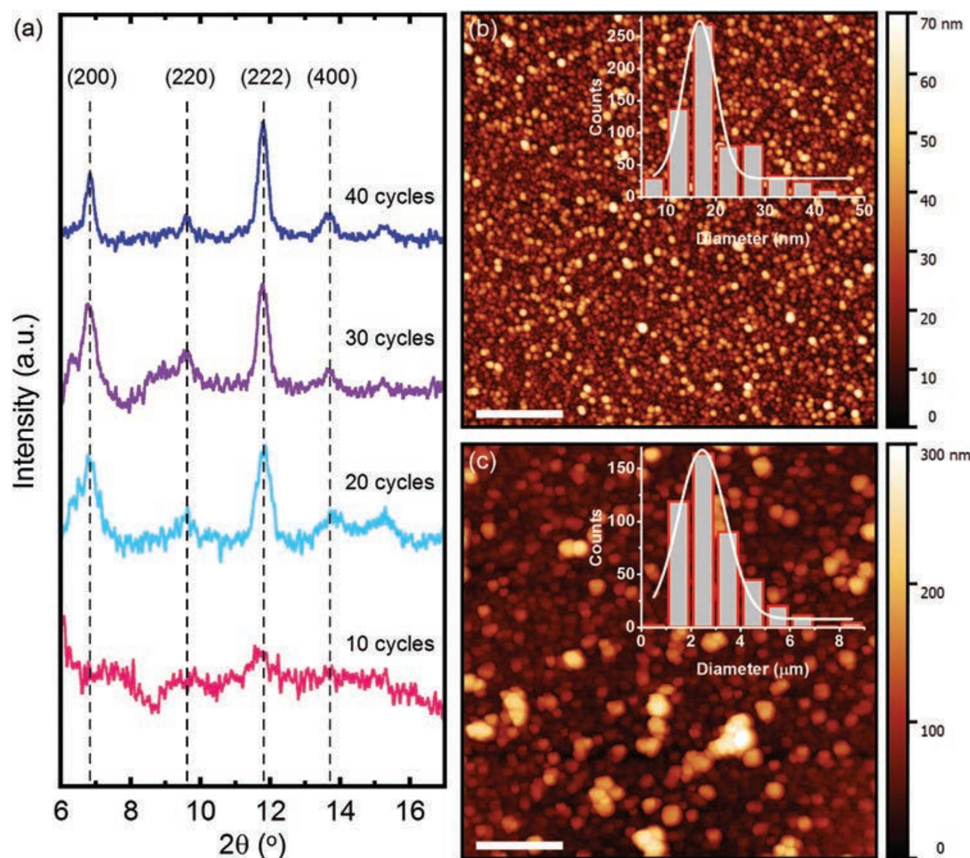

Figure 2. Structural and morphological characteristics of HKUST-1 SURMOF films. a) GIXRD pattern for different deposition cycles on functionalized Al_2O_3 surface. b,c) 5 μm × 5 μm AFM topography image of HKUST-1 SURMOF after 10 and 40 deposition cycles. Scale bars correspond to 1 μm. (inset) Equivalent histograms with the respective average particle sizes.

compatible with typical SURMOF films.[41] Parameters such as SAM chain length, temperature, humidity, and crystalline orientation of substrate also play an essential role in the SURMOF morphology.[41,55,56] The effective Al_2O_3 surface PHDA functionalization can be observed in the 1 μm × 1 μm AFM topography images from Figure S4 (Supporting Information). In Figure 2b (inset), the mean particle size is 16.5 ± 5.2 nm, while for Figure 2c, 2.4 ± 0.8 was obtained. Both histograms were plotted using data extracted from the images in Figure S5 (Supporting Information). The increase of *Rq* due to the particle size for thicker SURMOF films is coupled with the number of deposition cycles and the preferential growth directions observed in Figure 2a. Besides, the corresponding thicknesses for the related SURMOF films are around 20 and 80 nm, respectively, as shown in Figure S3 (Supporting Information).

HKUST-1 SURMOF films with different thicknesses were used to form standard metal/SAM-SURMOF/metal (MSM) parallel-plate capacitors, where the top electrode was made by thermal evaporation (see Figure S6, Supporting Information). The MSM devices were investigated via impedance spectroscopy in inert atmosphere conditions (N_2), and the SURMOF thicknesses were controlled using the number of deposition cycles (from 20 to 100). As the SURMOF film thickness reduces, the impedance measurements indicate an increased number of devices with a non-capacitive behavior—phase angle impedance (θ) >> −90°. For details, see the θ histograms in Figures S7 and S8 (Supporting Information). More than 80% of capacitors presented non-capacitive behavior for 20-cycles films, limiting the dielectric characterization of small HKUST-1 thicknesses in conventional MSM device structures. In this sense, the r-NM-based capacitor architecture becomes a powerful tool for determining the dielectric properties of damage-free SURMOFs thin films. Section S8 (Supporting Information) discusses the endurance of HKUST-1 SURMOF thin films to the fabrication process. Figure S9 (Supporting Information) shows XRD patterns for the film's integrity tests before and after exposure to the roll-up solution, revealing that the HKUST-1 structure is preserved.

Figure 3a,b shows θ and the capacitance values for MSM and h-Cap devices under the N_2 atmosphere (20-cycles HKUST-1 SURMOF films). While θ exhibits a capacitive behavior (≈−90°) for h-Caps (from 10^4 to 10^1 Hz), the values of θ for MSM devices vary considerably. Also, the error bars are substantially higher for MSM devices than for h-Caps, revealing the lack of reproducibility for MSM architecture. The corresponding capacitance characteristics for both configurations (Figure 3b) follow the same tendency observed by θ in Figure 3a. As shown in Figure 3c, the h-Cap architecture allowed us to measure the capacitive behavior for different SURMOF thicknesses from 10^4 to 10^1 Hz. The respective capacitance in the yellow region is

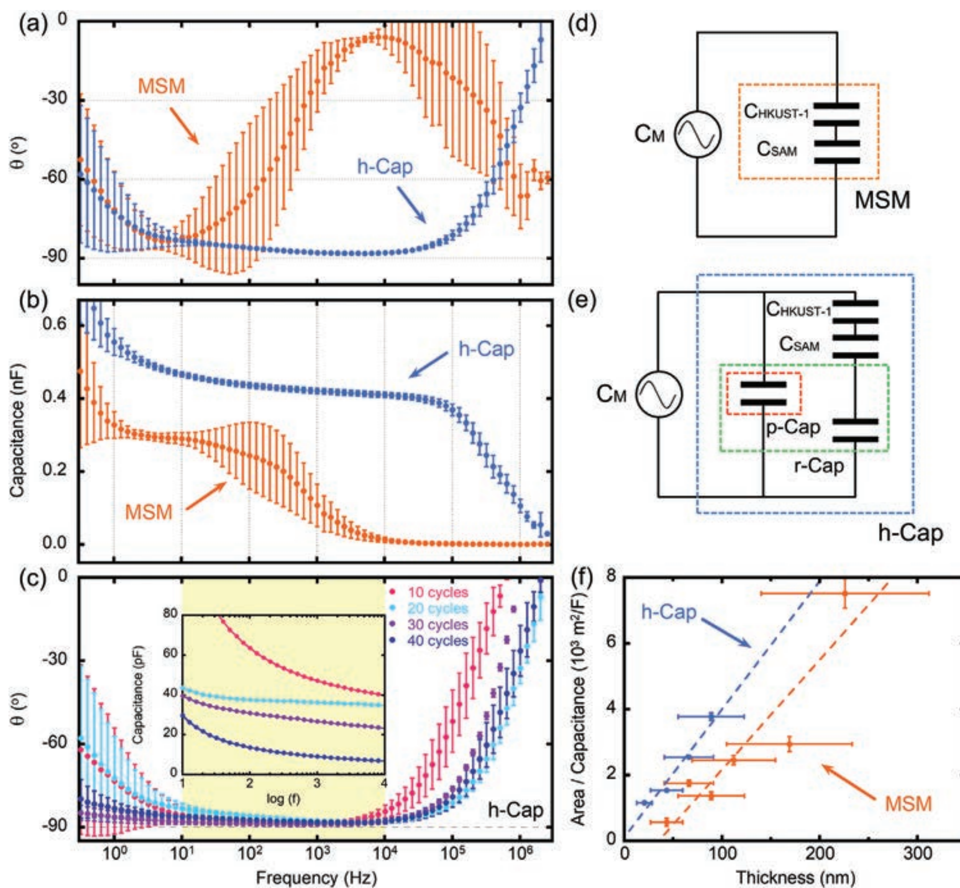

Figure 3. Impedance characteristics for MSM and h-Cap devices under N_2 atmosphere. a,b) Typical impedance θ and capacitance as a function of frequency for devices comprising 20 deposition cycles of HKUST-1 SURMOF films. c) θ as a function of frequency for h-Cap devices with different SURMOF deposition cycles. The highlighted region indicates the frequency range where the devices exhibit typical capacitor behavior; the inset shows the measured capacitance in this region. d,e) Equivalent circuit for MSM and h-Cap devices. f) Area/Capacitance as a function of HKUST-1 SURMOF thickness.

shown as an inset. Figure 3d,e presents the equivalent electric circuit for each architecture. This approach allows the determination of the dielectric properties of HKUST-1 SURMOF (see detail in Supporting Information, Section 9). The permittivity values were extracted from the angular coefficient of the linear regression from the plot Area/Capacitance versus thickness for both architectures, as shown in Figure 3f. The κ value of HKUST-1 is calculated following Equation (1)

$$\kappa = \frac{1}{\alpha.\varepsilon_0} \tag{1}$$

where α is the angular coefficient obtained from the data presented in Figure 3f, and ε_0 is the absolute dielectric permittivity of the vacuum. The linear regression coefficient (R^2) demonstrates a better agreement for the h-Cap devices (95%) than for MSM structures (86%). The fitted data delivers $\kappa = 2.0 \pm 0.5$ for the h-Cap and 3.4 ± 0.7 for MSM, with the error bars calculated by propagating the average values of five to twenty devices for different configurations. Both values agree with the results reported for bulk MOFs.[36,37,57]

The compacted tubular structure of h-Cap devices results from the layer's sequence and roll-up process. This feature is particularly interesting for hybrid and organic-based electronic devices, which degrade under hazardous agents.[58,59] Thus, taking this self-encapsulated characteristic as an advantage, we also evaluated the HKUST-1 SURMOF dielectric properties exposed to different volatile compounds and UV (λ = 365 nm) irradiation, as seen in Figure S10 (Supporting Information). HKUST-1 is a porous framework structure with a high surface area,[60] allowing diffusion of different molecules from the atmosphere into their pores. These molecules may induce different polarization effects, and UV irradiation may affect the organic linker. In the presence of an external applied electric field, both scenarios might result in distinct impedance responses. These effects can be seen for the MSM devices in Figure S10c,e (Supporting Information). However, for the h-Cap architecture, the access to the HKUST-1 SURMOF is blocked owing to the self-encapsulation. Apart from the minor variations in the dielectric response observed in Figure S10d,f (probably originated from small contributions of the outmost layers), the results for the tubular structure evidence a substantial improvement of the SURMOF layer protection compared with those obtained for MSM architecture. This is better elucidated in Figure S11 (Supporting Information), where the percentual θ variations in low frequencies are displayed for both device architectures. Furthermore, for 20 nm thick SURMOF films, θ values were fully preserved (Figure S12, Supporting Information)—indicating a possible increase in compactness of the h-Cap devices.

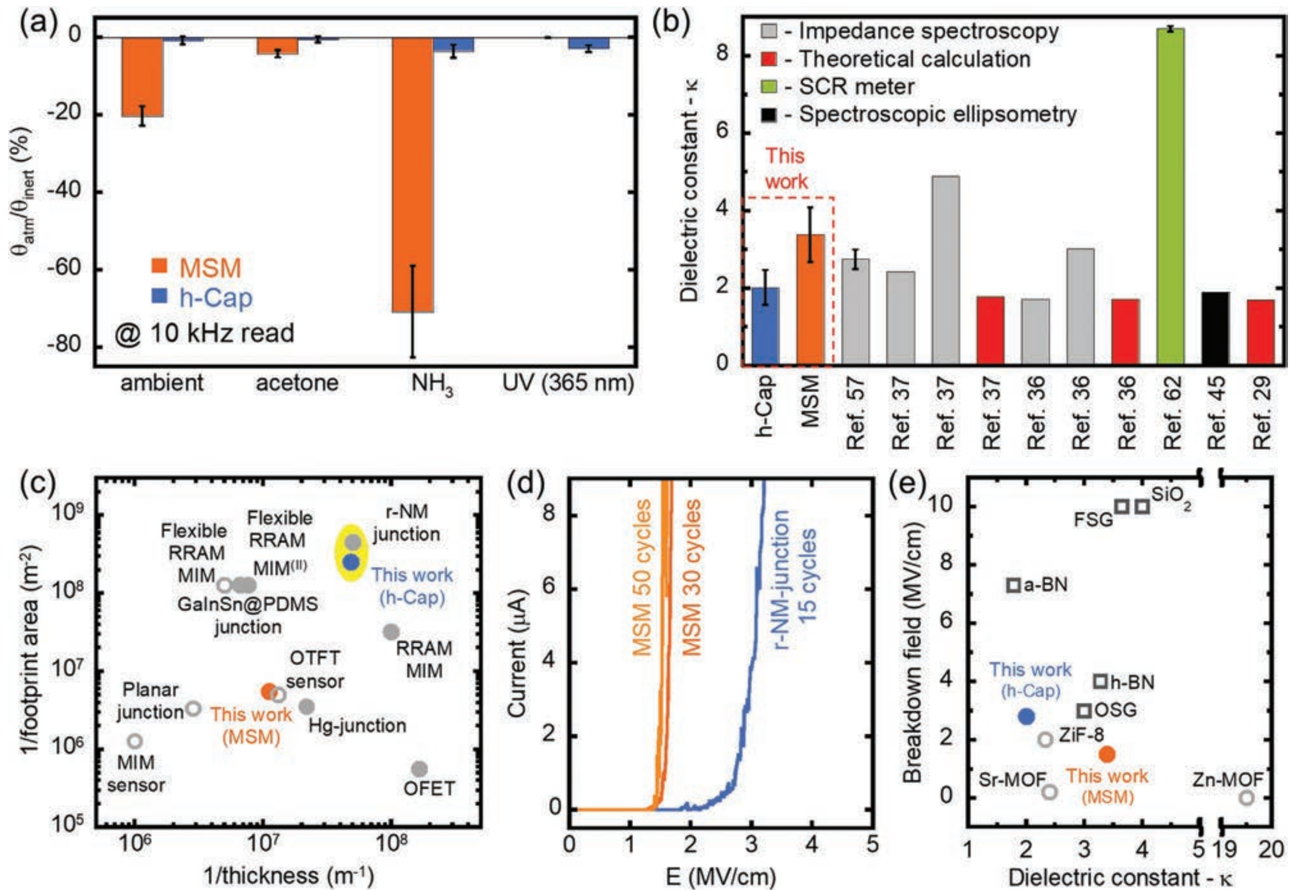

Figure 4. a) Percentage changes of θ at 10 kHz for MSM and h-Cap devices relative to the N_2 atmosphere. b) κ values for HKUST-1 obtained in this work compared to previously reported works. The error bars indicate the uncertainty of the data, which was not reported in most cases. c) A comparison of the inverse of footprint area versus the inverse of active layer's thickness from this work to other devices reported in the literature. d) Typical current versus applied electric field for MSM and r-NM-junction. e) Breakdown electric-field versus κ for this work compared with other low-κ materials reported in the literature. In (c) and (e), MOFs are open circles and SURMOFs solid circles; respective references can be found in Tables S1 and S2 (Supporting Information).

Figure 4a shows the changes of θ at 10 kHz (under hazardous agents) for both architectures. The percentage variations were calculated considering the data using the N_2 atmosphere as a reference. For the MSM devices measured at 10 kHz (the frequency region where a capacitive behavior is expected), θ variations are higher for ambient and NH_3 exposure conditions. However, for h-Cap devices, this tendency is not followed, and the measured values are kept primarily stable under the different exposure conditions. The respective changes in the capacitance are shown in Figure S13 (Supporting Information). These results confirm the effectiveness of the self-encapsulation process, indicating that the 3D structures provide some protection for the porous dielectric layer from lateral diffusion of vapors/gases, probably by the structure detachment from the substrate plane. However, further characterization of the tubular aspects is necessary to elaborate a complete explanation of the mechanisms of encapsulation evidenced here by the h-Cap devices.

Figure 4b compares the κ values of HKUST-1 obtained in this work with the results from the literature. The values of κ reported here, regardless of the architecture, are in excellent agreement with most data from the literature. As expected, the investigations performed by using theoretical calculations and spectroscopic ellipsometry result in lower κ values. Usually, these methods do not consider the orientational (dipolar) polarization caused by possible framework deformations. In particular, the Clausius-Mossotti relation (commonly used for the theoretical calculation of dielectric properties),[29] does not consider the contributions from orientational and vibrational polarizations, leading to underestimated dielectric permittivity values. Meanwhile, spectroscopic ellipsometry is usually employed by using ultra-high frequencies, inducing electronic polarization effects, and detecting the optical response from the permittivity alone.[45,61]

Furthermore, the SCR meter method allows obtaining the dielectric response restricted to a single frequency, resulting in tendentious κ values depending on the set frequency. Zeinali et al. reported using an SCR meter to determine the κ of HKUST-1 using interdigitated electrodes.[62] They found a considerable contribution from edge effects, which compromises the representativeness of the equivalent circuit used. This assumption justifies such outlier value found for the HKUST-1 κ (see Figure 4b). In comparison, impedance spectroscopy represents a reliable and complete method to

investigate the dielectric properties of low-κ materials incorporated into solid-state devices since electronic and ionic contributions can be included by adequately defining the frequency range. Thus, the results shown in Figure 4b, employing this method, allow valuable statistics regarding the HKUST-1 dielectric properties. The different values observed for MSM and h-Cap devices may be attributed to the interdiffusion of metallic atoms into the SURMOF layer during the MSM top electrical contact preparation.[42,43,47] Such a penetration reduces the separation of the capacitor plates, leading to higher (but not real) κ values. Since the roll-up method prevents the interdiffusion of metallic atoms, the electrodes' separation may be considered the SURMOF thicknesses.

The device dimensions are exploited in Figure 4c, where they are compared with selected works based on different MOFs and SURMOFs used as active layers. The inverse of footprint area versus the inverse of the active layer's thickness is a valuable benchmark to verify the integration capability for each approach without compromising the integrity of MOF and SURMOF layers. As evidenced, the r-NM-based devices present the highest aspect ratio. The r-NM-junction has a smaller footprint area because it follows the device concept of the vertical junction (see devices layout and fabrication steps in Figure S14, Supporting Information). This approach is usually applied to perform soft and self-adjusted top contact without damaging the ultrathin and porous films.[42,43,63] The h-Cap structure offers a more significant footprint area, creating ideal conditions to improve the charge accumulation at the HKUST-1 SURMOF interface. Consequently, the h-Cap can be considered a platform for a detailed investigation of its dielectric properties. The benchmarking demonstrates the r-NMs integrated into electronic devices as an exciting and powerful tool, making accessible specific intrinsic properties from ultrathin and porous films where conventional approaches do not fit.

The electrical breakdown strength was determined through the typical current versus the applied electric field to better evidence the application potential of ultrathin HKUST-1 SURMOF heterojunctions as a low-κ dielectric material (Figure 4d). Two different device architectures were considered for it: the MSM and r-NM-junction. The r-NM-junction was used to rule out any artifact due to metal diffusion into the SURMOF films, commonly observed in MSM architecture. Details regarding this vertical junction can be found in our previous work.[42] Furthermore, the r-NM-junction does not need the Al_2O_3 layer to grow the SURMOF, preventing the determination of unrealistic electrical breakdown strengths. The typical small device geometric area of the r-NM-junctions make difficult the adequate characterization of dielectrics, yet good to establishing the materials breakdown strength and charge transport investigation.[63] From Figure 4d, a breakdown field of about 1.5 MV cm^{-1} was obtained for MSM architecture for both SURMOF thicknesses. A superior breakdown field of 2.8 $MVcm^{-1}$ is obtained for the r-NM-junction, indicating that metal interdiffusion has affected the SURMOF films in MSM devices. Figure 4e compares the results obtained here and the state-of-the-art low-κ materials reported in the literature. As can be seen, both κ and breakdown electric fields are in excellent agreement with the literature. The aspect ratio is overcome by a 3 nm-thick film amorphous boron nitride (a-BN) alone.[17] Therefore, ultrathin SURMOF heterojunctions have great potential as low-κ dielectric materials once effectively integrated into a solid-state device.

After properly determining the dielectric properties of HKUST-1 films, FEM simulations were performed considering two parallel interconnects separated by an inter distance of 40 nm – a scenario similar to the interconnect systems employed in CMOS technology.[4,64] Different substrates, such as well-known dielectrics (SiO_2 and Al_2O_3), are compared to HKUST-1 in electric field distribution for an applied electric potential. The simulations were performed considering the different κ for the respective dielectrics, namely 2 (HKUST-1), 3.9 (SiO_2), and 9 (Al_2O_3). The κ values for the oxides were taken from the literature.[65,66] **Figure 5**a illustrates the two parallel interconnects on the HKUST-1 substrate; the electric potential of $V_{DC} = 150$ mV is applied to the left interconnect (force terminal) while the right one is kept grounded (*GND*, sense terminal). The inset shows the distribution of representative electric field lines, where a significant difference in flow through the air and substrate (dielectric) is noted. The electric field distribution is obtained by solving Laplace and Poisson's relations, shown in Equation (2)

$$\nabla^2\varphi = -\frac{\rho}{\varepsilon} \tag{2}$$

where ∇^2 is denoted as the Laplace operator, φ is the electric potential, ρ is the electric charge density, and ε is the electric permittivity. For the case where $\rho = 0$, the boundary conditions turn the problem described by Laplace's equation.

Considering a vertical line at $x = 0$ in the inset of Figure 5a, the calculated electric field distribution can be obtained for the different dielectrics for both grounded and float sense terminal configurations (see Figure 5b). For the case with a floating sense terminal, the distribution is nearly the same for all dielectrics. Setting the sense terminal to the ground shows a significant difference for the HKUST-1 substrate. As shown in Figure S15 (Supporting Information), the simulated system evidences a more responsive electric field distribution at the substrate, i.e., below its surface, with contributions in both plane axes. Next, we employed the sidewall dielectric approach to the parallel interconnects using the same dielectric material from the substrate (Figure 5c). This approach is widely known in CMSO-like configurations to reduce the inherent and undesired effects from R and C_p that significantly compromise the overall performance.[67] Thus, we assume the net described in Figure 5c as a scenario considering the dielectrics as ILD-like to insulate the parallel interconnects. As shown in Figure 5d, the respective electric field distribution exhibits a considerable reduction for both sense terminal configurations (ground and float) for HKUST-1, followed by SiO_2 and Al_2O_3 dielectrics. Furthermore, these results can be better explained by applying a classical approach, i.e., determining a Gaussian surface (S) around the sense electrode according to Gauss's law, Equation (3)

$$\Phi_D = Q_{free} = \oint_S \vec{D}.\mathrm{d}\vec{A} = \varepsilon.\oint_S \vec{E}.\mathrm{d}\vec{A} \tag{3}$$

where Φ_D is the electric flux through the Gaussian surface, Q_{free} the free charge, $\vec{D}$ the displacement of the flux, $\mathrm{d}\vec{A}$ an

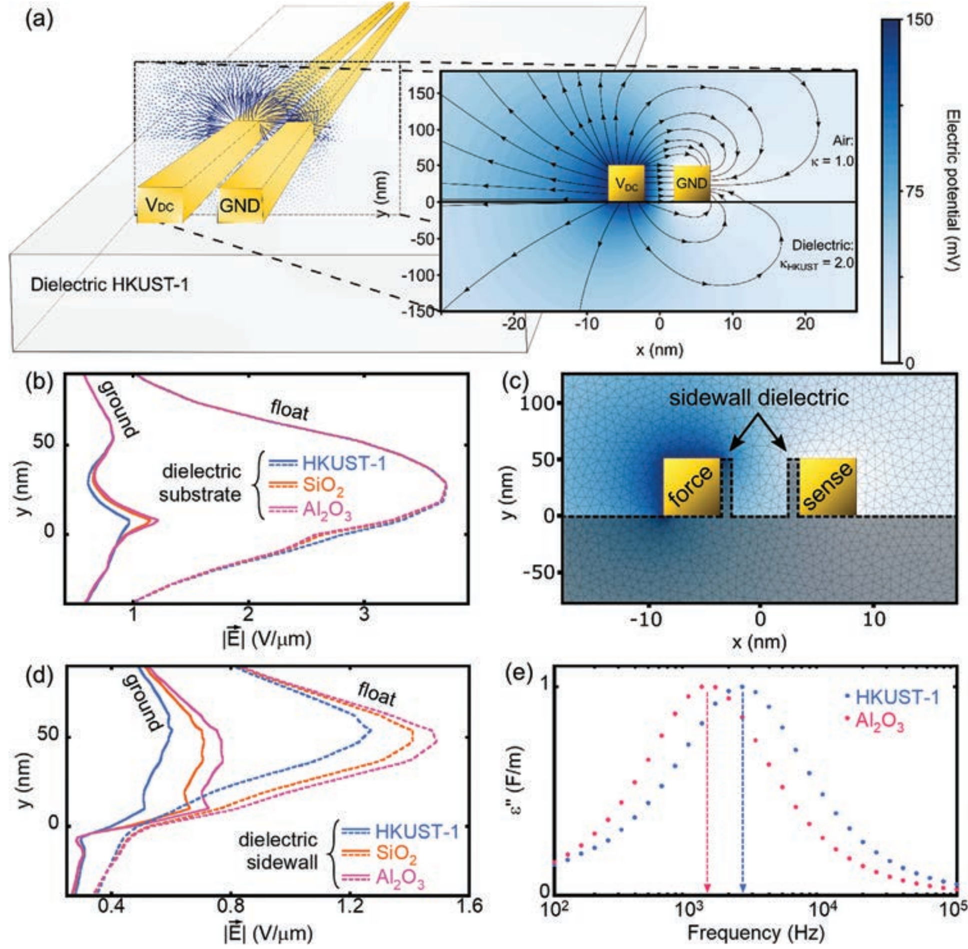

Figure 5. FEM simulations for HKUST-1, SiO_2, and Al_2O_3. a) Illustration of two parallel interconnects on HKUST-1 as substrate. V_{DC} and *GND* correspond to the force and sense terminals for an applied *DC* electric potential. (inset) Respective electric field lines distribution for cross-section. b) Electric field (in modulus) between the two parallel interconnects (vertical line, $x = 0$) for HKUST-1, SiO_2, and Al_2O_3 as substrate. c) Representation of the setup for simulation, considering the respective dielectrics as sidewalls for both parallel interconnects. d) Electric field (in modulus) between the two parallel interconnects (vertical line, $x = 0$) for different dielectrics as substrate and sidewalls. e) Experimental dielectric loss factor spectroscopy for HKUST-1 and Al_2O_3 as the dielectric layer in a MIM configuration. In (b) and (d), solid and dotted data lines represent grounded and float configurations for the sense electrode.

infinitesimal element related to S, ε the electric constant, and $\vec{E}$ the electric field.

Figure S16 (Supporting Information) illustrates the Gaussian surface around the sense terminal grounded. The free charge induced at this terminal was calculated for both dielectric configurations, i.e., with and without dielectric sidewall. Without a dielectric sidewall, the charge induced in the sense terminal for HKUST-1 as the substrate is smaller than for SiO_2 and Al_2O_3 dielectrics (see **Table 1**). Notably, the charge induced for Al_2O_3 at this configuration is more than twice the value obtained for HKUST-1. The same tendency is observed for the calculated capacitance. However, the charge induced reduces substantially with dielectric sidewall for all dielectrics due to the lower electric field distribution observed in Figure 5d. Nevertheless, HKUST-1 still possesses smaller values compared with the other dielectric materials.

Figure 5e shows the experimental dielectric loss factor spectroscopy for HKUST-1 and Al_2O_3 as the dielectric layer in the metal-insulator-metal (MIM) configuration. The thicknesses for both dielectric layers are about 80 nm—to mimic a scenario close to the situation exploited in FEM simulations. This thickness corresponds to 40 step-by-step deposition cycles of HKUST-1

Table 1. Calculated charge induced and capacitance from the FEM simulations considering the sense terminal grounded.

Dielectric configuration	Dielectric material	Charge induced in sense [pC]	Capacitance – Q_{charge}/V_{force} [pF]
Substrate only	HKUST-1	−4.24	28.26
	SiO_2	−5.88	39.24
	Al_2O_3	−10.06	67.06
Substrate + sidewall	HKUST-1	−1.48	9.90
	SiO_2	−1.96	13.08
	Al_2O_3	−2.94	19.60

SURMOF, as shown in Figure S3c,d (Supporting Information). It is worth mentioning that HKUST-1 films below this thickness have a reasonable probability of presenting a behavior different from a pure capacitor owing to the possible diffusion of metal atoms into the HKUST-1 pores during evaporation, as already detailed in the phase histograms from Figures S7 and S8 (Supporting Information). The dielectric loss factor (ε″) for each data point obtained from impedance spectroscopy (Figure S17, Supporting Information) was calculated following Equation (4)

$$\varepsilon'' = \frac{G}{\omega} \tag{4}$$

where G is the conductance and $\omega = 2\pi f$ is the angular frequency.

The peak observable for both dielectric losses evidence the different relaxation time responses—meaning that the related charge accumulation mechanisms are not responding to the applied *AC* signal owing to the higher frequencies. Such effect occurs first for HKUST-1 (at ≈2.54 kHz) followed by Al_2O_3 (at ≈1.38 kHz) in the employed MIM configuration, considering that the data acquisition begins at higher frequencies. The peak frequencies obtained indicate that HKUST-1 could provide, in principle, better switching performances than Al_2O_3.

3. Conclusion

In summary, we report a detailed investigation of the dielectric properties of ultrathin HKUST-1 SURMOF heterojunctions fully integrated into an r-NM-based capacitor. The device concept relies on a freestanding strained metallic tri-layer, providing a soft and robust top electrical contact on the porous SURMOF layer through a self-assembled device structure. By modeling the characteristic impedance data through equivalent circuits, a low-κ value of 2.0 ± 0.5 was obtained, in good agreement with the literature. The low-κ value and the breakdown field of 2.8 MV cm^{-1} provide one of the best aspect ratios reported so far, demonstrating the great potential of HKUST-1 SURMOF as the low-κ dielectric material. Besides, the device structure has good compactness in a tubular form. This feature reduced 90% of the original device footprint area and protected the SURMOF dielectric properties against hazardous agents. The experimental findings are explained using FEM simulations, considering the HKUST-1 as substrate and sidewalls for two parallel interconnects separated by nanometric distances. The results provide a consistent benchmarking on the dielectric properties of HKUST-1, compared with the well-established dielectrics used in electronics (SiO_2 and Al_2O_3), projecting this hybrid structure as a promising candidate for the new generation of low-κ materials.

Furthermore, the dielectric properties of ultrathin SURMOFs are effectively accessed at the nanoscale solid-state device, using a 3D functional device architecture fully compatible with standard microfabrication processes. Also, these devices are appealing to exploit exciting quantum-electrodynamical effects. The tube-shaped capacitors could operate as integrated optical microcavities to develop novel and advanced technologies in the context of optical sensors.

4. Experimental Section

Fabrication of Devices: The r-NM-based capacitors were fabricated on 9 × 9 μm^2 Si (100) substrates with a 2 µm thick SiO_2 layer on the surface. The metallic layers were patterned using conventional photolithography with AZ 5214E photoresist and deposited by electron-beam evaporation in a high vacuum (≈10^{-7} Torr), with a distance between the sample and target material in the deposition system of about 40 cm. The oxide layers, based on Al_2O_3, were deposited using atomic layer deposition, with TMA (trimethylaluminum) and H_2O precursors, at pressure values ranging from 120 to 560 mTorr (inside the deposition chamber). The first step was the patterning and creation of the sacrificial layer, composed of 20 nm thick germanium (Ge) layer deposited at 0.2 Å s^{-1}, followed by its surface oxidation under 90% of relative humidity (RH) during 16 h to create GeO_x (soluble in aqueous media), as illustrated in Figure S1a (Supporting Information). Then, the first metallic layers were formed by the patterning and deposition of Au (5 nm), Ti (10 nm), and Cr (10 nm), with deposition rates of 0.50 $Ås^{-1}$, 0.65 $Ås^{-1}$, and 0.90 $Ås^{-1}$ over the sacrificial layer, as can be seen in Figure S1b (Supporting Information). The tri-metallic layer has an essential role in the device concept: the weak adherence of Au on the GeO_x layer, associated with the stress created between Ti/Cr layers, produces the roll-up of the device after the removal of the sacrificial layer. In the sequence, 10 nm of Al_2O_3 was deposited over the strained metallic layer, followed by the patterning and deposition of 10 nm of Cr at 0.50 $Ås^{-1}$, configuring a conventional parallel-plate capacitor (Figure S1c,d, Supporting Information). Next, a second 10 nm thick Al_2O_3 layer over the second capacitor's plate, Figure S1e (Supporting Information). The second Al_2O_3 layer is responsible for insulating the plates after multiple windings for the rolled devices without the SURMOF. Then, a photoresist layer was deposited and patterned to prevent any damage to the devices while the contacting areas were clean. This procedure was performed by using a 1% (v/v) hydrofluoric acid (HF) aqueous solution, followed by the deposition of the Cr/Au contacting pads (20/40 nm), both at 1 Å s^{-1}. Also, the HF aqueous solution was used to create a trench over the superior region of the devices to facilitate the subsequent GeO_x dissolution. For the h-Cap, the second Al_2O_3 layer was functionalized with PHDA SAM, followed by HKUST-1 SURMOF growth using the LPE approach, as shown in Figure S1f (Supporting Information). Finally, the roll-up process (Figure 1Sg) was performed by immersing the devices into 80% (v/v) ethanolic aqueous solution at 50 °C for ≈60 min. Then, the samples were left to dry for at least 24 h in ambient conditions, followed by 24 h in the vacuum before electrical characterization.

The MSM devices were also fabricated on 9 × 9 μm^2 Si (100) substrates with a 2 µm thick SiO_2 layer on the surface. Cr/Au (20/60 nm) were deposited at 0.5 $Ås^{-1}$ on the entire substrate surface as the bottom electrode. In the sequence, the Au surface was either functionalized with mercaptohexadecanoic acid (MHDA.) SAM followed by the HKUST-1 SURMOF growth using LPE. Then, using a shadow mask, Au (40 nm) was deposited at 0.2–0.3 Å s^{-1} on the SURMOF surface, configuring the top electrode with an active device area of about 0.2 mm^2. A Cr layer (80 nm) was deposited as the bottom electrode on the same substrate (SiO_2) for the MIM devices with an oxide layer. Then, the oxide was grown by ALD, followed by the deposition of Au (40 nm) top electrode using the same shadow mask used for MSM devices. The number of devices on a chip is 121, as shown in Figure S6 (Supporting Information). After the fabrication, devices were left to dry for at least 24 h in the vacuum before electrical characterization.

Step-by-Step Growth of HKUST-1 SURMOF: HKUST-1 SURMOF was grown using a quasi-LPE approach on the Al_2O_3 layer. First, the Al_2O_3 layer was functionalized with PHDA SAM. The surface functionalization is done by immersing the sample into 5% (v/v) acetic acid in an isopropanol solution containing 0.5 × 10^{-3} м of PHDA for 1 h at 50 °C, followed by 19 h in room conditions. After being dried with N_2, the samples were introduced sequentially in 1 × 10^{-3} м copper acetate (2 min) and 1 × 10^{-3} м BTC (4 min) ethanolic solutions. To remove the nondeposited material, pre-washing and washing steps were employed between the precursor solutions (Figure S2, Supporting Information).

After the desired cycles were reached, the samples were dried with N_2. More details regarding HKUST-1 SURMOF growth can be found in a previous work.[41,42] The functionalization of Au surface for MSM devices was performed similarly by immersing the sample in 10% (v/v) acetic acid ethanolic solution containing 0.5 mM of MHDA SAM for 1 h at 50 °C, followed by 19 h in room conditions, and dried with N_2 in the sequence.

Characterization: SEM images were performed using a Field Emission Gun Scanning Electron Microscope (FEG-SEM) Inspect F50 from FEI (Japan). LSCM and conventional optical images were obtained using an LSCM VK-X200 from Keyence (USA). GIXRD patterns of the HKUST-1 SURMOF were acquired through X-ray synchrotron radiation at the XRD2 beamline in the Brazilian Synchrotron Light Laboratory (LNLS) (λ = 1.54979 Å and 2θ range from 6° to 17°). AFM topography images were obtained using a Park NX10 AFM; analyses were performed with Gwyddion software. The impedance spectroscopy was performed using a conventional probe station equipped with micromanipulators and an optical microscope; the contact is performed through conventional tungsten tips connected to the micromanipulators. The micromanipulators have triaxial connectors plugged into a Solartron 1260A Impedance Analyzer. The measurements were performed applying a sine-wave voltage of 100 mV amplitude and 0 V of offset, with 10 points per decade from 3×10^6 to 3×10^{-1} Hz. During the data acquisitions, a homemade chamber (≈50 cm^3) was used to keep the different environment conditions (N_2, RH, NH_3, and acetone). The N_2 and RH desired levels were controlled by adjusting water vapor and N_2 gas inside the camber. The NH_3 expositions were performed by placing a recipient inside the chamber containing 20 ml of 5% (v/v) aqueous ammonia solution (≈28%, Sigma Aldrich); the same volume was established for the saturated solution of acetone. For the UV exposition, a UV light provided by a mercury lamp (USHIO UV lamp USH-508S) with a luminous flux of 35 200 lm was used with a cumulative dose of 500 mJ cm^{-2}. All impedance data acquisitions were performed immediately after each exposition.

FEM Simulations: FEM simulations were performed using FeniCS (2019.1.0) library, i.e., Python library, to solve PDEs (Partial Differential Equations).[68] The complete simulation was performed with the assistance of several applications, namely GMSH (3.6.0), for geometry and mesh generation.[69] The mesh was imported into FeniCS to solve the electrostatic problem, and Paraview 5.9.0 was used as a post-processing tool.[70] The entire simulation was performed using a modern laptop (i7 8750H processor, 16 Gb dd4 ram, and 500 Gb SSD).

A square domain representing the device cross-section was modeled, with dimensions $\Omega = [0,2] \times [0,2]$ (μm $\times$ μm), $\Omega \in R^n$, and Dirichlet boundary conditions were prescribed.[68] The domain was divided into two subdomains, $\Omega_0 = [0,2] \times [0,1]$ and $\Omega_1 = [0,2] \times [1,2]$. The values for static relative permittivity were $\varepsilon_r(x,y) = \varepsilon^0_r$ in Ω_0 and $\varepsilon^1_r(x,y) = \varepsilon^1_r$ in Ω_1, where ε^0_r and ε^1_r were set to be constant for each medium. The relative permittivity of air was set to $\varepsilon_{air} = \varepsilon^0_r = 1$, while ε^1_r was set to be the static permittivity tensor ($\varepsilon^1_r xx = \varepsilon^1_r yy$) for HKUST-1, SiO_2, and Al_2O_3. The two parallel interconnects are set as Dirichlet boundary conditions with electric potential $V = V_{bias}$ = 150 mV on the left and both floating and grounded on the right. The mesh was processed as a set of dozens of thousands of unstructured P1 Lagrange elements.[68,71,72]

The variational formulation was derived, and the weak formulation in the standard notation for bilinear $a(u,v)$ and $L(v)$ linear forms[68] is shown in Equations (5) and (6). Then, the value-boundary problem was solved in FeniCS[68]

$$a(u,v) = \int_\Omega \varepsilon(x,y).\nabla u.\nabla v.\mathrm{d}x \quad (5)$$

$$L(v) = \int_\Omega f.v.\mathrm{d}x \quad (6)$$

where $u(x)$ and $v(x)$ are the tests (unknown) and trial functions, respectively. Therefore, the statement of the variational problem is to find $u \in V$ such that $a(u,v) = L(v)$, $\forall v \in \hat{V}$. The test space V is defined as Equations (7) and (8)

$$\hat{V} = \{v \in H^1(\Omega) : v = 0 \; on \, \partial\Omega\} \quad (7)$$

$$V = \{v \in H^1(\Omega) : v = u_0 \; on \, \partial\Omega\} \quad (8)$$

Test V and trial $\hat{V}$ function spaces are convenient Sobolev spaces. A complete description can be found elsewhere.[68,71]

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

R.M.L.S. fabricated devices; performed the electrical characterization, data evaluation, and interpretation; discussed results; wrote the manuscript and illustrations. L.G S.A. helped fabricate devices; supervised the study, data evaluation, and interpretation; discussed results; wrote the manuscript and illustrations. T.P.V. helped fabricate devices; performed SURMOF growth and characterization; helped with manuscript writing and illustrations. W.W.R.A. performed finite-element modeling simulations; discussed results; helped with manuscript writing and illustrations. D.H.S.C. helped with the fabrication of devices and illustrations. L.D.P. helped with the fabrication of planar devices and provided technical support for electrical characterization. C.C.C. performed SURMOF growth and characterization. C.W. helped with manuscript writing. C.C.B.B. supervised the study; helped with data interpretation; discussed results; helped with manuscript writing; and led the work. All authors have approved the final version of the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

dielectrics, HKUST-1, low-κ, metal-organic frameworks, SURMOFs

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