

Design and Characterization of a 500 kW 20 kHz Dual Active Bridge using 1.2 kV SiC MOSFETs

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Abstract—High power Silicon Carbide (SiC) semiconductor enable an increase of the power level for the Dual Active Bridge (DAB). This paper presents a concept for a novel high power DAB up to 500 kW. 1200 V SiC MOSFETs are used as power semiconductors, which are operated with a switching frequency of 20 kHz. In order to investigate the feasibility of such high power DABs basic design rules are presented and the influence of parasitic components is deduced. It is shown that these parasitic effects become more and more important with increasing power and therefore cannot be neglected as in the case of lower power DABs. Using a calorimetric measurement setup a detailed loss distribution is presented. Measurements confirm the concept for the parasitic influence and design target of 500 kW.

Keywords—DC/DC Converter , Dual Active Bridge, High Power Converter

I. INTRODUCTION

Recent improvements in the power level of Silicon Carbide (SiC) semiconductors enable high switching frequencies with higher power capability, even for low voltage MOSFETs. A DC-DC converter topology that particularly benefits from these developments is the Dual Active Bridge (DAB). The wide voltage range, high power density concerning weight and volume and soft switching capability as well as the galvanic isolation recommends the DAB as a promising topology for various applications [1]. In the past, resonant topologies such as the LLC resonant converter were used for higher power applications at low and medium voltage such as shown in [2] for a 300 kW converter. However, drawbacks of this topology are the requirement of additional resonant components (especially high current AC capacitors), the inflexibility in the control and operation with wide DC-voltage range. With the introduction of high-current SiC MOSFET modules, the power level of DABs is increased as well, shown in [3] for a 100 kW DAB. However, various applications such as Solid State Transformer (SST) and battery charging require higher power level for DC-DC converters, with the DAB as a promising candidate [4]. Because of that, the DAB is investigated up to 500 kW.

The basic equivalent circuit diagram of the DAB is shown in Fig. 1. It consists of four half bridges (HB) interconnected by a medium-frequency transformer (MFT). Depending on the setup, an auxiliary inductor in series

to the transformer might be necessary, or the transformer itself with its leakage inductance as well as the connection stray inductance alone is sufficient to provide the stray inductance L_σ . The power flow for the DAB is controlled by changing the phase shifts of these four half bridges. The resulting control parameters are the phase shift angles δ_1 , δ_2 and φ as shown in Fig. 1. This general modulation is called Triple Phase Shift (TPS). The most commonly used TPS modulations are the triangular and trapezoidal modulation [10]. However, more sophisticated modulations schemes can be used to minimize switching losses or overall losses as shown in [5] and [7]. In this paper, only Single Phase Shift (SPS) is used, because the primary and secondary voltage V_{DC} is always equal. For SPS, the phase shifts within the full bridges (HB1 to HB2 and HB3 to HB4) are equal to zero ($\delta_1 = \delta_2 = 0$) and the power flow is controlled only by the phase shift φ between the primary and secondary side. The transferred power can be calculated according to (1) and (2) [1]. For all considerations in this paper, a transformer transfer ratio of $n = 1$ is assumed.

$$P_{\text{out}} = \frac{1}{1/f_{\text{sw}}} \int_0^{1/f_{\text{sw}}} v_1(t) i_{L_\sigma}(t) dt \quad (1)$$

$$P_{\text{out}} = \frac{nV_{DC1}V_{DC2}}{2\pi f_{\text{sw}}L_\sigma} \cdot \varphi \cdot \left(1 - \frac{|\varphi|}{\pi}\right) \quad (2)$$

The maximum transmissible power for the DAB in SPS operation can be calculated from (2) and is achieved for $\varphi = \pm \frac{\pi}{2}$.

$$P_{\text{out,max}} = \pm \frac{nV_{DC1}V_{DC2}}{8f_{\text{sw}}L_\sigma} \quad (3)$$

Analyzing equation (3), it can be observed, that the stray inductance of the AC circuit L_σ is a critical design parameter to achieve high output power level of the DAB. It limits the maximum power throughput for given switching frequency f_{sw} , transformer transfer ratio n and DC voltages V_{DC} .

resulting equation is shown in (9) and describes a resonant oscillations depending mainly on the switching current $i_{L\sigma,0}$ and the time constant $\sqrt{L_\sigma C_{eq}}$. Because of the impact off the switching current, the commutation speed and the voltage error of every switching event can be different and do not compensate for each other over a full period. The difference in voltage for an ideal and a real resonant commutation is shown in Fig. 7 for two different switching currents. It can be observed, that with an increase in switching current the error is decreasing but has still an impact on the AC voltage v_{AC} and therefore has to be considered.

$$v_{AC1/2}(t) = V_{DC1/2} - \sqrt{\frac{L_\sigma}{C_{eq}}} (i_{L\sigma,0} \sin(\frac{t}{\sqrt{L_\sigma C_{eq}}})) + (V_{DC1/2} - v_{AC2/1}) (\cos(\frac{t}{\sqrt{L_\sigma C_{eq}}}) - 1) \quad (9)$$

This effect causes a voltage error at the stray inductance L_σ which can have a significant impact on the AC current as shown in [8]. In Fig. 5 the phase shift between primary and secondary side is only about 500 ns compared to the deadtime of 250 ns and therefore small deviations in commutation speed of the semiconductor have a significant impact on the resulting current waveform.

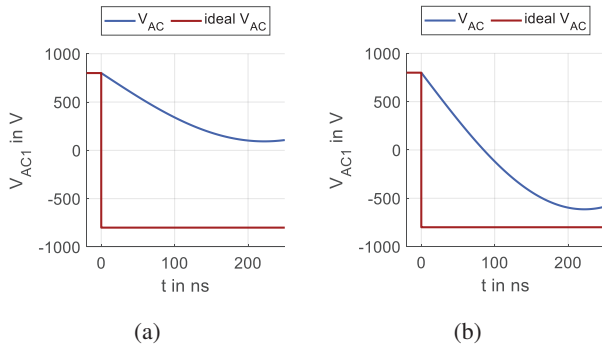


Fig. 7: Ideal and real AC voltage v_{AC} for resonant commutation at $V_{DC1} = V_{DC2} = 800$ V (a) $i_{L\sigma,0} = 100$ A (b) $i_{L\sigma,0} = 200$ A

C. HF oscillations

A high transformer winding capacitance can cause high frequency oscillations in the current and the output voltages v_{AC1} and v_{AC2} of the full bridges and the AC current $i_{L\sigma}$ as shown in Fig. 5 [9]. These oscillations can cause high losses in the ohmic components of the system and further reduce the efficiency of the DAB. The resulting HF equivalent circuit diagram for the oscillation is shown in Fig. 8. The main parasitic components for this system are the winding capacitances of the transformer C_{w1} and C_{w2} , the stray inductance of the transformer L_σ and the AC inductances L_{AC1} and L_{AC2} on the primary and secondary side.

$$Z_{prim} = \frac{(y_{ph2} + y_{22})}{(-y_{12}^2 + y_{11}y_{ph2} + y_{11}y_{22})} + \frac{1}{y_{ph1}} \quad (10)$$

$$Z_{sec} = \frac{(y_{ph1} + y_{11})}{(-y_{12}^2 + y_{22}y_{ph1} + y_{22}y_{11})} + \frac{1}{y_{ph2}} \quad (11)$$

with

$$\begin{aligned} y_{ph1} &= \frac{1}{R_{AC1} + j\omega L_{AC1}} \\ y_{ph2} &= \frac{1}{R_{AC2} + j\omega L_{AC2}} \\ y_{11} &= \frac{1}{j\omega L_\sigma} + j\omega C_C \\ y_{12} = y_{21} &= \frac{1}{j\omega L_\sigma} + j\omega(C_C - C_{w1}) \\ y_{22} &= \frac{1}{j\omega L_\sigma} + j\omega(C_C - C_{w2}) \end{aligned} \quad (12)$$

The resulting impedance seen from primary side Z_{prim} and secondary side Z_{sec} is shown in (10) and (11) with the zeros showing the resonant frequencies. This resonant circuit has two main resonant frequencies of which the lowest is the most important and is shown in Fig. 9. It can also be observed that the resonance frequency depends on the ratio of $\frac{L_{AC1}}{L_{AC2}}$ and is therefore highly depending on the actual hardware setup as shown in Fig. 10. To some extent this can be used to increase the resonance frequency by changing this ratio. To reduce undesirable oscillations the excitation at the resonance frequencies has to be avoided. A general guideline to reduce the excitation is to increase the first resonance to a higher frequency where the excitation from the semiconductor switching is reduced. A second approach consists of decreasing the $\frac{dv_{AC}}{dt}$ of the AC voltages $v_{AC,1/2}$ which significantly reduces the excitation of the resonant circuit [9]. One way to achieve this is by using snubber capacitor.

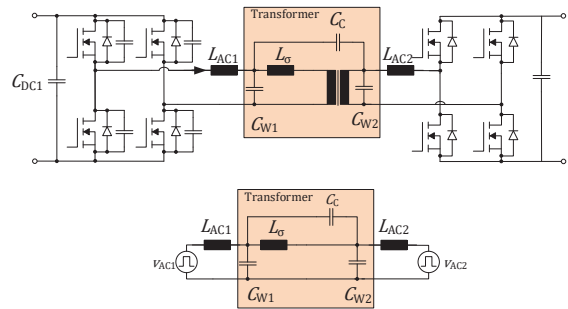


Fig. 8: High frequency equivalent circuit diagram for the AC circuit of the DAB

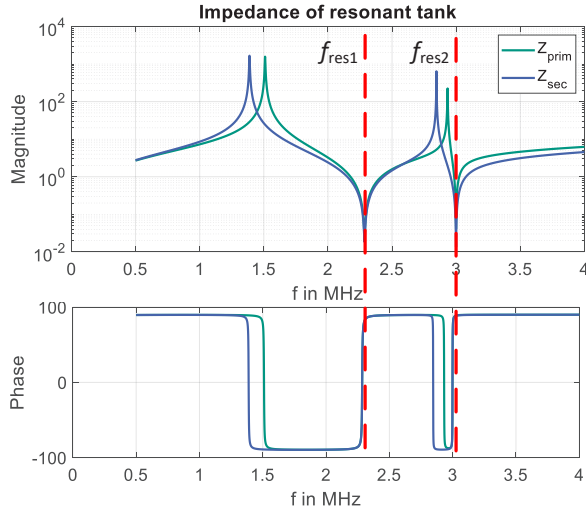


Fig. 9: Bode diagram of the impedance of the resonant tank seen from primary and secondary side

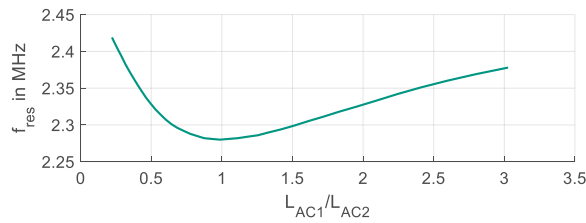


Fig. 10: First resonance frequency depending on the ratio of $\frac{L_{AC1}}{L_{AC2}}$

D. Parasitic voltage drop

The final considered parasitic mechanism which has to be considered is the voltage drop in the AC circuit caused by the AC resistance. The AC resistance mainly consists of the on state resistance of the MOSFETs R_{DSon} and it is generating a voltage drop from the DC-Link to the AC inductance. This results in a decreased voltage v_{AC1} and an increased voltage v_{AC2} for positive power transfer and vice versa for negative power. This change in the AC voltages is causing a voltage drop over the AC inductance and therefore, intensified by the low value of the AC inductance, an unexpected error in the current as shown in Fig. 5 occurs. In this example the additional AC resistance $R_{AC} = 8 \text{ m}\Omega$ is in the same range as the $R_{DS, on}$ of the turned on MOSFETs and therefore cannot be decreased any further. Especially for low AC inductances the difference of the current compared to theoretical analysis cannot be neglected and it is reducing the transferred power as well as the efficiency. Especially if considering triangular modulation with Zero Current Switching (ZCS) the voltage drop is important to consider, since for maximum efficiency in this modulation a switching at exactly zero current is necessary. This is not possible if the deviation in current caused by the voltage

error is not compensated by the modulation scheme.

IV. EXPERIMENTAL RESULTS

All experimental results were acquired using the presented DAB hardware setup with the parameters given in table I. The voltage ratio between the primary and secondary sides was kept constant at 1 : 1 for all measurements which means that $V_{DC1} = V_{DC2}$, this results in single phase shift modulation for all operation points shown. The general waveforms for the SPS operation are shown in Fig. 5. The maximum power of 504 kW was achieved with $V_{DC} = 800 \text{ V}$ and an efficiency of $\eta = 97.18\%$. Peak efficiency of the DAB is $\eta = 98.24\%$ at 110 kW and $V_{DC} = 500 \text{ V}$. The resulting efficiencies for different DC voltages V_{DC} and transferred power can be seen in Fig. 11.

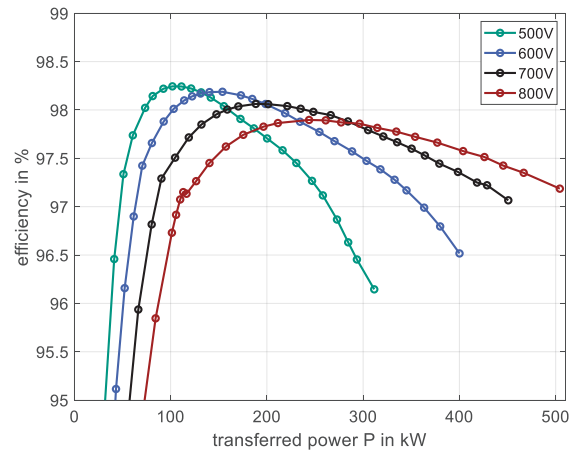


Fig. 11: Efficiency of the DAB for different DC-Link voltages V_{DC} and conversion ratio of 1 : 1

By comparing the calculated phase shift φ_{calc} acquired by using (1) with the setpoint phase shift φ_{set} , which is provided by the control, the impact of commutation can be seen. The result is shown in Fig. 12. It can be seen, that the setpoint phase shift φ_{set} is always lower than the calculated one. This can be explained with the voltage error for the commutation that can be calculated by using (9). Because the ideal formula always expects infinite fast commutation compared to the phase shift time T_φ an high error in transmitted power can occur if the phase shift is in the same range as the deadtime. This is the case for low inductances as shown in the DAB test bench. Additionally the parasitic voltage drop and the associated decrease in current does change the transferred power compared to the ideal DAB.

In Fig. 13 the setpoint phase shift φ_{set} for different voltages is shown. In Fig. 13 (a) the transfer characteristic is shown. It can be seen that if a certain transfer power is exceeded, a clearly visible step in the transfer characteristic occurs. This point marks the full ZVS border of the primary side. At this point the voltage error caused by commutation is changing drastically because the energy in the inductor is high enough to charge the output

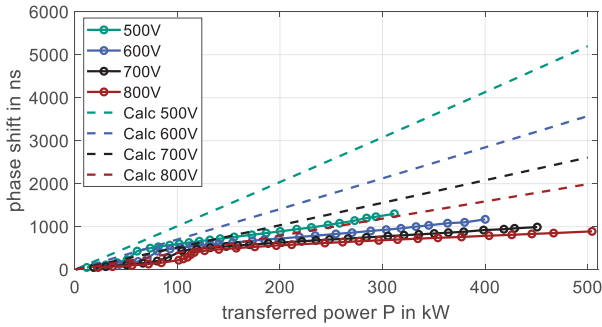


Fig. 12: Calculated phase shift φ compared to setpoint phase shift by control

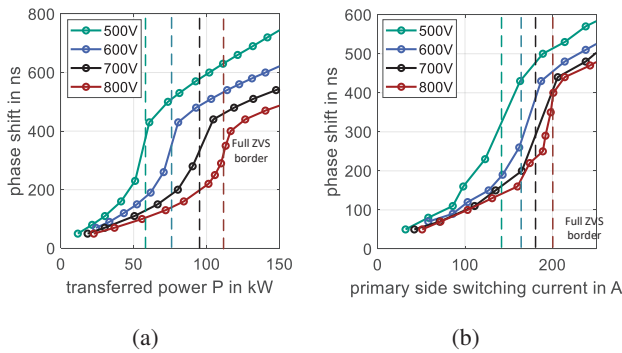


Fig. 13: (a) transferred power (b) switching current over phase shift φ with ZVS border

capacitances and the commutation speed does not change drastically anymore. Before this point the commutation has a sinusoidal form and takes much more time [8] (cf. Fig. 7). By comparing the ZVS border for different voltages it can be seen that the ZVS border is increasing in power level with higher voltages. This is expected because the energy in the capacitors E_C is increasing with voltage and as shown in (8) the energy in the inductor L_σ has to be higher to achieve full ZVS. This can also be seen by comparing the primary side switching currents as shown in Fig. 13 (b). With an increasing DC voltage, higher switching currents are necessary to charge the capacitances. It is important to note that the resulting change in trend of the transfer characteristics is highly depending on the operation point and power flow direction, since the $\frac{dv_{ac}}{dt}$ of the AC voltages depends on the operation point. The same behaviour can be seen in the measured primary side semiconductor losses shown in Fig. 14. The minimum of the overall semiconductor losses is at the border of full ZVS (indicated with the dotted lines). Prior to that point, the losses are decreasing because switching losses are dominant and decreasing with increasing transfer power. After the ZVS border the losses are increasing drastically and are dominated by turn off and conduction losses.

By looking at the secondary side losses the minimum is not so pronounced compared to the primary side. There

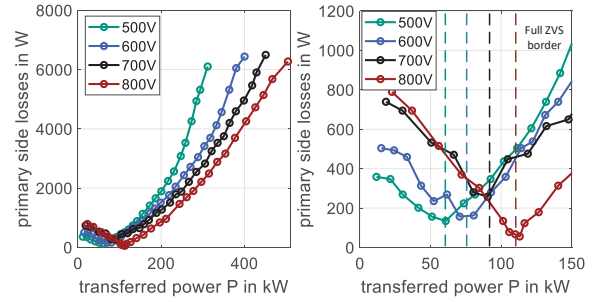


Fig. 14: Calorimetric measured losses in primary side semiconductors

are two reasons for that. First of all the switching current is significantly smaller as shown in Fig. 5 which is caused by the parasitic voltage drop. Therefore the ZVS border is achieved at higher output power compared to the primary side. Secondly the ratio between switching losses and conduction losses, at the ZVS border, is not that high compared to the primary side and therefore the secondary side is not so much dominated by the turn off losses. The reason for that is also the lower switching current on the secondary side. This results in the course as seen in Fig. 15. Until full ZVS is achieved the overall power loss is constant with power increase because the conduction losses are increasing with the same rate as the turn on losses are decreased. After the ZVS border is reached the losses are increasing as expected. This results in high power loss on the secondary side for low transferred power and decreased efficiency at light load.

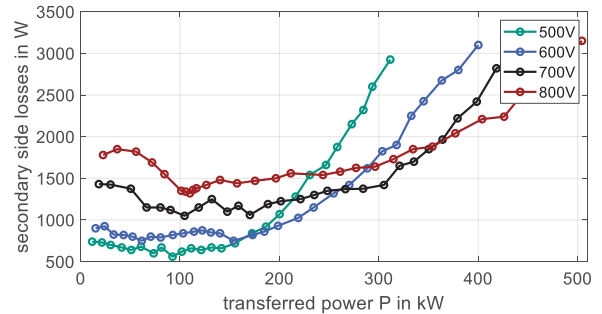


Fig. 15: Calorimetric measured losses in secondary side semiconductors

The additional losses caused by e.g. capacitors, busbar and transformer can be calculated by subtracting the semiconductor losses, acquired with the calorimetric measurement, from the overall losses measured electrically using the formula in (13). The resulting losses are shown in Fig. 16. It can be observed that for low power the losses are increasing with voltage which indicates a significant impact of the high frequency oscillations described earlier. With an increase in voltage the excitation of the resonant circuit is also increasing which results in higher additional losses $P_{v,additional}$. With an increase in

transferred power the conduction losses have a growing influence on the losses. Therefore at high power the losses are higher for lower voltages because of the overall higher AC current $i_{L\sigma}$.

$$P_{v,\text{additional}} = P_{v,\text{electrical}} - P_{v,\text{calorimetric}} \quad (13)$$

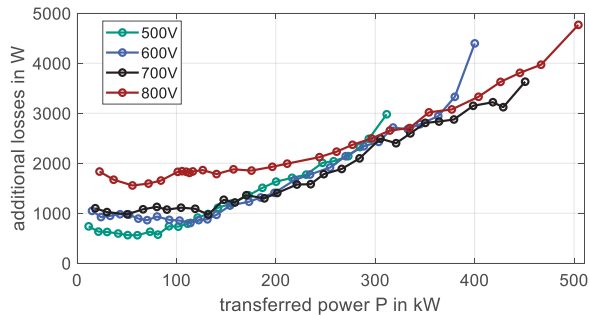


Fig. 16: Additional losses excluding semiconductor losses

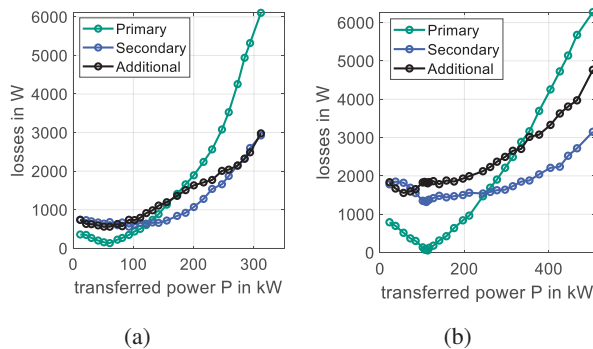


Fig. 17: Loss distribution for (a) $V_{DC} = 500\text{ V}$ (b) $V_{DC} = 800\text{ V}$

Figure 17 shows the distribution of the losses for $V_{DC} = 500\text{ V}$ and $V_{DC} = 800\text{ V}$. It can be seen that the additional losses are increasing with voltage rating and make up a larger proportion of the overall losses. For 500 V the additional losses are equal to the secondary side semiconductor losses at high power but for 800 V the additional losses exceeding the secondary side semiconductor losses by a large margin. The asymmetric power loss between primary and secondary side has to be considered when reaching the maximum power dissipation of the MOSFET modules because it limits the overall power throughput of the DAB even for $V_{DC1} = V_{DC2}$ operation.

V. CONCLUSIONS

In this paper a 500 kW Dual Active Bridge with a switching frequency of 20 kHz using 1.2 kV MOSFETs is presented. Important design criteria for a high power DAB are discussed and the influence of parasitic components (mainly the MOSFET output capacitance C_{oss} ,

AC resistance R_{AC} and transformer parasitic capacitances C_w and C_C), that specifically appear with low AC inductances necessary for high power transfer ratings, are explained. The influence of the main parasitic effects on the efficiency and operation of the DAB at different DC voltages was investigated by measurement and theoretical assumptions were validated. For that a calorimetric measurement for loss decomposition was presented. It can be observed that the influence of parasitics is decisive for the operation and efficiency of a high power DAB. The DAB prototype has demonstrated a peak power of 504 kW and the maximum efficiency of $\eta = 98.24\%$.

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