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A modular signal processing platform for grid and motor control, HIL and PHIL applications

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***Abstract*- In this paper a highly performant modular and fully adaptable real-time signal processing platform is introduced, which can be used to control all kinds of applications in the field of power electronics and electrical drive control, such as Hardware-in-the-Loop (HIL) systems, Power Hardware-in-the-Loop (PHIL) systems and power electronic systems for grid and drive applications. The proposed system was fully developed and built in the ETI, enabling full access to even the last register inside the FPGA and the whole software architecture. Another benefit of the in-house production is, that the costs are very low compared to proprietary system on the market and hence every researcher in the ETI has access to it. With this high-performance real-time signal processing platform, it is possible to push high performance research topics in the field of power electronics and electrical drive control forward.**

Keywords— HIL, rapid control prototyping, signal processing, system-on-chip

I. Introduction

The number of variable-speed drives (VSD) has increased significantly in recent years and will increase much more in the next decade. This increase is driven by two effects: First, higher efficiency standards, which also include partial loads, lead to a conversion of existing infrastructure towards VSD, e.g. for pumps, fans, etc. [1, 2]. Second, due to the new CO_2 standards for passenger cars of the European Union (EU) [3] and the improvement of electric vehicles (EV), the new registrations of EVs in EU was raised from 56000 cars in 2015 to 341000 cars in 2020 and is still increasing fast [4]. Driven by this trend, however, the requirements in the development of such drives are also increasing with regard to functionality, reliability and safety as well as the development costs and thus the development time. In order to meet these increasing requirements, both the development process and the development tools for VSD must be further improved in the same manner. As a result of this development, four main test or simulation levels can be distinguished today: Software-in-the-Loop (SIL), Hardware-in-the-Loop (HIL), Power Hardware-in-the-Loop (PHIL) and conventional motor test benches [5].

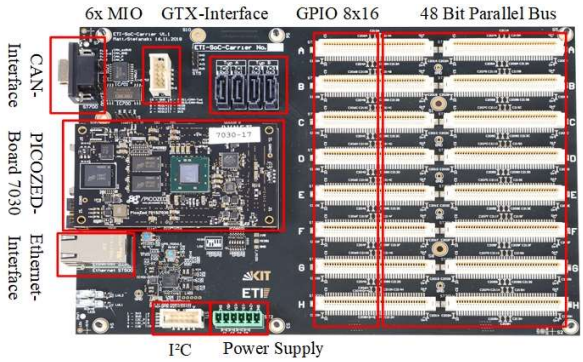


Fig. 1: Signal processing system mainboard

For HIL, PHIL, motor test benches and grid control a performant, modular and open signal processing system is mandatory enabling full access to all design layers. This is not the case with commercially available systems for rapid control prototyping like dSpace, Imperix or CompactRIO or for emulation (AVL-SET or Egston Power). Since many years such systems have been developed and were used in the ETI. This paper will present the latest version of it. In section I the concept is described based on the used System-on-Chip (SoC). In section II, the hardware of the proprietary developed system and the corresponding requirements are discussed. Afterwards, the software structure is illustrated in chapter III. In section IV, the designed workflow for the implementation of a control algorithm or a machine model on the signal processing system is described. Finally, Section V shows the utilization of the signal processing system for a HIL-system and a motor test bench with the corresponding measurement results demonstrating the performance of the system.

II. Signal Processing System Platform

Since the signal processing system platform is supposed to be used in different applications, e.g. as a Real-Time Simulation System (RTSS) for a HIL system or as a central control unit (CCU) for a motor test bench or even as the RTSS and CCU of a PHIL system, the platform has to be very versatile. Therefore, the signal processing system

Table 1: Characteristics of the SoM *PicoZed7030* and SoC *XC7Z030* [6, 7]

	PicoZed 7030
Processor Core	Dual Core ARM Cortex A9
On-Chip Memory	256 KB
Peripherals	CAN, UART, I2C, ...
Clock Rate	667 MHz
Computer Performance	1334 MFLOPS
Memory	1 GB DDR
Ethernet	10/100/1000 Mbit
Programmable Logic	Kintex-7
Logic Cells	125 000
PL IOs	250

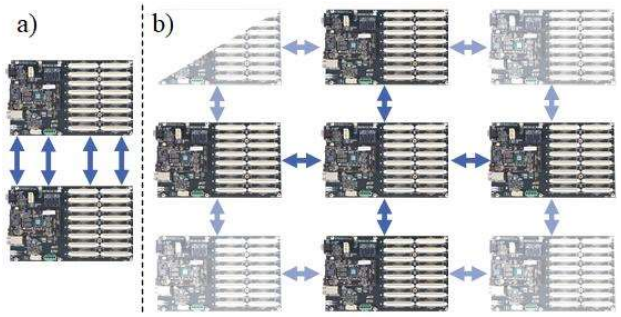


Fig. 2: Two possible Topologies for the GTX-Communication, a) 4 parallel bus between two mainboards, b) Cluster Topology with several mainboards

platform consists of a mainboard with several different expansion cards (EC) so that the range of functions can be adapted for different applications. In Fig. 1 the developed mainboard is depicted.

On the mainboard, the System-on-Module (SoM) *PICOZED 7030* is used. Its central logic chip is the System-on-Chip (SoC) *XC7Z030* from the SoC family Zynq-7000 manufactured by Xilinx [6]. It consists of the dual-core ARM *Cortex-A9* and the Kintex®-7 FPGA [7]. In Table 1, the important characteristics of the SoM and its SoC are listed. The four GTX interfaces of the Zynq are usable over SATA sockets on the mainboard. GTX is a Xilinx high-speed serial protocol which offers a data rate up to 6.6 Gbit/s [8]. With these interfaces it is possible to cluster several mainboards to one big system to increase the computing power of the system and the number of IOs. The mainboards can be connected in any topology and for higher data rate between two boards paralleling of multiple connections is also possible, as can be seen in Fig. 2.

Besides that, the mainboard provides a CAN-Interface, an SPI-Interface and an Ethernet-Interface. The data transfer to the Human Machine Interface (HMI) is carried out over Ethernet. Thus, a remote access to the signal processing system with a standard personal computer (PC) is possible. On the PC a LabVIEW based Monitor Control Tool (MCT) is used as the HMI, which was also developed in the ETI. There are eight slots for expansion cards. Each slot is directly connected with 16 IOs to the SoC-FPGA. Additionally, a 48-bit parallel bus is implemented which enables a communication between the eight expansion cards. The mainboard passes 5 V, ±15 V and 24 V from the power supply board (see Fig. 3 left) to the expansion cards and additionally generates 1.8 V and 3.3 V. In Fig. 3, the complete 19" signal processing system, consisting of two mainboards which communicate via GTX with each other, several expansion cards and the power supply board (left) is shown.

Fig. 3: 19"-Sub-Rack with two mainboards, several expansion cards and the power supply board on the left

A vast variety of expansion cards with different functions has been developed for the eight expansion card slots. The most important of these which also form the basis for the applications shown in Section V are discussed in the following.

A. Analog-Digital Interface Expansion Cards

There are two ECs that operate as the analog interface of the ETI-SoC-System, the ADC-EC and the HV-ADC-EC. Both based on the same ADC-chip, the *LTC2325-16* with four analog inputs which are simultaneous sampled with 5 Msps/Ch. The ADC-Chip has a resolution of 16 bits. The analog front-end of the ADC-EC allows an input voltage range of +/- 10.24 V for 12 analog channels. The latency of the whole measurement acquisition, consisting of the analog front-end, the analog-digital conversion, the digital interpretation of the data in the FPGA and the clock domain crossing is only 410 ns which is mandatory for HIL and PHIL applications.

The HV-ADC-EC has the same ADC chip but the analog front-end differs. At the HV-ADC-EC the analog front end is design for an input voltage range of +/- 1000 V. Since the ETI-SoC-System operates only with protective low voltage, the HV-ADC-EC is splitted in two PCBs. The analog front-end and the ADC-chip are placed on an external PCB. On this external PCB, a digital galvanic isolator (*MAX22445*), ensures that the ETI-SoC-System has no galvanic connection to the high voltage parts. In the ETI-SoC-System, a processing board is used for the communication to the external PCBs. The data transfer is done over Ethernet CAT7 cables via LVDS which features high immunity to EMI present in the testbench environment. The processing board can communicate with two external HV-ADC-ECs each with four analog channels so that eight analog high voltage signals can be interpreted with one slot of the ETI-SoC-System.

If not all voltage measurement channels have to be used, the data direction of the LVDS channels can be configured

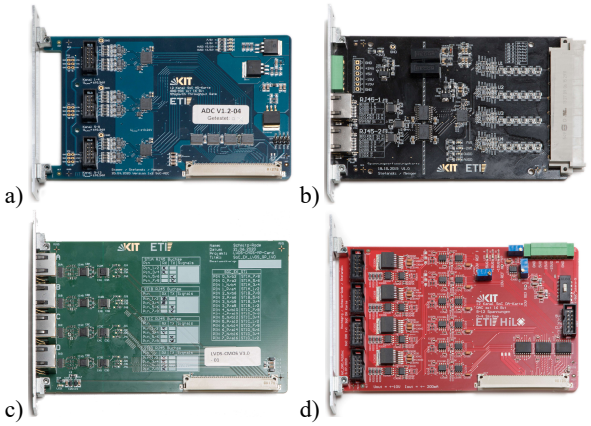


Fig. 4: Expansion cards for analog interfacing, a) ADC-EC, b) HV-ADC-EC, c) LVDS-EC, d) DAC-EC

individually with jumpers. Thus, any other LVDS-based interface can be realized quickly. For example, these can be isolated delta-sigma ADCs, high performance ADCs with direct LVDS interface, such as the LTC2386-18, or an interface to the local control unit of inverters. The three PCBs for the analog interface of the ETI-SoC-System are shown in Fig. 4.

B. Digital-Analog Interface Expansion Card

The digital-analog converter (DAC) expansion card has been developed as a counterpart to the ADC expansion card and is matched in terms of accuracy. Each channel of the 12 channels is based on the DAC-chip AD5543, which features a resolution of 16 bits and a sample rate of up to 2.27 Msps. The analog stage allows an output voltage range of +/-10 V. For direct emulation of compensation current transformers, four channels can be reconfigured via jumpers as direct current outputs. The signal is amplified by a boosting stage based on the LMH6321TS to a current range of +/-200 mA. During development, Monte Carlo simulations were performed with respect to component scattering and precision resistors were selected accordingly in order to meet the desired accuracy. The whole expansion card can be supplied directly from the ETI-SoC-System or optionally galvanically isolated via an external supply. The PCB of the DAC expansion card is shown in Fig. 4 d).

C. Digital Interface Expansion Cards

The two most important cards for the digital interface of the ETI-SoC-System are the general-purpose input/output (GP-IO)-EC and the fiber optical transceiver (FOC) EC, which are depicted in Fig. 5 a) and b).

The GPIO-EC has 16 channels, each with an individual level shifter IC (*SN74LVC1T45*). The signal direction (input/output), as well as the voltage level (3.3 V/5 V) is set manually for each channel by DIP multiway switches on the PCB. The EC is primarily used as a breakout board during development, to control power contactors, and to connect HMI buttons, LEDs, etc.

The FOC-EC has eight transmitters (AFBR-1624Z) and eight receivers (AFBR-2624Z) with 50 MBd each. It is primarily used as an interface between local control unit (LCU) FPGAs on converters, MMC-cells or other peripherals. A custom UART protocol with data and address bits was developed for data exchange between LCUs and the SoC [9]. The FOC-EC can also be used to directly transmit the gate signal to the power switches of a converter e.g. in medium voltage applications [10].

TABLE 2: OVERVIEW OF THE DEVELOPED EXPANSION CARDS

Expansion Card	Properties
Analog-Digital Converter	12 Channels with ±10.24 V to 16 bit @5 Msps
High Voltage Analog-Digital Converter	4 Channels with ±1000 V to 16 bit @5 Msps
Digital-Analog Converter	8 Channels with ±10 V to 16 bit @1 Msps 4 Channels with ±200 mA @1 Msps
GPIO level-shifter	16 x 3.3 V or 5 V GPIO
Fiber optical transceiver	8x 50 MBd transmitter 8x 50 MBd receiver
Speed Sensor	resolver / incremental encoder option

D. Speed Sensor Expansion Card

A multifunctional expansion card was developed for angle and speed measurements of electrical machines, which supports different types of position encoders. The first assembly option depicted in Fig. 5 c) allows the connection of resolvers. The position tracking loop and signal correction is enabled by the *AD2S1210*, a programmable resolver-to-digital-chip. Programmable gains of the excitation voltage amplifier stage as well as the analog front-end of the sine and cosine tracks allow a fast adaption to different resolver winding ratios.

The second assembly option allows the evaluation of digital encoders and incremental encoders. The input stage for the evaluation of the incremental encoders can be configured in two stages. One front-end enables the evaluation of incremental encoder signals up to 36 V. The other stage is designed for signal levels up to 5 V and an electrical frequency up to 1 MHz. Thus, encoders with a high number of lines can be used at high speeds which improves the resolution. Differential and single-ended signals are supported.

Besides the incremental encoder interface, a digital bidirectional serial interface based on the EIA-485 standard is implemented. Standard industrial position encoders based on the serial protocols SSI, EnDat or BISS can be read out via this interface after the corresponding protocol and state machine has been developed in the FPGA. With its enormously versatile configuration option, the expansion card can be quickly configured for new encoders.

E. Rapid Prototyping Expansion Cards

The expansion cards presented above cover most of the requirements that arise in the context of digital signal processing and control. For the fast integration of new sensors, measuring systems or new converter interfaces as well as for the test of new hardware circuits, one- or two-layer printed circuit boards can be manufactured with simple means (e.g. in the etching process).

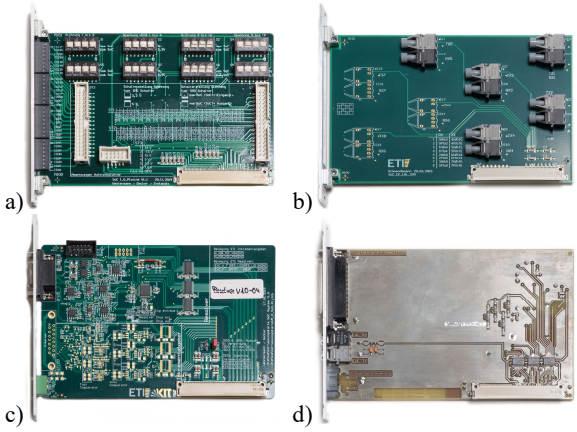


Fig. 5: Expansion cards for digital interfacing, a) GPIO-EC, b) FOC-EC, c) Speed-Sensor-EC, d) internally etched PCB

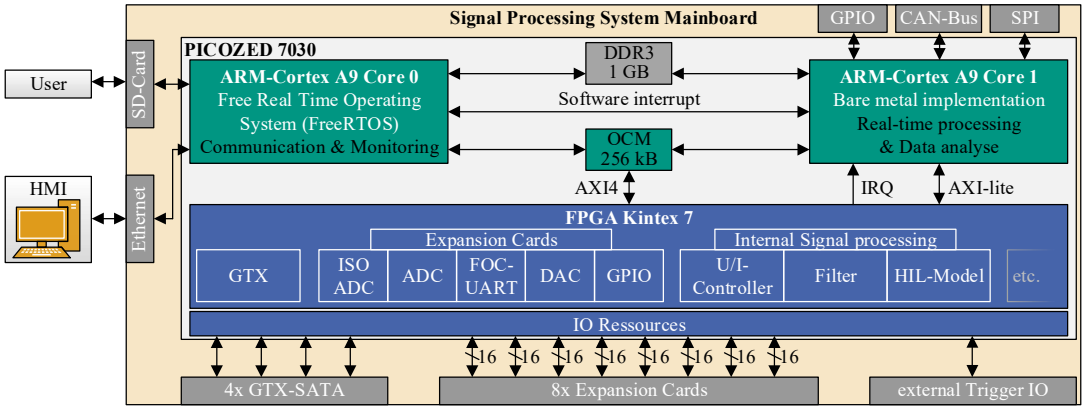


Fig. 6: Block diagram of the system with indicated software partitioning

This supplements the existing portfolio with the possibility to produce own expansion cards extending the functionality of the system with little effort.

To avoid expansion cards with edge connectors, as they are costly and difficult to manufacture, Hirose FX2 series connectors were selected for the connection between the ECs and the SoC-mainboard. These connectors provide high signal integrity but do not require complex soldering and are available in both SMD and THT mounting styles. The prototype of the converter interface card can be seen in Fig. 5 d).

III. SYSTEM ARCHITECTURE

Besides a powerful hardware platform, the used software and the development process significantly influence the performance of the entire system. In this context, the system design must enable fast implementation of new control methods, adaptable measurement data processing as well as the control of the system and visualization. The most important requirements for the system design are:

- Real-time capable implementation and deterministic execution of the control algorithm
- Lowest possible latency in the data exchange between FPGA and processors
- Control of the entire system and visualization of the measurement data on the host PC
- Fast and easy re-configurability of the implemented software, algorithms and expansion cards

In order to meet these requirements in the best possible way, it is necessary to take a detailed look at the structure of the used SoC.

The *Xilinx Zynq 7030* is a heterogeneous system-on-chip consisting of the Processing System (PS) and the Programmable Logic (PL). The PS contains a dual-core ARM Cortex A9 as well as the required peripheral controllers, e.g. CAN, SPI, GPIO, Ethernet, memory controller etc. The two application processors can access a common memory, the on-chip memory (OCM) for low latency data exchange. On the other hand, the PL consists of a Kintex-7 FPGA. The tight coupling of processors and the FPGA allows the best possible partitioning of measurement data processing and control algorithms, as required for a high-performance and high-frequency real-time control systems. A detailed block diagram depicted in Fig. 6 shows the realized software structure. To enable the real-time capability of the control algorithms, an asymmetric multiprocessor structure is implemented. Here, the lightweight real-time operating system FreeRTOS is used on the ARM core 0, which mainly handles communication with the host PC via Ethernet. The kernel is extended by a TCP stack and necessary monitoring and communication tasks between the processors and the HMI. The control algorithms are executed directly on processor core 1 without an underlying operating system as a bare-metal application. Together with the interrupt generation system located in the PL, this ensures the real-time requirement. For monitoring and set point changes, the processor cores exchange data via the OCM with asynchronous software interrupts. The described separation of the network communication on the ARM core 0 and the real-time control on the ARM core 1 leads to a high flexibility of the overall system. Modifications in the software structure only require the executable files to be changed via the Ethernet interface which are then stored on the SD-Card.

In addition to the control algorithms, a performant control system includes the measurement value acquisition and the corresponding data processing, as well as the control of the peripherals and power semiconductors. These functions are implemented in the FPGA of the SoC which serves as the interface to the ECs and via the GTX transceivers to other mainboards. The communication between the FPGA and ARM core 1 takes place via a dedicated high-performance port of the processing system, which provides direct access to the OCM and the DDR. The used protocol is the AXI4, which is part of the widely used Advanced Microcontroller Bus Architecture (AMBA) protocol. To achieve the best possible transfer rate, the data is written directly to or read from defined memory sections of the OCM in a communication burst of variable length. The data is then available to the control algorithm in ARM core 1 for further processing.

In contrast to the previously used data transfer method [11], the configuration of the DMA controller in each interrupt of the ARM core 1 is omitted in the proposed structure. Thus, the execution time is reduced enabling more complex algorithms at a given control frequency.

IV. RAPID PROTOTYPING WORKFLOW

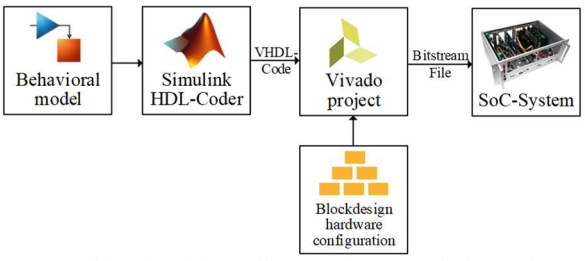
The new possibilities for partitioning signal processing

and control algorithms between ARM core 1 and the FPGA can only be used efficiently if the user is supported by a rapid prototyping software development workflow. By utilizing fully developed hard- and software modules, challenges in the field of machine or grid control, test bench assembly and (P)HIL can be addressed efficiently.

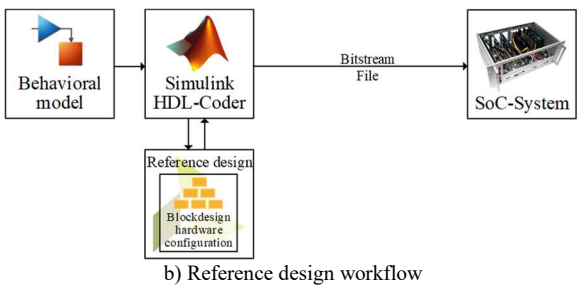
A. General considerations

The first step of the rapid prototyping workflow is to determine which ECs have to be used in the hardware configuration of the ETI-SoC-System for the required application. Then, the FPGA development is carried out in Xilinx Vivado. In addition to the Xilinx IP library, a separate IP core library was developed. This library contains the implementation of the ECs, PWM-modulator-, filter- and communication-blocks as well as the necessary timing and IO constraints. In the block design, the IP cores are easily interconnected to form more complex signal processing algorithms. Communication blocks are also available for data exchange between the FPGA and ARM core 1 of the SoC as well as for the communication between the SoC FPGA and other FPGAs e.g. a local control unit (LCU) FPGA on a converter. The use of interface definitions also eliminates the otherwise necessary and error-prone pin mapping of FPGA pins to the corresponding ECs. After successful synthesis and implementation, the Bitstream is exported for FPGA configuration.

The control algorithm is developed either directly in C or by generating C code from a Matlab/Simulink model. A custom Simulink interface library provides the user abstracted hardware accesses for communication with the FPGA, simple configuration of a CAN communication or access to SPI peripherals directly from the PS as well as blocks for communicating with the HMI. The compiled and executable file is then loaded directly onto the ETI-SoC-System with a LabVIEW based Monitor Control Tool (MCT) via the Ethernet interface and stored on the SD-Card. Furthermore, the FPGA configuration can be replaced and stored on the system via this interface. Thus, the system - both PL and PS - can be adapted quickly and flexibly. This enables efficient hardware/software co-design and thus a rapid development and implementation of novel control algorithms. In addition, the ability to reconfigure the entire software inside the application leads to high flexibility when working with distributed systems.



a) Traditional workflow with manual VHDL-code integration



b) Reference design workflow

Fig. 7: Flow diagram of the used workflows

The described workflow is efficient if the underlying signal processing in the FPGA is not changed and the rapid prototyping takes place on ARM core 1 which is the case for traditional machine or grid control. For model-based rapid prototyping of the FPGA software, as required for the efficient development of high-performance (P)HIL emulators of electric machines [11] for example, an additional procedure is developed. In this case, the FPGA block design with the needed expansion cards is registered in the Simulink HDL coder as a new custom reference design. Callbacks can be used to make the corresponding pins in the FPGA design known to the HDL coder. The model is then developed in an abstracted form in Simulink, utilizing the simulation and validation options as well as the HDL Workflow Advisor. During the VHDL code generation process, the model is connected to the defined interfaces of the reference design. The synthesis and implementation are performed underneath. Hence, the creation of an executable FPGA project can be done completely from Matlab/Simulink. This allows the concentration on the control algorithm, reduces the number of possible errors and speeds up the development process. The flow diagram of the proposed workflow is depicted in Fig. 7.

B. Libraries for Rapid Prototyping

The rapid and efficient development of complex signal processing and control systems is strongly supported by custom libraries at different levels of the development process. This makes it possible to focus on the research questions. The most important libraries are described briefly below.

1) Vivado IP-Repository

The Vivado IP repository manages the in-house developed IP cores for the rapid creation of a block design. Each IP core provides a function programmed and tested in VHDL. Via the GUI, the IP core can be customized for the corresponding project, e.g. for bit widths. The Vivado IP integrator contains its own version management with update function, so that changes and improvements to the IP core can be propagated quickly. Timing and IO constraints can also be defined locally in the IP core, which are then inherited by the main project. This simplifies the handling of clock domain crossing immensely, since the paths can be correctly constraint by design within the IP-core. The custom IP-repository includes more than 90 cores for signal processing, clock domain crossing, interface definitions of the expansion cards, modulators, transformations and filters at the moment and is continuously being further developed.

2) Simulink HDL-Library

The self-developed Simulink HDL library contains Simulink functions that have been optimized with respect to their HDL code generation capability. In particular, the

processing pipeline of the data is deterministically separated by *enabled delay* blocks. This is necessary since in power electronics applications, the calculations often have to be triggered at certain points in time inside one PWM period. A propagating data valid flag then activates the register stages at the correct times when the result of the previous calculation is finished. With that approach feedback loops can be implemented in a very efficient way. This leads to improved timing and thus to lower latencies. Furthermore, the fixed-point representation of the input and output data can be easily controlled via the setting options in the block masks, so that the user is facilitate at this point. For a fast simulation of the functions in Simulink, the *enabled delay* blocks can be deactivated with the help of a script. Currently, the library mainly contains coordinate transformations, trigonometric functions, multidimensional lookup tables, PLLs and the machine models developed for HIL use. Various voltage and current control models for grid connected inverters and dual active bridges as well as a battery HIL model and a near grid impedance model for PHIL applications as well as digital filters and measurement data processing are currently under development and will extend the library in the future.

3) Simulink-Control Library

Whereas the two previously explained libraries mainly aim at the efficient implementation of FPGA functions, functions and models optimized for execution on the ARM Core 1 are stored in the Simulink Control Library. This applies in particular to the various control models for AFE, machine controllers for PMSM and ASM, as well as filters, signal reconstruction and modulation methods. The individual controls are parameterized via script by entering a few route parameters. Using the library, a complex control system can be quickly built up, which can then be executed on the ARM core of the ETI-SoC-System via the C code generation of Matlab/Simulink.

4) Simulink hardware-abstraction-library

In order to fully utilize the hardware resources of the Zynq from the Matlab-C code generation, the hardware commands have to be integrated into Simulink as well. The blocks developed for this purpose are stored in the Simulink-hardware-abstraction-library. The most frequently used blocks are communication blocks for data exchange with the FPGA and monitoring blocks for data exchange with the HMI. In addition, the sending and receiving of CAN messages, the status monitoring of the CAN controllers, the connection of SPI peripherals and the reading and writing of MIO pins are also supported. Fig. 8 shows a simplified processing pipeline in which data is read from the FPGA and forwarded to monitoring.

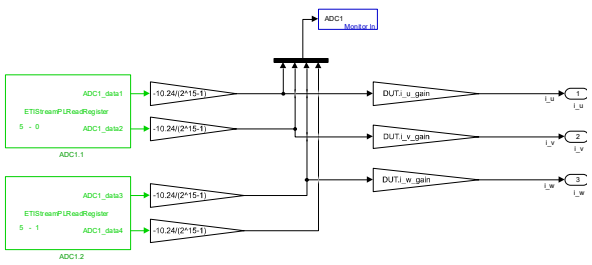


Fig. 8: Excerpt from a control model with FPGA data read (green) and monitoring output (blue)

V. APPLICATIONS

The ETI-SoC-System was primarily developed as a modular platform for controlling electric drive systems, converter systems and test benches. In the following some application examples for the system from the over 42 productive deployments are shown.

A. Hardware-in-the-Loop (HIL) system

The development of control methods in model-based simulation environments, such as Matlab/Simulink, enables fast and efficient testing of the new algorithms. In simulation, however, the influences of the hardware platform can only be reflected with great effort. Since the device under test (DUT) is often not yet available in the early development process, the algorithm is executed on the final hardware platform with an emulated model of the DUT. By using two independent SoC mainboards in a 19" frame - one as a control system and the other as an emulation system - a compact closed loop HIL system is provided.

The hardware setup of the HIL-System is based on the described expansion cards with minor changes. The core of the system is the DAC expansion card, which outputs the analog values of the represented system. For the emulation of the position encoder of the electrical machine, an expansion card was developed, which can selectable emulate a resolver, incremental encoder or sine/cosine encoder. An inverter interface card is used to read the gate signals of the control system.

The model of the implemented electrical drive system consisting of a B6 bridge commonly used at our institution [11] and a nonlinear flux-based PMSM model [12] was developed and verified in Simulink and test bench measurements and implemented on the FPGA of the ETI-SoC-System with the workflow described above. A mechanical load model was partitioned and executed on the ARM-core of the system but this model is not focus of this study.

Depending on their time constants and computational complexity the FPGA sub models are executed with different sample rates. The necessary decoupling between different execution frequencies is done with moving average filters increasing the accuracy during the signal transitions. A detailed overview of the different executions is given in Fig. 9

The inverter model is executed with a sample rate of 100 MHz to be able to detect the fast switching edges in the PWM pattern. By multiplying the DC-link voltage the phase voltages are then calculated from the switching

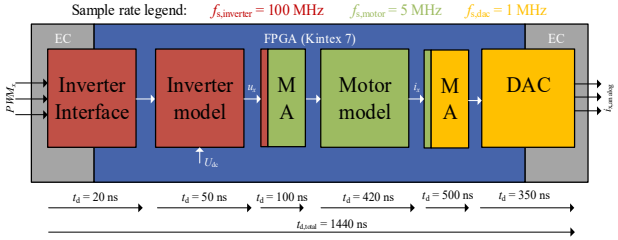


Fig. 9: Timing and sample-rate diagram of proposed HIL-System

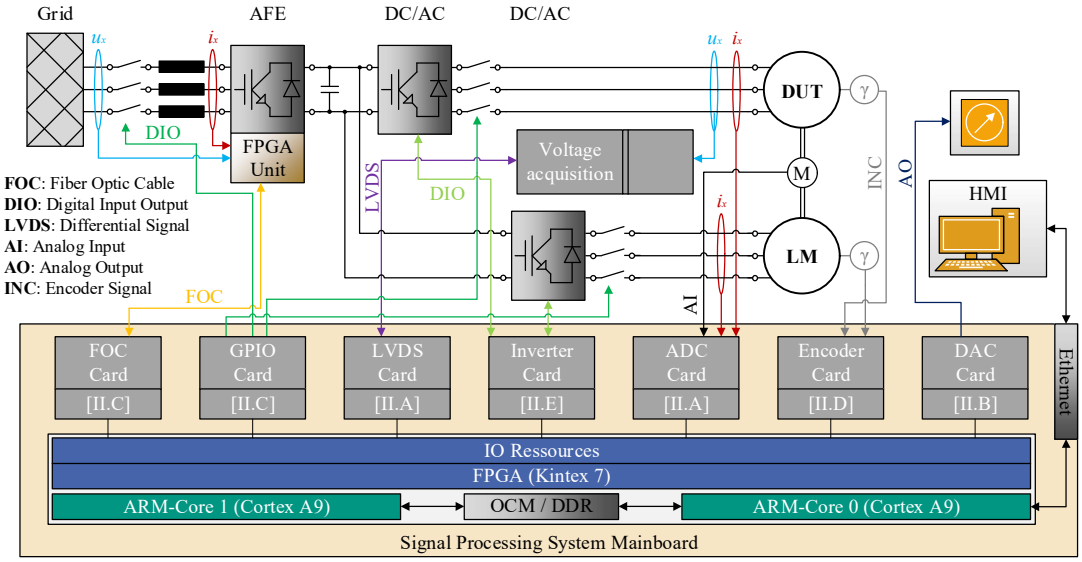


Fig. 10: Block diagram of a typical motor testbench setup based on the ETI-SoC-System

states. The current-dependent voltage drops can also be taken into account to correct the ideal phase voltages if the characteristics of the semiconductor module is known. The reconstructed phase voltages are decimated to the execution frequency of the motor model of 5 MHz via a moving average filter of depth 20. The moving average filter introduces a stochastic deadtime of half its group delay into the loop.

The nonlinear, flux-based PMSM motor model requires 42 FPGA clocks to calculate the new phase currents. This includes the necessary transformations of the phase voltages from the three-phase system into the dq-system and the currents vice versa, the calculation of the machine voltage equations as well as the lookup table accesses to the flux linkage maps. The calculated currents are then handed over to the DAC expansion card by a moving-average filter. In total, the whole HIL model has a stochastic dead time of 1.44 µs. This includes the signal propagation times from the hardware on the expansion cards, the digital-to-analog conversion, and the complete computation time in the FPGA. This dead time is acceptable for HIL operation, since it can be compensated in the closed loop system.

To show the performance of the HIL emulator, first measurements were performed. The first measurement shows the emulated machine current waveform of a single phase in closed-loop operation. On the control side, a standard PI-current controller in rotating frame with an execution frequency of 8 kHz was used. The pulse width modulated gate signals were then fed to the HIL emulator to calculate the current response of the emulated drive system. In Fig. 11 the measurements of the control system's integrated logic analyzer are presented. The mean dead time of 1.44 µs for model calculation and DA conversion on the HIL side as well as the time for AD conversion on the control side is back calculated in the post processing. Additional differences between the switching times and the expected current ripple can be explained by the emulated gate interlock time as well as quantization errors of the AD/DA conversion.

B. *Motor testbench*

The presented system is also used to control modular motor testbenches in order to be able to test the developed motor prototypes and control algorithms in real applications. By using the described expansion cards, the necessary functions and measurement points can be quickly set up and integrated. Fig. 10 shows a typical setup of a motor test bench. The two motors are coupled via a torque measuring shaft and are each controlled by their own drive converters. In the simplest case, the drive converters share a common DC link, so that only the losses of the electromechanical system have to be supplied which are directly fed from the grid by an AFE. In order to reduce the computing load on the ETI-SoC-System, the AFE is equipped with a LCU FPGA on which the DC link voltage control is executed. Thus, only the voltage setpoints have to be communicated via FOCs which makes the system immune to interferences. The control of the test bench

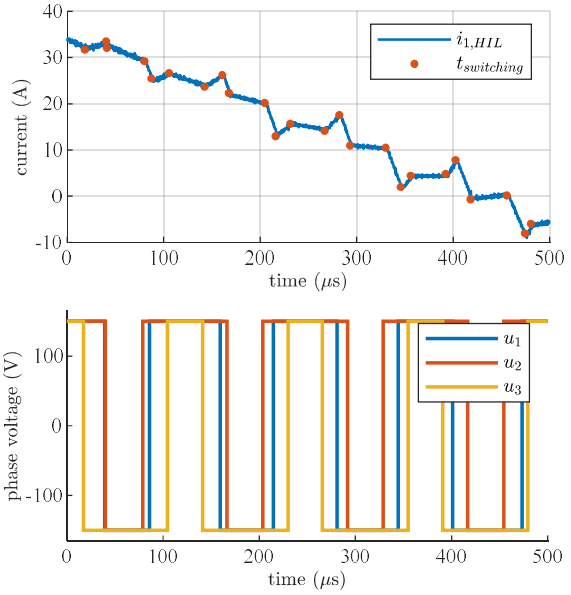


Fig. 11: Emulated current ripple (upper half) with corresponding output voltages (lower half) of the HIL system. Markers represent the switching times

peripherals, such as main contactors, cooling fans and LED indicators, is done via the GPIO expansion card with a test bench specific adapter PCB. For the necessary measurements, the described extension cards can be used modularly which allows fast adoption to the demands of a new measurement setup. Since the measured values are available at high sample rate in the FPGA, adapted signal preprocessing can be implemented, which relieves the further signal processing in the control. Based on the simple example, other measurement and inverter or converter configurations of any complexity can be implemented easily and quickly [10, 13, 14].

VI. CONCLUSION AND FUTURE WORK

In this paper, a flexible and powerful signal processing system based on a SoC was presented, which was fully developed and produced in the ETI. The modular design with interchangeable expansion cards allows easy and fast hardware customization. By using adapted rapid prototyping workflows - for the processor as well as for the FPGA - the used algorithms can be reconfigured quickly. This allows an application in the field of machine and grid control, as well as for the development of HIL and PHIL emulators. The performance of the overall system was demonstrated by presenting first measurement results from a HIL emulator of an electric drive system based on the new system.

As mentioned above, the ETI-SoC-System is applicable in wide areas of research [14], for motor and grid control [15, 16] as well as for HIL and PHIL [9, 17] applications. Although the current performance allows a use in a wide research area, a continuous further development of the system is planned and has already started. The use of wide bandgap semiconductors with very high switching frequencies places high demands on measurement acquisition and control. For this reason, the next generation of the system will include ADC and DAC expansion cards with higher sample rates as well as the *Xilinx Kria K26* SoM which is equipped with a significantly increased number of IO, FPGA and processor resources. This will enable the creation of a future-proof signal processing platform based on previous work.

REFERENCES

[1] *COMMISSION REGULATION (EC) No 640/2009 of 22 July 2009 implementing Directive 2005/32/EC of the European Parliament and of the Council with regard to ecodesign requirements for electric motors: CELEX32009R0640*, 2009.

[2] *COMMISSION REGULATION (EU) 2019/1781 of 1 October 2019 laying down ecodesign requirements for electric motors and variable speed drives pursuant to Directive 2009/125/EC of the European Parliament and of the Council: CELEX32019R1781*, 2019.

[3] *REGULATION (EU) 2019/ 631 OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL - of 17 April 2019 - setting CO2 emission performance standards for new passenger cars and for new light commercial vehicles, and repealing Regulations (EC) No 443 / 2009 and (EU) No 510 / 2011*, 2019.

[4] European Environment Agency (EEA), *Electric cars registered in the EU-27, Iceland, Norway and the United Kingdom.* [Online]. Available: https://www.eea.europa.eu/data-and-maps/indicators/proportion-of-vehicle-fleet-meeting-5/assessment (accessed: Oct. 8 2021).

[5] A. Bouscayrol, "Different types of Hardware-In-the-Loop simulation for electric drives," in *IEEE International Symposium on Industrial Electronics, 2008*, pp. 2146–2151.

[6] Avnet, Inc., "PicoZed™ 7Z015 / 7Z030 SOM Hardware User Guide,"

[7] Xilinx, Inc., "Zynq-7000 SoC Data Sheet: Overview (DS190),"

[8] Xilinx, Inc., "7 Series FPGAs GTX/GTH Transceivers User Guide (UG476),"

[9] R. Schwendemann, D. Schulz, L. Stefanski, and M. Hiller, "A 60 kW Power Hardware-in-the-Loop Test Bench for grid emulation based on a Series Hybrid Cascaded H-Bridge Converter," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*.

[10] S. Mersche, R. Schreier, P. Himmelmann, and M. Hiller, "Medium Voltage Power Electronic Building Block for Quasi-two-level Operation of a Flying Capacitor Converter," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE)*.

[11] R. Schwendemann, S. Decker, M. Hiller, and M. Braun, "A Modular Converter- and Signal-Processing-Platform for Academic Research in the Field of Power Electronics," in *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata, May. 2018 - May. 2018, pp. 3074–3080.

[12] L. Stefanski, R. Schwendemann, D. Bernet, M. Widenmeyer, A. Liske, and M. Hiller, "Cascaded H-Bridge based Parallel Hybrid Converter – A new Voltage Source for Power-Hardware-in-the-Loop Emulation Systems," in *2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL)*.

[13] J. Stoss *et al.,* "Design of an Intelligent, Modular IGBT/SiC Inverter Platform up to 400 kW for Fast Realization of New Test-Bench Concepts," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–8.

[14] F. Yüce and M. Hiller, "Investigation of Bond Wire Lift-Off by Analyzing the Controller Output Voltage Harmonics for the Purpose of Condition Monitoring," in *2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe)*, Lyon, France, Sep. 2020 - Sep. 2020, P.1-P.10.

[15] S. Decker, J. Stoss, A. Liske, M. Brodatzki, J. Kolb, and M. Braun, "Online Parameter Identification of Permanent Magnet Synchronous Machines with Nonlinear Magnetics based on the Inverter Induced Current Slopes and the dq-System Equations," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*.

[16] D. Braeckle, P. Himmelmann, L. Groll, V. Hagenmeyer, and M. Hiller, "Energy Pulsation Reduction in Modular Multilevel Converters Using Optimized Current Trajectories," *IEEE Open J. Power Electron.*, vol. 2, pp. 171–186, 2021, doi: 10.1109/OJPEL.2021.3065115.

[17] L. Stefanski *et al.,* "A novel high dynamic six phase 120 kW Power Hardware in the Loop Emulation Test Bench for emulating AC/DC Grids and Electrical Machines," in *2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*.