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TERAHERTZ SAMPLING RATES WITH PHOTONIC TIME-STRETCH FOR ELECTRON BEAM DIAGNOSTICS

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Abstract

To understand the underlying complex beam dynamics in electron storage rings often large numbers of single-shot measurements must be acquired continuously over a long period of time with extremely high temporal resolution. Photonic time-stretch is a measurement method that is able to overcome speed limitations of conventional digitizers and enable continuous ultra-fast single-shot terahertz spectroscopy with rates of trillions of consecutive frames. In this contribution, a novel ultra-fast data sampling system based on photonic time-stretch is presented and the performance is discussed. THERESA (TeraHErtz REadout SAmpling) is a data acquisition system based on the recent ZYNQ-RFSoC family. THERESA has been developed with an analog bandwidth of up to 20 GHz and a sampling rate of up to 90 GS s^{-1}. When combined with the photonic time-stretch setup, the system will be able to sample a THz signal with an unprecedented frame rate of 8 Tf s^{-1}. Continuous acquisition for long observation times will open up new possibilities in the detection of rare events in accelerator physics.

INTRODUCTION

Many scientific applications and experiments, especially in particle accelerator physics, require the continuous observation of non-repetitive and statistically rare events occurring on very short time scales. This imposes high technological challenges on Data Acquisition (DAQ) systems such as oscilloscopes. One of them is the limited temporal resolution of commercially available Analog-to-Digital-Converters (ADCs) [1]. In 1999 a first demonstration of a concept to overcome this limitation was presented [2]. To relax the demands on the data converter performance, prior to digitization, the signal under investigation is stretched in time using chirped optical pulses and the chromatic dispersion in optical fibers. This concept, also called Photonic Time-Stretch (PTS), is already successfully employed in combination with a real-time oscilloscope at the SOLEIL (Source optimisée de lumière d'énergie intermédiaire du LURE) synchrotron facility [3].

The second limitation is the short contiguous acquisition time of commercially available oscilloscopes, which is in the range of few milliseconds. Therefore, the continuous acquisition over long observation time (up to hours), e.g. for the study of the evolution of electron bunch profiles on a turn-by-turn basis, is not possible. To overcome these limitations THERESA, a new digitizer system suitable for PTS measurements, has been developed. THERESA consists of sixteen parallel sampling channels operating in time-interleaved mode, which enables a sampling rate of over 90 GS s^{-1} [4]. In the next sections an overview of the system is given and a description of the firmware architecture and calibration strategy is discussed.

ARCHITECTURE

The digitizer architecture with the photonic time-stretch system is shown in Fig. 1. It consists of an optical time-stretching path, developed at Lille University [3], a fast photo-detector and the THERESA sampling system. THERESA contains a wideband power-divider, a sampling board and a readout card based on the recent ZYNQ-RFSoC technology.

Time-Stretch Setup

The general principle of PTS is shown in Fig. 1. A broadband, chirped carrier laser pulse is fed through an electro-optical crystal which encodes the ultra-fast signal to be sampled onto to the laser pulse. The modulated laser pulses are then stretched in time by means of a long dispersive fiber until their duration is in the order of nanoseconds. The factor S, by which the pulse is slowed down, can be calculated by

$$S = 1 + \frac{L_2}{L_1}, \tag{1}$$

where L_1 and L_2 are the lengths of the two fibers [1, 3].

Sampling Board

The stretched and modulated pulse from the PTS is split into 16 identical signals by an active power divider. Each signal is fed into the individual channels on the THERESA card. High-bandwidth Track-and-Hold Amplifiers (THA) [5] device are employed to sample the input signal at a high rate. The sampling clock of the THAs is individually delayed by picosecond programmable delay chips [6]. One key feature of the THERESA architecture is its high flexibility in the sampling operation. The system can operate either in continuous or in single-shot sampling mode. In continuous mode, the phase of the sixteen parallel sampling channels are equally distributed over the sampling interval, which can

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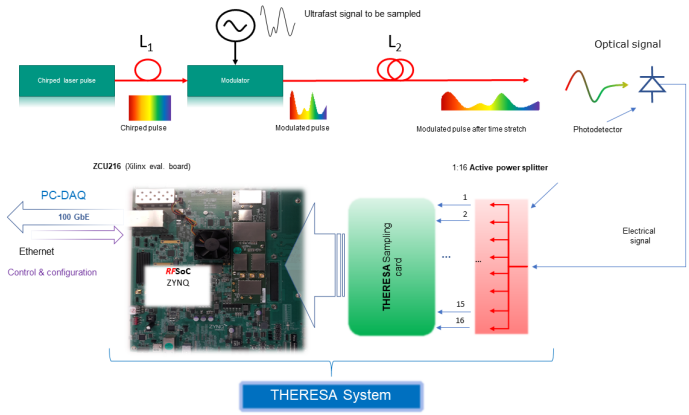

Figure 1: Architecture of the photonic time-stretch setup and the THERESA digitizer [4].

be a multiple of the sync clock period, as shown in figure Fig. 2.

In the single-shot sampling mode, the phase of sixteen sampling channels is set with a minimum time distance of 11 ps. In this mode, the system will sample an input signal at the frame rate of 90 GS s^{-1} [4].

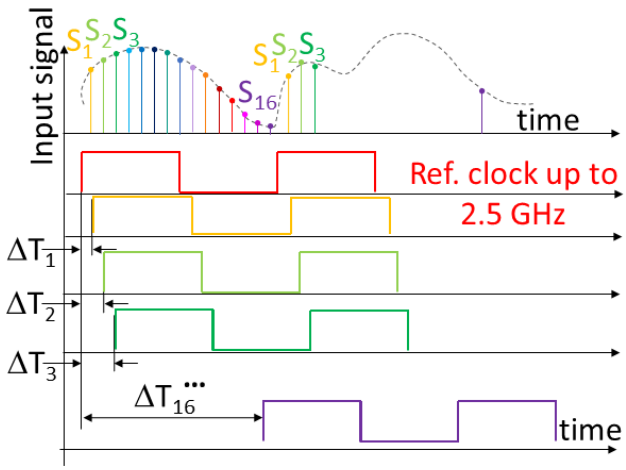

Figure 2: Working principle of the THERESA system in continuous mode [4].

Readout Card

The THERESA sampling card is connected to the Xilinx ZCU216 evaluation board, which is based on a ZYNQ UltraScale+ Radio Frequency System-on-Chip (RFSoC). This RFSoC integrates a Programmable Logic (PL), a Processing System (PS), sixteen 12-bit RF-ADCs and 14-bit RF-DACs, operating up to 2.5 GS s^{-1} and 10 GS s^{-1} respectively. Furthermore, the RFSoC hosts many peripherals on one single chip and, therefore, is an ideal platform for the integration of PL and System-on-Chip for data processing.

FIRMWARE

The THERESA sampling board integrates two DAC channels for the generation of test signals that can be employed for the test and calibration of the sampling channels. Therefore, the first important tasks of the firmware are the generation of the calibration signal and the data acquisition from the sampling channels. The firmware architecture employed for the calibration of the system takes advantage of the Xilinx RF Evaluation Tool [7], which provides an evaluation software combined with a hardware test platform for data generation and acquisition. The hardware-test platform can be easily extended with custom designs according to user requirements. The simplified block diagram of the current firmware is shown in Fig. 3. The data generated by the PS are stored to an external DDR memory via Direct Memory Access (DMA) and then converted to an analog signal by the Xilinx RF data converter Intellectual Property (IP) block. The signal from the DAC channels is propagated to the sampling channels on the THERESA board and digitized by the ADCs integrated in the RFSoC. The digital samples from the ADCs are temporarily stored in the memory and accessed by the processor for further data analysis. The PS hosts an embedded Linux system with an user space application that allows the access to all peripheries and communicates with the evaluation tool software. The software implements control, data generation, acquisition, visualization and analysis functions and, therefore, provides all necessary tools for assessing the THERESA system performance.

CALIBRATION AND CHARACTERIZATION

The software [7] provides all the tools necessary for characterization and calibration of the system. Online spectral analysis is performed on the acquired signals and presented to the user for a fast way of analyzing the spectral components. Furthermore, dynamic performance characteristics such as the Total Harmonic Distortion (THD), Signal-to-Noise Ratio (SNR) and Effective Number of Bits (ENOB) can be computed by the software. The calibration of the THERESA system is necessary to correct several mismatches intrinsic to the time-interleaving sampling method, like the additional spurs in the spectrum due to offset, gain,

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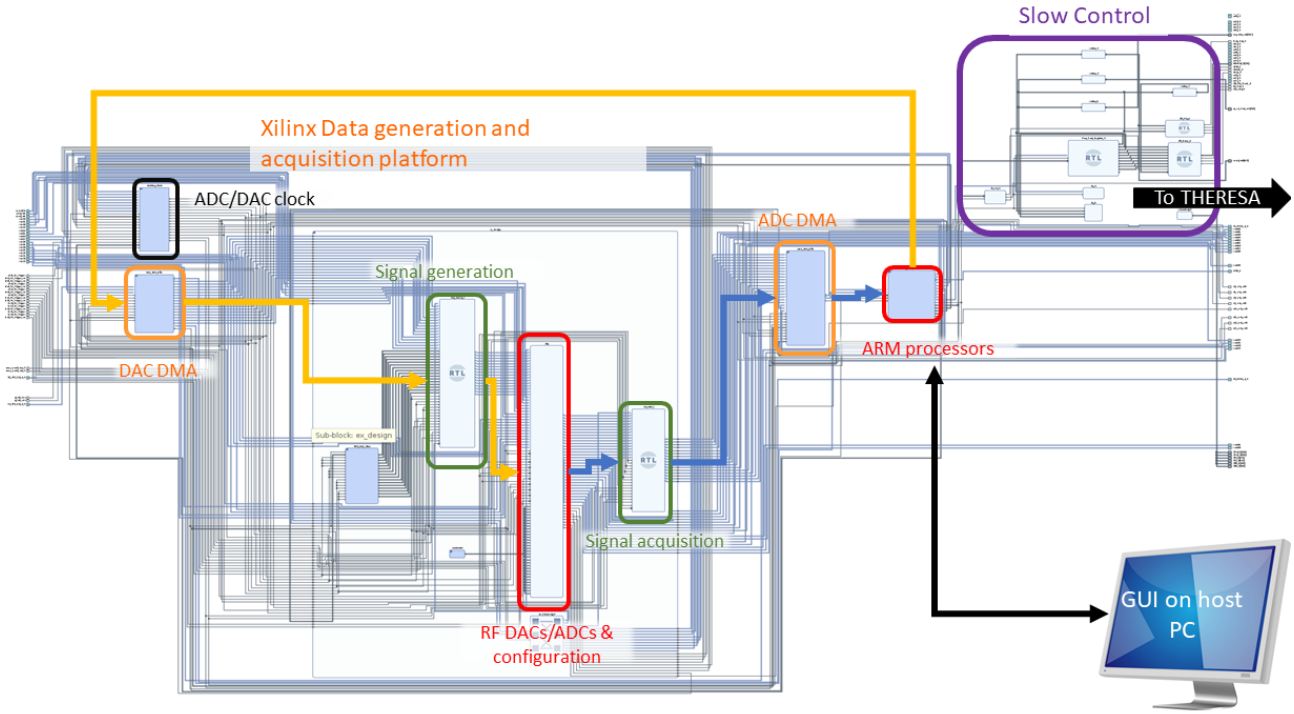

Figure 3: Block diagram of the firmware. It consists of the Xilinx RF evaluation platform [7] for signal generation, acquisition and the slow-control interface for configuration of the sampling board components. The processor hosts an embedded Linux system and is responsible of the communication with the RF Evaluation GUI running on a PC.

timing and bandwidth mismatches of the ADCs. Gain mismatch creates a frequency spur at f_s/M, while all of the other mismatches create components at $f_s/M \pm f_{IN}$, where f_s is the sampling frequency, M the number of ADCs in the array and f_{IN} the frequency of the input signal[1] [4, 8]. The offset and gain mismatches can be measured by applying a low frequency signal by the DAC. In order to compensate these mismatches, one ADC is taken as reference and the offset and gain of the other converters are matched to it. Phase and bandwidth mismatches can be measured by applying sinusoidal signals with different frequencies as described in [4]. To reduce these mismatches, the sampling clocks and analog traces are routed with a precise timing/length match in order to have a time skew down to 1.2 ps.

An example test setup for characterization and calibration is shown in Fig. 4. The output from the DAC channel is fed back via a power-divider to four ADC channels. The data converter reference sampling clock is provided by the Phase-Locked Loop (PLL) on the sampling board.

CONCLUSION

The measurement of events occurring in the time range of femtoseconds over long observation times poses great technological challenge on DAQ systems. It requires carefully designed high-bandwidth and low-noise sampling circuits and a readout systems capable of high data-throughput and processing. The latest generation of ZYNQ UltraScale+ RF-

[1] Assuming equidistant sampling points.

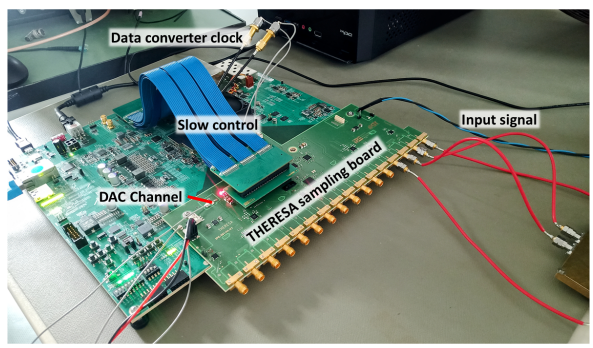

Figure 4: THERESA test setup for characterization and calibration.

SoC has proven to be an efficient platform that simplifies hardware and software design. The THERESA sampling system is a result of a close collaboration between engineers and beamline scientists. This collaboration has produced one of the fastest digitizer available in the scientific community with an analog bandwidth up to 20 GHz and a sampling rate up to 90 GS s^{-1}. When combined with the PTS setup developed at Lille University, the system will be able to sample an incoming optical signal with an unprecedented frame rate of 8 Tf s^{-1}. The continuous acquisition for long observation times by high data throughput readout electronics will open up new possibilities for real-time data processing and fast detection of rare events nowadays considered very difficult to observe.

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