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Institute:	Karlsruhe Institute of Technology (KIT) Elektrotechnisches Institut (ETI)
Type:	Conference Proceedings
Published at:	2022 IEEE 23rd Workshop on Control and Modeling for Power Electronics (COMPEL), Tel Aviv, June 20-23, 2022 Year: 2022 ISBN: 978-1-6654-1081-6
Hyperlinks:	DOI: 10.1109/COMPEL53829.2022.9830034

Hardware-in-the-Loop Setup for a Modular Multilevel Converter with Integrated Batteries

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***Abstract*—A hardware-in-the-loop setup to emulate a modular multilevel converter (MMC) with batteries integrated in its submodules is presented. It allows the testing of control methods without a real converter. A state-space MMC model is introduced, extended by RC battery models and implemented on an FPGA. The scalability of battery models for converters with large numbers of submodules is shown. The emulation closes the loop for a combined MMC-controller and battery management algorithm under test, running on an ARM processor. Given the modular approach, the level of detail for power electronics, batteries and control schemes can be adapted independently.**

***Index Terms*—Hardware-in-the-loop, HIL, MMC, Power Converter, Battery, Simulink, FPGA, Real-time**

I. Introduction

An MMC consists of three phases, each divided into an upper (p1, p2, p3) and lower arm (n1, n2, n3). Each arm is made up of multiple submodules, connected in series. A submodule includes an electrical energy storage and power electronics to connect the submodule's outputs to the energy storage or bypass it. The topology allows a bidirectional power exchange between its AC and DC side.

Here, the energy storage is a battery module and is connected to the submodules' outputs by a full bridge. These submodules are called Power Electronic Storage Blocks (PESB) hereafter. In Fig. 1, an overview of the topology with 20 PESBs per arm and a nominal power of 100 kW is given.

In contrast to typical battery storage systems for grid integration, the topology allows the combination of small and diverse battery modules. The PESBs can individually be equipped with a battery module of high energy, high power, or even a used battery module that is given a second life.

Hardware-in-the-loop (HIL) is an established approach in the development of both battery management system (BMS) algorithms [1], [2] and control methods for power converters [3], [4]. The HIL approach reduces development time and risks due to critical conditions for both, batteries and power electronics. In this paper, the MMC topology with integrated lithium-ion batteries is emulated, combining both of the above. HIL testing allows faster control system tests in real-time, enabling deployment of hybrid control and energy management strategies as in [5], [6], while being true to the real system, its interfaces and limits. This is an advantage over Software-in-the-Loop simulations sometimes used [7].

The authors acknowledge the financial support by the Federal Ministry for Economic Affairs and Climate Action of Germany in the project LeMoStore (project number 03EI4031B).

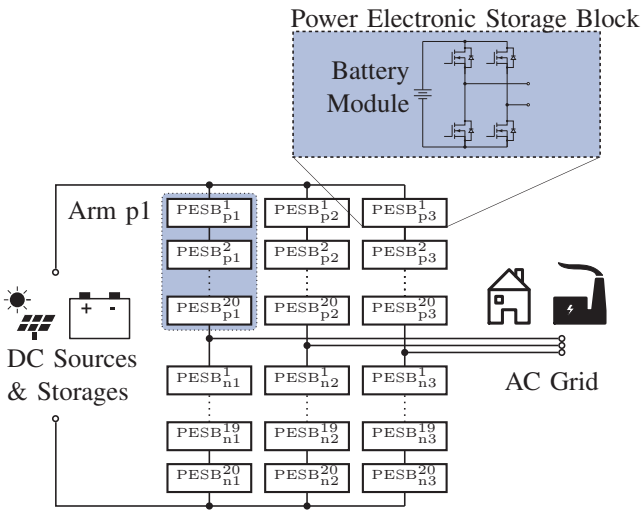

Fig. 1. Schematic overview of the MMC with integrated batteries.

In the following, the implementation of the HIL emulator on an FPGA with an MMC model and battery models is shown. The implementation on an FPGA offers advantages in scalability and performance due to its parallel logic [8]. Finally, the HIL setup is verified by tests of an exemplary control strategy including battery management.

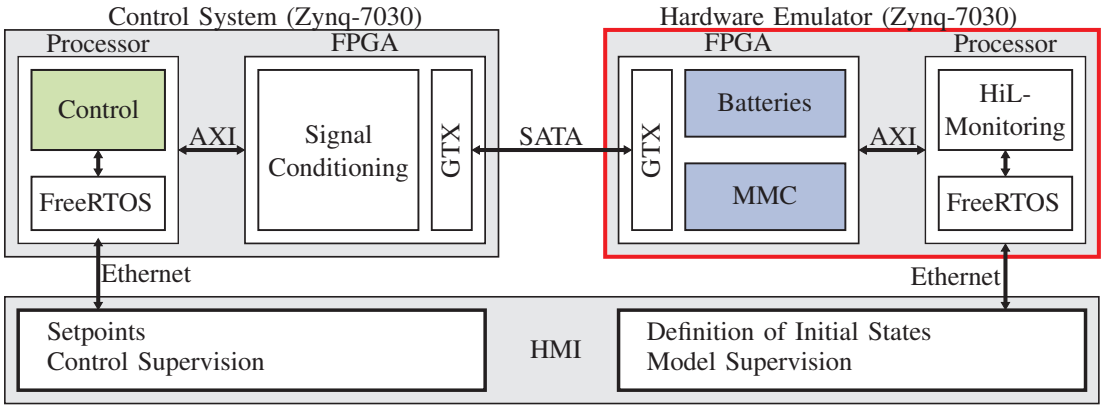

Fig. 2. Schematic overview of the HIL system. Control and emulator platform are based on the same hardware.

II. Hardware-in-the-Loop Platform

The HIL setup utilizes a system-on-chip platform based on the Zynq7030 [9], [10]. The setup is already in use for the control of power converters. Using the same platform for control and HIL emulation unifies the toolchains and interfaces and reduces development time.

Fig. 2 shows a schematic of the complete setup, Fig. 3 shows the real setup. The control system is the device under test. The focus of this paper is the hardware emulator, emulating the MMC as well as the batteries. It is interfaced with the controller by a digital GTX interface. Through this interface, it would also be feasible to connect multiple Zynq-Z7030 for larger setups. For the setup shown here, this is not required. The HMI is connected via Ethernet to both controller and emulator. The Zynq-Z7030 processor is running at 667 MHz, and the FPGA clock for the models shown later is set to 100 MHz. Both, the MMC model and the battery models are emulated on the FPGA. This achieves high clock rates and good scalability of the battery models, which is important for the high quantities of battery modules used in the MMC topology. For an efficient implementation, restrictions of fixed-point representation and timing constraints must be taken into account. The ARM core is left to realize monitoring functions. The controller running on the control system is also implemented on the ARM core.

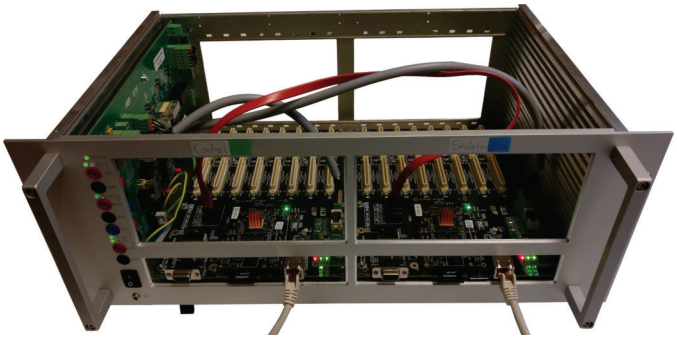

Fig. 3. Hardware-in-the-loop setup, the loop is closed with a digital interface over the cable in red.

To improve consistency and enable a fast transition from Simulation to HIL, VHDL and C-Code are both generated from Simulink. Bitstream generation for the FPGA is done from Simulink HDL coder using a Vivado Reference Design.

III. Modelling the MMC

In order to model the MMC, a state-space model is implemented as shown in [11]. The model uses averaged voltages and currents and transformations between the physical in- and outputs and the state-space variables. The presented HIL implementation of the MMC is directly based on this approach. The converter model is independent of the battery models which makes the implementation modular. The interface between MMC model and battery model is given by the arm currents which determine the currents for the battery models.

To be FPGA-synthesizable, the discretized state-space equations

$$\underline{x}(n+1) = \underline{A}\,\underline{x}(n) + \underline{B}\,\underline{u}(n) + \underline{F}\,\underline{z}(n) \quad (1)$$

$$\underline{y}(n) = \underline{C}\,\underline{x}(n) + \underline{D}\,\underline{u}(n) \quad (2)$$

from [11] are used, where they are derived in detail. Matrix $\underline{D}$ only contains zeros, additionally Matrix $\underline{F}$ must be considered for the AC and DC grid voltages. A schematic block diagram is shown in Fig. 4. The voltage vector $\underline{u}_{\mathrm{arm,ref}}$ represents the six reference voltages for the arms p1 to n3 set by the controller. The model outputs a vector containing the six arm currents $\underline{i}_{\mathrm{arm}}$. Additionally, the ac currents of the three phases are output as vector $\underline{i}_{\mathrm{ac}}$.

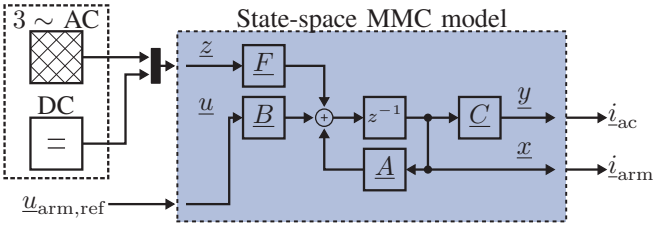

Fig. 4. Schematic MMC model with DC and AC grid.

The MMC model is running at a clock rate of 10 MHz. The matrix multiplications require pipelining registers, leading to an open-loop time of 2.6 µs.

IV. Modeling of Lithium-Ion Batteries

In the presented topology, each PESB contains a battery module. A battery module is here considered as a number of battery cells connected in parallel and in series including a BMS for balancing between the cells and safe operation. For each battery module, one battery cell is modeled and scaled accordingly as the variance between cells in a module is considered negligible. Cell and module models are specifically designed for scalability to a large number of battery modules.

A. Battery Cell

The electrical behavior of batteries is represented by an equivalent circuit model (ECM) with one or two RC elements [12] in this paper. The model parameters, such as open-circuit voltage and internal resistance change with state of charge (SoC), Temperature and Current. Corresponding Look-Up-Tables (LUT) are retrieved by measurements. Data used in this paper comes from discharge pulse sequences under varying conditions. The fixed-point conversion is done by considering the physical limits and setting up the LUTs and calculations accordingly. A comparable approach is shown in [13].

Fig. 5 shows the block diagram of a cell model. Depending on the required precision, a first or second-order RC model is used. The model requires inputs for current I_{cell}, temperature $\vartheta_{\mathrm{cell}}$ and the initial SoC SoC_0. The model contains multiple multi-dimensional LUTs, which are arranged in one dimension by concatenation. Resource usage is minimized by a centralized index calculation. This block simultaneously outputs the indices of all LUT entries adjacent to the requested values.

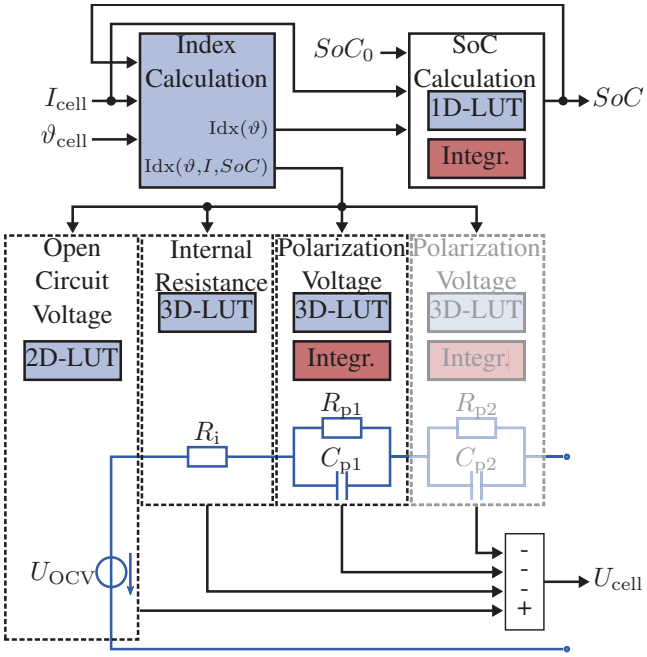

Fig. 5. Battery cell model optimized for FPGA.

From those 2/4/8 adjacent LUT entries, the output value is determined by linear/bilinear/trilinear interpolation, respectively. The SoC is calculated using Coulomb-Counting and the given initial SoC. Additionally, efficiency is considered by two 1D-LUTs, one for charging and the other for discharging. To determine the cell's voltage U_{cell}, the ECM is evaluated. The ECM is shown in blue in Fig. 5. For the validation in this paper, a 1RC model is used, in general models with 2 or more RC elements are also feasible. For both, coulomb counting and evaluation of the polarization capacitance, integrators are required which are critical in serialization as shown in the next section. With the LUTs located in Block RAM and interpolation in up to three dimensions, an FPGA synthesizable cell achieves an open-loop time of 270 ns. As the 3D-LUTs are called consecutively 8 times for interpolation, the maximum clock rate is limited to $100\,\mathrm{MHz}/8 = 12.5\,\mathrm{MHz}$.

B. Serializable Battery Modules

A battery module is represented by scaling the cell inputs and outputs and additionally considering the resistance of the interconnections in the module. This is shown highlighted in blue in the block diagram in Fig. 6.

Battery modules with differences in SoC or State of Health (SoH) but identical LUTs can be calculated with only few additional FPGA resources required. This is achieved by serially calculating the models using the same LUTs. In Fig. 6, the current $\underline{I}_{\mathrm{PESB}}$ and temperature $\underline{\vartheta}_{\mathrm{PESB}}$ are given as vectors, each containing 20 entries for 20 battery modules. Those vectors are serialized and processed in the battery module model one after another. The resulting voltage $\underline{U}_{\mathrm{PESB}}$ and the $\underline{SoC}$ are again represented as vectors after deserialization. This approach scales very well for this number of battery modules.

Two factors limit the number of battery modules serially calculated: Firstly, the achievable clock rate for 20 models calculated this way drops to 500 kHz, which still is enough, even for effects caused by Pulse-width modulation (PWM) used in the PESB. At a PWM frequency of 8 kHz, the battery modules are calculated 62.5 times per PWM cycle. The open-loop time, however, remains unchanged. Secondly, the integrators in the RC-model cannot be serialized as they constitute states of the individual cell. Therefore, the integrators require FPGA resources proportional to the number of batteries. In comparison to a single battery module, 20 serialized modules require identical Block RAM and approximately double FPGA LUT. On the Zynq-7030, the emulation of six times 20 PESB is close to the theoretical limit. However, this is not done as the routing and timing become problematic at high utilization.

Depending on the focus of emulation, not all battery modules in the MMC must be represented individually. The modeling approach in Simulink allows great modularity, making it possible to use a single (scaled and averaged) battery module for one full MMC arm while in another arm all battery modules are calculated. This allows efficient usage of FPGA resources where required.

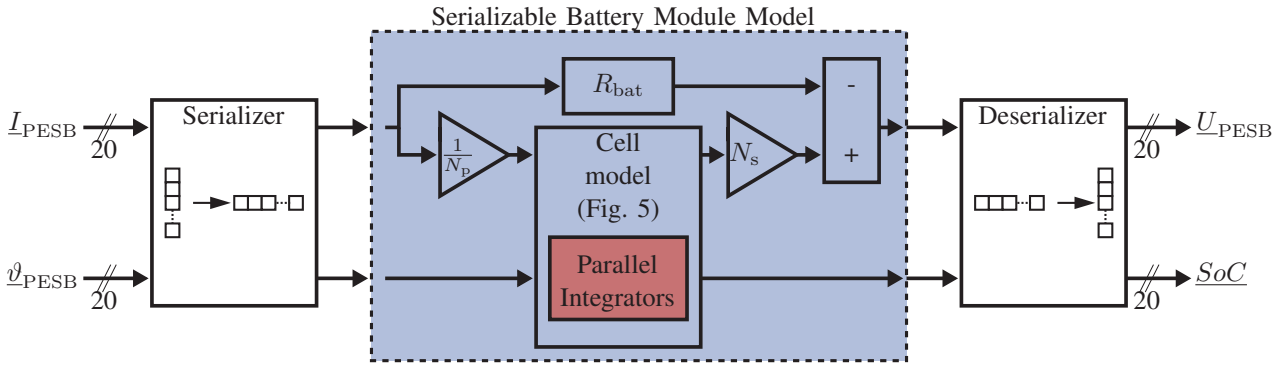

Fig. 6. Resource efficient, serialized battery modules.

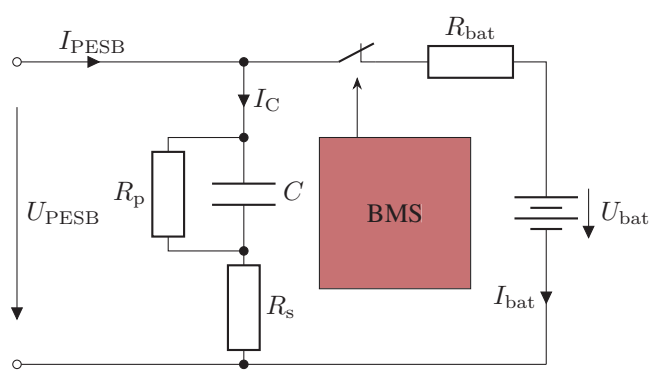

Fig. 7. Extended PESB model including capacitor and BMS safety features.

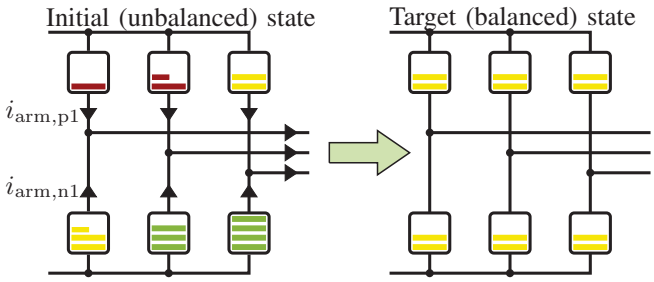

Fig. 8. Concept of balancing between MMC arms.

C. Additional features in the PESB

Additional resources can be used to extend the PESB models. A depiction of some features is shown in Fig. 7. For example, every battery module can be extended or replaced by a capacitor C with a series resistance R_{s} and parallel resistance R_{p}. The resistance R_{bat} represents the resistance between the battery module and capacitor due to possible plugs, cables and relays. With this model, the emulation of the capacitor current I_{C} and the influence on the battery current I_{bat} is possible as shown in chapter VI. Also, the emulation of safety features implemented in a real battery module's BMS is possible. This allows failure emulation, where the battery module is electrically disconnected from the MMC by its BMS in case of overcurrent, over-, undervoltage and others.

V. Control and Energy Management

To evaluate the HIL setup, a hybrid control and energy management strategy is adopted. The strategy aims at the balancing of initially spread battery SoCs. This is comparable to the balancing of capacitor voltages in a traditional MMC and is due to its comparably low complexity suitable for validation of the HIL setup. More advanced methods of energy management, such as shown in [6], also take SoH and other factors into consideration. Although the setup is capable of emulating such scenarios, those are not suitable for comprehensible validation of the HIL setup due to their complexity. To operate the MMC as a converter in the power grid, the required AC and DC voltages must be provided at all times. By controlling the AC and DC currents, the power transferred between each of these two sides and the batteries can be controlled independently. In [11], it is shown that the control problem of the MMC can be decoupled. In this decoupled representation of the MMC, internal currents can also be controlled independently, allowing the exchange of power between MMC arms.

A. Distributing Power between Arms

From an energy management's point of view, first, all battery modules in one MMC arm are combined into one virtual battery module. To each of those six virtual batteries, a new property is assigned. This property is a relative indicator of the need of charging or discharging this virtual battery. Here, the averaged SoC is used as this property. In Fig. 8 a simplified representation of the MMC is shown, where all battery modules in one arm are combined into one virtual battery and pictured with an exaggerated representation of their SoC. Using the decoupling from [11] and based on [14], the internal currents are balanced. The resulting currents are shown in chapter VI.

B. Distributing Power within one Arm

In addition to differences between the batteries in the MMC arms, differences between the battery modules within on MMC arm must also be addressed. This is done by the sorting algorithm, which decides which PESBs are activated and which are bypassed to achieve the required AC voltage. The

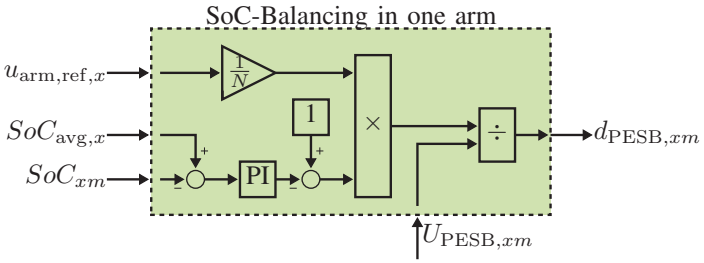

Fig. 9. PI controller for the SoC balancing [5] in the MMC arms $x = 1,..,6$ resulting in reference duty cycles for the individual PESB $m = 1,..,N$.

considered MMC's PESBs in one arm result in a combined nominal voltage significantly higher than the DC voltage. The reserve allows the selection of the active battery modules at any momentary AC voltage, as at no point in time all modules need to be active. To share possible high loads between battery modules, this reserve is also used to keep the Pulse-width modulation (PWM) at a duty cycle below one.

In [5], a method to balance SoC in one MMC arm is shown. It is based on a PI controller with the deviation between SoC in each submodule and average SoC in the arm as the input. In Fig. 9, a schematic of the control method is shown. $SoC_{\mathrm{avg},x}$ describes the average SoC in the respective arm, while SoC_{xi} describes the individual SoC of the PESB with index i in the arm. The PI controller's output adjusts the set voltage for the PESB. Thus, PESBs with higher SoC discharge faster, while PESBs with lower SoC discharge slower. Note that this simplified diagram only applies while power is drawn from the converter into the AC grid, as in other cases the signs must be switched. To demonstrate the functionality of the HIL setup, this method is implemented and used for the results shown in Chapter VI. It should be noted, that the SoCs in this setup are not estimated but directly retrieved from the models. Therefore, any error typically introduced by an estimator is neglected as this is not part of this paper.

VI. Validation

To verify the modeling approach, the setup is tested with the exemplary control algorithm. An MMC with 20 PESBs per arm and a 14s14p-battery module per PESB is considered, the key data is summarized in tab. I. Each of the battery modules in the arm p1 is modeled, the remaining arms are modeled as one averaged battery module each. First, the FPGA optimized battery model is validated.

A. Battery Model Validation

A parameterized and validated simulation model is considered as given for the battery cell. For FPGA synthesis, fixed-point conversion and adaptation of the LUTs to improve interpolation on the FPGA are required. In Fig. 10a, a comparison of battery module voltage over discharged capacity for one discharge cycle is shown. The measured value is shown as reference in red, in blue the voltage of the simulated 1RC model is shown. The FPGA-synthesizable model results in the voltage depicted in green. Fig. 10b shows the error of

TABLE I
Key Data of the Emulated MMC

Property	Value
Nominal voltage	700 V DC, 400 V 3-phase AC
Nominal Power	100 kW
Number of PESBs	20 per arm, 120 total
Battery modules	14s14p Li-Ion
Battery nominal voltage	51.8 V
Battery nominal capacity	65 A h
Buffer capacitor	6 mF
Total energy capacity	400 kW h

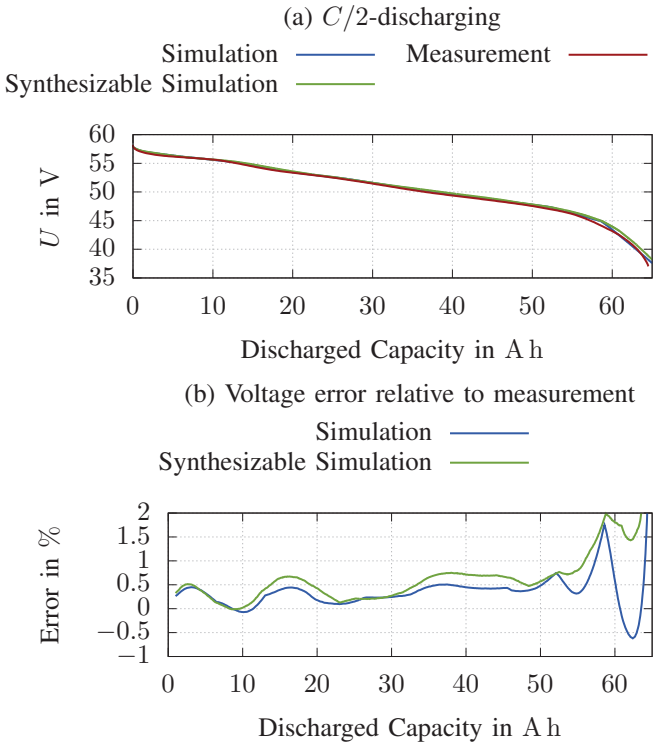

Fig. 10. Comparison of battery voltage during discharge at a rate of 0.5 C.

the models relative to the measured value. The error in the synthesizable model is slightly higher in comparison to the simulation model. However, the introduced error in battery voltage is mostly below 1 %, with the exception of low SoC. In part, this error comes from the simulation model due to LUT resolution and measurement errors. The effect is amplified by inter- and extrapolation errors in the synthesizable model. For higher currents not shown in the figure, the error is similarly small. Only for currents close to the maximum parameterized values, the error becomes more significant due to the same effects. Overall, the deviation introduced by conversion for the FPGA is small as expected.

B. Pulse Width Modulation Validation

One advantage of a real-time capable battery model is the possibility to investigate faster and slower processes with one

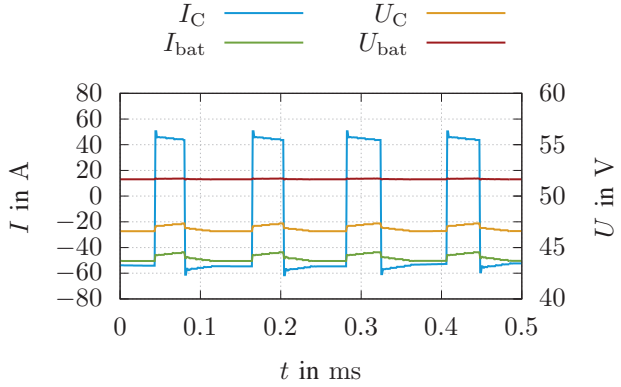

Fig. 11. Battery current resulting from PWM, buffered by the capacitor.

model. A basic modulator for PWM is implemented to test the behavior of the emulator. The PWM is running at 8 kHz. Live visualization via the HMI and the processor is not suitable for frequencies of multiple kiloHz. Instead, the data is logged via a JTAG connection from the FPGA. A PESB as shown in Fig. 7 is emulated and the voltages and currents of battery module and capacitor are logged. Exemplary data while power is drawn from the PESB is shown in Fig. 11. The voltage U_{PESB} is here equal to the capacitor voltage U_{C}.

The data suggests, that the interaction between capacitor and battery is as expected. Around $t = 0.1\,\mathrm{ms}$, the PESB is active, resulting in a negative current for both capacitor and battery. While the absolute value of I_{C} decreases during this phase, the battery takes over more of the current. The capacitor voltage I_{C} is always below the battery voltage because of the negative power flow and R_{bat}. While the PESB is bypassed, current flows from battery to capacitor. This can be seen around $t = 0.3\,\mathrm{ms}$. This shows that the capacitor has the expected buffering effect and limits current peaks at the battery module.

C. Converter Model and Full Setup Validation

The converter model is validated in a scenario, where the converter's batteries are discharged into the AC grid at 100 kW. In this scenario, no power is exchanged between the converter and its DC side. First, the arm currents in an ideal scenario with no balancing required are shown in Fig. 12a. All arm currents are defined positive in the direction towards the AC grid. In this case, $I_{\mathrm{arm,p}} = I_{\mathrm{arm,n}}$ results in all three legs, so that not all currents are visible in the figure.

To demonstrate the balancing between arms, the SoCs of battery modules within one arm are set identical while the modules in different arms are given different initial SoCs. For comprehensibility, the initial SoCs are sorted ascending from p1 to n3, similarly as shown in Fig. 8. The resulting currents to balance the SoCs are shown in Fig. 12b. Arm voltage and current constitute the average power delivered from or to the battery modules in the arm. The battery voltages resulting for the six arms shown in Fig. 13 correspond to the expected power behavior. When comparing this to the diagram

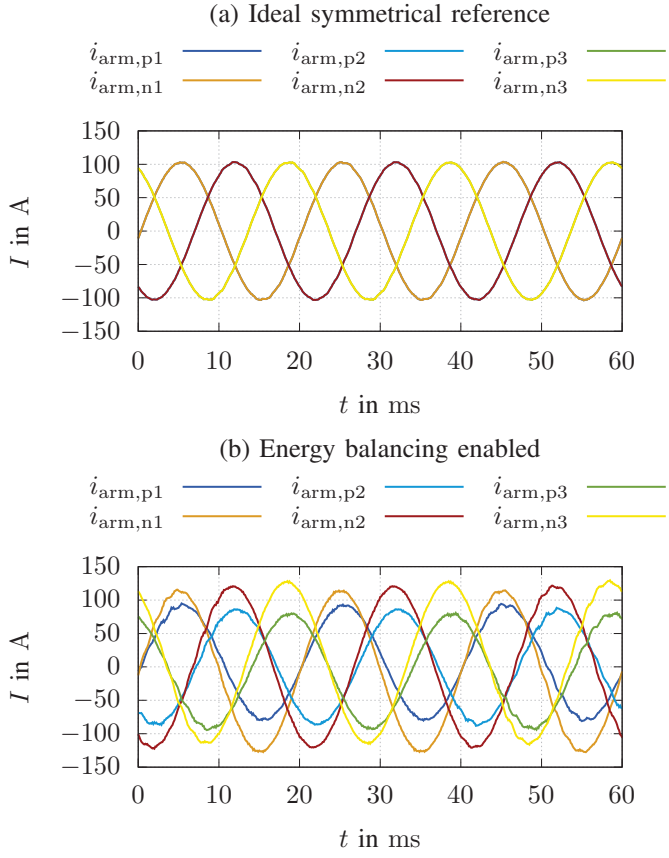

Fig. 12. Arm currents one battery per arm with and without balancing.

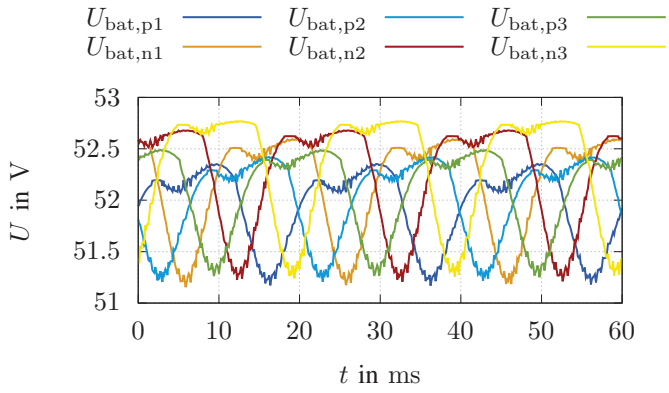

Fig. 13. PESB battery voltage for each arm.

in Fig. 12b, it can be seen that the controller sets the arm voltages such that a higher current is drawn from arms with higher average battery voltage (indicating higher SoC).

Fig. 14 shows the deviation of the SoC in all six MMC arms from the mean value over 30 min . This deviation is given as

$$\Delta SoC_x = \frac{1}{6} \cdot \left(\sum_{i=1}^{6} SoC_i\right) - SoC_x. \tag{3}$$

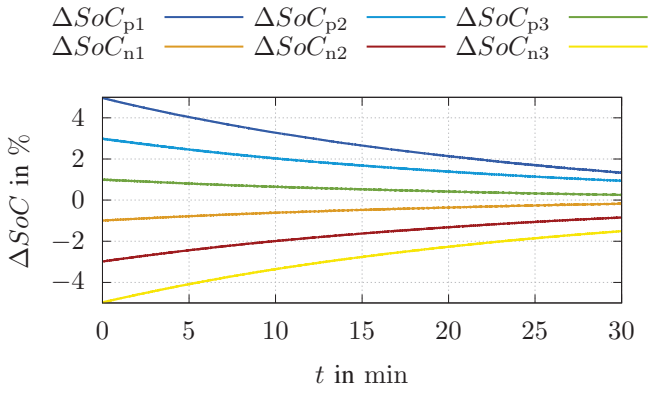

Fig. 14. Deviation between the SoCs over time.

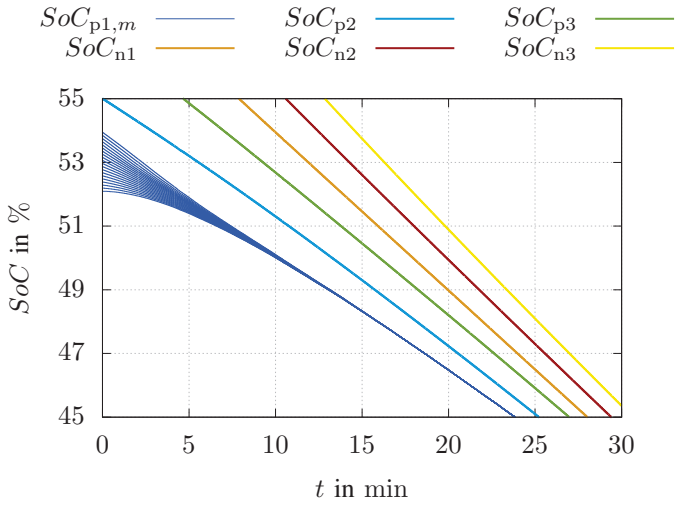

Fig. 15. State of charge of the battery modules. For arm p1, the SoCs of all 20 PESB are shown.

Due to high battery capacity in comparison to the drawn power, battery SoCs show very smooth behavior. It is also evident, that the controller manages to make the SoC approach each other.

In addition to the SoC of the single virtual battery module in each arms, Fig. 15 shows the SoC of all individual SoCs in the arm p1. For comprehensibility, the initial SoCs are again sorted ascending with the PESB index. Therefore, the PESBs are not individually labeled in the figure. It is evident, that the balancing within the arms works as expected, while simultaneously the SoCs between arms are balanced.

VII. Conclusion

A scalable approach for a hardware-in-the-loop setup for a modular multilevel converter with integrated batteries is shown. The system modeling, battery modeling and control approach are verified to operate stable on the presented system. With the setup, control and energy management strategies can be evaluated simultaneously, as effects with varying time constants can be investigated. Effects on the scale of PWM and AC frequency can be emulated as well as long-term effects, such as volatility in power demand. In contrast to software simulations, the real software and hardware is used, simplifying the transfer to the final system. For future works, this setup enables the testing of sophisticated hybrid control and energy management algorithms. Further developments include the consideration of aging mechanisms.

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