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Power Hardware-in-the-Loop Test Bench for Permanent Magnet Synchronous Machines based on a Parallel Hybrid Converter

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***Abstract*—This paper presents a Power Hardware-in-the-Loop (PHIL) emulation test bench for emulating highly utilized permanent magnet synchronous machines (PMSM). The output stage of the PHIL is a Cascaded H-bridge based Parallel Hybrid Converter (PHC) with a 17-level output voltage and an effective switching frequency of 1 MHz. The nonlinear machine is emulated with a sampling frequency of 5 MHz and is implemented on a field programmable gate array (FPGA) using *Matlab/Simulink*'s *HDL Coder*. For this purpose, the time-discretized model equations of a PMSM and the PHIL test bench are derived and their mapping into an HDL code-generable and fully fixed-point transformed model in *Simulink* is described. To enable the high model sampling rate of 5 MHz, it is optimized for a low clock cycle count and the nonlinear relations between the machine currents and flux linkages are stored in lookup tables (LUT). The measurements are carried out in steady-state operation as well as for highly dynamic current and rotor speed steps. They demonstrate the excellent performance of the presented PHIL test bench, which even perfectly reproduces the current ripple of the modeled PMSM.**

***Index Terms*—Power-Hardware-in-the-Loop, Machine Emulation, Real-Time Simulation System, Parallel Hybrid Converter**

I. Introduction

The trend to replace expensive and space-consuming machine test benches (Fig. 1) with modern Power-Hardware-in-the-Loop (PHIL) emulation test benches (Fig. 2) for testing of drive inverters, their control units and the closed loop control algorithms has become more and more common in recent years. A PHIL emulator herein offers the ability to analyze a drive inverter, typically denoted as a Device under Test (DUT), at an early stage of electrical drivetrain development, without the need for a real machine [1,2]. The DUT is connected via the linear inductive coupling network (L_{CN}, R_{CN}) to the emulation converter of the PHIL test bench, which then emulates the terminal behavior of an electrical machine. To do so, the output voltages $u_{\mathrm{S},x}$ ($x \in \{1,2,3\}$) of the DUT are measured by the Real-Time Simulation System (RTSS) and the machine model calculates the resulting phase currents $i_{\mathrm{S},x}$ and current slopes $\frac{\mathrm{d}i_{\mathrm{S},x}}{\mathrm{d}t}$ of the machine to be mimicked. The PHIL model then calculates the reference output voltages of the PHIL converter $u_{\mathrm{PHIL},x}$ in order to set precisely the currents and current slopes in the coupling chokes L_{CN} calculated by the machine model [3]. For a precise emulation that even correctly emulates the current ripple of a machine [4–6], the RTSS must measure the voltages and the currents at the PHIL test bench terminals with a low latency and a high sampling frequency ($f_{\mathrm{sample}} > 1\,\mathrm{MHz}$) [3]. The rotor speed thereby is specified by the operator or calculated by a higher-level mechanical model, which is not part of this paper. In Section II of this paper, the time-discretized model equations of a non-linear permanent magnet synchronous machine (PMSM) as well as the PHIL test bench are derived, leading to a calculation scheme for the reference values of the PHIL emulation converter output voltages $u^*_{\mathrm{PHIL,x}}$. The implementation of this calculation scheme in an optimized HDL code-generable and fully fixed-point transformed Simulink model is described in Section III as well as the implementation on a Kintex 7 FPGA. In Section IV, the operation principle of the Parallel

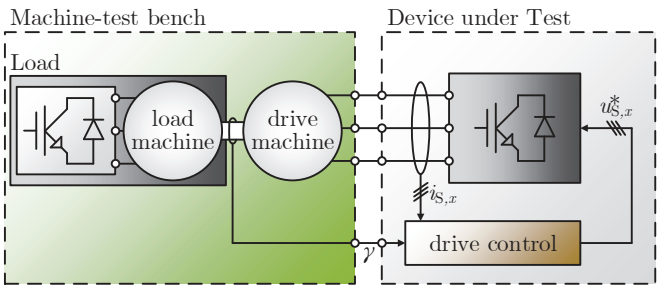

Fig. 1: Rotating machine test bench

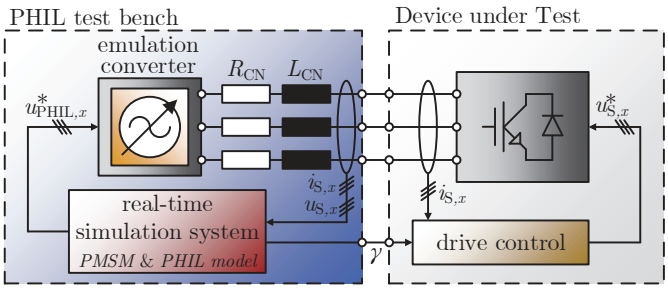

Fig. 2: Power Hardware-in-the-Loop Emulation test bench

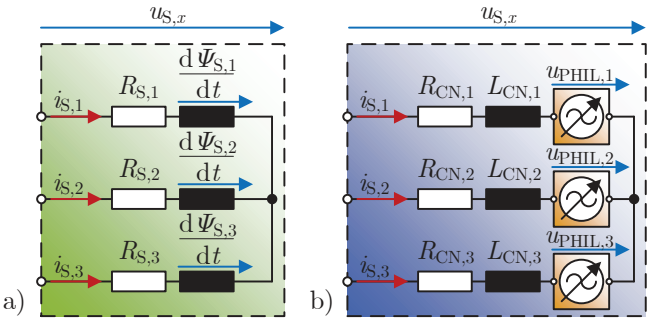

Fig. 3: Equivalent circuit diagram of the PMSM and the PHIL-emulation test bench

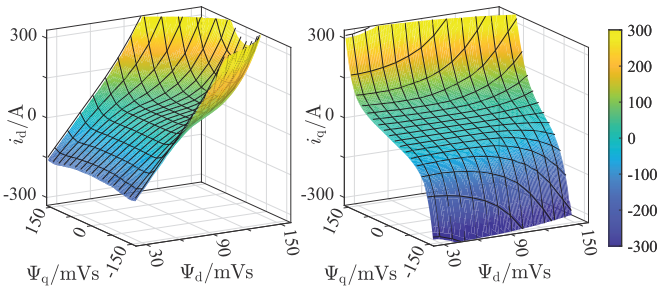

Fig. 4: Stator currents depending on the stator flux linkages Ψ_d and Ψ_q

Hybrid Converter (PHC) is described, which is used as the emulation converter of the PHIL test bench. Finally, in Section V measurements are presented and compared with simulation results.

II. System Modeling

A. PMSM

The PMSM model describes the reaction of the machine based on the DUT output voltages $u_{\mathrm{S},x}$ and considers non-linearities caused by saturation and cross-coupling effects. Based on the three phase equivalent circuit diagram (ECD) in Fig. 3 a), the voltage equation of a single PMSM phase is derived in (1). $R_{\mathrm{S},x}$ denotes the stator resistance, $i_{\mathrm{S},x}$ the stator currents, $\frac{\mathrm{d}\Psi_{\mathrm{S},x}}{\mathrm{d}t}$ the induced voltages, $\Psi_{\mathrm{S},x}$ the stator flux linkages and $u_{\mathrm{S},x}$ are the output voltages of the DUT inverter. Using the amplitude-invariant Park Transformation, the stator voltage equation (1) is transformed into the rotor fixed dq-system (2).

$$u_{\mathrm{S},x} = R_{\mathrm{S},x} i_{\mathrm{S},x} + \frac{\mathrm{d}\Psi_{\mathrm{S},x}}{\mathrm{d}t} \tag{1}$$

$$\begin{aligned} u_{\mathrm{S,d}} &= R_\mathrm{S} i_{\mathrm{S,d}} + \frac{\mathrm{d}\Psi_\mathrm{d}}{\mathrm{d}t} - \omega\Psi_\mathrm{q} \\ u_{\mathrm{S,q}} &= R_\mathrm{S} i_{\mathrm{S,q}} + \frac{\mathrm{d}\Psi_\mathrm{q}}{\mathrm{d}t} + \omega\Psi_\mathrm{d} \end{aligned} \tag{2}$$

In this paper, the flux-based machine model is used as in [7,8], thus the machine currents $i^*_{\mathrm{S,d}} = i_{\mathrm{S,d}}(\Psi_\mathrm{d}, \Psi_\mathrm{q})$ and $i^*_{\mathrm{S,q}} = i_{\mathrm{S,q}}(\Psi_\mathrm{d}, \Psi_\mathrm{q})$ are determined by the flux linkages Ψ_d and Ψ_q. The asterisk * indicates that this is a model output value or reference value and not a real measured value. To determine the flux linkages of the machine, the voltage equations (2) are rearranged to the derivatives of the flux linkages $\frac{\mathrm{d}\Psi_\mathrm{d}}{\mathrm{d}t}$ resp. $\frac{\mathrm{d}\Psi_\mathrm{q}}{\mathrm{d}t}$ and integrated, leading to (3).

$$\begin{aligned} \Psi_\mathrm{d} &= \int (u_{\mathrm{S,d}} - R_\mathrm{S} i^*_{\mathrm{S,d}}(\Psi_\mathrm{d}, \Psi_\mathrm{q}) + \omega\Psi_\mathrm{q})\mathrm{d}t \\ \Psi_\mathrm{q} &= \int (u_{\mathrm{S,q}} - R_\mathrm{S} i^*_{\mathrm{S,q}}(\Psi_\mathrm{d}, \Psi_\mathrm{q}) - \omega\Psi_\mathrm{d})\mathrm{d}t \end{aligned} \tag{3}$$

It is not possible to describe the non-linear relation between the machine flux linkages and the machine currents with simple analytical equations. Thus, the relations are stored in lookup tables (LUT) and have to be obtained either by the use of finite element method (FEM) or by measurements of a real machine in a rotating test bench. The LUTs of the machine used in this paper were obtained in [9] by inverting the measured flux linkage functions $\Psi_\mathrm{d}(i_{\mathrm{S,d}}, i_{\mathrm{S,q}})$ and $\Psi_\mathrm{q}(i_{\mathrm{S,d}}, i_{\mathrm{S,q}})$ and are depicted in Fig. 4.

B. PHIL Model

To compute the PHIL converter reference output voltages $u^*_{\mathrm{PHIL},x}$, a model of the PHIL test bench is needed. In Fig. 3 b) the ECD of a PHIL emulation test bench with an voltage source as emulation converter, the line resistance $R_{\mathrm{CN},x}$ and coupling inductance $L_{\mathrm{CN},x}$ of the coupling network is depicted. Similar to the derivation of the PMSM model equations, the voltage equation of the ECD, which is given for a single phase in (4), is transformed into the dq-system and then rearranged to the ideal PHIL reference values $u^*_{\mathrm{PHIL,dq,ideal}}$, leading to (5).

$$u_{\mathrm{S},x} = R_{\mathrm{CN},x} i_{\mathrm{S},x} + L_{\mathrm{CN},x} \frac{\mathrm{d}i_{\mathrm{S},x}}{\mathrm{d}t} + u_{\mathrm{PHIL},x} \tag{4}$$

$$\begin{aligned} u^*_{\mathrm{PHIL,d,ideal}} &= u_{\mathrm{S,d}} - R_\mathrm{CN} i^*_{\mathrm{S,d}} - L_\mathrm{CN}\left(\frac{\mathrm{d}i^*_{\mathrm{S,d}}}{\mathrm{d}t} - \omega i^*_{\mathrm{S,q}}\right) \\ u^*_{\mathrm{PHIL,q,ideal}} &= u_{\mathrm{S,q}} - R_\mathrm{CN} i^*_{\mathrm{S,q}} - L_\mathrm{CN}\left(\frac{\mathrm{d}i^*_{\mathrm{S,q}}}{\mathrm{d}t} + \omega i^*_{\mathrm{S,d}}\right) \end{aligned} \tag{5}$$

However, with these ideal PHIL reference values, the currents in the coupling network of the PHIL test bench are controlled only in open loop. In the real system, deviations caused by the effects of dead times, measurement errors, the PHIL emulator not being an ideal voltage source, and non-linear parameters of the coupling network must be compensated by closing the loop. Additional proportional controllers in parallel with the ideal PHIL model (6) achieves this by minimizing the differences between the calculated machine model currents $i^*_{\mathrm{S,dq}}$ and the real currents measured $i_{\mathrm{S,dq}}$ in the coupling network of the PHIL test bench.

$$\begin{aligned} u^*_{\mathrm{PHIL,d}} &= u^*_{\mathrm{PHIL,d,ideal}} + K_\mathrm{p}(i_{\mathrm{S,d}} - i^*_{\mathrm{S,d}}) \\ u^*_{\mathrm{PHIL,q}} &= u^*_{\mathrm{PHIL,q,ideal}} + K_\mathrm{p}(i_{\mathrm{S,q}} - i^*_{\mathrm{S,q}}) \end{aligned} \tag{6}$$

The proportionality factor K_p depends highly on the system dead time of the PHIL test bench, the dynamics and accuracy of the measuring equipment as well as on the output voltage quality of the emulation converter itself and therefore cannot be specified with concrete values.

C. Time Discretization

For the implementation of the PMSM and PHIL model on the field programmable gate array (FPGA) of the RTSS they must be causal with time-discrete and value-discrete variables. Therefore, (3) and (6) are discretized using the forward Euler method with the RTSS model sampling time $t_\mathrm{S} = \frac{1}{f_\mathrm{S,RTSS}}$. This leads to (7) for the flux linkages $\Psi_{\mathrm{dq},k+1}$ and to (9) for the PHIL reference voltages $u^*_{\mathrm{PHIL,dq},k+1}$ at the next sampling time step $k+1$. As depicted in (8), the machine currents $i^*_{\mathrm{dq},k+1}$, which are required for the calculation of $u^*_{\mathrm{PHIL,dq},k+1}$ and for $\Psi_{\mathrm{dq},k+2}$, are read out from LUTs using the calculated $\Psi_{\mathrm{dq},k+1}$ values.

$$\begin{aligned} \Psi_{\mathrm{d},k+1} &= \Psi_{\mathrm{d},k} + t_\mathrm{S}(u_{\mathrm{S,d},k} - R_\mathrm{S} i^*_{\mathrm{S,d},k} + \omega_k \Psi_{\mathrm{q},k}) \\ \Psi_{\mathrm{q},k+1} &= \Psi_{\mathrm{q},k} + t_\mathrm{S}(u_{\mathrm{S,q},k} - R_\mathrm{S} i^*_{\mathrm{S,q},k} - \omega_k \Psi_{\mathrm{d},k}) \end{aligned} \tag{7}$$

$$\begin{aligned} i^*_{\mathrm{S,d},k+1} &= i_\mathrm{S,d}(\Psi_{\mathrm{d},k+1}, \Psi_{\mathrm{q},k+1}) \\ i^*_{\mathrm{S,q},k+1} &= i_\mathrm{S,q}(\Psi_{\mathrm{d},k+1}, \Psi_{\mathrm{q},k+1}) \end{aligned} \tag{8}$$

$$\begin{aligned} u^*_{\mathrm{PHIL,d},k+1} =& u_{\mathrm{S,d},k} - R_\mathrm{CN} i^*_{\mathrm{S,d},k+1} \\ & - L_\mathrm{CN}\left(\frac{i^*_{\mathrm{S,d},k+1} - i^*_{\mathrm{S,d},k}}{t_\mathrm{S}} - \omega_k i^*_{\mathrm{S,q},k+1}\right) \\ & + K_\mathrm{p}(i_{\mathrm{S,d},k+1} - i^*_{\mathrm{S,d},k+1}) \\ u^*_{\mathrm{PHIL,q},k+1} =& u_{\mathrm{S,q},k} - R_\mathrm{CN} i^*_{\mathrm{S,q},k+1} \\ & - L_\mathrm{CN}\left(\frac{i^*_{\mathrm{S,q},k+1} - i^*_{\mathrm{S,q},k}}{t_\mathrm{S}} + \omega_k i^*_{\mathrm{S,d},k+1}\right) \\ & + K_\mathrm{p}(i_{\mathrm{S,q},k+1} - i^*_{\mathrm{S,q},k+1}) \end{aligned} \tag{9}$$

The rotor position angle γ^*_{k+1} needed for the emulation of the rotor position sensor is computed with (10). The angles for the transformation of the measured values into the dq-system and the inverse transformation of the PHIL reference values into the 123-system also use γ^*_{k+1}, but take into account the system dead times of the measurement and the emulation converter and turn the angle back or forward accordingly.

$$\gamma_{k+1} = \gamma_k + \omega_k t_\mathrm{S} \tag{10}$$

Finally, the new reference output voltage values $u^*_{\mathrm{PHIL},x,k+1}$ are fed forward to the Central Control Unit (CCU) of the PHIL emulation converter. The CCU is responsible for the control and safe operation of the emulation converter and directly controls the power electronics. In PHIL test benches, it is common for safety reasons that the functions of the CCU and the RTSS are not combined in a single unit. As mentioned above, the sampling frequency $f_\mathrm{S,RTSS}$ of the RTSS should be as high as possible in order to calculate the nonlinear behavior of the machine as accurately as possible. However, the modulation frequency $f_\mathrm{S,PHIL}$ of the emulation converter is usually lower than the sampling frequency of the RTSS. Therefore the PHIL reference values $u^*_\mathrm{PHIL,x}$ must be down-sampled by a factor of $F = \frac{f_\mathrm{S,RTSS}}{f_\mathrm{S,PHIL}}$. A moving-average (MA) filter of length F is used to low-pass filter the $u^*_\mathrm{PHIL,dq}$ values inside the RTSS and inside the PHIL emulation converter CCU the decimation takes place.

III. Implementation

A. Real-Time Simulation System

For the use as a CCU of power electronic systems (e.g. the PHIL converter) and for the use as a RTSS for HIL and PHIL applications a modular signal processing system based on the *ZYNQ7030* System-on-Chip (SoC) from *Xilinx* was developed [8,10,11]. As shown in Fig. 5, the mainboard-based system has eight slots for expansion cards (EC) that are directly connected to the *Kintex 7* FPGA of the *ZYNQ7030* SoC. The SoC itself is placed on the commercially available System-on-Module (SoM) *PICOZED 7030*. To adapt the SoC system to each application, custom ECs were developed as digital interfaces to the power electronics hardware and for fast analog signal sampling ($5\,\mathrm{MS/s}$). Due to limited space, please refer to [11] for a more detailed description of the SoC system hardware, the designed ECs and the system architecture, in which the developed SoC system is addressed in detail. For data exchange between the CCU-FPGA of the PHIL converter and the RTSS-FPGA of the PHIL test bench, e.g. the PHIL output voltage reference values, the GTX interfaces are used.

B. Software Workflow

For efficient development of a high-performance PHIL emulator test bench a fast model-based rapid prototyping of the FPGA software is required. Therefore a custom Reference Design of the PHIL RTSS's FPGA block design with the needed IP cores and ECs is registered in the *Simulink HDL Coder*. Callbacks are used to make the corresponding pins in the FPGA design known to the *Matlab HDL Coder*. The models which should be implemented in the RTSS is then developed in an abstracted form in *Simulink*, utilizing the simulation and validation options as well as the *HDL Workflow Advisor*. During the HDL code generation process, the model is connected to the defined interfaces of the Reference Design and the bitstream generation is performed underneath. Hence, the creation of the executable FPGA project is done completely from *Matlab/Simulink*.

C. RTSS Model

RTSS model is tested and improved early in the development process by including the later-used PHIL test bench in the *Matlab- Simulink* simulation. In a first step, the simulation considers and incorporates the real system latencies, measurement bandwidth and resolution constraints of the signal processing. Later, the model of the emulation converter with its control algorithm is also integrated into the *Simulink* model. Thus, the interaction between the emulation converter (and its control) and the RTSS model is tested, stability validated, and the RTSS model is finalized for HDL code generation. The basic structure of the RTSS model is depicted in Fig. 6. Next, the method used for timing control is explained, followed by a description of the RTSS model itself.

Timing Control: To have full control of the timing and thus increase the model execution frequency, no multicycle path constrains where used, in contrast to [4,7]. Instead, the model is manually timed by the careful use of pipeline stages.

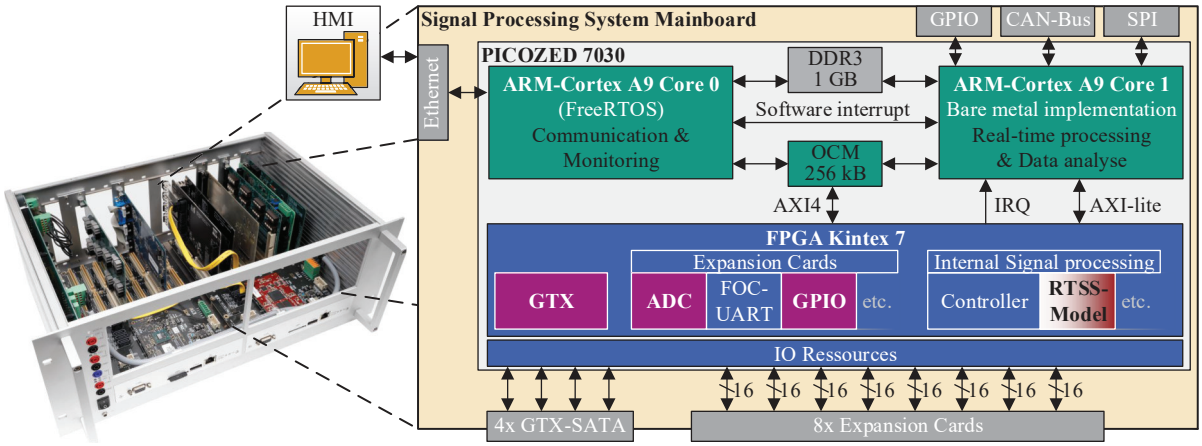

Fig. 5: Left: 19"-Sub-Rack with two mainboards and several expansions cards; Right: Block diagram of the used signal processing system with indicated software partitioning

After each mathematical operation an enabled delay as a register block for signal piplining is placed. Synchronization and triggering of sub-functions running in parallel is realized by a propagating DataValid signal. It is active for one FPGA clock cycle and determines the execution frequency $f_{\mathrm{S,RTSS}}$ of the model. With this technique the necessary FPGA clock cycle count of the model is determined during the development process in *Simulink*. The depicted RTSS model takes 44 clock cycles and the clock frequency of the used *Kintex 7* FPGA is 100 MHz. To allow the model execution frequency of 5 MHz (20 clock cycles), additional mid synchronization stages are placed around the longest model internal feedback loop. In this case the calculation of Ψ_{dq} with the PMSM-model and determination of the machine currents i^*_{dq} values takes 19 clock cycles. To simplify the figure, only the synchronization stages (in, mid, out), which synchronize all signals at once, are shown and the individual pipeline registers of the sub-functions are omitted. This allows the processing of new measured values $(k+1)$ to begin before the previous ones (k and $k-1$) have been processed completely.

Model Description: The input synchronization stage, triggered by the ADC's DataValid-Out signal, samples the reference and control values of the HMI as well as the measured values of the ADC and stores them for 20 clock cycles. The measured values are then converted from the integer range to the fixed-point range and transformed into the dq-system by means of the rotor position angle calculated in parallel. Thereby the measurement dead time t_{ADC} is considered and a correspondingly turned back rotor position angle $\gamma_k - \omega_k t_{\mathrm{ADC}}$ is used. After the first mid-synchronization stage, the PMSM model calculates the new values of the flux linkage with (7). Due to memory limitations, the resolution of the LUTs is limited (128x128 breakpoints), so the four breakpoints closest to the calculated $\Psi_{\mathrm{dq},k+1}$ values are read out of the LUTs and the current values $\mathrm{i}^*_{\mathrm{dq},k+1}$ are bilinearly interpolated. The calculated PMSM model currents and the measurement values are then passed to the second mid stage. Afterwards the reference values for the PHIL emulator are calculated with (9), low-pass filtered with MA-filters and transformed back into the 123-system considering the emulator dead time ($\gamma_k + \omega_k t_{\mathrm{PHC}}$). Finally, the reference values are transferred to the PHC based PHIL emulator by GTX and the rotor position angle γ_k is output as a encoder signal with 4096 steps.

To improve the development process of the RTSS Model an other future projects, all sub-functions (transformations, PMSM/PHIL model, LUT access, interpolation, filters, etc.) of the RTSS model were directly created as masked *Simulink* blocks for a new developed *Simulink* HDL library. The blocks are configurable via their masks (e.g. input value range, output fixed-point bit width, gain parameters, etc.) and are reused as linked library blocks for the design of more complex blocks/models. Since the mask configurations of higher-level blocks are passed on to the masks of lower-level blocks, this significantly simplifies the fixed-point conversation, speeds

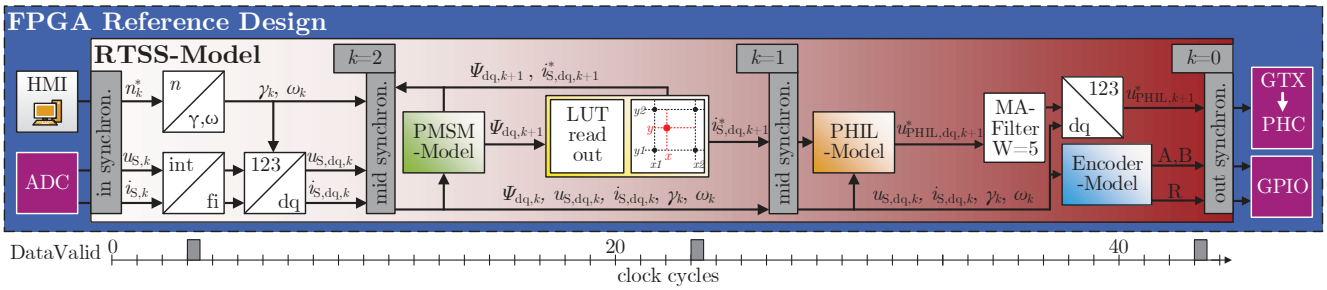

Fig. 6: Block diagram of the RTSS model implementation in *Matlab/Simulink* for the HDL code generation

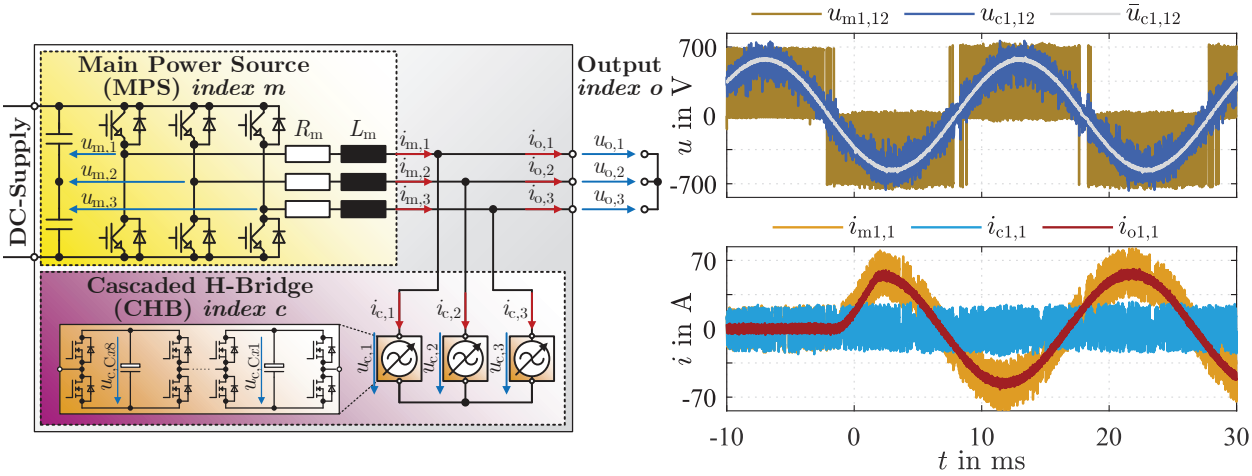

Fig. 7: Equivalent circuit of the Parallel Hybrid Converter on the left, and on the right measurement results of the PHC emulating an $400\,\mathrm{V}/50\,\mathrm{Hz}$ grid connected to a $30\,\mathrm{kVA}$ DUT-Active-Front-End

up development, and simplifies the maintenance of complex models such as the one presented here. [11] gives a more detailed overview of the developed software workflow and the self-developed libraries.

IV. PHIL Emulation Converter

The Cascaded H-Bridge (CHB) based Parallel Hybrid Converter (PHC) topology depicted on the left in Fig. 7 is used as the PHIL-converter. It combines the high output voltage quality and dynamics of a low power 17-level Cascaded H-Bridge (CHB) converter in star configuration with the high efficiency and high power density of a 2-level voltage source converter as Main Power Source (MPS).

A. Operating Principle

The general operating principle of the PHC is explained in the following. Since it is easier to understand if the output voltage of the PHC is solely sinusoidal, a grid application is chosen as an example, with the measurement results depicted on the right of Fig. 7. For the measurement, the PHC emulates an ideal $400\,\mathrm{V}$ $50\,\mathrm{Hz}$ grid and an Active-Front-End (AFE) as DUT performs a $30\,\mathrm{kW}$ load step. The phase 1 to phase 2 voltages of the MPS $u_{\mathrm{m},12}$ and the CHB $u_{\mathrm{c},12}$ ($\bar{u}_{\mathrm{c},12}$ averaged over $10\,\mu\mathrm{s}$) are shown in the upper plot. In the lower plot the phase 1 currents of the MPS $i_{\mathrm{m},1}$, the CHB $i_{\mathrm{c},1}$ and the PHC output $i_{\mathrm{o},1}$ are shown. The high dynamic low-power 17-level CHB converter with a high modulation frequency $f_{\mathrm{c,SW}} = 1\,\mathrm{MHz}$ acts as a quasi-ideal voltage source on the output terminals of the PHC. Thus, the CHB defines the output voltage $u_{\mathrm{o},x}$ and controls the output current $i_{\mathrm{o},x}$ of the PHC. Thereby, the MPS is connected in parallel to the CHB via an inductive coupling network (L_{m}, R_{m}) and provides as a current source the bulk of the PHC output current ($i_{\mathrm{m},x} \approx i_{\mathrm{o},x}$). As a result due to Kirchhoff's current law, the CHB only has to provide the current differences $i_{\mathrm{c},x} = i_{\mathrm{m},x} - i_{\mathrm{o},x}$ between the output currents and the MPS currents. Therefore, the load step shown in Fig. 7 has no effect on the CHB current. Thus, the MPS provides the total active and fundamental reactive output power of the PHC, whereas the CHB only has to provide distortion reactive power. This allows the CHB to be rated at only $\approx 11\%$ of the MPS power rating [12]. In contrast to the high modulation frequency $f_{\mathrm{c,SW}} = 1\,\mathrm{MHz}$ of the CHB, the MPS has a low, operating point dependent average switching frequency $\bar{f}_{\mathrm{m,SW}} \approx 5.4\,\mathrm{kHz} - 14.5\,\mathrm{kHz} \ll f_{\mathrm{c,SW}}$ [8]. The CHB has eight H-bridge cells per phase an thus a theoretical effective switching frequency of each CHB MOSFET of $\frac{f_{\mathrm{c,SW}}}{2 \cdot n_{\mathrm{Cells}}} = \frac{1\,\mathrm{MHz}}{2 \cdot 8} = 62.5\,\mathrm{kHz}$. The real effective switching frequency of each MOSFET is operating point dependent between this value and $\approx 67.5\,\mathrm{kHz}$ due to additional switching events caused by the cell sorting algorithm. The topology and its control concept are firstly introduced in [13]. In [12] the six-phase $120\,\mathrm{kVA}$ laboratory prototype consisting of two PHCs for a back to back PHIL testbench with the DUT in between is presented in detail. The implementation of the PHC's energy and current controller and CHB modulation on the CCU FPGA is also discussed there.

B. Experimental Setup

Fig. 8 shows a simplified schematic of the experimental setup. The setup consists of the 2x3-phase PHIL test bench presented in [12] (blue box) with its two PHCs as emulation converters, each with its own galvanically isolated power supply (only depicted for System 1) and one central RTSS for the machine-model and grid-model calculation. Also part of the setup is the DUT depicted in the gray box, consisting of a drive converter, an AFE for power supply and a control unit. The inductive coupling network required for the emulation of a machine is located between PHIL System 1 and the DUT drive inverter. The parameters of PHIL test bench, DUT as well as emulated machine and are given in Tab. I.

PHIL-System 1 is used to emulate the PMSM. As the machine is designed for a DC link voltage of $300\,\mathrm{V}$, the DUT AFE cannot be connected to a regular $400\,\mathrm{V}$ grid. Therefore the PHIL-System 2 emulates an ideal $50\,\mathrm{Hz}$ $125\,\mathrm{V}$ grid, which

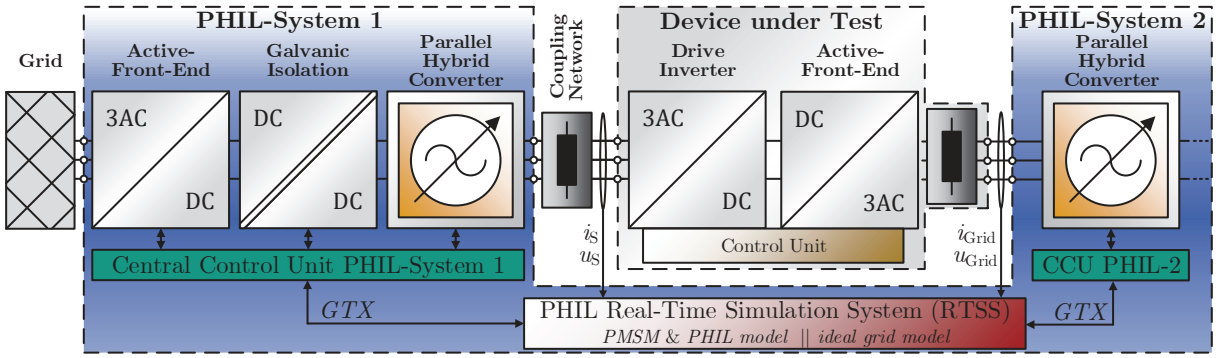

Fig. 8: PHIL emulation test bench for simultaneous emulation of two systems connected to one DUT in the center

allows a DC link voltage of 300 V or less. The topics of grid emulation and grid converters are not part of this paper, thus they are not discussed further. A predictive trajectory controller for saturated cross-coupled permanent magnet synchronous machines presented in [9] is used to control the drive inverter of the DUT. The high-power inverter system originally used therein to characterize the real machine which is now emulated and determine its parameters is not available. Therefore, a inverter system with a lower power rating is used as the DUT in the experimental setup. However, this DUT is sufficient for the validation measurements of the developed PHIL test bench and the implemented machine model.

V. Measurement Results

In this section, the validation measurement results of the presented machine emulation PHIL test bench are presented. For this purpose, measurements were carried out in steady-state operation and during dynamic current and speed steps. A 8-channel oscilloscope *MSO58-5-BW-1000* from *Tektronix* was used to record the measurements. The output voltages of the DUT and the PHIL-emulator were measured with *BumbleBee* high voltage differential probes from *PMK* and the currents in the coupling network between DUT and PHIL-emulator were measured with *HIOKI-3274* current probes. Simultaneously, the measured values of the ADCs as well as the machine model output values were recorded in the RTSS FPGA using an Integrated Logic Analyzer (ILA) IP core from *Xilinx* with a sampling frequency of $f_{\mathrm{ILA,sample}} = 1\,\mathrm{MHz}$ over a length of 4096 sampling points. The trigger out singal of the ILA was output by the RTSS FPGA and used to trigger the oscilloscope. This method ensures that the measurements in the oscilloscope are synchronous with the measurements of the ILA.

A. Steady-State Operation

In Fig. 9 the measurement results for steady state operations at $4000\,\mathrm{rpm}$ and DUT current reference value of $i^*_{\mathrm{S,d,DUT}} = -5\,\mathrm{A}$ and $i^*_{\mathrm{S,q,DUT}} = -50\,\mathrm{A}$ are depicted. The current $i_{\mathrm{S},1}$ in the coupling network is directly measured with the MSO58 scope, wheres the line to star voltages $u_{\mathrm{S},1}$ and $u_{\mathrm{PHIL},1}$ are calculated from the directly measured line-to-line voltages. The reference voltage for the PHIL emulation converter $u^*_{\mathrm{PHIL},1}$ and the machine current $i^*_{\mathrm{S},1}$ calculated by

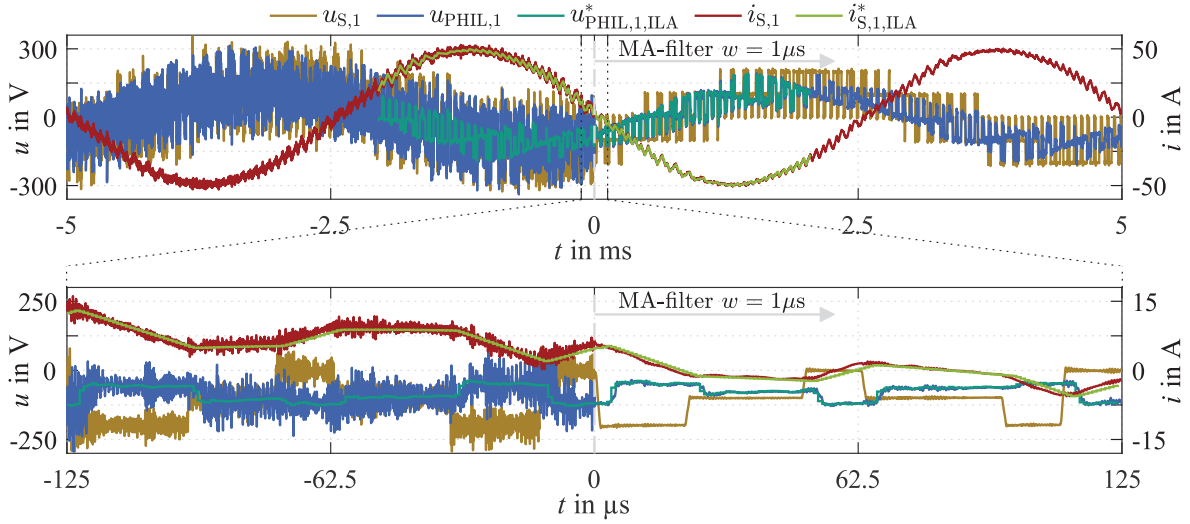

Fig. 9: Steady state operation at $4000\,\mathrm{rpm}$ and DUT reference values $i^*_{\mathrm{S,d,DUT}} = -5\,\mathrm{A}$, $i^*_{\mathrm{S,q,DUT}} = -50\,\mathrm{A}$. The lower plot zooms to the marked area of the upper one. Scope data $u_{\mathrm{S},1}$, $u_{\mathrm{PHIL},1}$, $i_{\mathrm{S},1}$ are filtered with a MA-filter with window length $w = 1\,\mu\mathrm{s}$ for $t > 0\,\mathrm{s}$.

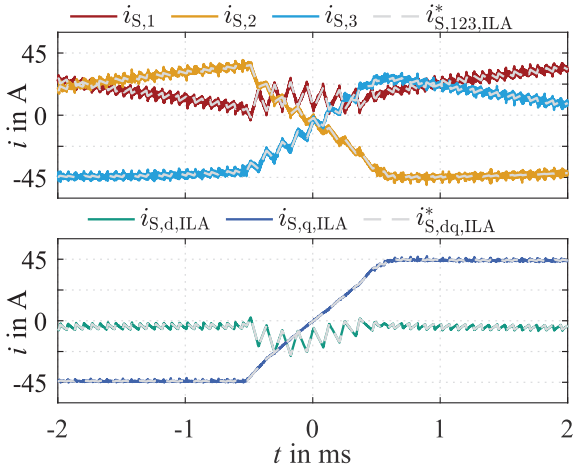

Fig. 10: Current reversal step from $i^*_{\mathrm{S,q,DUT}} = -45\,\mathrm{A}$ to $i^*_{\mathrm{S,q,DUT}} = 45\,\mathrm{A}$ at $1000\,\mathrm{rpm}$ and $i^*_{\mathrm{S,d,DUT}} = -5\,\mathrm{A}$.

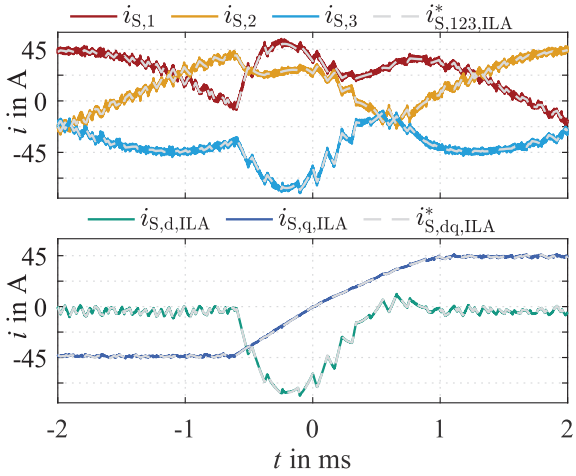

Fig. 11: Current reversal step from $i^*_{\mathrm{S,q,DUT}} = -45\,\mathrm{A}$ to $i^*_{\mathrm{S,q,DUT}} = 45\,\mathrm{A}$ at $4000\,\mathrm{rpm}$ and $i^*_{\mathrm{S,d,DUT}} = -5\,\mathrm{A}$.

the PMSM-model are recorded with $f_{\mathrm{ILA,sample}} = 1\,\mathrm{MHz}$ for time range $-2.048\,\mathrm{ms} < t < 2.047\,\mathrm{ms}$ with the ILA in RTSS FPGA. The scope measurement data are depicted unfiltered for $t < 0\,\mu\mathrm{s}$ and filtered in post-processing with a symmetric moving average filter in with window length of $w = 1\,\mu\mathrm{s}$ for $t > 0\,\mu\mathrm{s}$. This suppresses noise from the emulator converter, which has a switching frequency of $f_{\mathrm{S,PHIL}} = 1\,\mathrm{MHz}$, and allows better comparison of reference and measurement data. In the lower plot of Fig. 9 a zoom on the marked area of the upper plot is shown. As can be seen, the output voltage $u_{\mathrm{PHIL},1}$ of the emulation converter precisely tracks the reference voltage value $u^*_{\mathrm{PHIL},1}$ calculated by the RTSS with only a short latency. Thus, the real current $i_{\mathrm{S},1}$ flowing between the PHIL test bench and the DUT corresponds almost exactly to the current $i^*_{\mathrm{S},1}$ calculated by the PMSM model and even the current ripple is reproduced with high accuracy.

TABLE I: Parameters of the experimental setup

DUT drive inverter / AFE	**Value**
RMS Phase Current max.	35 A
DC link voltage	300 V
control & switching frequency	8 kHz
PMSM	**Value**
Voltage nom.	214 V
Current nom. / max.	169 / 300 A
Number of pole pairs	3
Torque nom. / max.	130 / 220 Nm
Speed nom. / max.	4200 / 11 000 rpm
Shaft power nom. / max.	57 / 97 kW
Stator resistance typ.	10.5 mΩ
Grid Model	**Value**
Line-Line Voltage	125 V
Frequency	50 Hz
PHIL	**Value**
RTSS model frequency $f_{\mathrm{S,RTSS}}$	5 MHz
PHIL switching frequency $f_{\mathrm{S,PHIL}}$	1 MHz
Coupling network resistance R_{CN}	11 mΩ
Coupling network inductance L_{CN}	495 µH

B. Dynamic Operation

Measurements at rotor speeds of $1000\,\mathrm{rpm}$ and $4000\,\mathrm{rpm}$ are shown in Fig. 10 and Fig. 11 for reversing q-current steps at $\gamma_{\mathrm{el}} = 180°$ from $i^*_{\mathrm{S,q,DUT}} = -45\,\mathrm{A}$ to $i^*_{\mathrm{S,q,DUT}} = 45\,\mathrm{A}$ with $i^*_{\mathrm{S,d,DUT}} = -5\,\mathrm{A}$. The upper plots show the phase currents $i_{\mathrm{S},123}$ measured by the scope and in gray the calculated PMSM model currents $i^*_{\mathrm{S},123,\mathrm{ILA}}$ recorded by the ILA. Similarly, the lower plots show the dq-transformed currents $i_{\mathrm{S,dq,ILA}}$ between DUT and PHIL measured by the RTSS and in gray the dq-currents $i^*_{\mathrm{S,dq,ILA}}$ calculated by the PMSM model. The measurements clearly show that the emulation of the modeled PMSM is almost perfect even for dynamic current steps, independent of the rotor speed resp. the electrical frequency. The deviation between model current $i^*_{\mathrm{S},x,\mathrm{ILA}}$ and real current $i_{\mathrm{S},x}$ is very small, as in steady-state operation ($x \in \{123, \mathrm{dq}\}$). This clearly shows that the novel PHC topology is perfectly suited to be used as an emulation converter in a PHIL test bench.

The measurements shown up to this point could also be performed with a conventional rotating machine test bench. The following exemplary measurements with instantaneous speed step changes, however, can only be performed with a PHIL test bench. The speed steps are performed at the same rotor position angle $\gamma_{\mathrm{el}} = 180°$ at the time $t = 0\,\mathrm{ms}$ within one RTSS model sample step k ($f_{\mathrm{S,RTSS}} = 1\,\mathrm{MHz}$). Shown are only the phase-currents $i_{\mathrm{S},123}$ measured by the scope and dq-currents $i_{\mathrm{S,dq,ILA}}$ recorded by the ILA for the time range of $-2.048\,\mathrm{ms} < t < 2.047\,\mathrm{ms}$. To improve visibility, the PMSM model currents $i^*_{\mathrm{S},x,\mathrm{ILA}}$ are omitted from the figures. In Fig. 12 the speed is reversed from $-1000\,\mathrm{rpm}$ to $1000\,\mathrm{rpm}$. In Fig. 13, the rotor speed changes from $1000\,\mathrm{rpm}$ to $4000\,\mathrm{rpm}$, which is a simple emulation of a rotor shaft breakage, without using a specific mechanical model in the RTSS. The last measurement in Fig. 14 shows a speed drop from $1000\,\mathrm{rpm}$ to $0\,\mathrm{rpm}$, which corresponds to the emulation of an abruptly locked rotor.

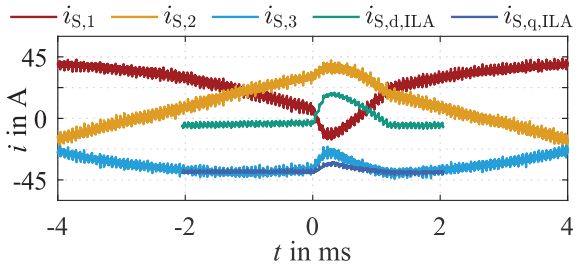

Fig. 12: Speed reversal step from $-1000\,\mathrm{rpm}$ to $1000\,\mathrm{rpm}$ with $i^*_{\mathrm{S,d,DUT}} = -5\,\mathrm{A}$ and $i^*_{\mathrm{S,q,DUT}} = -40\,\mathrm{A}$.

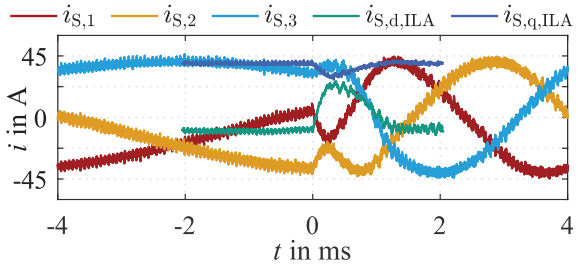

Fig. 13: Speed step from $1000\,\mathrm{rpm}$ to $4000\,\mathrm{rpm}$ with $i^*_{\mathrm{S,d,DUT}} = -10\,\mathrm{A}$ and $i^*_{\mathrm{S,q,DUT}} = -40\,\mathrm{A}$.

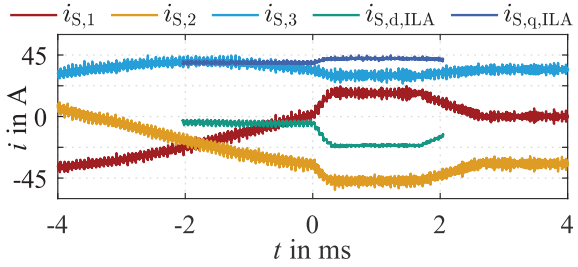

Fig. 14: Speed drop from $1000\,\mathrm{rpm}$ to $0\,\mathrm{rpm}$ with $i^*_{\mathrm{S,d,DUT}} = -5\,\mathrm{A}$ and $i^*_{\mathrm{S,q,DUT}} = 40\,\mathrm{A}$.

VI. Conclusion

In this paper, the concept of a Power Hardware-in-the-Loop (PHIL) test bench for the emulation of electrical machines is presented. Then the time-discretized model equations of a permanent magnet synchronous machines (PMSM) and the PHIL emulator are derived for the implementation on an field programmable gate array (FPGA). Also presented in this paper are an in-house designed, highly adaptable signal processing system used as the PHIL converter Central Control Unit (CCU) and as the Real-Time-Simulation-System (RTSS), the developed rapid prototyping workflow as well as the RTSS model derived from the PMSM and PHIL model equations. Next, the topology and operating principle of the novel Cascaded H-Bridge (CHB) based Parallel Hybrid Converter (PHC) used as the PHIL emulation converter is introduced and the structure of the experimental setup is presented. Measurements in stady-state operations and during dynamic current steps validate the high performance of the developed PHIL test bench, which even reproduces the current ripple calculated by the PMSM model perfectly. Finally, instantaneous speed step changes are shown, which are similar to failure situations like a rotor shaft breakage or a blocking rotor. The ability to emulate a machine based only on its parameters and to reproducibly test a drive inverter in fault situations are unique features of high-performance PHIL test benches. The results of this work clearly demonstrate that the PHIL system presented in this paper fulfills these requirements excellently.

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