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Hardware-in-the-Loop Setup for a Modular Multilevel Converter with Integrated Batteries

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Concept

HIL setup for a combined converter and energy storage
- Averaged modular multilevel converter (MMC) model
- Real-time capable, scalable battery module models
- Testing of combined energy management and control algorithms

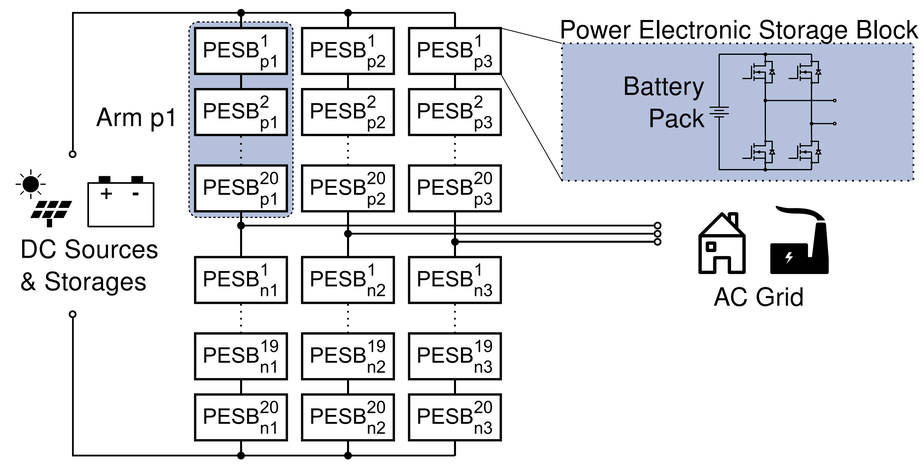

Figure 1: Schematic overview of the MMC with integrated batteries.

Key Data of the Emulated System				
120 PESB	700 V DC	400 V AC	100 kW	400 kWh

Platform

System-on-a-Chip-Platform based on Zynq-7030 (ETI-SoC-System)
- Identical platform for control and emulation

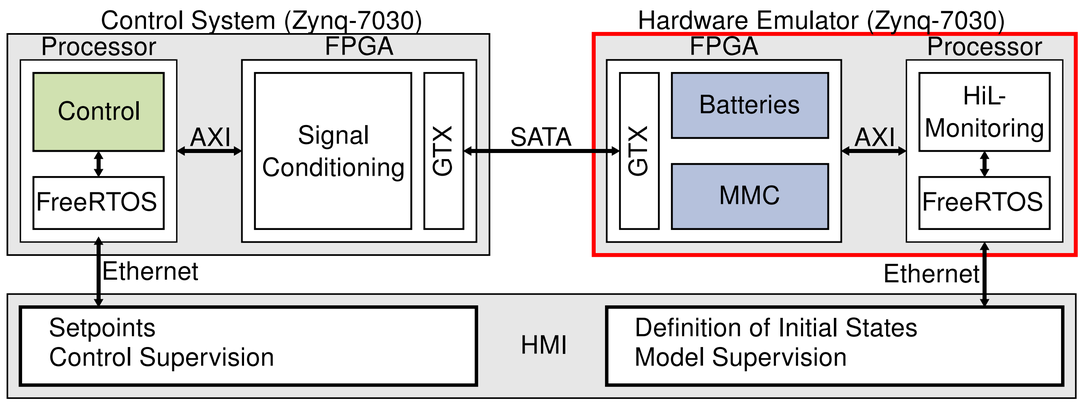

Figure 2: Schematic overview of the HiL setup.

MMC Modeling

State-space model
- Clock rate up to 10 MHz
- Open-loop time of 2.6 µs

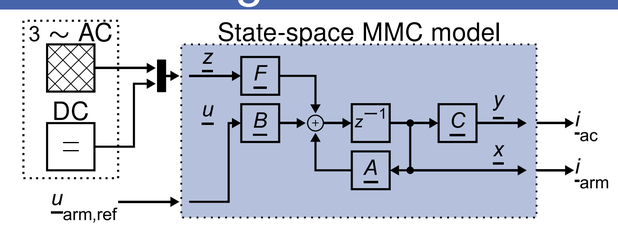

Figure 3: MMC model with DC and AC grid.

Battery Modeling

Battery Modules
- Look-up-tables from discharge pulse tests
- 1RC and 2RC models

Additional Features
- Buffer capacitor
- BMS failure detection

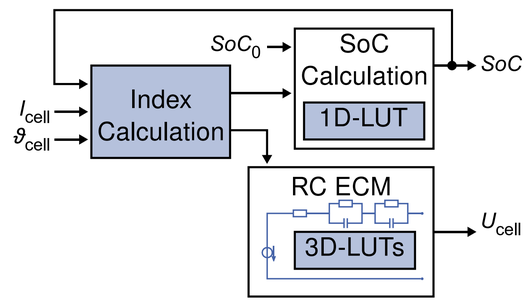

Figure 4: Battery cell model optimized for FPGA.

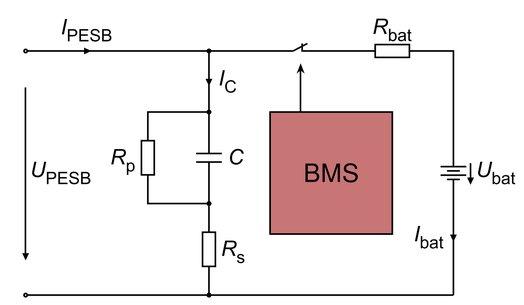

Figure 5: Additional features in the PESB.

Serialized Modules
- Clock rate up to 500 kHz
- Open-loop time of 270 ns

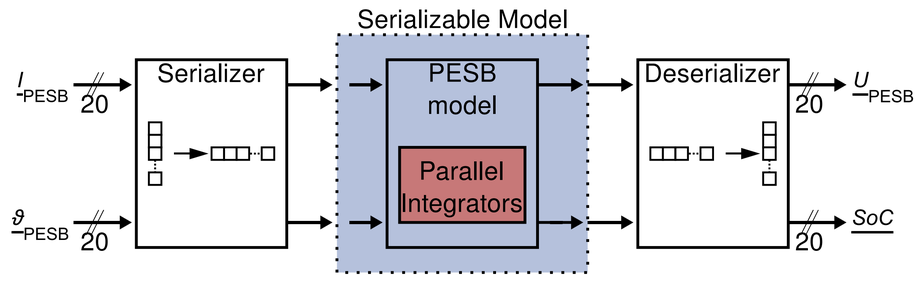

Figure 6: Resource efficient, serialized battery modules.

Validation: Exemplary Control and Energy Management

HIL data captured while 100 kW delivered from the batteries to the AC grid.
SoC balancing between
- PESB in one arm, by sorting algorithm
- Arms, using internal currents

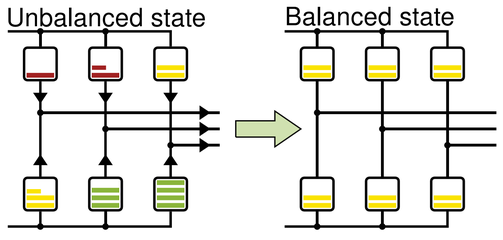

Figure 7: Balancing between MMC arms.

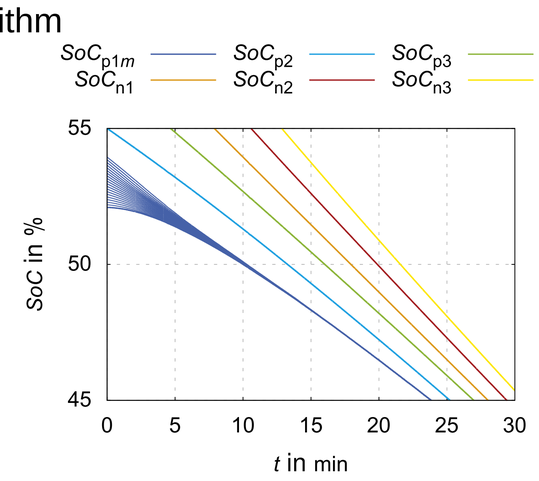

Figure 8: Balancing process over 30 minutes. The SoCs of all 20 PESB are shown for arm p1.

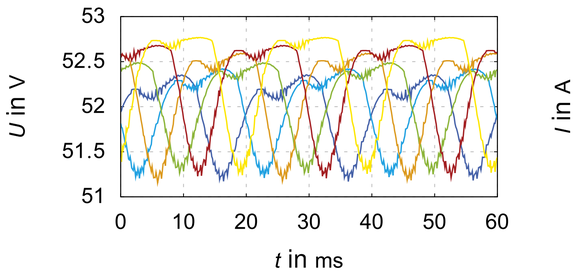

Figure 9: Battery voltages while discharging.

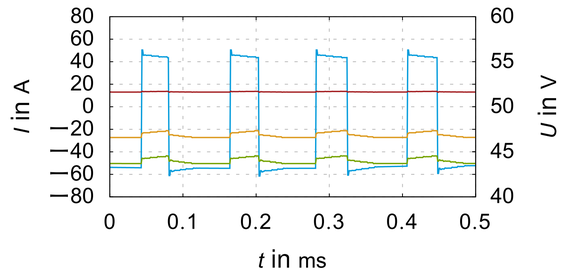

Figure 10: Effect of PWM on battery and capacitor.

Outlook

- Optimization of hybrid control and energy management algorithms
- Battery aging modeling, lifetime optimization

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