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A novel high dynamic six phase 120 kW Power-Hardware-in-the-Loop Emulation Test Bench for emulating AC/DC Grids and Electrical Machines

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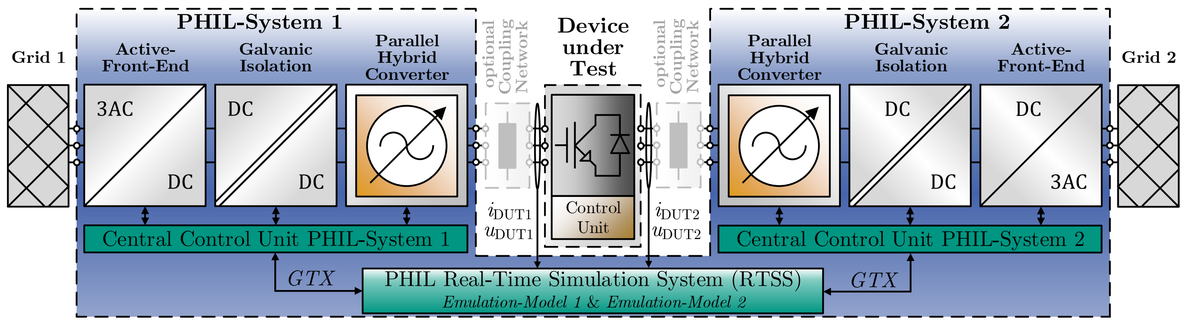
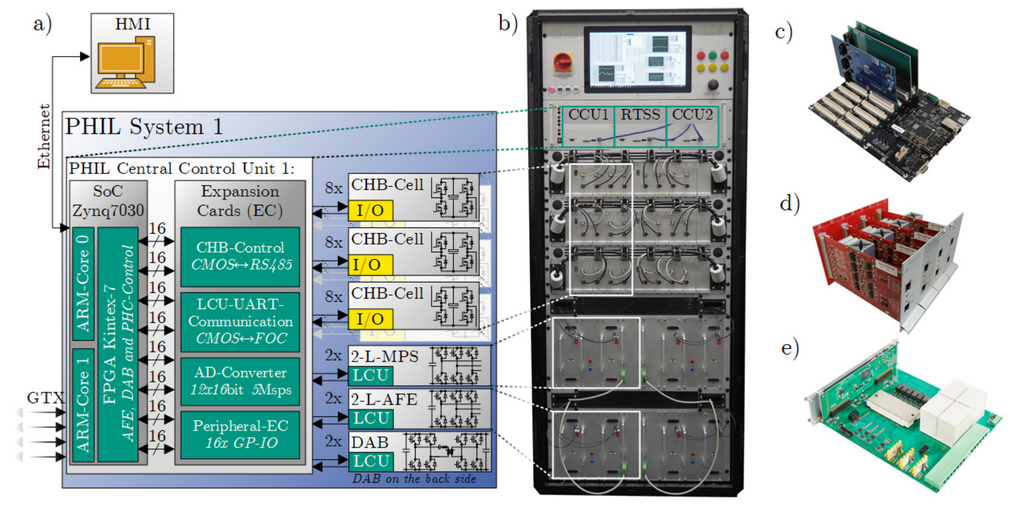
Abstract: This paper presents a highly customizable 120kVA Power-Hardware-in-the-Loop test bench. The output stage consist of two identical Parallel Hybrid Converters each with a 17-level output voltage and an effective switching frequency of 1 MHz. The Parallel Hybrid Converters can provide 3-phase AC or bipolar DC as output voltage. Thus, one 6-AC, 3-AC or DC system or two systems with 2x3-AC, 1x3-AC and 1xDC or 2xDC can be emulated.

Power-Hardware-in-the-Loop (PHIL) test bench



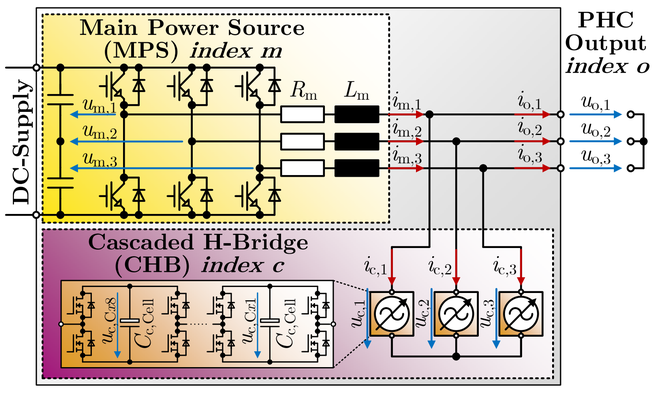
- Two three phase PHIL systems, each with an 60 kVA output stage, capable of emulating a DC or an AC system
- Output stages with a highly dynamic 17-level output voltage and an effective switching frequency of 1 MHz



a) Control structure of PHIL-System 1; b) laboratory prototype; c) Signal processing system (CCU & RTSS); d) CHB phase with four double H-bridge cells; e) 30kVA single-board converter with SiC-B6-bridge (AFE, MPS)

Parallel Hybrid Converter as PHIL output stage

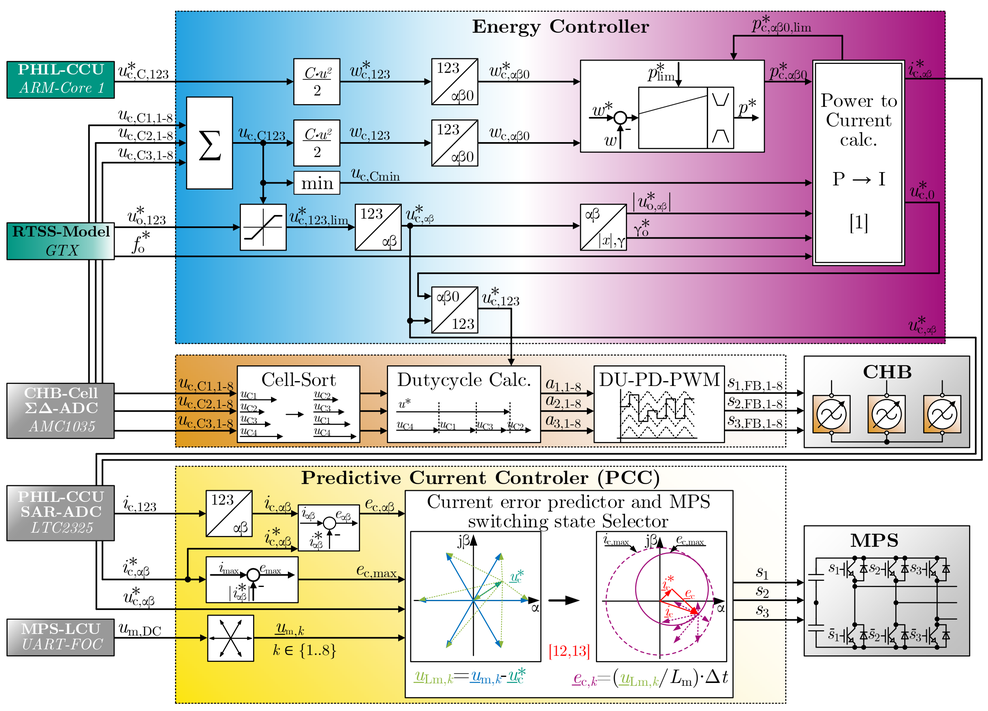
Topology:



Parallel Hybrid Converter Output

- Voltage only defined by the low-power multilevel converter (CHB)
  → $u_o = u_c$
- Active power current only delivered by the high power two level converter (MPS)
  → $i_{o,123} = i_{m,123} - i_{c,123} \approx i_{m,123}$
  with $\frac{i_{c,rms}}{i_{m,rms}} \approx 11\%$

Cascaded control scheme and CHB modulation:



Energy Controller

- Three PI Controller balance the CHB cell capacitor voltages
- Power reference values p_c^* to current reference values i_c^* calculation based on [1] depending on the operating point

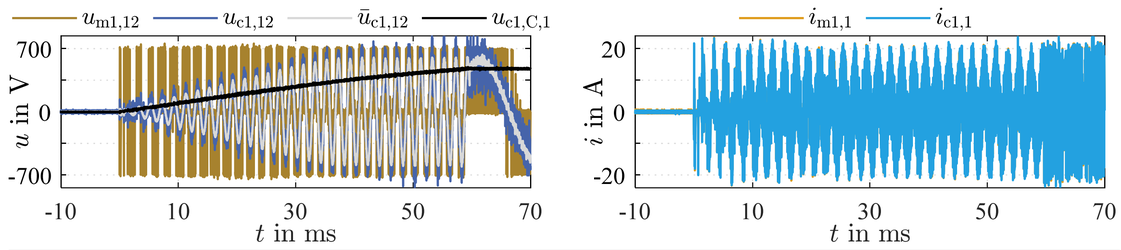
Predictive Current Controller

- Determines the switching states of the MPS and therefore controls and limits the CHB currents

CHB Modulator

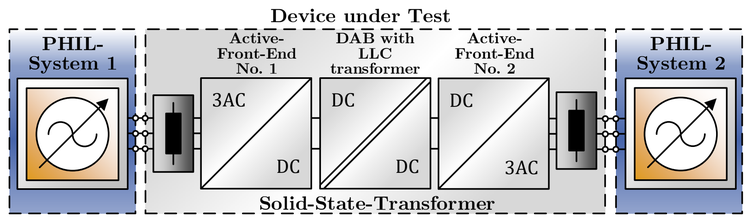
- Balances the CHB cell voltages in each arm and determines which CHB cells are used to form the output

Measurements result active CHB pre-charge

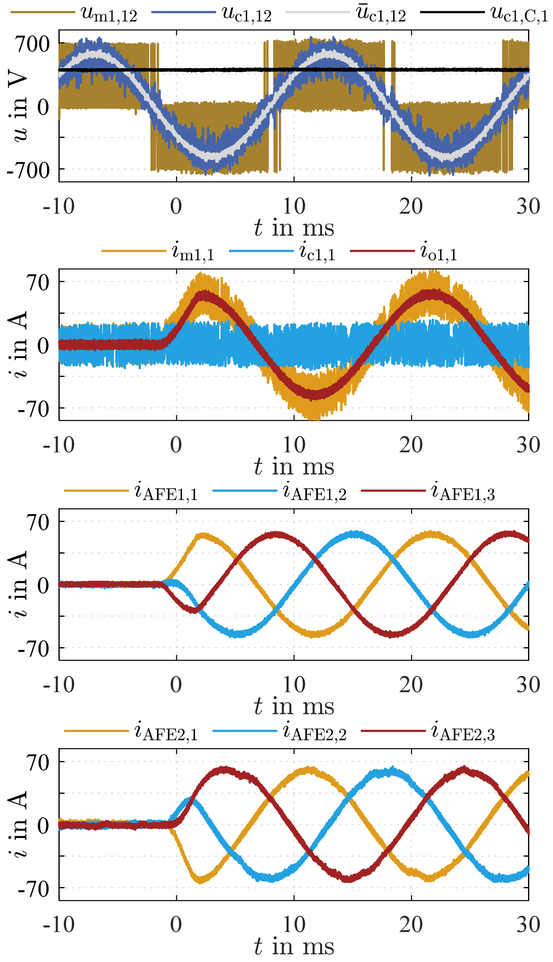


Active pre-charge of the CHB cell capacitors to an arm voltage of $u^*_{c,C,x} = 480V$ with a $f^*_o = 500Hz$ and $\hat{u}^*_{c,x} = 325V$

Grid emulation measurements result



Each of the two PHIL systems emulates an ideal 50 Hz 400 V grid. A 30kVA solid-state transformer (SST) is connected to the PHIL test bench as a DUT. At t = 1.2 ms, the SST performs a load step from 0 kW to 29 kW.



- The line to line output voltage of PHIL-System 1 $u_{c1,12}$ is depicted in blue and is only defined by the low power high dynamic CHB. The grey curve is the CHB output voltage filtered in post-processing with a 1µs wide MA-Filter.
- The 29 kW load step does not effect the arm voltage $u_{c1,C1}$ of the CHB or its output voltage $u_{c1,12}$ nor is it visible in the CHB current $i_{c1,1}$.
- The fundamental output current of the PHIL system is fully supplied by MPS a the high power two level converter regardless of the operating point, thereby limiting the CHB output current to the MPS current ripple.
- The output voltage and current of the PHC/PHIL are not affected by the switching 2-level voltage of the MPS and the current ripple of the PHC/PHIL output current is only caused by the AFE1 and AFE2 switching with 50 kHz.
- The low power CHB has a effective switching frequency of 1 MHz ($\bar{f}_{c,SW,MOSFET} = 63.8\,kHz$) and the high-power 2-level MPS has a low average switching frequency of $\bar{f}_{m,SW} = 6.2\,kHz$.

➢ **Conclusion:** Due to advantageous converter configuration, the Parallel Hybrid Converter has the same output voltage characteristics as full-power multilevel converters previously used as PHIL output stage, but has inherently higher power density and lower costs compared to them. The low power CHB only has to carry the current ripple of the 2L-VSC used as Main Power Source (MPS), however it defines the output voltage of the PHC.

[1] L. Stefanski, D. Bernet, M. Schnarrenberger, C. Rollbühler, A. Liske, and M. Hiller, "Cascaded h-bridge based parallel hybrid converter—a novel topology for perfectly sinusoidal high power voltage sources," in IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, pp. 1639–1646.