



Progress of the ECHO SDR Readout Hardware for Multiplexed MMCs

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Abstract

The electron capture in ^{163}Ho (ECHO) experiment seeks to achieve sub-eV sensitivity of the electron neutrino mass through calorimetric decay spectroscopy of ^{163}Ho in large arrays of cryogenic magnetic microcalorimeters (MMCs). Microwave SQUID multiplexing serves to efficiently increase the number of readout channels, thus calorimeters per array and ultimately per cryostat. A corresponding frequency multiplexing room temperature software-defined radio (SDR) system is in development to enable the readout of this increased number of MMCs per cable. The SDR consists of a custom FPGA platform that provides signal generation and analysis capabilities, as well as tailored signal conversion and analog conditioning front end electronics that enable the room-temperature-to-cryogenic interface. Ultimately, the system will read out 400 multiplexer channels with double pixel detectors through a bandwidth of 4 GHz (IEEE C band). As high-resolution data converters are limited in sample rate, the C-band is split into five sub-bands using a two-stage mixing method. In this contribution, a prototype of the heterodyne RF design is presented. It comprises one of the five 800 MHz sub-bands for a target frequency range between 4 and 8 GHz. Furthermore, the second version of the A/D converter stage is presented, capable of generating and digitizing up to five complex basebands using 1 GSs⁻¹ converters, the reference clocks and a flux-ramp signal. We will show first results of their single and combined characterization in the lab. The current state of the prototype hardware enables preliminary measurements, only limited in bandwidth and with slightly higher noise. Potential improvements could be derived and will be implemented in the full bandwidth, 5-sub-band RF PCB design.

Keywords Magnetic microcalorimeters · Software-defined radio · Frequency-division multiplexing · Microwave SQUID multiplexer · Data acquisition

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1 Introduction

Superconducting and cryogenic detectors show outstanding properties and sensitivity. Notable examples are transition-edge sensors (TESs) [1], superconducting nanowire detectors [2], kinetic inductance detectors (KIDs) [3] and magnetic microcalorimeters (MMCs) [4]. They can be tailored to a wide range of use cases by variation of their geometry and building them into compound assemblies.

The outstanding sensitivity comes at the cost of difficult to attain temperatures and complicated readout for large detector arrays. SQUID multiplexing [5, 6] and microwave SQUID multiplexing [7, 8] allow a reduction in wiring, but come at a cost of a more complex readout [9, 10]. In the electron capture in $^{163}\text{Holmium}$ (ECHO) experiment, microwave SQUID multiplexed MMCs are used [11].

The experiment employs fifteen signal chains, each containing a multiplexer with 400 channels with two MMC pixels per channel and will require highly parallel data acquisition [11, 12]. This allows a total event rate beyond 100 kBq, thereby decreasing the measurement time for the decay energy histogram. The kinematic endpoint energy is used to investigate the neutrino mass [11]. In the following, this work describes the prototype development of the analog signal generation, conditioning and analysis electronics for the SDR to be used in the ECHO experiment.

The readout of the cryogenic multiplexers utilizes microwave signals. A comb of continuous wave (CW) tones is applied, representing frequency division multiplexing, with each tone probing one channel. As the target channel isolation demands 10 MHz of spacing, the 4 GHz of signal bandwidth is divided up into 400 multiplexer channels. Signal generation, data acquisition and online decimation are implemented on a custom, FPGA-based SDR platform. It is segmented into three parts (Fig. 1): The digital electronics MPSoC Board with FPGA, analog/digital (A/D) and digital/analog (D/A) Converter Board, as well as a RF-Mixer Board including level matching circuitry [9].

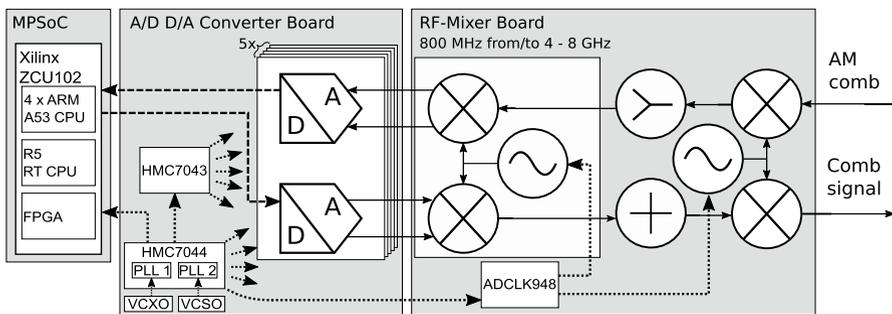


Fig. 1 Block diagram view of the current SDR system, showing the PCBs and clock tree. The modular schematic allows extension of usable bandwidth through up to five DA/AD and IQ mixer stages (white sections) [13]. The signals are then combined and divided at IF (junctions shown as + and-) . Here, only one of the five sub-bands is in use

No currently available high dynamic range (> 8 bit) converters can individually cover the full bandwidth, necessitating parallel signal treatment on the room temperature side. The 4 GHz acquisition bandwidth is split into five sub-bands spanning 800MHz each. I & Q mixing ensures spectral efficiency. Frequency and phase stability are paramount. Thus, one high quality 100 MHz clock reference is shared across all PCBs (Fig. 1). It is fanned out from the A/D D/A Converter Board to the RF-Mixer and MPSoC Board. Output levels and phase noise contributions are evaluated at all stages, from clocking over D/A and A/D conversion as well as the RF-Mixing stage.

2 Global Clock Generation

The root of the clock tree is the HMC7044 clock generator chip, integrated into the A/D D/A Converter Board. It contains two phase-locked loops (PLLs) in a jitter cleaning topology. The first low loop bandwidth PLL uses an external KVG GmbH 100MHz voltage controlled crystal oscillator (VCXO) to provide a jitter cleaned frequency reference to the second PLL. The second, higher loop bandwidth PLL can be operated with an internal 3 GHz VCO or an external Crystek corp. 1 GHz voltage-controlled surface-acoustic-wave (SAW) oscillator (VCSO) to improve the phase noise in the mid-range region. The HMC7044 phase detector frequency, loop bandwidth and reference frequencies can be chosen at will to shape the resulting phase noise and optimize for the input bandwidth (400 MHz). The clocks are distributed and further fanned out with a HMC7043 clock repeater chip. The clock chips supply the A/D and D/A converters with the device clock (DCLK) and the *Sysref* reference signal to support JESD204B subclass 1 operation. The clock chips also provide outputs to the MPSoC Board and a reference clock for the RF-Mixer Board to achieve overall synchronization.

The clock on the prototype A/D D/A Converter Board works as expected and fulfills the data sheet's specification of the HMC7044 to a large extent. Exempt is the range from 100 Hz to 10 kHz that exceeds it and needs further investigation. Furthermore, board layout-related spurious frequencies from the power supply, spurs from the reference input and the VCXO is observed on the VCSO signal. The phase noise around 10 kHz is reduced when using the external VCSO (compare Fig. 2). As expected, there is little visible difference in phase noise from the generator HMC7044 to the repeater HMC7043 (Fig. 2). Both clock chips show essentially identical RMS jitter behavior up to 1 MHz at 72 fs, but their difference amounts to a 30 fs increase for larger integration bandwidths. The total jitter for the internal clock (compare Table 1) allows a theoretical SNR of approx. 67.5 dB for input signals up to 400 MHz using the internal VCO. Solving the spurious issues through a layout revision should yield an improvement of up to 6 dB.

Two of the A/D D/A Converter Board's clock signals are provided as reference for the RF-Mixer Board end (Fig. 1), where the clock signal is buffered and fanned out again by an ADCLK948 chip.

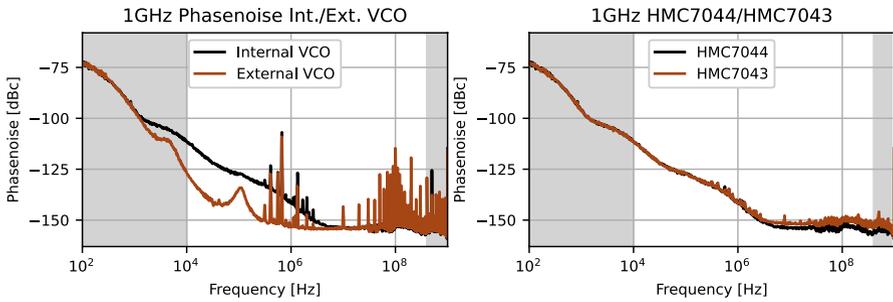


Fig. 2 Phase noise of the clock signals for the A/D D/A conversion stage and the reference for the HF-VCO on the mixing stage. Phase noise spectrum of the HMC7044 chip with internal VCO and external VCO (VCSO-914, 1 GHz) (left). Phase noise spectrum of the HMC7044 source with internal VCO and the HMC7043 repeater chip (right). Measured with baluns without amplitude compensation. Spurious frequencies from power supply were removed (compare Table 1)

Table 1 RMS jitter values for the clock generation and distribution tree on the A/D D/A Converter Board at 1 GHz

Source	RMS jitter	
	Incl. Spurs (fs)	Excl. Spurs (fs)
HMC7044 ext.	651	94
HMC7044 int.	168	114
HMC7043 int.	168	143

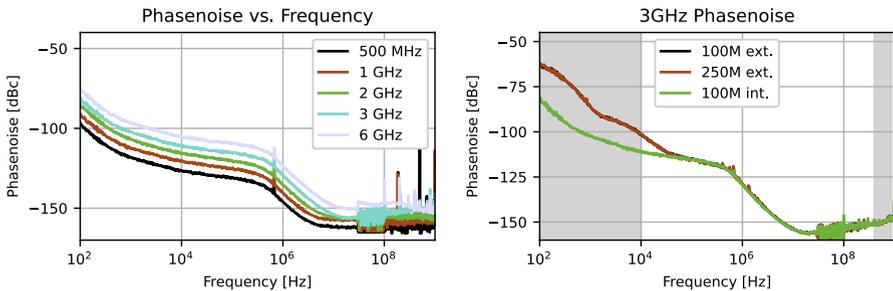


Fig. 3 Phase noise of the LMX2594 local oscillators at different frequencies (left) and comparison of a 3 GHz LO tone of a standalone onboard TCXO to the clock tree reference (right). The RMS jitter is calculated through integration of the phase noise within the band of interest (limits in grey). It is around 80 fs and does not change with frequency

The local oscillators (LO) for all RF mixing stages consist of LMX2594 low phase noise PLL chips. The LO output is filtered to the respective band for suppression of harmonic spurs. The data sheet specifies a lower bound of 47 fs RMS jitter at 8 GHz.¹ This is neither reproduced by the manufacturer's evaluation PCB (52 fs) nor by the prototype (58 fs), likely due to limited slew rate from a sinusoidal

¹ Integration bandwidth from 100 Hz to 100 MHz.

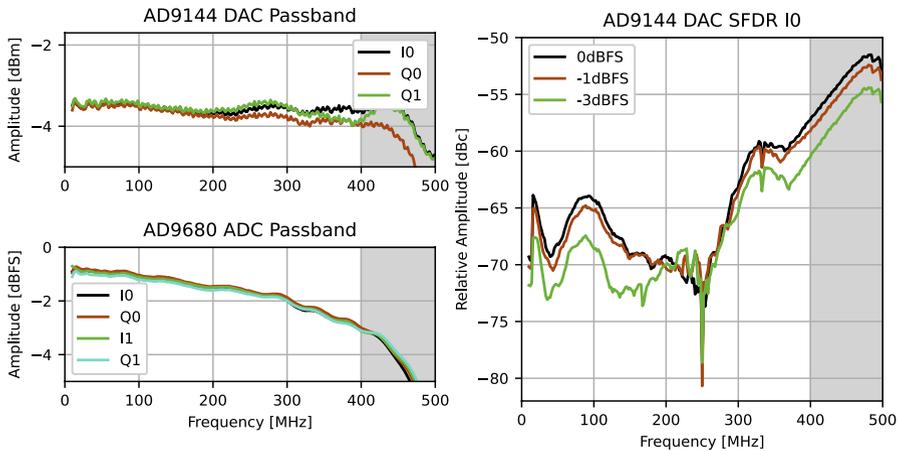


Fig. 4 Baseband transmission characteristics of A/D and D/A converters. The ADC frequency response, measured at 1 dBm input level, resulting in approx. -1 dBFS digital signal amplitude at 50MHz (bottom left). The DAC frequency response, generated at 0 dBFS digital signal amplitude (top left). The balun interface band distortion was compensated with premeasured data. The measured SFDR of the DAC is shown for different output powers (right)

reference. Increasing the integration bandwidth to 1 GHz increases RMS jitter by 5 fs. When operating with the onboard reference, the local oscillators achieve better than 90 fs of RMS jitter for all LO frequencies (Fig. 3) and are in agreement with the local TCXO reference of 80 fs (Fig. 3). The global clock does not yet provide a better close in noise behavior but prevents frequency drift due to inaccurate TCXO reference frequencies. For the desired range there is a difference of roughly 10 fs. As the front end is operating at a higher temperature and also includes a fan-out buffer in the clock path, this slight degradation is anticipated. Overall performance with an external reference is thus nominal. In conclusion, the reference frequency jitter is not substantially affected by the local oscillators and works as expected.

3 A/D D/A Converter Board

The complex basebands require five I & Q signal pairs or ten separate ADC and DAC channels. AD9144 DAC chips with four channels and AD9680-1000 ADCs with two channels have been chosen. Each I & Q pair covers a complex baseband of 800 MHz. The modular A/D and D/A concept proposed in [9] was consolidated onto a single, revised board, after the sub-components were tested successfully. This new revision eliminates the need for additional connectors for the high-speed signals and enables clustering of analog connections, consequently unifying all baseband connectivity into a single differential pair connector. The measurements of the converters were performed with an additional balun conversion card.

The prototypes output and input frequency response is depicted in Fig. 4. The DAC side shows little slope from the LFCN-400+ reconstruction filter and

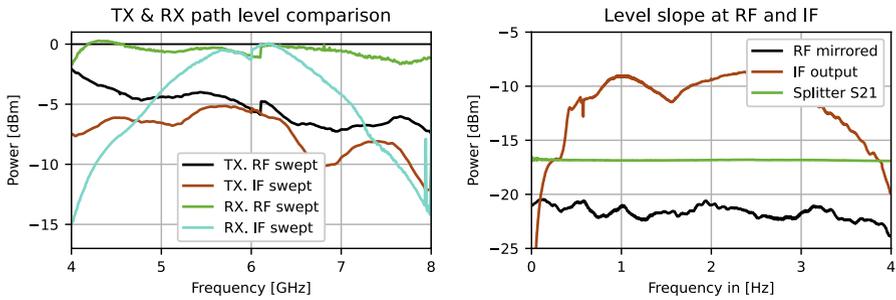


Fig. 5 Signal slope and level fluctuation of the TX and RX RF paths when sweeping the IF or RF LO (left). Some slope is already compensated by equalization ICs. RF, IF and VNA measured splitter/combiner characteristic compared (right). A strong IF dependence is apparent, which is caused by the return loss on the splitter/combiner and uncompensated (De) Modulator IF slope

fluctuation, as well as tight channel grouping. The congruence holds true for the ADC. However, there is roughly a 2 dB slope towards the 400MHz edge of band, which is partly caused by the employed LFCN-320+ anti-aliasing filter. In 0 dBFS operation, the DAC yields a worst-case spur suppression of -57 dBc (at 400 MHz) in the first Nyquist zone. This undercuts the value in the data sheet, due to the intrinsic attenuation of the enabled inverse sinc filter on the chip. In sum, the A/D D/A Converter Board is ready to be deployed with minor tuning along the way.

4 RF-Mixer Board

For the RF front end, exotic components are avoided in favor of commercially available radio hardware. Hence, modulation and demodulation are performed by wireless communications integrated circuits (LTC5588 and LTC5586). Because of their limited frequency range a second stage of conversion is employed utilizing an LTC5549. Combining and splitting of the signal on the intermediate frequency (IF) avoids doubling the amount of local oscillators. The prototype RF-Mixer Board only contains a single IF conversion stage. It also uses single-ended signaling the complex baseband and LO, which will change to differential lines for the final setup to further increase the signal-to-noise ratio (SNR). Additionally, the clock signal is routed in a differential fashion.

The prototype was successfully built and characterized as follows. The RF output and input frequency response is measured to determine flatness of the band for both the eventual 4–8 GHz band and the IF stage (Fig. 5 left). The transmission branch features some level slope (Fig. 5) mostly caused by additional amplification and variable attenuation circuitry of the evaluated prototype. The strong IF frequency dependence (Fig. 5 right) is traced to the -10 dB reflection coefficient of the devices connected to the resistive IF combiner. This splitter/combiner will thus be replaced by a directional coupler-based signal consolidation scheme with higher isolation. Similarly, the IF amplification stage biasing circuitry notch around 1.5 GHz is alleviated by damping resistors and shunting capacitors. A trade-off between output flatness and SFDR is

made by sweeping either the RF or IF LO. The variation of all LOs will be constrained in the future due to filtering. Local oscillator spurs are addressed through phase-locked-loop staging in the clock tree, avoidance of fractional operation ($\Sigma\Delta$ modulation of the N-divider for arbitrary frequencies [14]), loop filter adjustments and supply isolation. Overall, the single baseband prototype RF-Mixer Board requires baseband compensation. It is thus fully functional, albeit at a slightly degraded SNR. These issues will be addressed for the final five baseband version.

5 Summary

A first complete assembly containing all qualitative stages of the room temperature SDR electronics for the ECHO experiment was assembled and evaluated. This complete chain of the SDR system was proven to be fully functional. Clocking performance is sufficient for the intended SNR, albeit coming with avoidable spurious contributions, originating from a routing error of the clock distribution IC. The A/D D/A Converter Board shows nominal level flatness and SFDR, whereas the RF-Mixer Board exhibits major sloping. The latter could be traced to separately addressable IF and RF contributions. Local oscillator performance is to spec, while the final baseband connectivity will ultimately be characterized in the next iteration. The identified limitations will be addressed for the next prototype at full RF bandwidth and data rate. This yields a confident positive outlook for the advancements of the electronics of the ECHO experiment.

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Data Availability The data sets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

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