A W-band Low-Power Gilbert Cell Mixer with Image Rejection in 130-nm SiGe BiCMOS Technology

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***Abstract* — This paper presents a 100-GHz Gilbert cell down-conversion mixer with an integrated image rejection functionality, implemented in a 0.13-µm SiGe BiCMOS technology. The maximum measured conversion gain is 3.7 dB with an LO power of only –10 dBm, while the image rejection ratio (IRR) is 38 dBc at an RF frequency of 100 GHz. The circuit consumes 8 mW of power without buffers, and its core part occupies only 0.048 mm^2 of IC area.**

***Keywords* — millimeter wave mixers, image, conversion gain.**

I. Introduction

The mm-wave band gets nowadays an increasing attention due to higher achievable data rates, required by various applications. Modern communication systems often include large phased arrays, consisting of tens or even hundreds of elements. Depending on the beamforming type, such arrays contain a large number of corresponding RF chains that, in turn, makes area and power efficiency of individual components a crucial factor.

Nowadays various receiver architectures are being actively investigated. Most common RF-beamforming phased arrays suffer from challenging phase-shifter implementation, especially at frequencies above 100 GHz. High losses inevitably require compensation in the receive chain, either by the use of an active phase shifter or additional post-amplifiers, leading to larger power and area consumption. Both metrics are crucial for large-scale phased arrays, used in example for Massive MIMO systems,. due to tight element spacing requirements and overall energy efficiency. IF beamforming phased arrays can be an alternative solution, in which the signal is first down-converted to an intermediate frequency and then the phase shifting is applied. The IF beamforming and in particular high-IF beamforming (e.g., IF of 10 to 20 GHz) architecture has certain advantages for signal frequencies of 100 GHz and above.

Achieving low RMS phase and magnitude errors, as commonly required by modern beyond-5G systems at these frequencies may be very challenging in an RF beamforming architecture. Moving phase shifting to IF partially alleviates this problem, at the same time phase shifters designed for the high-IF beamforming architecture are naturally more compact in comparison to a conventional IF beamforming case. However, the image signal problem is not actively considered for IF beamforming receivers, even though its degrading effect remains important. For example, in work [1], no additional image filtering was used and IRR of 20 dB was achieved mostly by LNA gain response. However, this value might not be sufficient for many applications, since low IRR leads to an increase in NF and the image signal can significantly degrade the overall chain performance. The use of an IQ modulator ([2], [3]) is the most common way of suppressing the image signal. In this case, the image is cancelled by the modulator architecture itself without additional filtering. However, its performance is significantly dependent on the phase and amplitude imbalances between I and Q branches. To solve this problem, certain compensation and calibration approaches may be used, as in [2]. However, these methods also result in an increased area and complexity. Moreover, to provide a 90° phase difference typically a coupler or a polyphase filter is needed, which very often requires a similar area as the mixer itself, or results in high loss, requiring additional gain stages.

In this paper, a compact and low-power W-band down-conversion mixer with an incorporated band-stop filter for the image suppression is presented. The mixer is implemented in IHP's SG13G2 BiCMOS technology. The presented mixer is suitable for a high-IF beamforming architecture with an IF frequency of 20 GHz.

II. Circuit Design

The mixer topology is based on a Gilbert cell formed by transistors Q_{1-6}, as shown on Fig. 1. The Gilbert cell is followed by a common-collector buffer ($Q_{7,8}$) to decouple the low output impedance of 50 Ω of the measurement environment. The circuit is intended to down-convert a 100 GHz input signal to the intermediate frequency of 20 GHz using a corresponding 80-GHz LO signal. Simulated 3-dB bandwidth is 29 GHz.

Minimizing the power consumption was achieved through the use of very small devices, since they require less current. Thus, the transistors Q_{1-4} have the smallest available device size in the used technology. At the same time, since a transconductance stage (transistors $Q_{5,6}$) of the Gilbert cell directly impacts the linearity, devices with twice larger

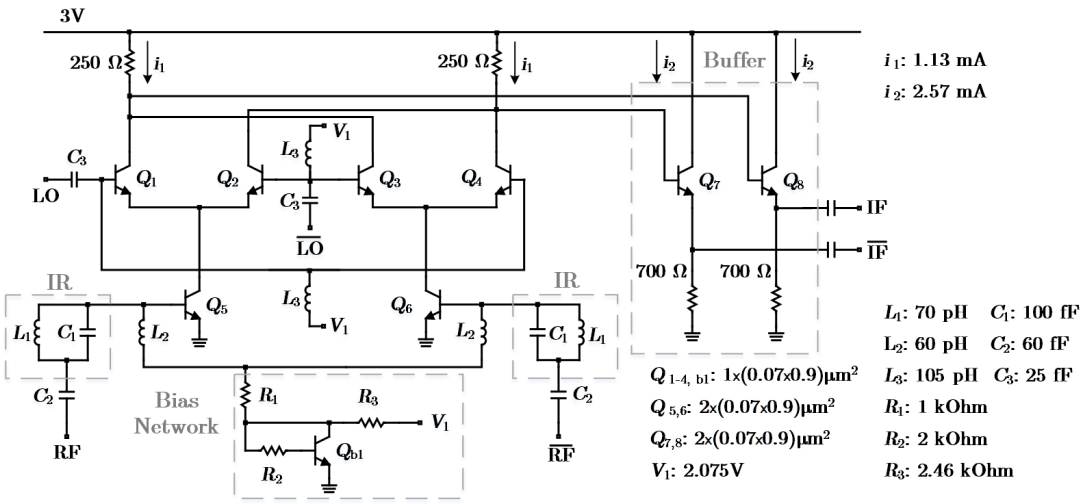

Fig. 1. Schematic of the proposed mixer.

emitter area were chosen as a trade-off between the power consumption and linearity.

Due to very low DC currents, provided by $Q_{5,6}$ transistors, Q_{1-4} operate close to a cut-off region. Further, due to the relatively high impedance of these small devices, a low LO signal power of –10 dBm is sufficient to ensure full switching of the quad devices and thus to maximize the conversion gain. This is an adventurous property of this design, especially when integration into a multi-channel architecture is envisioned, where LO distribution with sufficient signal power can become quite challenging.

The image rejection functionality is implemented through the use of a band-stop filter, implemented as a parallel resonator at the RF input that is composed of L_1 and C_1, chosen for a center frequency of 60 GHz. At 100 GHz, the resonant circuit acts capacitive, which in combination with C_2 and L_2 forms an L-type matching network to match the input impedance.

The smallest device size that is able to ensure the appropriate output matching (return loss better than –10 dB) and linearity were chosen for the output buffer. The input matching for the LO port at 80 GHz is done similarly to the RF port, using a shunt inductor L_3 and a series capacitor C_3.

Components R_{1-3} and Q_{b1} form a current mirror forming the bias network. Resistors $R_{1,2}$ are used to isolate the RF signal and are scaled to accommodate different base currents, since the current mirror and g_m-stage transistors have different sizes. Resistor R_3 is used to transform V_1 to a proper V_{CE} voltage for transistors $Q_{5,6}$.

The Gilbert cell uses resistive 250 Ω loads to reduce the chip area, because due to RF and LO input matching networks the layout contains many bulky components. The chosen value provides sufficient gain and necessary voltage at the collector node of the switching stage devices.

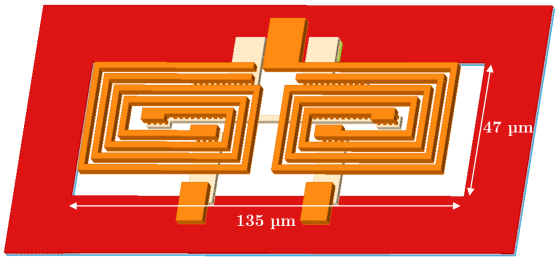

Fig. 2. Marchand balun.

The designed Gilbert cell consumes 8 mW of power and the active circuit core occupies 0.048 mm^2 of IC area. The total power consumption of the circuit including the common-collector buffer is 23 mW. The simulated single-sideband noise figure is 15 dB.

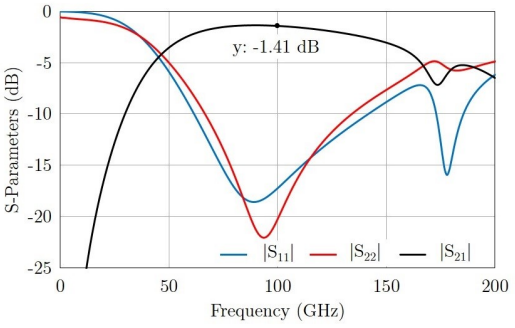

Fig. 3. S-Parameters of the balun.

Two Marchand baluns at RF and LO inputs are included for the measurement purposes. The 3D view of the side coupled balun is shown in Fig. 2. Fig. 3 and Fig. 4 present its simulated

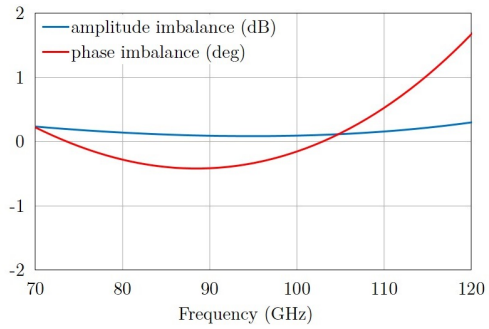

Fig. 4. Amplitude and phase imbalances of the balun.

performance, namely S-parameters as well as amplitude and phase imbalances. The balun exhibits 1.41 dB of excess loss at 100 GHz. The simulated amplitude and phase imbalances are 0.092 dB and 0.15° at the same frequency.

The total area of the chip with baluns and measurement pads, shown in Fig. 5, is 0.31 mm^2.

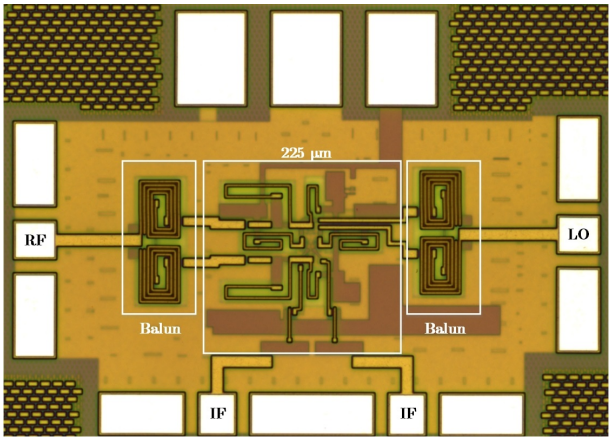

Fig. 5. Chip photograph.

III. Experimental Results

The measurements have been carried out using a broadband on-wafer system including a Keysight N5247B VNA. In Fig. 6, simulated and measured s-parameters for the RF and LO ports are shown. Noticeable frequency shifts in the measurement data are presumably caused by slight inaccuracies due to piece-wise EM simulation of the mixer and the baluns.

For the conversion gain measurement, a 3-port scalar mixer/converter (SMC) mode of the VNA was used instead of the spectrum analyzer mode. A separate signal generator was used as a source for the LO signal. The results are presented in Fig. 7. This measurement is done by sweeping f_{RF}, while keeping fixed $f_{\mathrm{LO}} = 80$ GHz with an LO power of –10 dBm. A solid line is a fitting curve for the measurement data shown as a set of dots, caused by calibration imperfections. Due to equipment limitations, the measurement has been performed for the limited RF frequency range of 90 – 110 GHz, and 55 – 65 GHz to confirm the image rejection functionality. A

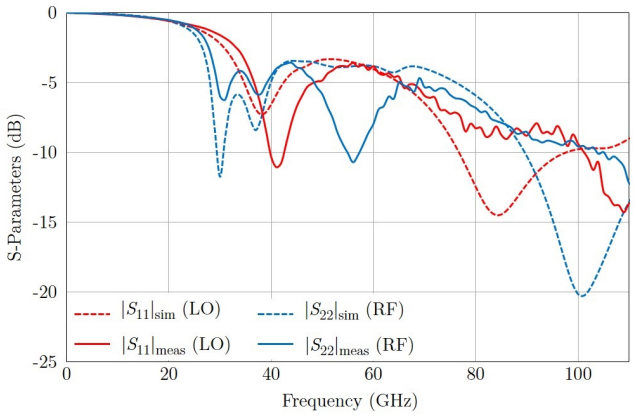

Fig. 6. S-parameters for RF and LO inputs.

comparison to the simulated data demonstrates a good match and an IRR better than 35 dBc for the RF frequency range of 90 – 105 GHz. At 100 GHz, an IRR is 38 dBc. The notch at 80 GHz is due to on-chip DC-blocking capacitors that suppress the IF signal when RF and LO frequencies are both at 80 GHz.

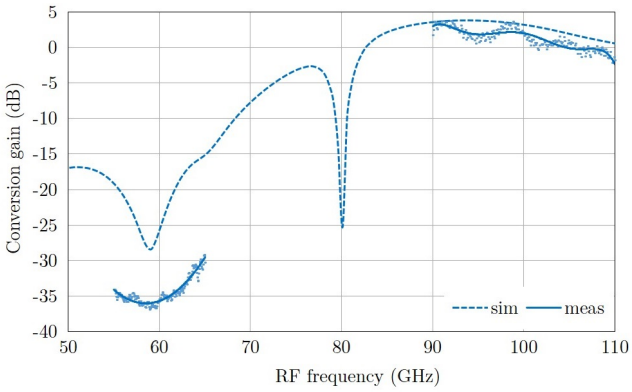

Fig. 7. Conversion gain versus RF frequency. Dip at 60 GHz demonstrates image suppression. $P_{\mathrm{LO}} = -10$ dBm. $f_{\mathrm{LO}} = 80$ GHz.

Fig. 8 shows the simulated and measured conversion gain versus LO power at $f_{\mathrm{RF}} = 100$ GHz, $f_{\mathrm{LO}} = 80$ GHz, $f_{\mathrm{IF}} = 20$ GHz, and $P_{\mathrm{RF}} = -30$ dBm. The power level of –10 dBm for LO signal was eventually chosen, because its further increase does not result in a significant gain improvement, as can be seen from the simulation curve.

Fig. 9 presents a dependence of the conversion gain on a RF power at $f_{\mathrm{RF}} = 100$ GHz, $f_{\mathrm{LO}} = 80$ GHz, $f_{\mathrm{IF}} = 20$ GHz, and $P_{\mathrm{LO}} = -10$ dBm. The simulated input-reffered 1-dB compression point is –11.5 dBm and the measured value is –12.3 dBm.

IV. Conclusion

In this paper, we presented a compact low-power 100-GHz down-converting mixer in 130-nm SiGe BiCMOS. Due to an integrated band-stop filter, an image suppression with an IRR of 38 dBc was achieved. This mixer is suitable for a receiver

Table 1. Performance Summary

	Technology	f_{RF}, GHz	f_{IF}	CG, dB	LO power, dBm	Input $P_{1\mathrm{dB}}$, dBm	IRR, dBc; Topology	P_{DC}, mW	Area, mm^2
[2]	65-nm CMOS	65	1.25 MHz	0±1	2	n/a	>40 (IQ modulator)	40.8	0.861[(1)]
[3]	100-nm GaAs pHEMT	93	50 MHz	–8.7	10	n/a	19.2 – 47.9 (IQ modulator)	–	2.72[(1)]
[4]	130-nm SiGe	135	5 GHz	32	0	-41	no IR	65	0.2
[5]	90-nm CMOS	94	0.1 GHz	14.6	1	–8.7	no IR	5	0.358
[6]	22-nm FD-SOI CMOS	70	3.8 GHz	12 – 15	n/a	-5.6 – -8	17 – 32 (Mixer-first; IQ modulator)	36	1.68[(2)]
[7]	22 nm FDSOI	60	1 MHz	21	-3	-16.2	no IR	5.25	0.065
This work	130-nm SiGe	100	20 GHz	3.7	–10	–12.3	38 (Gilbert cell)	8	0.048

[(1)] including pads
[(2)] whole receiver

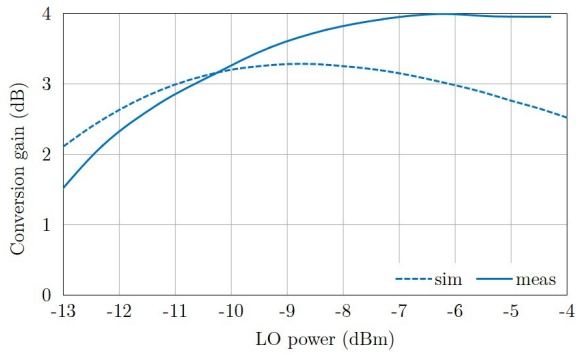

Fig. 8. Conversion gain versus LO power. $P_{\mathrm{RF}} = -30$ dBm.

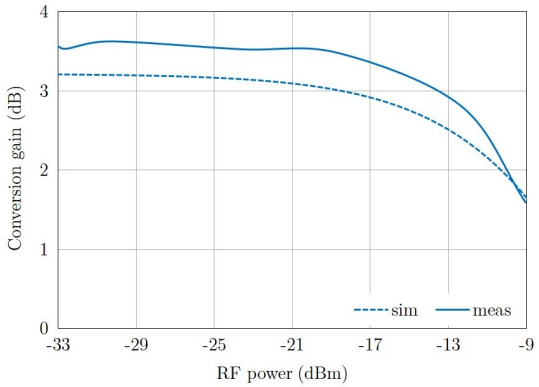

Fig. 9. Conversion gain versus RF power. $P_{\mathrm{LO}} = -10$ dBm.

chain without the use of IQ architecture, which may reduce the occupied area in multi-channel architectures.

Performance of the mixer as well as an overview of previously published works, implemented in various technologies with a comparable RF frequency, is shown in Table 1. The proposed mixer operates with a much lower LO power, which makes the overall implementation easier in this frequency range. According to this comparison, an image rejection was previously either typically implemented with the use of IQ architecture or not considered at all. The table also demonstrates that we present one of the most compact designs.

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