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SUB-NANOSECOND SWITCHING OF HV SiC MOS TRANSISTORS FOR IMPACT IONISATION TRIGGERING

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Abstract

Pulse generators with multi kV/kA pulses are necessary in particle accelerator environment for beam transfer magnets. Traditionally these generators are using thyratrons – until recently the only switches capable of switching such pulses within tens of ns. There is a strong demand to replace thyratrons by semiconductor switches to avoid their future obsolescence. Very promising candidates are components from the family of fast ionisation dynistors triggered by impact ionisation. Their sub-nanosecond switching time and extreme current densities can provide performances superior to that of thyratrons. Recent investigations showed that impact ionisation triggering is feasible also in cheap industrial thyristors. The main issue is the generation of triggering pulses with slew rates in the multi kV/ns region and with the required output current for charging the parasitic capacitance of the thyristor. We present an approach of generating > 1 kV/ns pulses by ultra-boosted gate driving of HV SiC MOS transistors. We found that the MOS lifetime under these extreme triggering conditions can still reach more than 10^8 pulses – enough for kicker generator applications in particle accelerators.

INTRODUCTION

Fast beam transfer kicker magnets in particle accelerator environment require up to 80 kV and 30 kA rated pulse generators. Presently used thyratrons suffer from various imperfections like current and total conducted charge limitation, risk of spontaneous firing, need of complex triggering and biasing electronics and risk of the future obsolescence due to limited market demand. A very promising replacement candidate is the family of the components derived from Fast Ionisation Dynistors (FID) – a concept developed at the Ioffe institute in St. Petersburg [1]. The concept is based on the generation of a fast ionisation wave front inside the reversely biased p-n junction, leading to the creation of an electron-hole plasma with electric field collapsing in the region already filled with e-h plasma and resulting in an ionisation front propagating with a speed higher than the charge carrier velocity. Thus, sub-nanosecond switching can be achieved with a current slew rate and current densities not achievable under normal triggering [2]. Recently it was shown that standard slow industrial thyristors can be triggered in the same way [3] as well as highly interdigitated fast switching GTO-like thyristors [4]. The generation of the HV triggering pulse with dU/dt > 1 kV/ns is challenging and the solution traditionally used is based on a drift step recovery diodes (DSRD) – components not commercially available yet. Another inconvenience of this solution is the time delay necessary to build-up the current in an energy storage coil and for DSRD charge pumping, which is difficult to reduce under several hundreds of ns. This presents a significant limitation for a component capable of sub-ns switching which must wait hundreds of ns for the triggering generator charging-up and cannot hence fully profit from its speed in accelerator systems where short turn-on delay is required.

One of the alternatives to DSRD based generators is a photoconductive semiconductor switch (PCSS) based solution proposed in [5]. It requires a powerful laser for PCSS activation and very fast laser driver using an S-diode for laser current pulse sharpening. The remaining problem of this solution is the PCSS lifetime and commercial availability PCSS and S-diode.

METHOD

We propose a fast generator based on the boosted commutation of a cheap commercially available HV SiC MOS. The "gate boosting" technology was described in recent works done at KIT [6]. Increasing of the commutation speed of silicon IGBTs and MOS transistors was achieved by a transient triggering pulses with up to 80 V amplitude to counterbalance the effects of MOS/IGBT leads inductance and internal parasitic capacitances. Reduction of rise time (Tr) by a factor of up to ~ 8 was reported. In frame of this work gate voltage at wafer level was measured and the "boosting voltage" was limited to not exceed recommended maximum gate-source voltage. Later work inspired by this technique allowed further shortening of SiC MOS Tr by a factor of up to ~ 10 [7].

Since our target applications – CERN kicker systems – are performing up to ~ 10^8 pulses during their lifetime, we chose to use a more aggressive triggering approach, potentially reducing component lifetime while keeping it compatible with the kicker system lifetime. We did not try to measure nor to limit the gate-source voltage at wafer level; the only parameter we strictly observed was the total injected MOS gate charge (Qtot). We limited it to a value extrapolated from the component datasheet Qtot curve to its maximum authorised gate-source voltage. This condition can be automatically fulfilled by a series capacitor Cs between driver output and the MOS gate with the value according to the Eq. (1):

$$(Udrmax - Ugmax) \times Cs = Qtot(@Ugmax), \quad (1)$$

where Udrmax is the gate driver circuit maximum output voltage, Ugmax is the absolute maximum allowed gate-source voltage; Cs is the value of the series capacitor between driver output and MOS gate and Qtot(@Ugmax) is the total gate charge value extrapolated from datasheet Qtot curve to Ugmax. The Eq. (1) is derived from two simple assumptions: a) the driver output voltage, series capacitor

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and the SiC MOS gate voltages are zero before triggering; b) after SiC complete turn-on the driver output voltage is Udrmax, the MOS transistor gate-source voltage is Ugmax and the series capacitor is charged to the difference between the two voltages (Udrmax – Ugmax) and it hence accumulated the charge of Cs x (Udrmax-Ugmax). As Cs is in series with the MOS gate, the same charge was delivered to the MOS gate. We intentionally neglect transient period and accept a limited duration overvoltage on the gate-source insulator. To fully profit from the gate boosting principle, the driver output slew rate needs to be very high as well. Hence, we designed an ultra-fast MOS gate driver with sub-ns rise time, maximum output voltage higher than the already published 80V and with sufficiently high output current. To achieve this performance, the driver needs to be designed with very low gate charge MOS transistors, using the components in the smallest SMD packages possible to create a very compact PCB design with short tracks, carefully decoupled supply voltage and with gate boosting of each driver's MOS. Since the impact ionization application requires only fast rising edges, the switch requirements are reduced to those of a fast-closing switch with no need for its fast opening. Therefore, the driver design was kept simple and compact and instead of a traditional totem pole output stage it uses a topology with a pull-up PMOS and a pull-down resistor, as shown in Fig. 1.

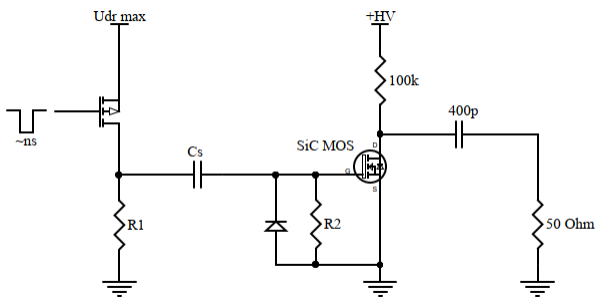

Figure 1: Schematic of super boosting setup.

RESULTS

Measurement of the driver output voltage with 160 V supply into a resistive 50 Ohm load (18 GHz attenuator) is shown on Fig. 2. The output voltage slew rate we measured is ~ 240 V/ns and transition time from zero to 100 V is roughly 410 ps but due to the step response of our 1 GHz scope (350 ps), the real performance is better. Measurement shows interesting negative transient before positive rise which corresponds to a capacitive coupling from PMOS gate to drain via its parasitic gate-drain capacitance before PMOS turn-on starts. The reason is our aggressive super boosting of the PMOS gate. From the negative transient duration one can deduce that PMOS turn-on delay is also in sub-ns region. This negative transient was very likely the reason for SiC gate damage we observed during tests at the beginning of this project. To reduce SiC gate insulator stress, a protection diode between gate and source was added as shown on Fig. 1.

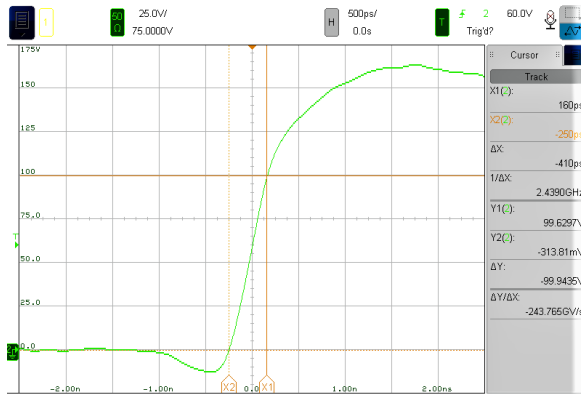

Figure 2: Driver output voltage measurement with 160 V driver supply and 50 Ohm load (attenuator with 18 GHz BW) on Keysight scope DSO-X 6002 (1 GHz BW).

Reliability test with 50 Ohm resistive load was done up to more than $5x10^{10}$ pulses with no sign of deterioration.

Measurement of commutation speed on several 1.2 kV rated Si and SiC transistors operating at 1 kV into 50 Ohm load with this driver confirmed Tr reduction by a factor of up to 20. Lifetime tests showed no observable damage to SiC after more than 50 million pulses.

The most detailed tests were done on 1.7 kV rated SiC MOS - IMBF170R450M1 from Infineon which recently became commercially available. We measured Tr of 950 ps @Uds = 1.3kV with the driver voltage of 160V but in view of scope BW, the real Tr is certainly shorter. Gate-source and load voltage measurements for 1.3 kV operation with 160V driver voltage is on Fig. 3.

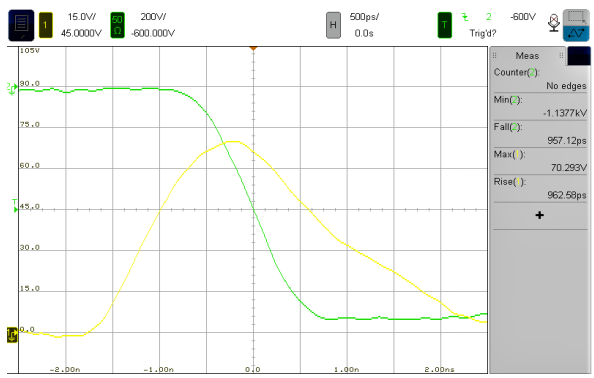

Figure 3: Gate-source voltage (yellow, 15V/div) and load voltage (50 Ohm, green, 200V/div) with 160 V driver; measurement on SiC MOS IMBF170R450M1 operating at Uds = 1.3 kV.

The gate voltage rise time is logically longer compared to the resistive load due to gate parasitic capacitances. It was measured by a 700 MHz passive probe on the leads of its TO263-7 package right at the plastic body level. Negative feedback effect of the SiC g-d capacitance is clearly visible and results in significant reduction of the gate voltage during the drain-source voltage collapse. Due to component leads/bonding wires inductances and gate parasitic capacitances the gate overvoltage amplitude at the wafer

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level is lower and duration is shorter than the one we measured on its leads.

At the beginning of this project it happened, that non-respecting total gate charge condition described in Eq. (1) lead to fast degradation of drain-source leakage current until fatal MOS failure. That is why we periodically measure SiC leakage current during reliability test with the goal to detect the start of leakage current degradation as a sign of approaching failure. The drain-source leakage current of IMBF170R450M1 is extremely low: 100 pA @1.3 kV, which makes this task challenging. During the reliability test with 160 V driver the leakage current remained at this value until ~ 7.5×10^9 pulses and since then it started to rise to 1 nA@7.75×10^9 pulses and to 1.5 nA@8×10^9 pulses but still without visible effect on the load voltage.

Damage to SiC gate insulator due to excessive voltage on the gate is described by the time dependent dielectric breakdown (TDDB) phenomenon. Breakdown mechanism is explained by a cumulative charge trapping on SiC defects, leading to a local field enhancement and resulting at certain point in local current tunnelling until SiO_2 insulator damage. As the phenomenon is cumulative, the shorter is individual overvoltage duration the higher number of pulses will component survive before failure. The current tunnelling at the final phase tends to explain the increased drain-source leakage current in approach of fatal failure.

To find a limit of super boosting approach we modified the gate driver to increase its output voltage up to 280 V. The series capacitance Cs was modified accordingly. SiC rise time was reduced by another ~ 140 ps down to less than 810 ps and overvoltage on the gate lead increased up to > 86 V but with reduced overvoltage duration (~ 2 ns) as shown on Fig. 4. Reliability test was done up to more than 500 million pulses with no visible deterioration of SiC performance. Gate-source and load voltage measurements are on Fig. 4.

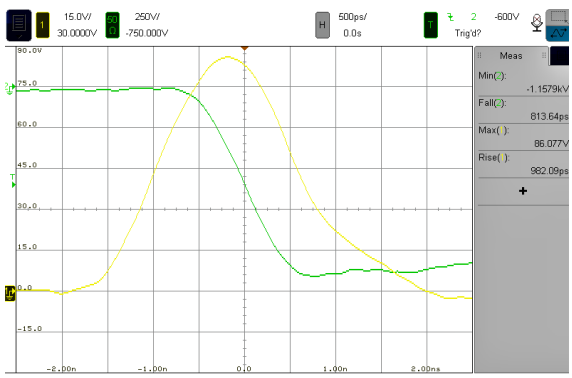

Figure 4: Gate-source (yellow) and load voltage (green) with 280 V driver and Uds = 1.3 kV; measurements are influenced by scope and probe BW limitation (1 GHz and 700 MHz respectively).

Further boosting of the output voltage slew rate was achieved by a two-stage Marx generator with Si sharpening diodes (BY229) used as avalanche switches. Measurement of the Marx generator output voltage is on Fig. 5.

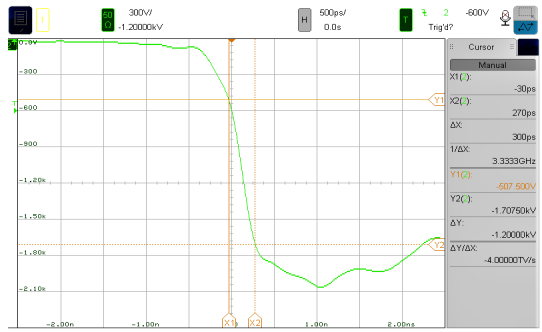

Figure 5: Output of the two stage Marx generator with Si diode sharpener; due to scope BW the real slew rate is higher than 4 kV/ns measured.

CONCLUSION

We confirmed the feasibility of a multi kV/ns pulse generator based on super boosted SiC MOS with Si diode sharpener. The reliability of the super boosted driver and that of the HV SiC was found more than sufficient for particle accelerator beam transfer kicker applications. The Si diode sharpener allowed further increase of the output voltage slew rate up to more than 4 kV/ns, but its lifetime is not sufficient and better results are expected with HV GaAs diodes we recently acquired from the German company 3-5 Power Electronics. Tests on 3.3 kV rated SiC MOSFETs that recently became commercially available have started and are as promising as the ones hereby presented.

REFERENCES

[1] I. V. Grekhov and A. F. Kardo-Susoev, "Formation of sub nanosecond current drops due to the delayed avalanche breakdown of Si p-n junctions", *Sov. Tech. Phys. Lett.*, vol. 5, pp. 395–399, 1979.

[2] I. V. Grekhov, "Pulse power generation in nano- and subnanosecond range by means of ionizing fronts in semiconductors: the state of the art and future prospects", *IEEE Trans. Plasma Sci.*, vol. 38, pp. 1118-1123, 2010. doi:10.1109/tps.2010.2043857

[3] A. I. Gusev, S. K. Lyubutin, S. N. Rukin, and S. N. Tsyranov, "High-Power Thyristor Switching via an Overvoltage Pulse with Nanosecond Rise Time", *Semiconductors*, vol. 50, pp. 394-403, 2016. doi:10.1134/s1063782616030106

[4] A. I. Gusev *et al.*, "Fast high-power thyristors triggered in impact-ionization wave mode", *J. Instrum.*, vol. 14, p. 10006, 2019. doi:10.1088/1748-0221/14/10/p10006

[5] A. I. Gusev, L. Pecastaing, A. De Ferron, I. Prudaev, and B. Novac, "A new approach for triggering thyristors in impact-ionisation wave mode using an avalanche S-diode", presented at 47th IEEE Int. Conf. on Plasma Sciences (ICOPS 20), Singapore, Dec. 2020, paper TA7-S2-030, unpublished.

[6] M. Hochberg, M. Sack, and G. Mueller, "Analysing a gate-boosting circuit for fast switching", in *Proc. IEEE Int. Power Modulator High Voltage Conf. (IPMHVC)*, San Francisco, CA, USA, Jul. 2016, pp. 171–175. doi:10.1109/IPMHVC.2016.8012918

[7] M. Azizi, J. J. van Oorschot, and T. Huiskamp, "Ultrafast switching of SiC MOSFETs for high-voltage pulsed-power circuits", *IEEE Trans. Plasma Sci.*, vol. 48, no. 12, pp. 4262-4272, 2020. doi:10.1109/TPS.2020.3039372