GaN-Based Modular Multilevel Converter for Low-Voltage Grid Enables High Efficiency

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Keywords

≪Modular Multilevel Converters (MMC)≫, ≪Gallium Nitride (GaN)≫, ≪Efficiency≫, ≪Grid-connected converter≫

Abstract

Gallium Nitride (GaN) semiconductors with low inductance packages enable low switching losses and high efficiency. In this paper we present a compact arm PCB design with low loop inductance, allowing for fast and efficient switching. The PCB includes four full-bridge cells for a 7 kW Modular Multilevel Converter (MMC) for low-voltage grid applications.

Introduction

Modular Multilevel Converters (MMC) are frequently used in high-voltage DC transmission systems and other applications like medium-voltage motor drives [1]. Even in applications for the low-voltage grid, the advantageous partial load efficiency of unipolar Si-MOSFETs compared to bipolar Si-IGBTs and a reduced filtering effort brings the MMC topology into consideration. But the benefit of reduced conduction losses, is often overcompensated by an increased communication, gate driving and control effort. By using Gallium Nitride (GaN) enhancement-mode high electron mobility transistors (E-HEMTs) instead of Si-MOSFETs, the driving effort can be reduced, due to lower input capacitance and a driving voltage level of only 5 V. GaN also features a lower output capacitance and zero reverse-recovery loss [2].

In order to analyze and validate the expected performance benefits of using GaN-E-HEMTs as power semiconductors in an MMC, a prototype is built. The MMC is being used in a research project to replace conventional photovoltaic (PV) and battery inverters, which are typically based on two- or three-level topologies. The MMC approach offers the possibility to connect batteries to half of the four full-bridge cells of each MMC arm, as it is shown in Fig. 1. Besides the battery connection to the MMC cells, a single high voltage (HV) battery, e.g. from electric cars can be directly connected to the main DC-bus of the MMC with no additional booster stage, as the MMC offers an intrinsic voltage boost capability. This feature can also be used to save the PV booster stage, as present in typical residential PV inverters, when a PV string instead of a HV-battery is connected to the DC side.

Due to its compact size, this MMC can also be used for educational purposes, e.g. to teach the control strategies of an MMC [3].

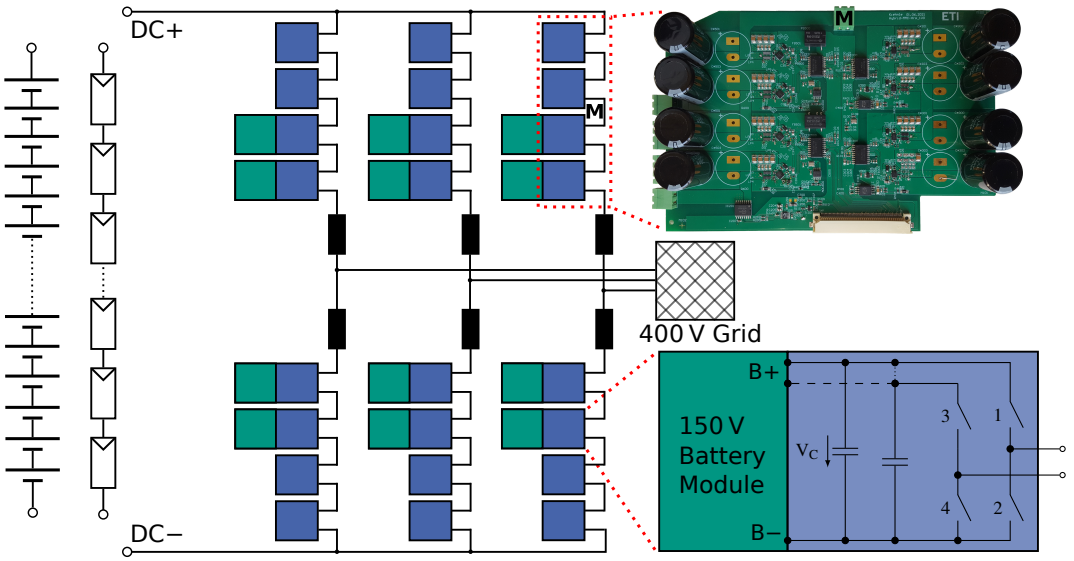


Fig. 1: Hybrid-MMC overview

In this paper, the GaN-based arm PCB with a low internal power consumption is presented. Measurement results of one full-bridge cell and the whole MMC are shown and an overall efficiency estimation is carried out.

Modular Multilevel Converter Arm PCB

The GaN-based arm PCB in Fig. 2 is intended to be used as one arm in an MMC. The four-layer PCB contains four full-bridge cells connected in series on the PCB and has a copper thickness of 70 µm. In the following, the signal section, the power section and the switching behavior of the developed four-cell arm PCB are described in detail.

Signal Section

The white connector on the bottom of Fig. 2 is used to plug the PCB into the mainboard of the ETI-SoC-System, an in-house-developed signal processing system based on the Zynq 7030 system-on-chip (SoC) from Xilinx [4]. The 16 signal pins of the white connector are directly connected to the Kintex 7 field programmable gate array (FPGA) of the SoC. The white connector is also used to provide power for the voltage and current measurement as well as the gate drivers, thus no dedicated cell supply is necessary. The overall power consumption of the PCB with four cells switching at 100 kHz and active measurements is only 1.0 W from the 5 V mainboard rail.

The FPGA of the Zynq generates the PWM signals with a time resolution of 2 ns and processes the data of the current and voltage measurements. For the cell voltage measurements, four delta-sigma ($\Delta\Sigma$) analog digital converters (ADC) are placed directly on the PCB. The ADC clock of 10 MHz is generated on the PCB, so each measurement channel needs only one FPGA pin. The delta-sigma bitstream can be easily evaluated in the FPGA, since the maximum analog level produces a stream of ones and zeros that are high only 90 % of the time, so there occur still enough edges for clock recovery. For the arm current measurement, a ±50 A AMR current sensor with a bandwidth of 1.5 MHz is connected to a 16 bit / 5 MSps SAR ADC. Both of these are located inside the blue box (●) in Fig. 2.

To provide galvanic isolation, fiber optical transceivers are often used in MMCs. But in favour of a much lower power consumption, isolators based on a SiO_2 isolation barrier are used. They feature 5 kV_{rms} isolation with a common mode transient immunity (CMTI) of ±100 V/ns. They also shift the FPGA voltage level of 1.8 V to isolated 5 V signals and provide 5 V supply for the cells using an integrated DC-DC converter.

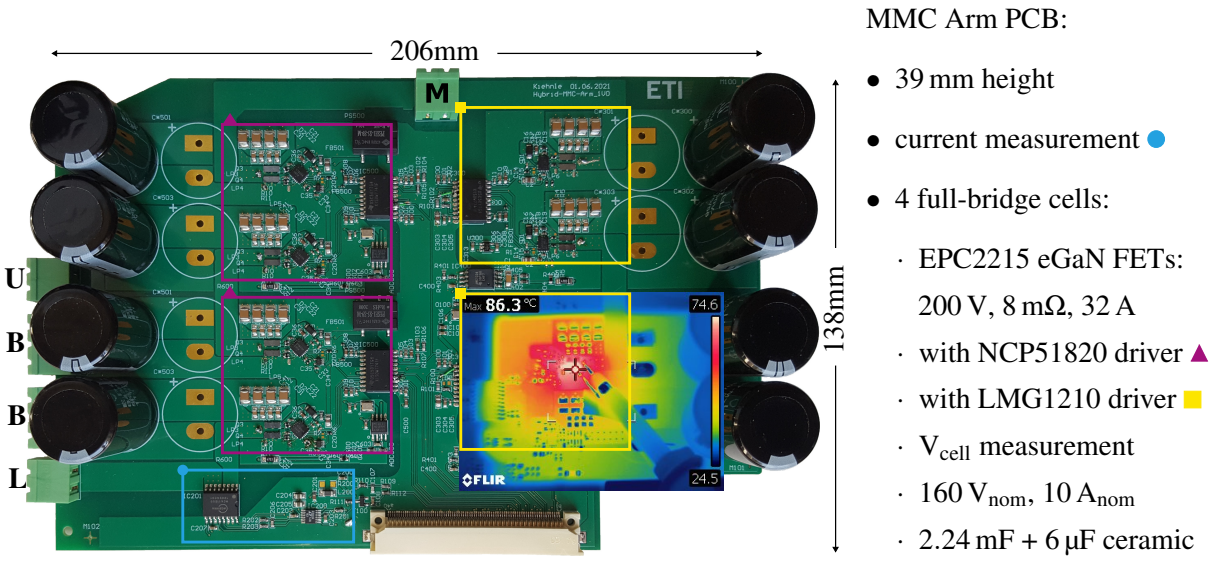


Fig. 2: MMC arm PCB with thermal image at 160 V, 10 A; $C_{\text{cell,installed}} = 1.12\,\text{mF}$

Power Section

Besides the mandatory upper (U) and lower (L) power terminals for an MMC arm, the PCB offers a middle (M) connection, which enables to split the necessary arm inductance into multiple parts. Therefore, the inductors can be smaller and the trace length to the inductors is reduced. This minimizes the polygon areas with switched potential in order to minimize EMI. Additional terminals (B) of the cells on the left in Fig. 2 offer the possibility to connect batteries to half of the cells. Both half-bridges in those cells have their positive terminals separated and the battery terminals therefore have three electrical contacts. This possibility allows the evaluation of circuits, which eliminate AC-phase pulsating battery currents, which would occur with directly connected batteries [5].

All cells use EPC2215 GaN E-HEMTs, but two different gate drivers are used to minimize switching losses on the one hand, while maintaining long ON-state periods on the other hand. Therefore, two cells optimized for minimal switching losses use the LMG1210 half-bridge gate driver, where a very short deadtime between 0.5 ns and 20 ns can be configured. The other two cells with the battery connectors use the NCP51820 half-bridge gate driver, which offers a minimal deadtime of 25 ns. To save power for an extra supply, both use bootstrapping to supply the high side gate, which needs to be charged to 5 V for a low $R_{\text{DS(on)}}$. The NCP51820 driver has an integrated LDO-regulator on the high side. Thus, a higher voltage of 9 V is bootstrapped, which allows the battery backed modules to be turned on for a complete half-wave of the 50 Hz grid. During this period, the voltage of the bootstrap capacitor decreases without affecting the gate voltage. This feature requires an additional DC-DC-converter, which provides isolated 9 V from the 5 V mainboard supply.

Switching Behaviour

In the PCB design, it is mandatory to follow the layout rules for fast switching GaN devices [6]. In order to check the design for an acceptable switching behaviour, measurements were made with the NCP51820 driver using its minimal deadtime of 25 ns. A voltage V_c of 160 V was supplied to one half-bridge (see Fig. 3). V_{DS} of the low side E-HEMT was measured with an RL load first connected to the positive DC terminal (DC+) and second to the negative DC terminal (DC-) in order to reverse the current direction through the low side E-HEMT.

With a duty cycle of 50 % and a load current of 10 A, the switching waveform in Fig. 3 was measured with an 1 GHz Oscilloscope and a 500 MHz probe directly soldered onto the PCB. While the load was connected to the negative DC terminal, the rise time (10% to 90%) was much higher compared to the common double pulse test approach [7], where the inductor is connected to DC+. But even with this fast rise time of 3.47 ns, only minimal voltage overshoot of 5.9 V occurs due to the small commutation loop.

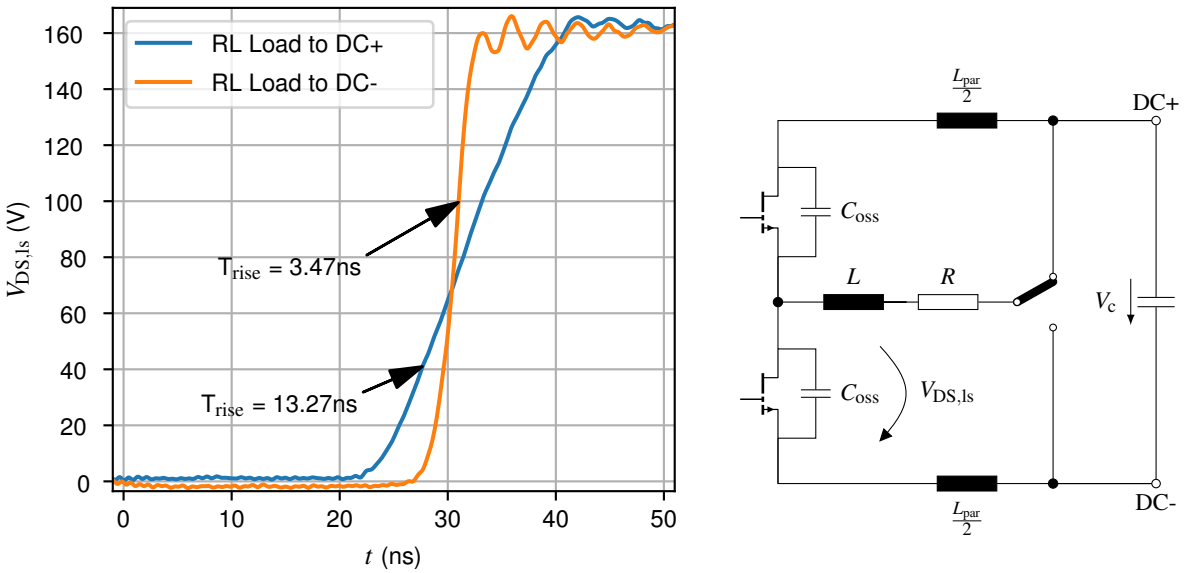


Fig. 3: Turn-off behaviour of low side transistor in GaN half-bridge with $R_{g,on} = 2.7\,\Omega$, $R_{g,off} = 1.0\,\Omega$, $L = 65\,\mu H$, $R = 8\,\Omega$ and $V_c = 160\,V$

In order to measure the parasitic inductance L_{par} of the commutation loop, conventional methods, which require the current through the transistor, cannot be used, as the loop is too small for a current sensor. Therefore the parasitic inductance is estimated by the ringing frequency f_{res} and the equivalent circuit model shown in Fig. 3. In the waveform in Fig. 3, a ringing frequency of 332.7 MHz can be extracted. With a drain-source capacitance C_{oss} of 390 nF according to the data sheet [8], equation (1) can be used to calculate the parasitic inductance of 0.65 nH.

$$L_{par,estim} = \frac{1}{C_{oss}(2\pi f_{res})^2} \tag{1}$$

In order to check these assumptions, an LTspice simulation with the transistor model from EPC was used. The results in Table I show a strong correlation between L_{par} and the estimated inductance. Layout improvements can be easily evaluated with this method.

Table I: Commutation loop parasitic inductance estimation.

	LTspice	LTspice	LTspice	PCB
V_c	100 V	160 V	160 V	160 V
C_{oss}	390 pF	350 pF	350 pF	350 pF
f_{res}	230 MHz	244 MHz	347 MHz	332.7 MHz
L_{par}	1.2 nH	1.2 nH	0.6 nH	unknown
$L_{par,estim}$	1.23 nH	1.22 nH	0.60 nH	0.65 nH

The low inductance of the commutation loop allows the cells to work at even higher DC-link voltages. A cell voltage of $V_c = 180\,V$ was successfully tested, which could be useful in case of grid faults, where the converter has to stay connected to the grid up to voltage levels of $1.25\,V_{nom}$, according to the latest grid codes in Germany [9].

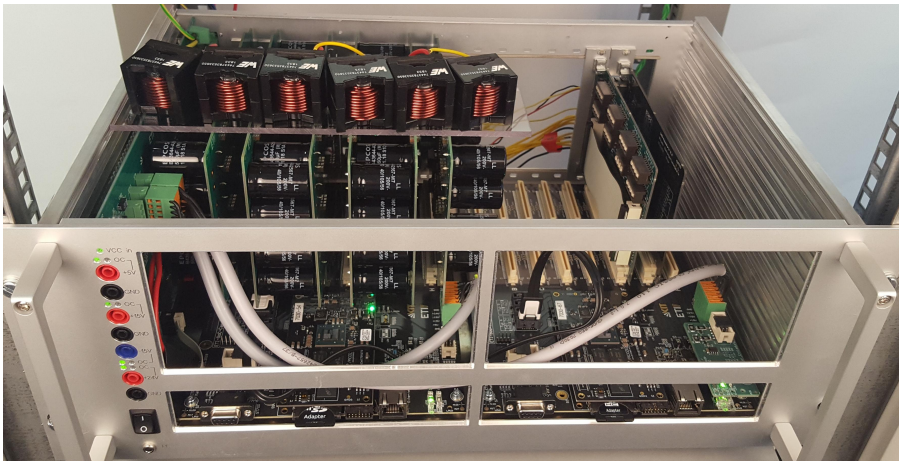
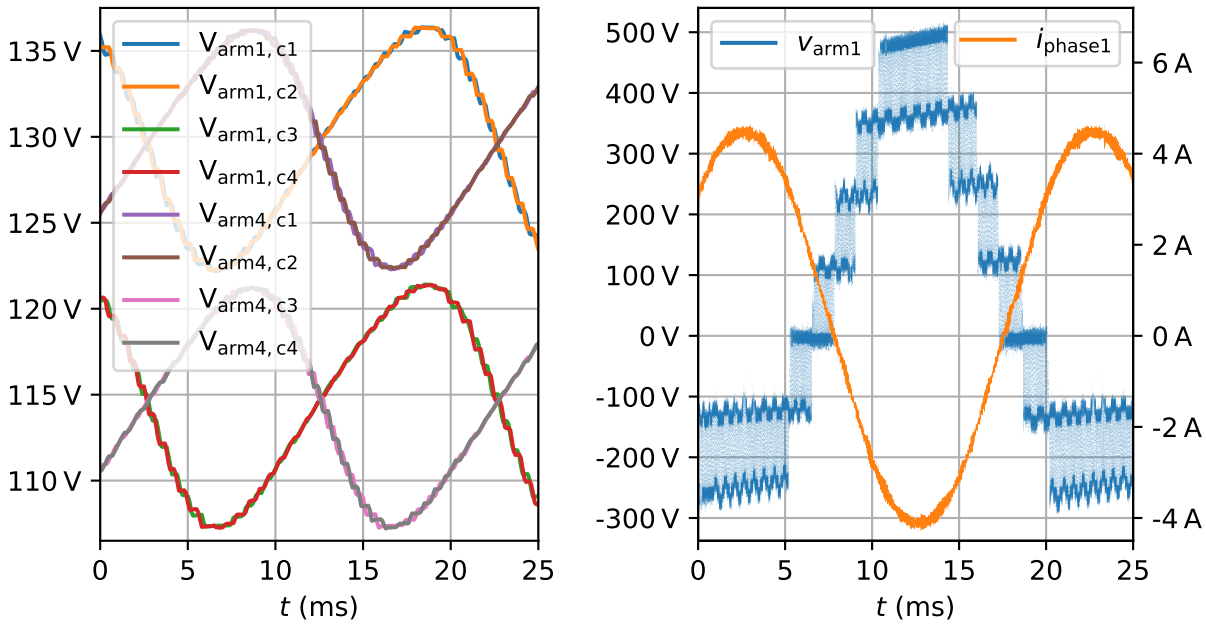


Fig. 4: MMC prototype in a 19-inch rack

MMC Prototype Measurements

In Fig. 4 the assembled MMC is shown. Six Arm PCBs are plugged into the ETI-SoC-Carrier, which is processing all the signals [4]. The arm inductors are visible on top of the PCBs and are connected to the (M) connection point, which was mentioned before. A second ETI-SoC-Carrier board is used for two peripheral cards, which control the AC- and DC-contactors in the system and measure the grid voltage. But those features will be integrated in an enlarged carrier board in the future.

For the integration of batteries into the MMC, it is mandatory to operate the modules at different voltage levels. In the extreme case, which is not recommended for long battery life, the 40-cell, 1.1 kWh battery module operates between 100 V and 168 V.



(a) Different cell voltage levels

(b) Phase current and unfiltered arm voltage

Fig. 5: MMC measurement data of one phase of the prototype

In Fig. 5(a) the cell capacitor voltages of the upper (arm1) and lower (arm4) of the first phase of the MMC are shown. It can be seen that the control implementation allows different cell voltage levels within the cells of one arm. The cells 1 and 2 are operated at a nominal voltage of 130 V, while the future battery backed cells 3 and 4 are set to 115 V. This level can then be matched to the battery voltage

level and the mains frequency related energy ripple of the battery backed cells will mostly disappear. The measurements of Fig. 5(a) were recorded with the TCP/IP interface of the ETI-SoC-System. It is running the MMC energy controller on an ARM processor with an update rate of 10 kHz and allows access to all system variables with the same rate. The current controllers for the internal-, DC-, and grid-currents are implemented in the FPGA of the Zynq SoC, running at a control frequency of 100 kHz.

In Fig. 5(b) the unfiltered output voltage v_{arm1} of the upper MMC arm of phase 1 is shown. It can be seen, that the full-bridge cells allow for positive and negative voltages. In this case an MMC DC voltage of only 200 V was used to drive a resistive load at an RMS voltage level of 400 V and an output power of 2 kW. Those measurement were recorded with an external oscilloscope.

MMC Efficiency

In the upcoming renewable energy based grid, efficient power converters and battery storages are mandatory. The PCB design has been trimmed to an efficient operation. But the arm modules with a total power consumption of 6 W are only one part of an efficient converter. Therefore the signal processing system itself has been taken into account with another 5 W. But the main loss is still caused by the switching and conduction losses of the semiconductors. Those losses have been calculated with the official LTspice model of the EPC2215 GaN transistor at a cell voltage of 160 V.

The temperature dependent increase in $R_{\text{DS(on)}}$ has been taken into account and the temperature was calculated based on thermal measurements (see Fig. 2). The currents have been calculated with a simple MMC model and the formula for the arm current is shown in equation (2).

$$I_{\text{arm,rms}} = \frac{I_{\text{dc}}}{3} + \frac{I_{\text{ac,rms}}}{2} = \frac{P_{\text{in}}}{V_{\text{dc}} \cdot 3} + \frac{I_{\text{ac,rms}}}{2} \tag{2}$$

A MMC DC-bus voltage V_{dc} of 460 V and an effective switching frequency of 200 kHz per arm, which equals to 25 kHz per half-bridge, has been used for the calculation. The arm inductor of Fig. 1 was modelled with a resistance of 13 mΩ. The losses in capacitors and PCB traces have been neglected for now.

In Fig. 6 the converter DC to AC efficiency at different input power levels is shown. Especially at lower power levels, it can be seen that the power consumption P_{control}, which includes the gate signal generation, measurements and the processing system has a major impact on the total efficiency of the converter, as they make up for one third of the total losses. For an MMC in the low power range, this factor would get worse if optical isolation or even dedicated cell microcontrollers would have been used.

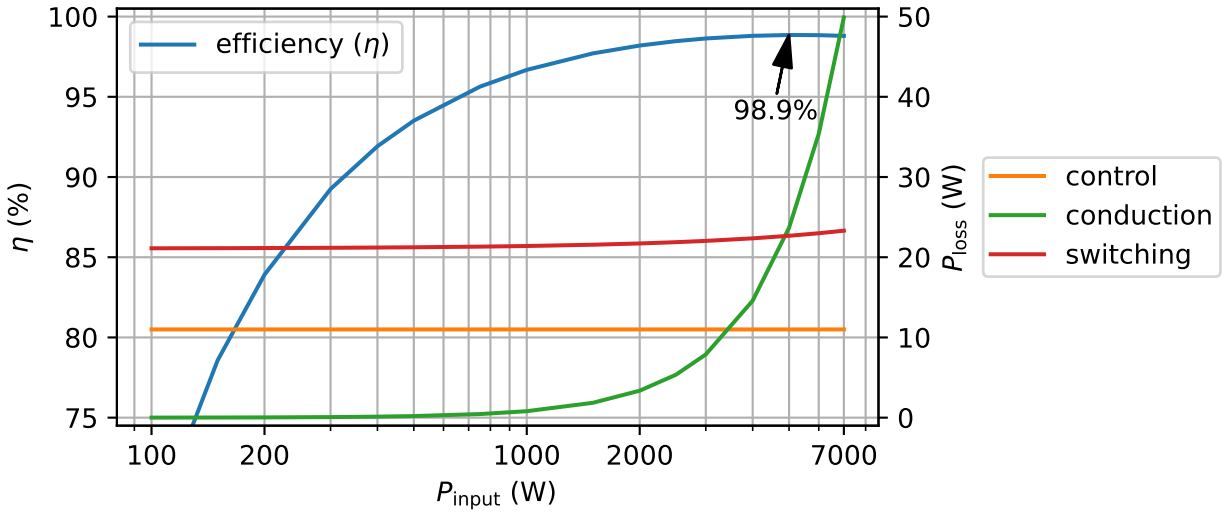


Fig. 6: MMC efficiency and power losses

Conclusion

A GaN-based arm PCB was presented, which enables an MMC with up to 98.9 % theoretical efficiency, although the complex control system for MMCs is taken into account. The switching behaviour of an half-bridge was measured and the parasitic inductance of the commutation loop was calculated to verify a good layout. Further, the assembled MMC prototype with first measurements has been shown. The MMC control implementation supports different cell voltage levels, which allows to connect batteries to half of the full-bridge cells. Finally, the total loss distribution of the MMC was estimated to show the impact of the low internal power consumption of the presented GaN-based arm PCB.

Outlook

There is still room for optimizations, e.g. some of the cells can be configured as half-bridge cells because no negative DC-bus voltage will be necessary for most applications. Thereby the switching and conduction losses can be reduced further. In future research, half of the cells will be connected to batteries.

Practical efficiency will be measured in future work, when methods to minimize cell voltages by capacitor voltage ripple shaping [10] and advanced circulating current controllers, which allow for decrease in capacitor losses [11] have been implemented.

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