Hardware Prototype for the Quasi-Two-Level Operation of a Three-Phase Flying Capacitor Converter for Medium Voltage Applications

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***Abstract*—Today's standard medium voltage converters are operated with low switching frequencies and contain bulky passive components. One concept to change this is the Quasi-Two-Level operation of a multilevel converter with SiC semiconductors. A three-phase hardware setup for a Quasi-Two-Level Flying Capacitor Converter with control and measurement results in a test setup are presented.**

***Index Terms*—medium voltage, multilevel converter, SiC-MOSFET**

I. Introduction

Most of today's medium voltage converters are either based on the Modular Multilevel Converter (MMC) technology or on 3/5-Level approaches which are operated at low switching frequencies and contain bulky line filters. Both concepts still lead to relatively high costs due to extensive use of materials in passive components, which is a major reason for the slow spread of medium voltage power converters in grid applications. One promising concept is the Quasi-Two-Level operation (Q2O) of multilevel converters with fast switching semiconductors. The Flying Capacitor Converter (FC) with Q2O is considered as a possible realization of such a medium voltage converter in this paper. This concept was presented in [1] and [2]. The approach of Quasi-Two-Level operation of an MMC is presented in [3] and [4]. But for the same number of output voltage levels, significantly more semiconductors are needed by an MMC than by an FC. With both multilevel converters, the required passive components can be reduced with the Q2O. The medium voltage applications in focus are in the voltage classes up to $5\,\mathrm{kV}$. The main focus is on grid applications, but machine applications such as in traction drives are also possible.

II. Fundamentals of Flying Capacitor Converter

The concept of the Flying Capacitor Converter (FC) was first introduced in [5]. The multilevel voltage is generated by switching capacitors into the active current path. An n-level FC ($n \in \mathbb{N}$) is made of $2{\cdot}(n{-}1)$ power semiconductor switches and $(n-2)$ capacitors in addition to the DC link capacitor. An exemplary 5-level FC converter is shown in fig. 1. Each commutation cell of the FC consists of one high side and one low side semiconductor together with the corresponding capacitor. To avoid a short circuit between the capacitors of two adjacent cells, only one transistor of each cell may be conductive at each time.

Each capacitor C_i has a different nominal voltage $V_{\mathrm{c,nom},i}$.

$$V_{\mathrm{c,nom},i} = V_{\mathrm{dc}} \cdot \frac{n-1-i}{n-1} \quad i \in [1...(n-2)] \tag{1}$$

To simplify the construction, the converter is built using modular components, i.e. Power Electronic Building Blocks (PEBBs). Since the commutation cell is the repeating circuit element, the PEBB consists of one commutation cell, as can be seen in fig. 1. An n-level converter requires $(n{-}1)$ PEBBs. The mean voltage for the semiconductors in a PEBB can be calculated with eq. (2).

$$V_{\mathrm{PEBB,nom}} = \frac{V_{\mathrm{dc}}}{n-1} \quad n \in \mathbb{N} \tag{2}$$

During operation, the applied voltage across the semiconductors always deviates from the mean voltage, because the capacitor voltages are free-floating and are not clamped by external voltages sources. Hence, the voltage across the capacitors varies if the capacitor is switched into the output current path. This is the case for all multilevel output voltage levels except $+\frac{V_{\mathrm{dc}}}{2}$ and $-\frac{V_{\mathrm{dc}}}{2}$. It is necessary to balance the capacitor voltages to keep their deviation within acceptable limits.

Depending on the operation mode, there are different ways of achieving this: Conventional multilevel operation with Alternative Phase Opposition Disposition (APOD) modulation or Phase Disposition (PD) works by exchanging carrier signals symmetrically for the corresponding semiconductor.

For Quasi-Two-Level operation (Q2O) various types of balancing algorithms exist. These algorithms were presented in [1], [2] and [6]. A comparison and explanation of the

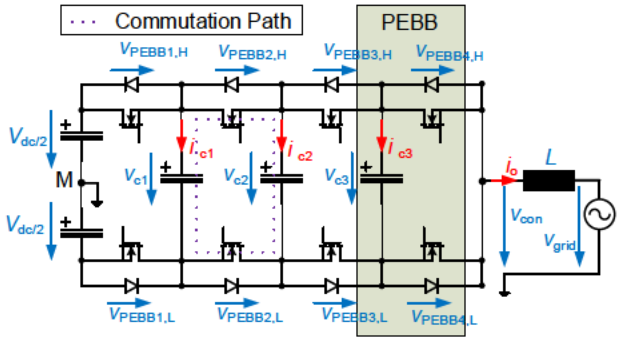

Fig. 1. 5-level flying capacitor converter, single phase design

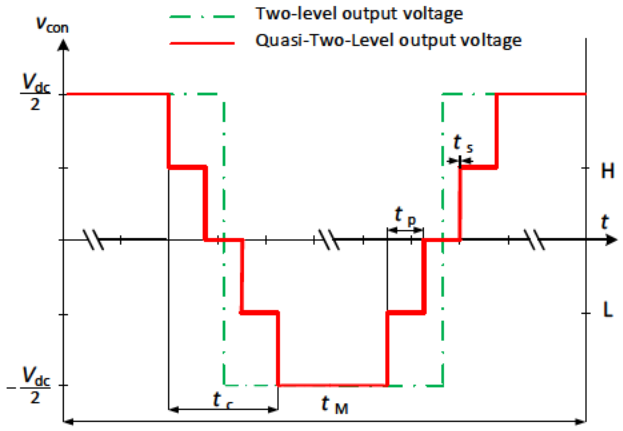

Fig. 2. Quasi-Two-Level output voltage principle

algorithms can be found in [7]. Another analysis of Q2O of the FC for medium-voltage applications was presented in [8].

A very similar topology to the FC is the Packed U-Cell (PUC) Converter. In [9], a review of the topology and control is presented. The main difference between these converters is that the FC has a central DC link and the PUC does not. In the PUC, instead of the DC link, there is an electrical connection, which is the reference potential or the second connection point of the converter output voltage v_{con}. The capacitor with the highest voltage level is used as DC source with the reference potential. In the FC, the DC link is connected to ground at one point, which then represents the reference potential or the second connection point of the converter output voltage v_{con}. In three-phase operation, the difference is more obvious. The three single-phase PUCs become a three-phase converter in star connection. In the FC, all three phases are connected to the same DC link and this DC link requires a smaller capacity than the three single-phase DC links. The modulation and balancing algorithms differ due to these topological differences, but both use the very similar principles for modulation and balancing of the capacitor voltage.

III. Quasi-Two-Level Operation

The fundamental idea of the Quasi-Two-Level Operation is to use the multilevel topology in combination with a two-level modulation scheme. Hence, the applied control and modulation strategies are very similar to the well-established ones used for two-level converters. Additionally, the beneficial switching characteristic of multilevel converters in terms of reduced $\mathrm{d}v/\mathrm{d}t$ and small overvoltage stress at high output voltage levels can be realized. The advantages of the lower $\mathrm{d}v/\mathrm{d}t$ at the Quasi-Two-Level Operation was shown in [10]. In applications with long cables, minimizing the overvoltage stress is a significant factor in increasing the lifetime of the cables.

The voltage-trajectory across the output filter is the same compared to the two-level modulation. In fig. 2 as simplified output voltage (red line) of the Quasi-Two-Level modulation and for comparison the output voltage of a two-level converter (dashed-dotted green line) are shown.

The transient output voltage level time t_p must be longer than the switching time of the semiconductors $t_s < t_p$. The time t_C is in the range of usual locking times with less than 5% of the modulation time t_m. In the graphic, the time axis is not shown to scale so that the multilevel voltages are visible.

IV. Problem with Idle Mode

A multilevel converter requires a current flow through the capacitors in order to keep the capacitor voltages at their nominal values. For the FC, the current flow through the capacitors equals the output current i_o. In many applications the RMS value of the output current should be zero, i.e. during idle mode. In Quasi-Two-Level operation, the output current flows through the capacitors only during the transient switching events. Converter with a stepped and clocked output voltage always generate a current ripple in the output current. The peaks of the output current with a current ripple always differ from the RMS value within a modulation period. The peaks are not zero even with an RMS output current of zero. Thus the problem with missing output current does not exist, because the switching events always occur at the peaks of the output current.

For the capacitor voltage balancing, the sign and approximate value of the output current must be predicted, because these critically influence the selection of the switching states selected by the balancing algorithms. In most applications, the average values of the modulation periods are measured and controlled. In fig. 3 it is shown why this approach is not enough for balancing in idle operation - i.e. very small output currents. The average value of a modulation period is positive and the current peaks in period k are also positive and in period $k+1$ the peaks are positive and negative . Therefore, for Quasi-Two-Level operation, the following approximation is chosen based on a purely inductive output filter. For other output filters or applications, this must be adjusted for the idle mode.

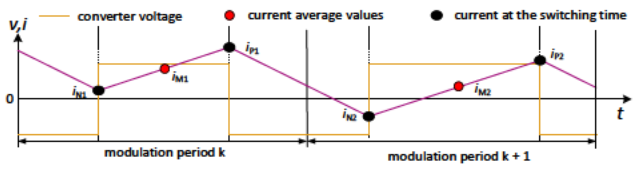

Fig. 3. Precalculation of the current curve

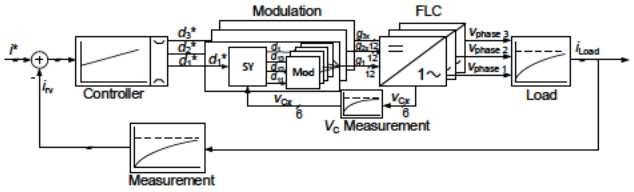

Fig. 4. Signal structure of the control

$$v_{\mathrm{L}} = L \cdot \frac{di}{dt} \rightarrow \Delta i = \frac{v_{\mathrm{L}} \cdot \Delta t}{L} \tag{3}$$

In modulation period k with the actual duty cycle d_1 and the new duty cycle d_2 of period $k+1$, i_{N2} and i_{P2} can be predicted. Before that i_{P1} should be calculated (see fig. 3).

$$i_{\mathrm{P1}} = i_{\mathrm{M1}} + \frac{v_{\mathrm{con}} - v_{\mathrm{grid}}}{L} \cdot \frac{d_1}{2} \cdot t_{\mathrm{M}} \tag{4}$$

Based on the result from eq. (4) i_{N2} and i_{P2} can be calculated.

$$i_{\mathrm{N2}} = i_{\mathrm{P1}} + \frac{v_{\mathrm{con}} - v_{\mathrm{grid}}}{L} \left(\frac{1-d_1}{2} \cdot t_{\mathrm{M}} + \frac{1-d_2}{2} \cdot t_{\mathrm{M}} \right) \tag{5}$$

$$i_{\mathrm{P2}} = i_{\mathrm{N2}} + \frac{v_{\mathrm{con}} - v_{\mathrm{grid}}}{L} \left(d_2 \cdot t_{\mathrm{M}} \right) \tag{6}$$

With the precalculated values of i_{P2} and i_{N2}, the idle mode does not need to be handled differently from any other operating point.

V. Control Structures

The current control structure of the FC in Quasi-Two-Level operation does slightly differ from that of a three-phase bridge. The structure is shown in fig. 4. It consists of the current controller itself, the modulation with gate signal generation, the power stage, the load and the measuring element.

The only difference is the modulation for the Quasi-Two-Level operation of the FC. The modulation consists of two parts per phase, the balancing algorithm (marked "SY") and the actual gate signal generation ("Mod"). The balancing algorithm calculates the duty cycles d_{xy} for the respective PEBB from the duty cycle d_x. As It depends on the actual capacitor voltages, this measurement forms an additional loop within the control structure. Then, with the individual duty cycles d_{xy}, the gate signals g_{xy} are generated by a sine-triangle comparison ("Mod"). The index x represents the phase and the index y represents the PEBB.

In contrast to the three-phase bridge where only one sine-triangle comparison for each half-bridge is needed, the FC with Quasi-Two-Level modulation requires one sine-triangle comparison for each PEBB. Although the controller is drawn in the structure as a PI controller any kind of other controller type is possible. The power stage here is the three-phase FC consisting of three single-phase FCs which share the DC link. In this case the load is represented by the output filter of the converter. However, in the actual application it could be substituted as the grid or an electrical machine. In fig. 4 the load is represented as a low-pass element, but depending on the application the characteristic of the load might differ.

A. Implementation

The described control structure was realized in the hardware prototype with an in-house developed signal processing system [11], utilizes a system on chip (SoC). Here, the components of control structure split among the ARM core and FPGA. To provide enough IO ports for three-phase operation, two SoC-systems linked with an GTX connection were used. GTX is a High Speed Serial communication with a transfer rate of up to $6.6\,\mathrm{Gbit/s}$ designed by the manufacturer of the SoC. The functions requiring a high time resolution like the interpretation of the measurements (ADCs) and the gate signal generation are realized in the FPGA. The closed-loop control and the balancing algorithms are implemented in the ARM core, because it is simpler to implement with C code and floating-point values. The implemented structure is shown in fig. 5. The FPGA is operated with $f_{\mathrm{FPGA}} = 250\,\mathrm{MHz}$ for the generation of the gate signals. Thereby, the necessary resolution of the switching times needed for the short t_{p} can be realized. The interrupt frequency of the ARM core is $f_{\mathrm{arm}} = 20\,\mathrm{kHz}$, because the demonstrator is working with a switching frequency of $f_{\mathrm{S}} = 10\,\mathrm{kHz}$. The balancing algorithm is executed twice per modulation period $t_{\mathrm{M}} = \frac{1}{f_{\mathrm{S}}}$.

Functions necessary for operation, such as a state machine and error handling, are also implemented in the ARM cores, but not included in the diagram for the sake of comprehensibility. The control of the fans and the temperature monitoring of the PEBB are implemented in the FPGA, but again not depicted.

The signal processing introduces dead times into the structure of the control. These dead times can be easily taken into account in the control of the output current, but this is not directly possible with the balancing of the capacitor voltages. For this purpose, an extra method is implemented for compensation and is described in the following section.

B. Dead Time Compensation by Voltage Measurements

The balancing algorithms are always executed twice per modulation period t_{M}. However, the duty cycle d_{xy} for generating the gate signals can only be changed at specific time slots so to not distort the voltage-time-integral at the output. In fig. 6 the time sequence is shown. The effect of dead time of the balancing $\frac{t_{\mathrm{M}}}{2}$ must be compensated to minimize the voltage deviations of the capacitor voltages.

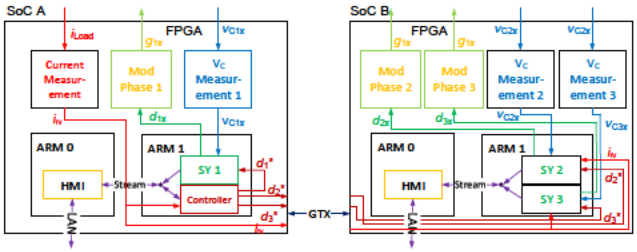

Fig. 5. Implemented control signal structure

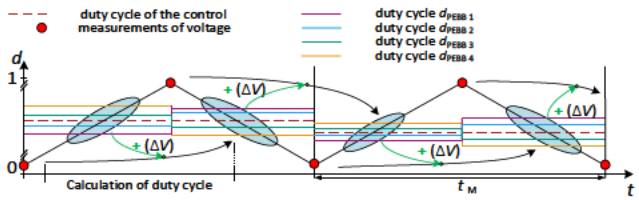

Fig. 6. Time diagram of the prediction of the capacitor voltages

In general, the voltage of a capacitor can be described according to eq. (7).

$$V_{\mathrm{C}} = \frac{1}{C} \int i_{\mathrm{C}}\, dt + V_{\mathrm{C0}} \tag{7}$$

With stationary values eq. (8) is obtained.

$$\Delta V_{\mathrm{C}} = \frac{1}{C} \cdot I_{\mathrm{O}} \cdot t_{\mathrm{c}} \tag{8}$$

For each of the capacitors used, the capacitor voltage change ΔV_{C} must be calculated individually in each phase.

$$\begin{pmatrix} \Delta V_{\mathrm{C1}} \\ \Delta V_{\mathrm{C2}} \\ \Delta V_{\mathrm{C3}} \end{pmatrix} = \begin{pmatrix} \frac{1}{C_1} \\ \frac{1}{C_2} \\ \frac{1}{C_3} \end{pmatrix} \cdot I_{\mathrm{O}} \cdot \begin{pmatrix} t_{\mathrm{c1}} \\ t_{\mathrm{c2}} \\ t_{\mathrm{c3}} \end{pmatrix}^{\mathsf{T}} \cdot \Big[K\Big] \tag{9}$$

The time t_{cn} is the sum of the $t_{\mathrm{p},nz}$ of the corresponding capacitor. Respectively, the time t_{cz} is the time how long the output current flows through the corresponding capacitor in the switching sequence just executed. The index n is the index for the capacitors in the 5-level FC. The index z is the index for the three multilevel voltage levels in the switching sequence of the 5-level FC.

$$\big[K\big] = \begin{bmatrix} k(C_1, t_{\mathrm{p11}}) & k(C_2, t_{\mathrm{p12}}) & k(C_3, t_{\mathrm{p13}}) \\ k(C_1, t_{\mathrm{p21}}) & k(C_2, t_{\mathrm{p22}}) & k(C_3, t_{\mathrm{p23}}) \\ k(C_1, t_{\mathrm{p31}}) & k(C_2, t_{\mathrm{p32}}) & k(C_3, t_{\mathrm{p33}}) \end{bmatrix} \tag{10}$$

Equation (11) gives the assignment of the states of each step. The assignment varies depending on the switching sequence.

$$k(C_n, t_{\mathrm{p},nz}) := \begin{cases} 1 \cdot \frac{t_{\mathrm{p},nz}}{t_{\mathrm{cn}}}, & \text{C is charged} \\ 0, & \text{no change} \\ -1 \cdot \frac{t_{\mathrm{p},nz}}{t_{\mathrm{cn}}}, & \text{C is discharged} \end{cases} \tag{11}$$

Finally, the corrected voltage $V_{\mathrm{C,corr}}$ results from the sum of the measured capacitor voltage V_{C} and the additionally calculated voltage offset ΔV_{C}.

$$\big(V_{\mathrm{C,corr}}\big) = \big(V_{\mathrm{C}}\big) + \big(\Delta V_{\mathrm{C}}\big) \tag{12}$$

VI. Hardware Set-Up

To validate simulative observations, a full-scale prototype was built. A three-phase FC with up to 7 levels per phase is implemented. The phases are realized with the PEBBs presented in [12].

A. Power Electronic Building Block

A PEBB consists of the power semiconductors, the capacitors and the necessary peripherals. These are the gate units, the measurement circuitry of the capacitor voltage and the heat sink temperature as well as the fan control. A picture of the PEBB is shown in fig. 7. With the modular design, the presented approach is to build a complete inverter by simply connecting interchangeable units. This means that the insulation of the PEBB must be designed for the highest possible voltage, i.e. DC-Link voltage. This is one of the reasons why this topology is not used for high voltage applications. The PEBB internally isolates the medium voltage from its power supply and higher-level control. The isolation voltage of the PEBB exceeds the allowed DC link voltage (4 kV) as a continuous load.

For the Quasi-Two-Level operation mode it is essential that a power semiconductor is turned on and off as fast as possible. Therefore, SiC-MOSFETs as fast switching semiconductors are selected. Most commercially available packages feature half bridges or three-phase bridges configurations, single semiconductors are very rare. Therefore, a half bridge module is selected. This is also the reason why the design as shown in fig. 7 consists of two PEBBs. The prototype is built with CAS300M12BM2 - 1200 V, 300 A SiC-Semiconductor modules. The output current is tested up to $I_{\mathrm{O}} = 150$ A.

The capacitance is implemented with two different types of capacitors connected in parallel. One part are ceramic capacitors connected to the modules with a minimized stray inductance to minimize overvoltage at the semiconductors. The larger part consists of film capacitors which are adapted to the voltage of the corresponding flying capacitor. Although the capacitors of different PEBBs differ in voltage rating they always provide the same total capacitance of 1 µF. The different capacitors also differ in their physical size.

B. Prototype Converter

The converter is implemented in a cabinet with 4 floors. In fig. 8 the converter output side is shown. On the lowest floor

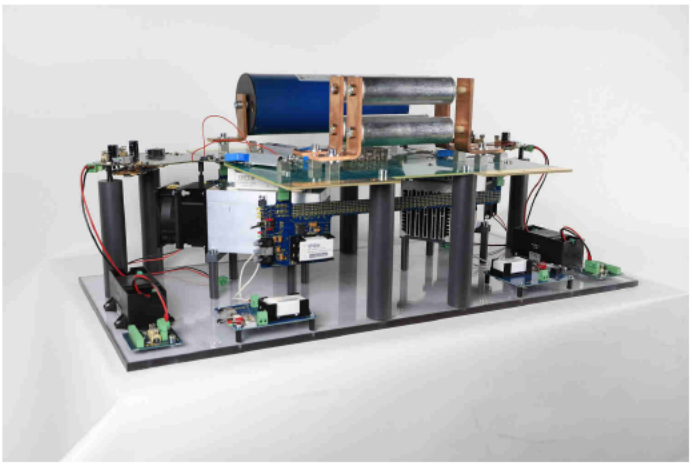

Fig. 7. Picture of a double Power Electronic Building Block for the flying capacitor converter

there are the control unit containing the signal processing unit and the auxiliary power supplies for other peripherals. Above each floor contains one phase of the converter. At the end of each corresponding phase, the output current measurement is realized with a current sensor. At the other end, the central DC link is implemented, which vertical interconnects the three phases. The structure is realized with six PEBBs, i.e. three double PEBBs per phase. This results in a 7-level FC. This setup can also be operated with only the two front double PEBBs, resulting in a 5-level FC. The converter is designed for $V_{\mathrm{PEBB,nom}} = 800\,\mathrm{V}$. $V_{\mathrm{PEBB,nom}} = 650\,\mathrm{V}$ will be the maximum in operation. Thus, the maximum DC link voltage is up to $4\,\mathrm{kV}$ as a 7-Level FC or $2.6\,\mathrm{kV}$ as a 5-Level FC. The theoretical output power of the inverter is about $350\,\mathrm{kW}$ with an AC output voltage up to $2.4\,\mathrm{kV}$.

C. Test-setup

The converter is used in a test setting that has as little influence as possible on the operation of the converter. A direct connection to the medium voltage grid would be too dangerous for operation at the lab. The studies are executed in a laboratory area specifically set up for the medium voltage. Therefore, the converter is supplied by a DC source, which generates a galvanically isolated medium voltage from low voltage. A three-phase choke is used as the load with $5\,\mathrm{mH}$. The structure is shown in fig. 9. In order to operate the converter, the capacitors must be precharged so that the distribution of the DC link voltage results in the semiconductors according to eq. (2). The precharging algorithm presented in [7] is used for all three phases simultaneously. The precharging of the flying capacitors is done together with the DC link capacitor. The voltage of the DC source is ramped up and it charges the capacitors with a constant current. After the capacitors are charged, the control structure from fig. 4 starts immediately.

VII. Measurements

Measurements were made at two different DC link voltages. First at a low DC link voltage during start-up and then at a DC

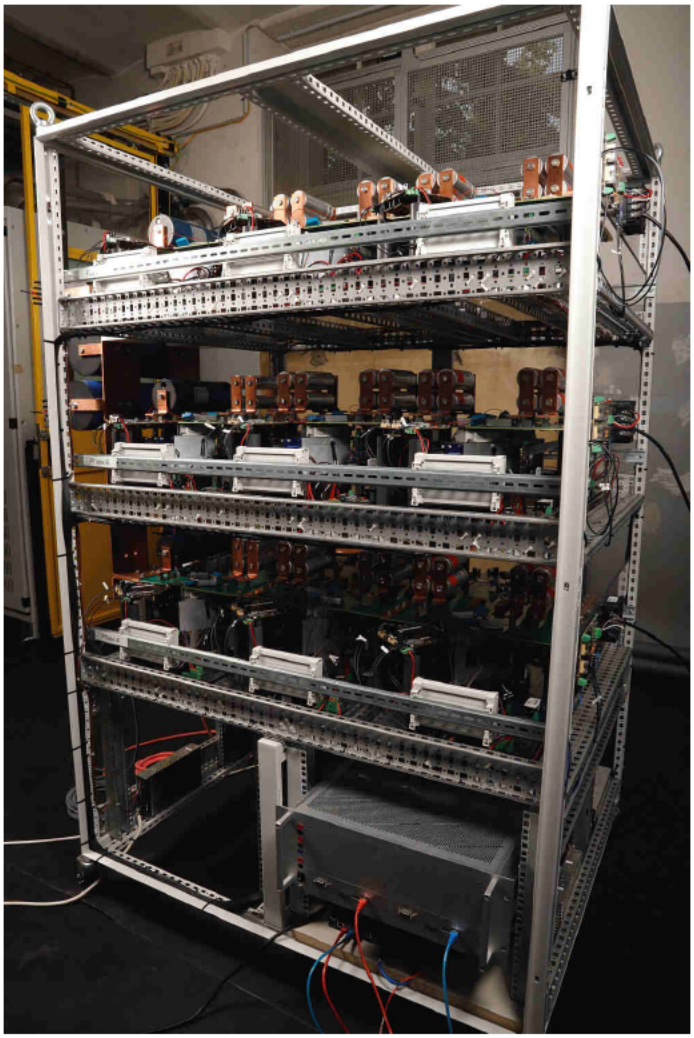

Fig. 8. Picture of the tree phase five/seven-level Flying Capacitor Converter

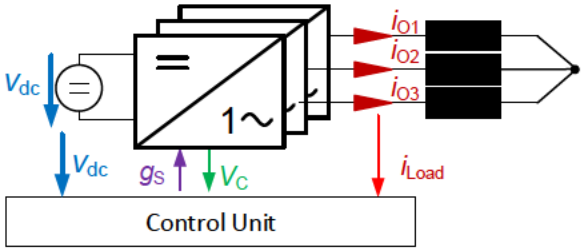

Fig. 9. tree phase Test-setup

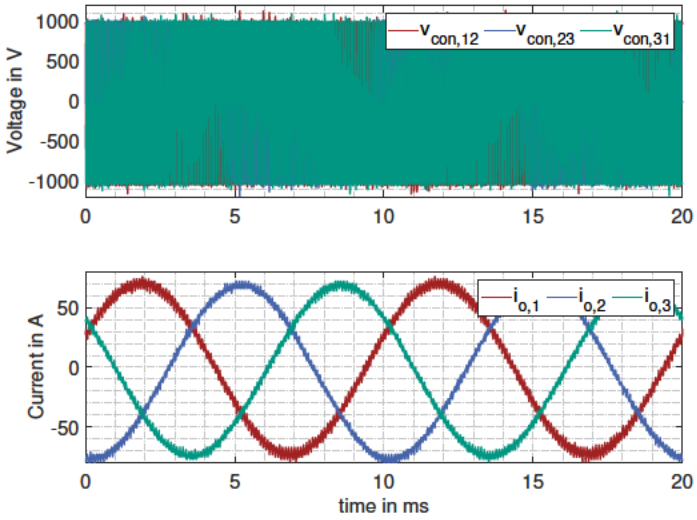

Fig. 10. Three-phase output voltage and output current with two AC-periods

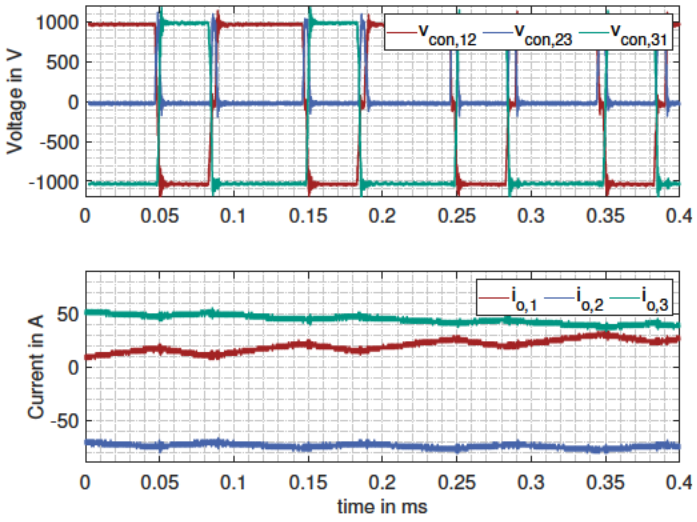

Fig. 11. Three-phase output voltage and output current with four modulation periods t_{M}

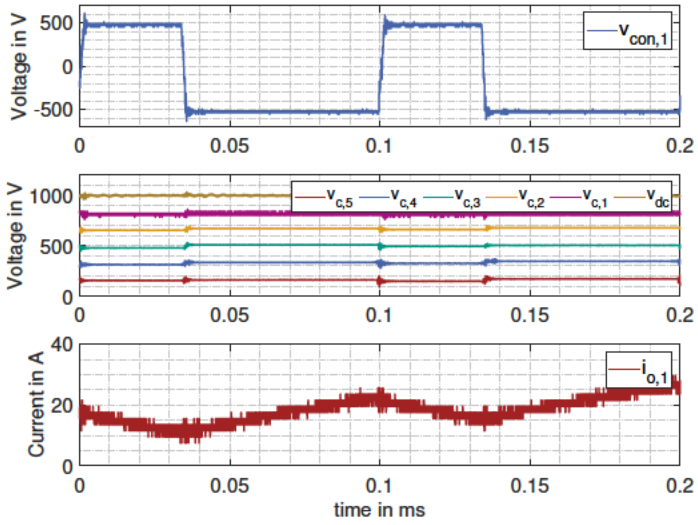

Fig. 12. Single phase output voltage, capacitor voltage and output current with two modulation periods t_{M}

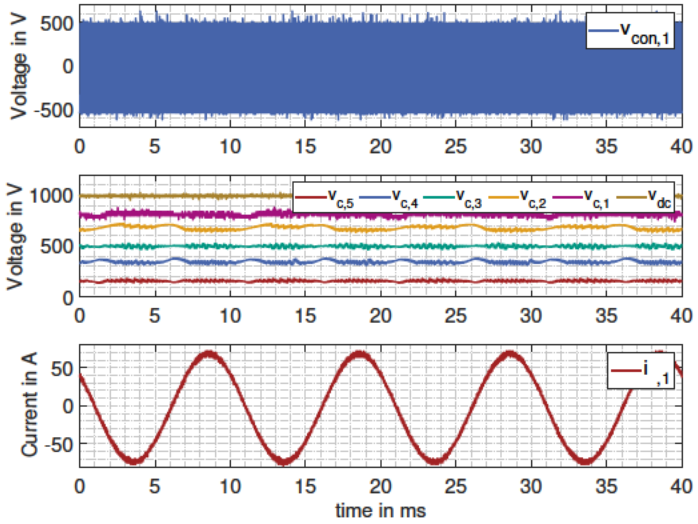

Fig. 13. Single phase output voltage, capacitor voltage and output current with two AC-periods

link voltage in the medium voltage range in the corresponding test location. In each case, the test setup was based on fig. 9. A simple output current control for a three-phase system with PI controllers was used. This is implemented in the controller block in fig. 4.

During the first measurement, several operating points of the three-phase output current were measured. The graphs figs. 10 to 13 shows measurement at 70A output current, with the active current and reactive current portions being equal. The DC link voltage at measurement was 1000 V. The nominal voltage of one PEBB is $V_{\mathrm{PEBB,nom}} = 167\,\mathrm{V}$.

In fig. 10, the three-phase output voltage and output current waveforms with two AC-periods is shown. The three-phase output voltage was measured line to line, hence $v_{\mathrm{con},12}$ which means between phase one and two. To archive a larger voltage drop across the choke, an output current frequency of 100 Hz was controlled. The current waveform is three-phase sinusoidal with a small current ripple due to the load's large inductance at the output.

In fig. 11, the voltage curve of four modulation periods t_{M} of the three-phase output voltage and output current is shown. The moment of this measurement fig. 10 is at about $t = 9.5\,\mathrm{ms}$. The five short intermediate stages of the Quasi-Two-Level Operation are not discernible in the voltage changes. The overvoltage is smaller than 100 V because the smaller voltage steps reduce it significantly. This is a target of Quasi-Two-Level operation and is thus achieved.

In fig. 12 the single phase output voltage, capacitor voltages of phase one and the output current for two modulation periods are shown. The voltage $v_{\mathrm{con},1}$ was measured against $-\frac{V_{\mathrm{dc}}}{2}$. However, the DC link voltage was also measured and half of it was subtracted directly from the output voltage. This formed the virtual potential point M, which is drawn in fig. 1.

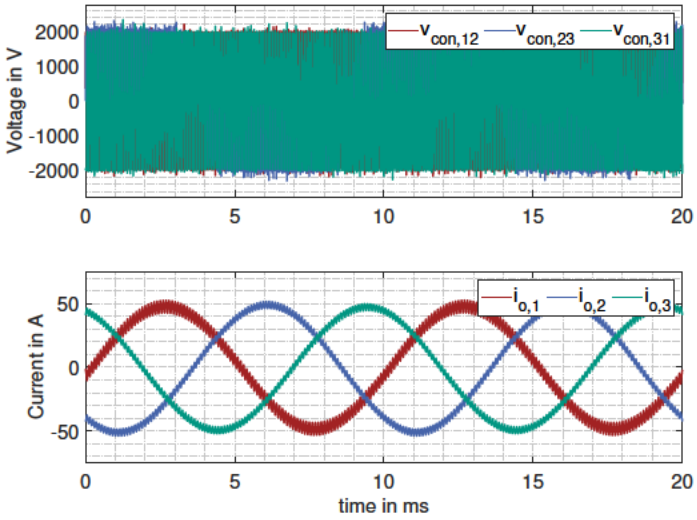

Fig. 14. Three-phase output voltage and output current with two AC-periods by medium voltage operation

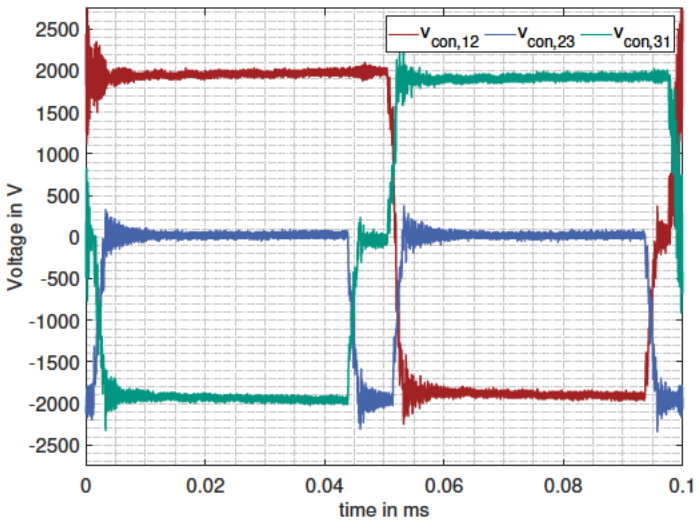

Fig. 15. Three-phase output voltage with one modulation periods t_{M} by medium voltage operation

The five short intermediate stages are visible in the output voltage $v_{\mathrm{con},1}$ during the transients between positive and negative voltage. The ratio of the switching time t_{C} to the pulse width $d \cdot t_{\mathrm{M}}$ is well visible.

In this measurement, $t_{\mathrm{C}} = 5 \cdot 400\,\mathrm{ns}$ compared to the modulation period of $t_{\mathrm{M}} = 100\,\mu\mathrm{s}$. It shows that t_{C} is only a few percent of the modulation period t_{M}.

It can be seen from the capacitor voltage waveforms that the capacitors only change their voltages during the switching operations of the MOSFET. During the two modulation periods this happens four times. These short conduction durations of the capacitor for the output current is the reason that a small capacitance value can be chosen. Another goal of Quasi-Two-Level operation is to minimize the capacitance required in a multilevel converter. The shorter t_{p} could be, the capacity can be designed smaller.

In fig. 13 the single phase output voltage, capacitor voltage of phase one and the output current for two AC-periods are shown. The voltage $v_{\mathrm{con},1}$ was measured with the same principle as in fig. 12. This measurement illustrates the stable operation of the capacitor voltage balancing. The voltage deviations of the capacitor voltages remain within the acceptable range.

In this measurements a balancing algorithm with fixed switching sequence and variable times of the multilevel voltage steps was used. This balancing algorithm was first presented in [6] and a comparison with other balancing algorithms was presented in [7]. During startup, this algorithm [6] was implemented first, since it is easier to implement. This algorithm [6] was chosen here for the demonstration of the function of the full converter system, because the other algorithms were not yet fully implemented with the 7-level hardware.

The DC link voltage for medium voltage test was selected to 2000 V by 7-Level operation, which is not the maximum possible. The testing is done step by step with increasing

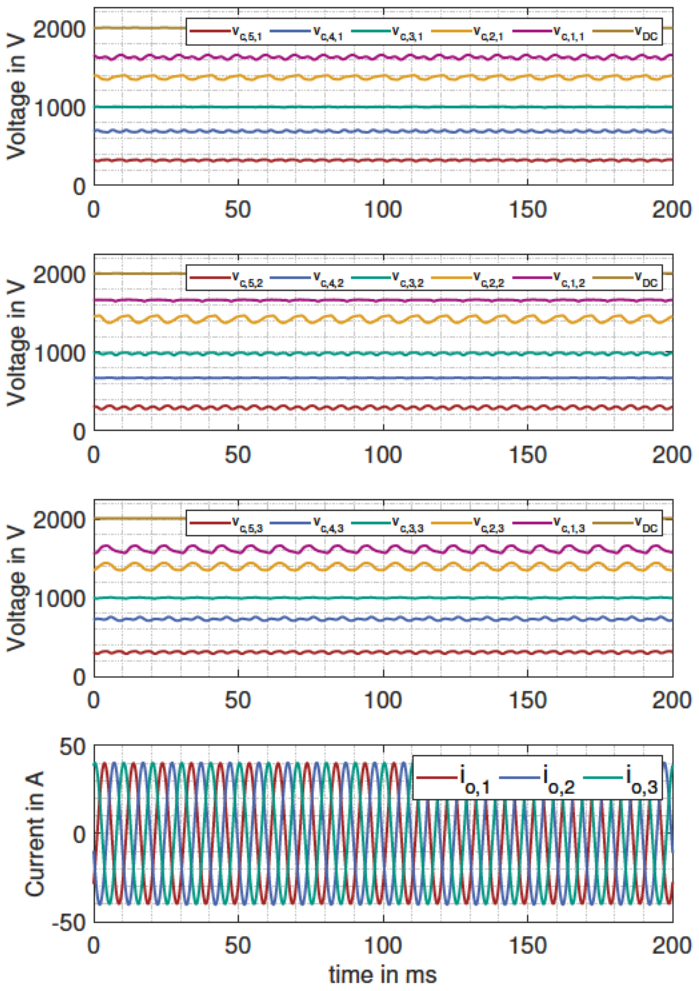

Fig. 16. Three-phase output current and the fifteen capacitor voltages and DC link voltage for twenty AC-periods by medium voltage operation

DC link voltage as the limits of the system have not been tested yet. In fig. 14 the three-phase output voltage and three-phase output current at the higher DC link voltage for two AC-periods is shown. The nominal voltage of one PEBB was $V_{\mathrm{PEBB,nom}} = 334\,\mathrm{V}$ during these measurement. For the output voltage, it can be seen that the overvoltages are small compared to the high DC link voltage. In the output currents, it can be seen that the current ripple is larger due to the larger phase voltage. The current ripple for phase 1 is larger because this phase is wrapped around the middle leg of the three-phase choke. For this winding, the inductance is slightly smaller than for the other two windings because the magnetic resistance is lower.

In fig. 15 the three-phase output voltage for one modulation period t_{M} is shown. Due to the high temporal resolution, the transient voltage levels are recognizable and the three voltage levels of the phase-to-phase voltage can be identified.

In fig. 16 all capacitor voltages of the three phases of the FC and the corresponding phase currents are plotted. The measurement equipment installed in the converter system was used for this. The bandwidth of capacitor voltage measurements is $1\,\mathrm{MHz}$ and for current measurements it is $100\,\mathrm{kHz}$. The bandwidth and accuracy is lower than the equipment used for the other measurements. For balancing, the capacitor voltage is measured only twice per modulation period t_{M}, which is why the capacitor voltage curves are smooth.

However, it could be shown here that the FC in three-phase operation is a three single-phase FC with a phase shift at the operating point and the slightly different capacitor voltage characteristics due to the asymmetry in the converter phases. This is clearly visible in the graph with the capacitor voltage variations. The current control regulates the average value of the respective phase current for one modulation period, therefore the current ripple is missing for the three-phase output currents. This measurement also shows the long-term stability of the capacitor balancing algorithm at constantly changing operating points due to the AC current.

VIII. Conclusion

This paper presents a full-scale hardware setup of an 7-level flying capacitor designed for Quasi-Two-Level operation for medium-voltage applications. The control structure of the Quasi-Two-Level of the FC was presented and the implementation on the institute's own signal processing system was explained. The idle mode as a critical operating point was considered, and it was explained why this problem can be easily solved for Quasi-Two-Level operation. An approach to compensate the dead time of voltage measurement, which is necessary for the implementation of capacitor voltage balancing, was introduced. The structure of the converter system with the used PEBB was explained. The test setting of the measurements was described. Measurements were done to demonstrate the operation of the converter system with Quasi-Two-Level operation. These measurements demonstrated the small overvoltage stress during switching at the output voltages by Quasi-Two-Level operation.

The stability of the implemented balancing algorithm has been validated. For this purpose, capacitor voltage waveforms over several AC periods were presented.

It was further demonstrated that such small capacitances of the flying capacitors are sufficient for this mode of operation. It has been shown that Quasi-Two-Level operation of the flying capacitor is a workable approach for medium-voltage converters with higher switching frequencies.

However,The voltage stress is comparably small, when using Quasi-Two-Level operation and fast-switching semiconductors, such as SiC low-voltage semiconductors. In medium voltage applications, low overvoltages are important for the lifetime of the isolations.

References

[1] S. Mersche, D. Bernet and M. Hiller, "Quasi-Two-Level Flying-Capacitor-Converter for Medium Voltage Grid Applications," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 2019, pp. 3666-3673, doi: 10.1109/ECCE.2019.8913201.

[2] P. Czyz, P. Papamanolis, T. Guillod, F. Krismer and J. W. Kolar, "New 40kV / 300kVA Quasi-2-Level Operated 5-Level Flying Capacitor SiC "Super-Switch" IPM," 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia), Busan, Korea (South), 2019, pp. 813-820.

[3] Axel Mertens and Jakub Kucka, "Quasi Two-Level PWM Operation of an MMC Phase Leg With Reduced Module Capacitance", IEEE Transactions on Power Electronics 2016 Vol. 31 Number 10 pages 6765-6769 , doi: 10.1109/TPEL.2016.2537372

[4] I. A. Gowaid and G. P. Adam and Ahmed M. Massoud and Shehab Ahmed and Derrick Holliday and B. W. Williams, "Quasi Two-Level Operation of Modular Multilevel Converter for Use in a High-Power DC Transformer With DC Fault Isolation Capability" 2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 2019, pp. P.1-P.9, doi: 10.23919/EPE.2019.8915445.

[5] T. Meynard and H. Foch, "Multilevel choppers for high voltage applications", EPE J., vol. 2, no. 1, pp. 45-50, Mar. 1992.

[6] S. Gierschner, Y. Hein, M. Gierschner, A. Sajid and H. Eckel, "Quasi-Two-Level Operation of a Five-Level Flying-Capacitor Converter," 2015 IEEE Transactions on Power Electronics, Vol. 30 pp.108-123 , doi: 10.1109/TPEL.2014.2306453.

[7] S. Mersche, M. Bayer, K. Rickert and M. Hiller, "Analysis of balancing algorithms for Quasi-Two/Three-level Single Phase Operation of a Flying Capacitor Converter," 2022 24rd European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), 2022.

[8] Anatolii Tcai, Thiwanka Wijekoon, Marco Liserre, "Evaluation of Flying Capacitor Quasi 2-level Modulation for MV Applications" 2021 PCIM Europe digital days, Nuernberg, GER, 2021, ISBN 978-3-8007-5515-8.

[9] H. Vahedi, H. Y. Kanaan and K. Al-Haddad, "PUC converter review: Topology, control and applications," IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society, 2015, pp. 004334-004339, doi: 10.1109/IECON.2015.7392774.

[10] F. Bertoldi, M. Pathmanathan, R. S. Kanchan, K. Spiliotis and J. Driesen, Quasi-Two-Level Converter for overvoltage mitigation in medium voltage drives, The 2018 International Power Electronics Conference Niigata Japan, 10.23919/IPEC.2018.8507745.

[11] Benedikt Schmitz-Rode, Lukas Stefanski, Rüdiger Schwendemann, Simon Decker, Stefan Mersche, Philip Kiehnle, Patrick Himmelmann, Andreas Liske, Marc Hiller, "A modular signal processing platform for grid and motor control, HIL and PHIL applications", ECCE Asia 2022.

[12] S. Mersche, R. Schreier, P. Himmelmann and M. Hiller, "Medium Voltage Power Electronic Building Block for Quasi-two-level Operation of a Flying Capacitor Converter," 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), 2021, pp. P.1-P.10.