# W-Band 6-Bit Active Phase Shifter Using Differential Lange coupler in SiGe BiCMOS

Kateryna Smirnova, Mark van der Heijden, Xin Yang, Konstantinos Giannakidis, Domine Leenaerts, Ahmet Çağrı Ulusoy

***Abstract*— This paper presents a W-band vector-modulator based phase shifter with a 6-bit resolution, implemented in a SiGe:C BiCMOS technology. The phase shifter maintains the RMS amplitude and phase errors lower than 1 dB and 6.6°, respectively, for the frequency range of 86–106 GHz without digital calibration. The maximum average gain is 2.3 dB with the 3-dB bandwidth achieving 31 GHz. The circuit consumes 49 mW of power including the phase control circuitry from a 2.4 V supply voltage, 34 mW of which is used by the Gilbert cell. A novel compact differential Lange coupler is used as an IQ splitter. The core part occupies only 0.027 mm$^2$ of the IC area.**

***Index Terms*—Millimeter wave phase shifters, SiGe, W-band.**

## I. Introduction

MODERN mm-wave communication systems use very large phased arrays to achieve high precision for user detection. Analog beamforming remains frequently used nowadays, due to its power-efficiency in comparison to digital beamforming. However, this trend imposes strict requirements on a phase shifter that becomes in this case the most crucial component as its performance defines the full beamforming accuracy.

At W-band frequencies, the implementation of a phase shifter becomes considerably challenging. Besides, both passive and active solutions exhibit various limitations thus making the choice between them not obvious. Passive phase shifters become smaller as the frequency increases and provide high linearity, but their losses also increase and require an additional amplification, which in turn limits the linearity compared to a fully passive implementation and increases the overall die size. High linearity is typically important for a receiving chain, since a phase shifter comes after the LNA and thus receives an amplified (large) signal. Various hybrid implementations as well as fully active phase shifters become dominant in mm-wave frequencies. Due to limited spacing between antenna elements, phase shifters have to be as compact as possible to be used in large mm-wave arrays. That is why in this work, we demonstrate a compact solution for an active phase shifter.

In this paper, we present a differential active phase shifter for 86–106 GHz operation with a 6-bit resolution. The circuit is implemented in NXP's SiGe:C BiCMOS technology with a 6-layer back end of line [1], and uses a novel differential Lange coupler as an IQ splitter, discussed in detail in the following section.

This work has received funding from the European Union's Horizon 2020 research and innovation programme under the Marie Skłodowska Curie grant agreement No 860023. *(Corresponding author: Kateryna Smirnova)*

Kateryna Smirnova and Ahmet Çağrı Ulusoy are with the Institute of Radio Frequency Engineering and Electronics (IHE), Karlsruhe Institute of Technology, Karlsruhe, Germany (e-mail: kateryna.smirnova@kit.edu).

Domine Leenaerts, Mark van der Heijden, Xin Yang and Konstantinos Giannakidis are with NXP Semiconductors, Eindhoven, The Netherlands.

## II. Circuit Design

### A. Phase Shifter

The vector modulator uses a differential architecture, based on a Gilbert cell topology, formed by $Q_1$ and $Q_2$, as shown in Fig. 1. Transistors $Q_3$ are used as a common-base buffer to reduce the load-sensitivity of the circuit. This causes an increase in power consumption, but it is an effective solution to minimize phase and amplitude errors over frequency, while maintaining a small chip size. Components $L_1$, $L_2$ and $C_2$ form an output matching network. Decoupling capacitors are

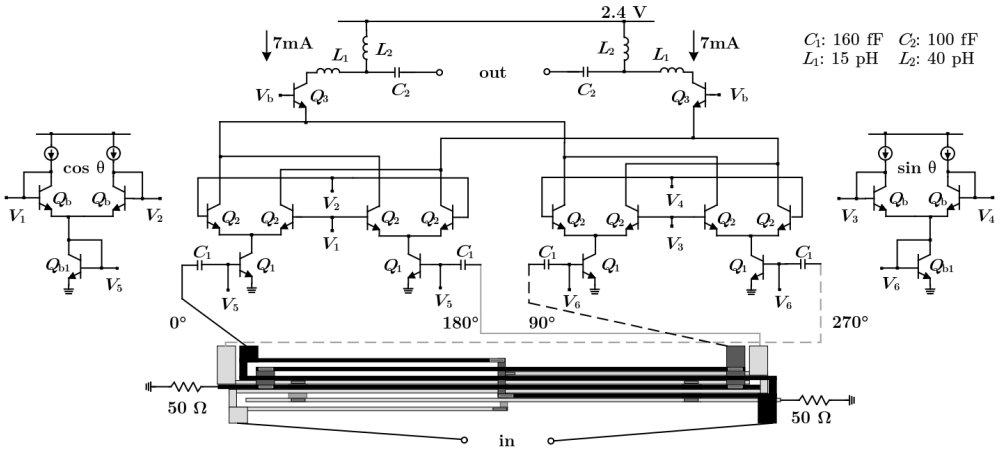


Fig. 1. Simplified schematic.

not shown in schematic but are included at the Vcc and Vb nodes. Besides, available spacing at the silicon between DC pads is used for extra DC decoupling.

The circuit operation is based on a current-steering architecture, where signals with 0°, 90°, 180°, and 270° relative phases, obtained from the differential coupler, are provided at the input. By varying $V_{1-4}$, one can control current steering between all $Q_2$ transistors and thus ensure that the required portions of each input signal (for vector summation) reach the output. This approach has the advantage of reduced linearity and amplitude variations between different phase settings in comparison to applying the control signal directly on $Q_1$.

The 6-bit phase control is provided by the control circuitry consisting of $Q_{\rm b}$, $Q_{\rm b1}$ in a current mirror topology. This bias network provides phase control voltages $V_{1-4}$ and $V_{\rm BE}$ voltages (for $Q_1$) $V_{5,6}$ that remain constant for all phase settings. Currents flowing through the $Q_{\rm b}$ transistors satisfy cos- and sin- functions in a differential way, thus targeting constant amplitude for all phase states in an ideal case. The control variable theta makes a full 360° circle with a step of 5.625°, reflecting the 6-bit precision.

The linearity of an active phase shifter is potentially worse than a passive variant. In this circuit the linearity is dominated by the transconductance devices $Q_1$, which are dimensioned to improve linearity. Also thanks to the common-base output stage, a high simulated average output 1-dB compression point of 0.6 dBm is achieved at 96 GHz. The circuit exhibits the average simulated noise figure of 12.3 dB at 96 GHz.

### *B. Differential Lange Coupler*

An IQ splitter is known to be the bulkiest component of any vector modulator, occupying more than half of the overall IC area in some cases. Therefore, exploring more compact solutions remains crucial. To provide differential I and Q signals to a vector-sum phase shifter, one can use a combination of a coupler and two baluns, as in [2]–[4]. Alternatively, a combination of a balun and a differential coupler can be used, as shown in [5].

This paper presents an area-efficient differential coupler (Fig. 2) built in essence by two conventional Lange couplers due to its good comprise between insertion loss, chip area, and bandwidth. However, instead of placing both couplers in the same horizontal plane, the second coupler was placed under the first one vertically, resulting in obtaining differential operation on the same footprint. As a first step, couplers 1 and 2 were designed and optimized separately. The line width and spacing in coupler 1 is 3 µm, following design rules for the m6 layer. Since the m1 and m6 thickness is unequal, two stacked thin layers (m1 and m2) are used for coupler 2 to partially compensate for the imbalance in ohmic losses and achieve comparable performance.

As the next design step, two couplers were placed together and optimized as one differential structure. To reduce unwanted interaction between two structures, coupler 2 was horizontally flipped relative to coupler 1, increasing the separation between input lines. Additionally, the horizontal offset was introduced to increase further the distance between the lines

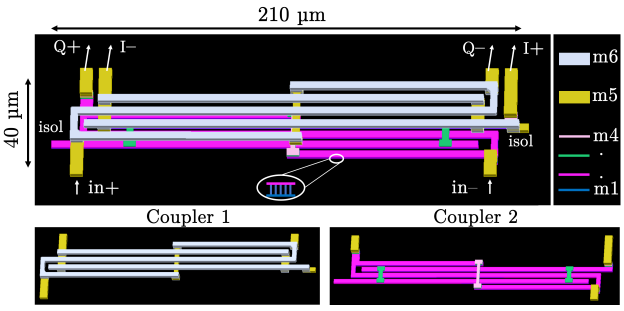


Fig. 2. Differential Lange coupler, its building blocks and metal layers.

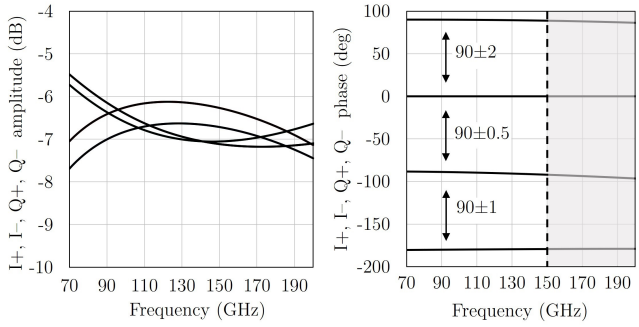


Fig. 3. IQ splitter simulation results

on m6 and m2. For the same reason, only two layers are used for coupler 2. Simulation results are shown in Fig. 3.

## III. Experimental Results

The die microphotograph with RF and DC pads is shown in Fig. 4. The active circuit core occupies 0.027 mm$^2$ of the IC area. The small signal measurements have been carried out using a broadband on-wafer system with Keysight N5290A VNA in a 4-port mixed mode configuration. The designed phase shifter consumes 49 mW of power including the control bias circuitry, from which the Gilbert cell itself uses 34 mW from a 2.4 V supply. Fig. 5 presents measured gain for all phase states and provides a comparison between simulated and measured average gain versus frequency. The maximum average gain is 2.3 dB. The average measured gain is in good

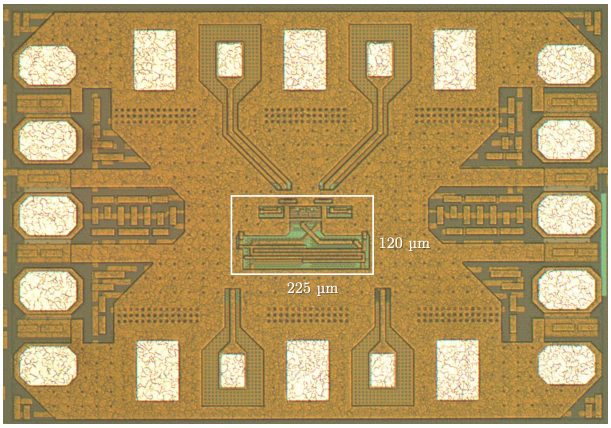


Fig. 4. Chip photograph.

TABLE I
PERFORMANCE SUMMARY

| | Technology | Frequency, GHz | Resolution, bits | Average gain, dB | RMS gain error, dB | RMS phase error, deg | $OP_{1dB}$, dBm | $P_{DC}$, mW | Area, mm$^2$ |
|---|---|---|---|---|---|---|---|---|---|
| [6] | 130-nm SiGe | 92–100 | 5 | 9.5 | 1.8 | 5 | –4 | 31 | 0.82$^{(1)}$ |
| [3] | 130-nm SiGe | 72–82 | 6 | 7 | 0.76 | 3.5 | –3 | 60 | 0.31 |
| [7]* | 28-nm CMOS | 80–100 | 6 | –9 | 0.24 | 2.2 | –10$^{(2)}$ | 7.7 | 0.11 |
| [2] | 45nm SOI CMOS | 57.7–84.2 | 5 | -6 | 1.1 | 10.1 | –1 | 17 | 0.11 |
| [8] | 55-nm SiGe | 71–76 | 6 | –2 | 0.36 | 2.1 | – | 12.8 | 0.38 |
| [9] | SiGe | 85–110 | 4 | –5 | 1 | 7.5 | –9$^{(3)}$ | 10$^{(4)}$ | – |
| This work | SiGe | 86–106 | 6 | 2.3 | 1 | 6.6 | 0.6$^{(2)}$ | 49 | 0.027$^{(5)}$ |

* calibrated $^{(1)}$including LNA $^{(2)}$simulated $^{(3)}$calculated from $IP_{1dB} = -3$ dBm $^{(4)}$ w/o DAC $^{(5)}$differential

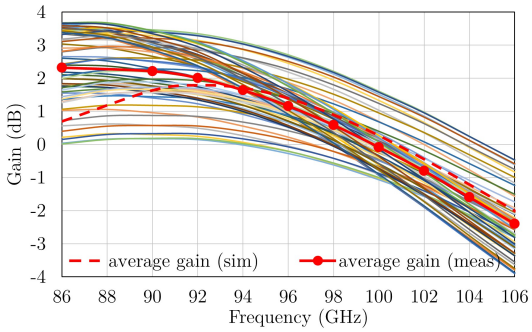


Fig. 5. Measured gain for all phase settings with overlay of simulated average gain.

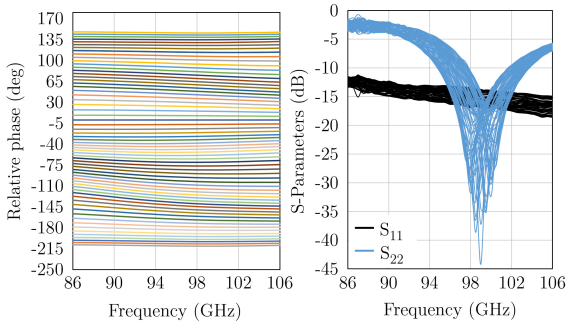


Fig. 6. Measured relative phase and return losses.

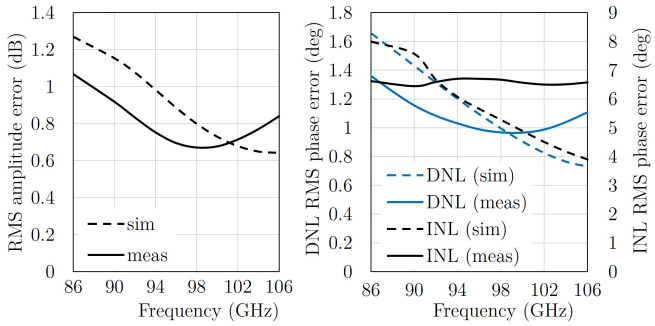


Fig. 7. Measured amplitude and phase RMS error.

agreement with simulated data, especially in the 92–106 GHz span. The relative phase is obtained by normalizing all 64 measured states to one of the states and is shown in Fig. 6.

The measured frequency behavior of the amplitude RMS error is shown in Fig. 7. The minimum amplitude RMS error (RMSE) is 0.67 dB at 98 GHz and for the frequency range 86–106 GHz, remains below 1 dB.

Phase RMS error (Fig. 7) is calculated according to an integral nonlinearity (INL) definition., i.e. the error in comparison to an ideal set of phase values. INL RMS phase error eventually represents full accumulated phase error across all states and is conventionally used as the phase RMS error definition in the literature. Another definition namely differential nonlinearity (DNL) RMS phase error is calculated as an average error between each state and the previous one and describes the phase shifting monotonicity. Both metrics belong to the industrial standards in the field of mm-wave 6G systems. The presented phase shifter exhibits 6.4° of INL RMSE and remains below 6.6° at 86–106 GHz. The phase shifter has the minimum DNL RMSE of 0.98° while remaining better than 1.35° across the same frequency range. During the measurement no additional bits for digital calibration were used, which leaves room for improvement, especially considering the flat frequency response of INL RMS phase error.

## IV. CONCLUSION

This paper presents a differential W-band 6-bit active phase shifter. An overview of previously published designs is shown in Table 1. The vector sum phase shifter is based on a Gilbert cell topology with a CB buffer stage to reduce the performance variations between different phase settings and a compact differential coupler design to minimize IC area. The achieved RMS gain and phase errors over the wide frequency range, without trimming, are excellent. As a result of the transistors size optimization, the circuit exhibits higher $OP_{1dB}$ among the works listed, but at the cost of higher power consumption. To our knowledge, the presented vector modulator occupies the smallest IC area among reported W-band 6-bit phase shifters which makes it an attractive candidate for large mm-wave phased arrays.

## REFERENCES


[1] W. D. van Noort, A. Rodriguez, H. Sun, F. Zaato, N. Zhang, T. Nesheiwat, F. Neuilly, J. Melai, and E. Hijzen, "BiCMOS technology improvements for microwave application," in *2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, 2008, pp. 93–96.

[2] N. Hosseinzadeh and J. F. Buckwalter, "A compact, 37% fractional bandwidth millimeter-wave phase shifter using a wideband lange coupler for 60-GHz and E-band systems," in *2017 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2017, pp. 1–4.

[3] H. Li, J. Chen, D. Hou, and W. Hong, "A W-band 6-bit phase shifter with 7 dB gain and 1.35° RMS phase error in 130 nm SiGe BiCMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 10, pp. 1839–1843, 2020.

[4] H. Li, J. Chen, D. Hou, Z. Li, R. Zhou, and W. Hong, "A 94 GHz scalable 2 × 2 phased-array receiver in SiGe BiCMOS for high data-rate communication," in *2021 IEEE Custom Integrated Circuits Conference (CICC)*, 2021, pp. 1–2.

[5] K. Zhao, L. Qiu, J. Chen, Q. Dong, Y.-C. Kuan, Q. J. Gu, C. Song, and Z. XU, "An E-band subradix active phase shifter with ¡ 0.69° RMS phase error and 16-dB attenuation in 28-nm CMOS," in *2022 IEEE/MTT-S International Microwave Symposium - IMS 2022*, 2022, pp. 145–148.

[6] S. Afroz and K.-J. Koh, "W-band (92–100 GHz) phased-array receive channel with quadrature-hybrid-based vector modulator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 7, pp. 2070–2082, 2018.

[7] Y. Kim and S. Hong, "A W-band vector modulator using short-channel transistor current sources and impedance compensation varactors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, pp. 1–1, 2022.

[8] T. N. Ross, S. Tiller, K. T. Ansari, and M. Repeta, "A 6-bit phase shifter at E-band using a feedback-controlled variable attenuator," in *2018 48th European Microwave Conference (EuMC)*, 2018, pp. 800–803.

[9] F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90-100-GHz 4x4 SiGe BiCMOS polarimetric transmit/receive phased array with simultaneous receive-beams capabilities," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 3099–3114, 2013.