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Validation of the Quasi-Two-Level Operation for a Flying Capacitor Converter in Medium-Voltage Applications †

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Abstract: Standard medium-voltage converters are operated at low switching frequencies using bulky passive components. One concept to change this involves the quasi-two-level operation (Q2O) of multilevel converters that use fast-switching semiconductors to minimize the need for passive components. The flying capacitor converter (FCC) uses SiC semiconductors and operates with Q2O to minimize passive components. In this paper, two different quasi-two-level algorithms are analyzed. A medium-voltage prototype was built and low-voltage and medium-voltage measurements were used to validate the concept. A particular focus is on the overvoltage, the $\mathrm{d}v/\mathrm{d}t$ behavior of the converter, as well as the dynamic behavior.

Keywords: DC–AC converters; optimization; control or power converters

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1. Introduction

Applications for medium-voltage converters in the grid are expected to increase in the future. For example, converter-based power generation systems for renewable energy are growing in both individual power and overall count. Additionally, power transmission is increasingly relying on power electronics, e.g., conventional transformers are being replaced by solid-state transformers [1]. Standard medium-voltage converters for these applications are either based on Modular multilevel converter (MMC) technology with a high number of cells or on three- or five-level converter topologies, which operate at low-switching frequencies and contain bulky line filters. Both concepts are still relatively expensive due to the high material input for the passive components. One promising concept involves the quasi-two-level operation of multilevel converters to minimize the passive components. This concept has already been investigated for the flying capacitor converter [2–6], the modular multilevel converter [7–9], and other topologies [10].

The Q2O aims to retain the benefits of low-voltage transients and low overvoltage from multilevel inverters, resulting in a high-performance two-level inverter. Due to the minimized passive components in the converter, the advantages of the smaller THD in the output voltage and output current are reduced.

For medium-voltage applications in voltage classes up to 5 kV that we focus on here, the FCC with Q2O is clearly superior to the MMC with Q2O [11]. As an example, for the same number of output voltage levels of the proposed FCC, significantly more semiconductors are needed by an MMC than by an FCC. The main focus is on the grid applications, but machine applications (such as in traction drives) are also possible.

To validate the different targets of the Q2O approach, which is presented in this paper, preliminary work has already been published by the authors. First, the simulation results of the Q2O by FCC with a novel symmetry algorithm and the corresponding design of the capacitor capacity in [2] were presented. The developed power electronic building block (PEBB) was presented with the initial measurements in [12]. For a single-phase

operation, an analysis of the presented balancing algorithms with associated measurements using PEBB was presented in [13]. The full-scale hardware built for the validation of the Q2O was described in [14] with initial measurements. In this article, the necessary data from the previous publications are summarized in the Section 1, so that the main part of the measurement results could be evaluated and understood. The validation of the Q2O, overvoltage, voltage transients, and frequency spectra of output voltages and output currents are investigated in the measurements in this article. Furthermore, measurement results for the dynamic performance and efficiency of the prototype are presented.

2. Fundamentals of Flying Capacitor Converter

The concept of the flying capacitor converter (FCC) was first introduced in [15]. The multilevel voltage is generated by switching capacitors into the active current path. An N-level FCC ($N \in \mathbb{N}$) is made of $2 \cdot (N-1)$ power semiconductor switches and $(N-2)$ capacitors in addition to the DC-link capacitor. An exemplary five-level FCC is shown in Figure 1. Each commutation cell of the FCC consists of one high side and one low side semiconductor together with the corresponding capacitor. To avoid a short circuit between the capacitors of two adjacent cells, only one transistor of each cell may be conductive at any time.

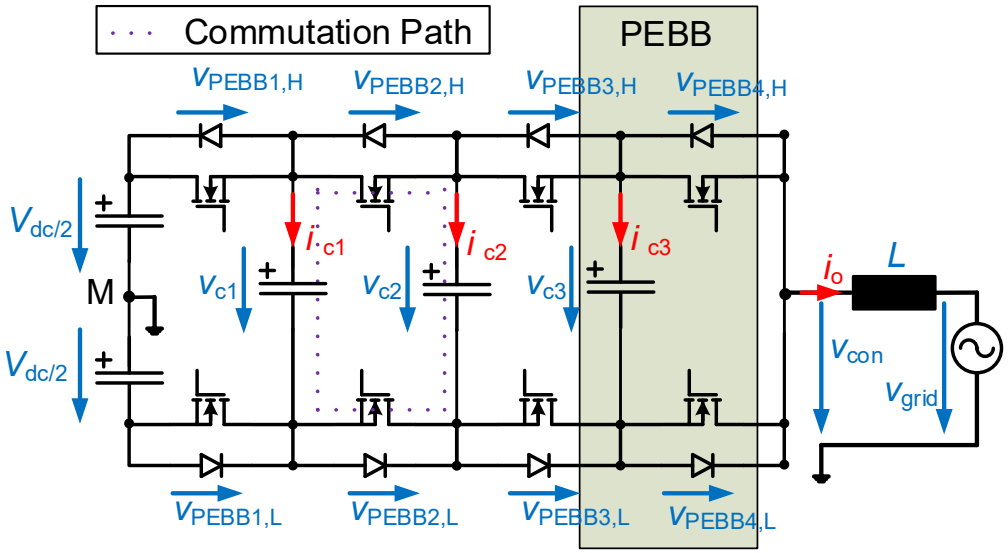


Figure 1. One phase leg of a five-level flying capacitor converter.

Each capacitor C_i has a different nominal voltage $V_{c,nom,i}$.

$$V_{c,nom,i} = V_{dc} \cdot \frac{N-1-i}{N-1} \quad i \in [1...(N-2)] \tag{1}$$

To simplify the construction, the converter is constructed using modular components, i.e., power electronic building blocks. Since the commutation cell is the repeating circuit element, a PEBB consists of one commutation cell, as can be seen in Figure 1. An N-level converter requires $(N-1)$ PEBBs. The nominal voltage across one semiconductor in one PEBB is calculated in Figure 2.

$$V_{PEBB,nom} = \frac{V_{dc}}{N-1} \quad N \in \mathbb{N} \tag{2}$$

During operation, the voltage applied across the semiconductors always deviates from the mean voltage, since the capacitor voltages are free-floating and not clamped by external voltage sources. Hence, the voltage across one capacitor varies if the capacitor is

switched into the active current path. This is the case for all multilevel output voltage levels except $+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$, where no floating capacitors are switched into the active current path. Therefore, it is necessary to balance the capacitor voltages to keep the deviation within acceptable limits.

How the output voltage of the FCC is generated can be seen in Figure 2 in the two exemplary switching states, $LHHH$ and $LLHH$. The sum of the capacitor voltages in the active current path defines the output voltage. For each output voltage level, there is a combinatorial multiplicity of possible switching states. The different switching states influence the individual capacitor voltages.

Depending on the operation mode, there are different ways to balance the capacitor voltages. For the conventional multilevel operation with alternative phase opposition disposition (APOD) modulation or phase disposition (PD), the balancing is done by exchanging carrier signals symmetrically for the corresponding semiconductor.

For quasi-two-level operations (Q2O), various types of balancing algorithms exist; more details are given in Section 3.3.

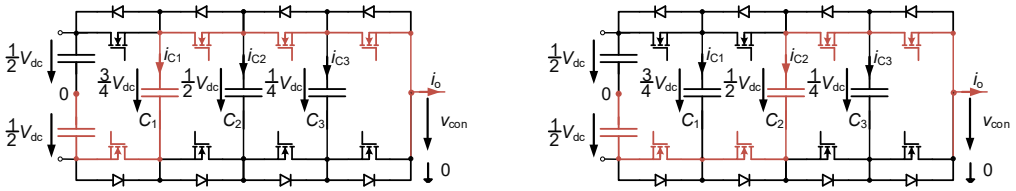


Figure 2. Exemplary switching states of the FCC. (**a**) State $LHHH$ with $+\frac{V_{dc}}{4}$ output voltage. (**b**) State $LLHH$ with zero output voltage.

3. Quasi-Two-Level Operation

The fundamental idea of the quasi-two-level operation is to use the multilevel topology in combination with a two-level modulation scheme. Hence, the applied control and modulation strategies are very similar to the well-established ones used for two-level converters. Additionally, the beneficial switching characteristics of multilevel converters in terms of reduced $\mathrm{d}v/\mathrm{d}t$ and small overvoltage stress at high output voltage levels can be realized. In [16,17], the advantages of quasi-two-level operation are discussed. For example, the lower $\mathrm{d}v/\mathrm{d}t$ in a quasi-two-level operation drastically reduces the overvoltage stress in long cables and, thus, increases the cable's lifetime.

3.1. Principle of Operation

The voltage trajectory across the output filter is the same compared to the two-level modulation. In Figure 3, a simplified output voltage (red line) of the quasi-two-level modulation, and for comparison, the output voltage of a two-level converter (dashed-dotted green line) and the output voltage of a multilevel converter (dotted blue line), are shown.

Via the quasi-two-level modulation, the switching frequency of the semiconductor corresponds exactly to the modulation frequency $\frac{1}{t_m}$ for a two-level converter. Each modulation period of each voltage level is used. By the multilevel operation, the switching frequencies of the semiconductors only correspond to $\frac{1}{N-1} \cdot \frac{1}{t_m}$. Each modulation period is only switched between the two nearest voltage levels, so the multilevel voltage is effective at the output.

By the quasi-two-level modulation, the transient output voltage level time t_p must be longer than the switching time of the semiconductors $t_s < t_p$. The time t_c to change from $+\frac{V_{dc}}{2}$ to $-\frac{V_{dc}}{2}$ is in the range of conventional dead times with less than 5% of the modulation time t_m.

In Figure 2, examples for the output voltage levels $+\frac{V_{dc}}{4}$ and zero are shown.

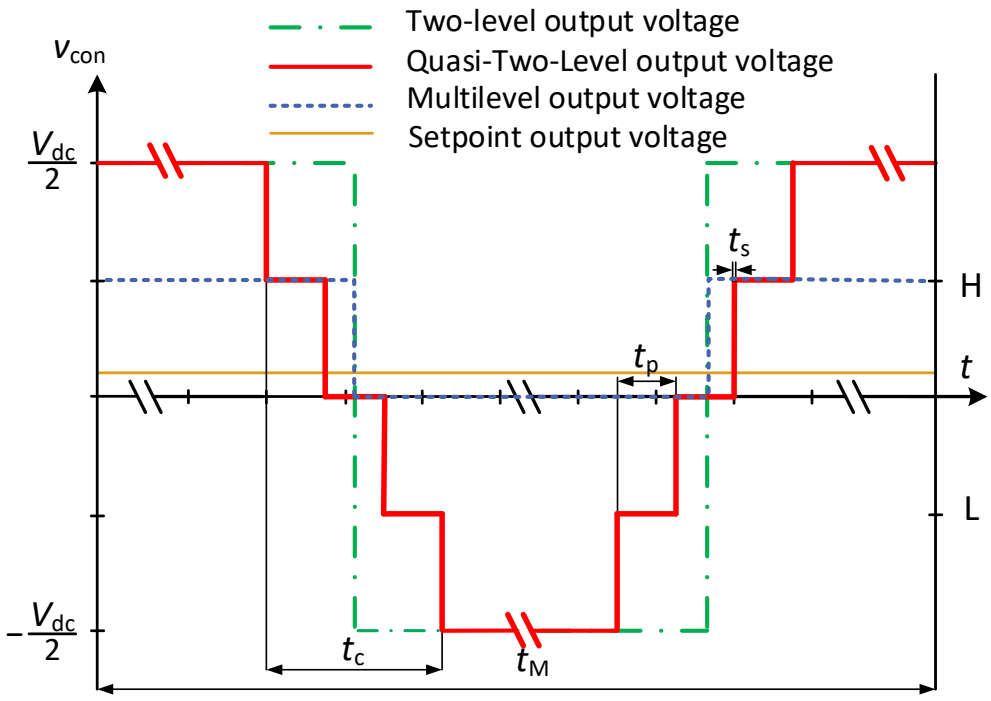


Figure 3. Quasi-Two-Level output voltage principle.

3.2. Control Structure

The current control structure of the FCC in the quasi-two-level operation only slightly differs from that of a conventional two-level converter. The structure is shown in Figure 4. It consists of the current controller itself, the modulator with gate signal generation, the power stage, the load, and the measuring element.

The only difference is within the modulator, since a modulation for the quasi-two-level operation of the FCC is needed. The modulation consists of two parts per phase, the balancing algorithm (marked "SY") and the actual gate signal generation ("Mod"). The balancing algorithm calculates the duty cycles d_{xy} for each PEBB using the phase leg duty cycle d_x determined by the controller. Index x represents the phase and index y represents the PEBB. As the cell duty cycle d_{xy} depends on the actual capacitor voltages, this measurement forms an additional loop within the control structure. Then, with the individual duty cycles d_{xy}, the gate signals G_{xy} are generated by a sine-triangle comparison in the "Mod" block.

Although the controller is drawn in the structure as a PI controller, any other kind of controller is possible. The power stage here is the three-phase FCC consisting of three single-phase FCCs, which share a common DC-link. The low-pass load is represented by the output filter of the converter, as can be seen in Figure 4. However, in the actual application, it could be substituted by the grid or an electrical machine.

For the measurements with the prototype, a conventional output current control in the rotating coordinate system with PI controllers was used. The structure of the PI controllers is shown in Figure 5. Since the controlled system is a choke without an additional voltage source, the reference angle had to be generated for the rotating reference system itself. The PI controllers only control DC variables; therefore, the AC output currents are first transformed to the reference system using the Clark transformation (3/2) and subsequent Park transformation (VD).

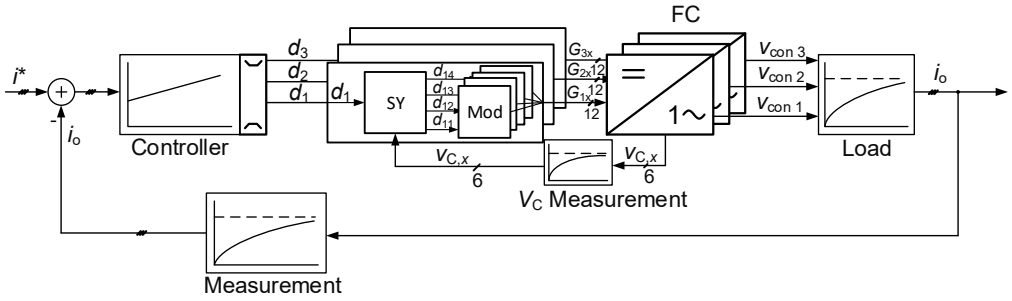


Figure 4. Signal structure of Q2O of FCC.

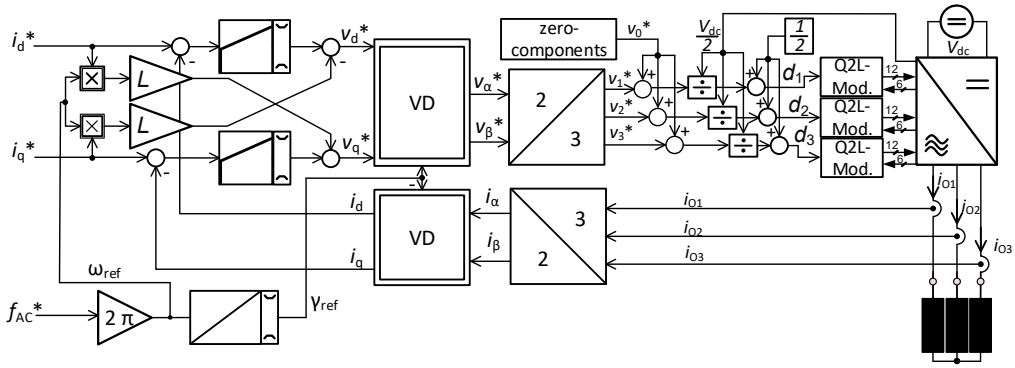


Figure 5. Signal structure of the output current controller.

The PI controllers were designed as compensating current controllers for the time-constant of the choke. The dynamics of the PI controllers were limited by the dead time of the digital signal processing used. The set points of the two voltage components were transformed back in the signal structure using the inverse Park transform and inverse Clark transform.

For a larger phase-to-phase voltage, a triple-frequency sinusoidal zero component was modulated onto the single-phase voltage set points. For the calculation of the duty cycle d_x, the voltage set point was normalized to half the DC-link voltage and the duty cycle level $d_x = 0.5$ corresponded to zero voltage at the output. The duty cycles d_x were sent to the balancing algorithms and modulation, which closed the control loop via the FCC.

3.3. Balancing Algorithm and Modulation

The Q2O of the FCC with a balancing algorithm was presented independently in [2–4]. The main goal for the Q2O is the reduction of overvoltage. To achieve minimal overvoltage, only one PEBB is allowed to change its state at once per switching state transition in Q2O. Thus, the commutation circuit is within one PEBB and is, therefore, as small as possible. This results in a restriction in the balancing algorithm of the FCC.

In Figure 6, the switching scheme of a single-phase 5-level FCC is shown with the aforementioned restriction. The capacitor current i_{cx} is positive if the output current i_o flows in the same direction. It can be seen that for voltage steps between $+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$, any current flow direction through the respective capacitor is possible. At the voltage levels $+\frac{V_{dc}}{2}$ (state $HHHH$) and $-\frac{V_{dc}}{2}$ (state $LLLL$), the output current does not flow through any of the capacitors.

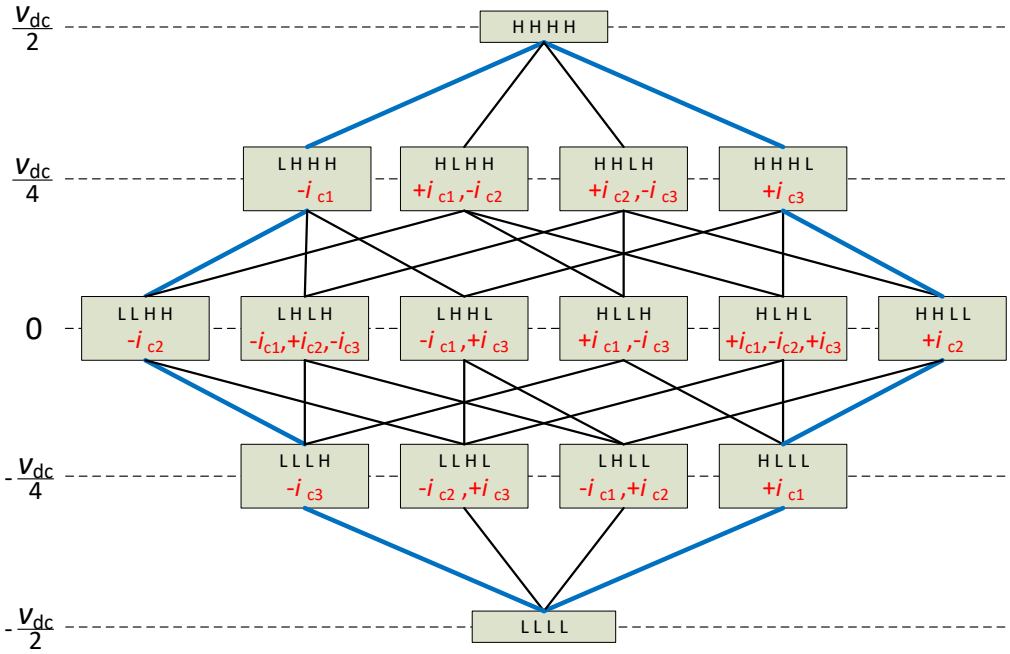


Figure 6. Switching state chart for a 5-level flying capacitor.

The problem of balancing was fundamentally solved with two different methods. The first method [3,4] has a fixed switching sequence and varies the plateau time t_p, i.e., the time an intermediate voltage is active. However, the plateau time t_p must always be greater than the switching time t_s of the semiconductor to achieve multiple levels. The algorithms of [4] only use the switching sequences marked in thick blue in Figure 6. Depending on the capacitor voltage, the plateau time t_p is selected to be either minimal ($t_{p,min}$) or maximal ($t_{p,max}$). The maximum of the plateau t_p depends on the capacitance value and the permissible voltage range in operation. The minimum of the plateau t_p depends on the dead-time time of the used semiconductors, which correlates with the switching times of the semiconductors ($t_p > t_s$). If the switching state reduces the deviation of the actual capacitor voltage $v_{c,i}$ and the calculated mean value of the capacitor voltage $v_{c,nom,i}$, the associated plateau time t_p is maximized, otherwise, the plateau time t_p is minimized.

The second method, formulated and investigated in previous work [2], varies the switching sequence while the plateau time t_p is fixed. For those algorithms, all possible switching sequences in Figure 6 are used. An optimal path is selected depending on the deviation of the actual capacitor voltage $v_{c,i}$ and the calculated mean value of the capacitor voltage $v_{c,nom,i}$. It is calculated for each switching state to see if it has a positive influence, then the path with the highest positive influence is selected. Here, the allowable range of the plateau time t_p is also limited by the above-mentioned parameters, but a fixed value is used for this algorithm. $t_{p,fix}$ is chosen to be greater than t_s and as small as possible so that the capacitor voltage deviations are small.

The principle of the modulation of the quasi-two-level algorithm described in [2] is illustrated in Figure 7. A carrier-based modulation with a carrier for each PEBB is used to generate the gate signals G_{xy}. Each PEBB has a different duty cycle to switch with the time delay (so that the quasi-two-level output voltage is generated). Once the switching sequence and plateau time t_{pi} for each level is identified with the described methods, the final step is to calculate the individual duty cycles d_{xy} of each PEBB and pass them to the modulator. The modulator generates the gate signals for the two semiconductors. In Figure 7 the curve for the high-side semiconductor is drawn. The low-side semiconductor switches inverse to the drawn signals, where a corresponding interlock of the signals is implemented in the modulator.

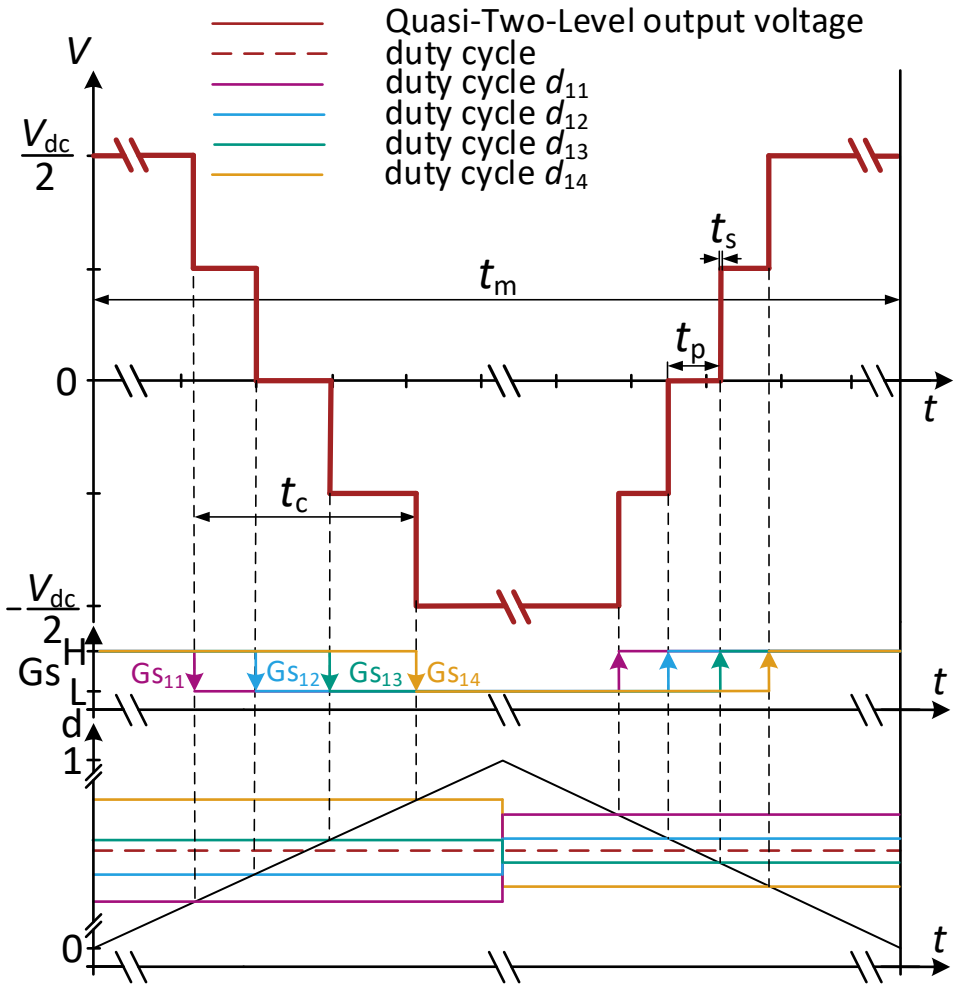


Figure 7. Carrier-based modulation with the balancing of the Q2O at FCC.

In [13], an analysis of the different methods has already been presented. It is evident that the algorithms with a fixed switching sequence are easier to implement. The capacitor voltage deviations are different and the overvoltages also differ. The validation with measurements was performed with the single-phase hardware prototype at that time. In addition to that measurements, a three-phase setup is presented in Section 5.1.

In [18], an optimized combination of these two methods is presented.

3.4. Reduction Opportunities for the Passive Components

The components, which are primarily reduced by the Q2O at multilevel converters, are the capacitors. The power semiconductors cannot be altered compared to conventional 2L VSC; the design of the output filters does not differ from the same number of effective output voltage levels and the modulation frequency.

The resulting capacitance C_{Q2O} of the FCC can be calculated according to Section 3.

$$C_{Q2O} = \frac{t_{CC} \cdot \hat{i}_o}{\Delta V_{c,max}} \tag{3}$$

Here, the permitted capacitor voltage ripple $\Delta V_{c,max}$ is selected in the range of 10% to 20% of nominal capacitor voltage $V_{PEBB,nom}$, which is defined in Equation (2).

The maximum output current $\hat{i}_o$ is determined from the total system. The conduction time of one capacitor t_{CC} is determined based on the balancing algorithm. It varies between t_p and t_c.

For reducing the capacitance, the conduction time t_{CC} should be as small as possible. This can be achieved by using fast-switching semiconductors for the Q2O, so that t_s is small and thus t_p resp. t_c becomes small, too. The reduction in size is primarily due to the ratio of $\frac{t_{CC}}{t_M}$, i.e., the shortened conduction time of the capacitors compared to the normal multilevel converter modulation. With fast-switching semiconductors, such as SiC, the capacitance can be reduced by a factor of 10 to 100 compared to the conventional multilevel FCC.

4. Hardware Prototype

To validate the results of the simulation analysis of the lower overvoltage, lower $\mathrm{d}v/\mathrm{d}t$, and the balancing algorithms, a full-scale FCC prototype with seven levels per phase was designed and constructed.

The converter system described below is the first published three-phase FCC with Q2O in medium-voltage range. In the past, mainly low-voltage prototypes have been built [6,18] or a single-phase FCC with Q2O in the medium-voltage range [3,19].

4.1. PEBB

The test and validation of the PEBB are presented in [12]. A PEBB consists of two power semiconductors, one flying capacitor, and the necessary peripherals, such as the gate units, the measurement circuit for the capacitor voltage, the heat sink temperature, as well as the fan control. A picture of two PEBBs, arranged in a so-called double-PEBB configuration, is shown in Figure 8. The goal is to design a modular system, consisting of interchangeable units that are connected to each other. This means that the insulation of the PEBB must be designed for the highest possible voltage, i.e., the DC-link voltage. That is one of the reasons why this topology is not used for high-voltage applications. The PEBB is designed to ensure the safe isolation of the medium voltage from the auxiliary power supply and signal processing. The isolation is designed for values for medium-voltage levels above 4 kV.

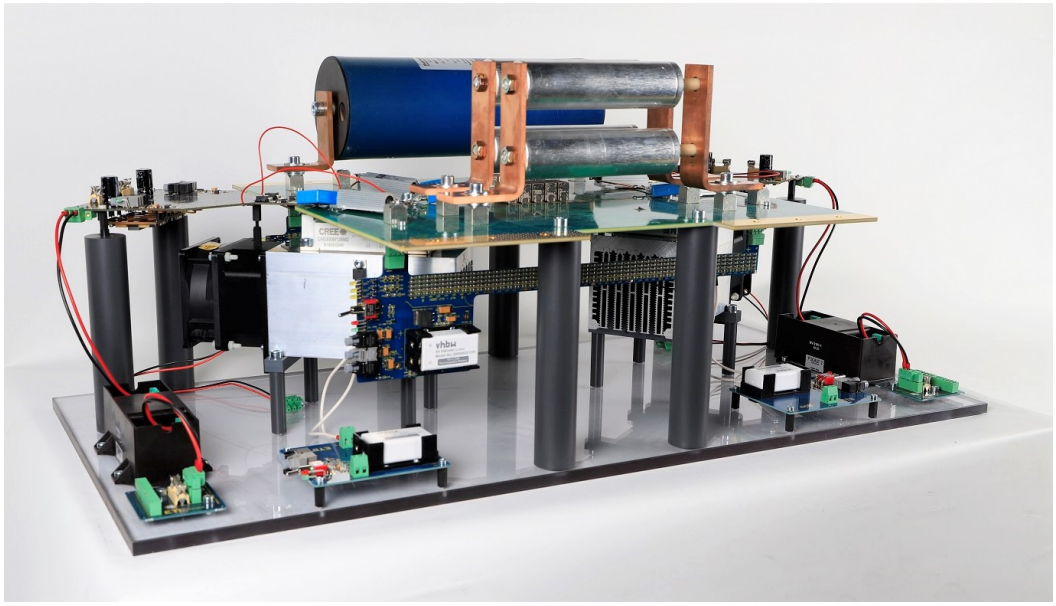


Figure 8. The double power electronic building block for the flying capacitor converter.

For the quasi-two-level operation mode, it is essential that the power semiconductors are turned on and off as fast as possible. Therefore, SiC-MOSFETs as fast-switching semiconductors are selected. Most commercially available packages feature half bridges or three-phase bridge configurations. Therefore, a half-bridge module is selected. This is also the reason why the design as shown in Figure 8 consists of two PEBBs. The prototype is built with SiC-MOSFET module CAS300M12BM2 with a blocking voltage of 1200 V and a current rating of 300 A. The output current I_O is tested up to 150 A.

The capacitance is implemented with two different types of capacitors connected in parallel. One part consists of ceramic capacitors connected to the modules with a minimized stray inductance to minimize the overvoltage at the semiconductors. The ceramic capacitors consist of five CR2613s, each with a capacitance of 11.7 nF and a nominal voltage of 10 kV. The second part consists of film capacitors, which are adapted to the voltage of the corresponding flying capacitor. Although the capacitors of different PEBBs vary in voltage ratings, they always provide the same total capacitance of 1 µF.

4.2. Full-Scale Prototype

The full-scale prototype was presented in [14]. The converter is implemented in a cabinet with four floors. In Figure 9 the converter system is shown. On the lowest floor, the control unit containing the signal processing system and the auxiliary power supplies for the peripherals is placed. The described control structure of the FCC was realized with an in-house developed signal processing system [20], based on a system on chip (SoC). Above, each floor contains one phase of the converter. On the right side of each corresponding phase, the output current measurement is realized with the current sensor LTC 200 with a measuring range of ±300 A and bandwidth of 100 kHz. On the left side, the central DC-link is implemented, which vertically interconnects the three phases. The structure consists of six PEBBs per phase, each phase is realized by three double PEBBs. This results in a seven-level FCC. The setup can also be operated using only the first two double PEBBs on the front, resulting in a five-level FCC. For the measurements, the five-level operation was realized in such a way that the last double PEBB with all four semiconductors is permanently switched on. The converter is designed for $V_{\mathrm{PEBB,nom}} = 800\,\mathrm{V}$. Through operation, it has been shown that the voltage deviations of the capacitors are larger than predicted, so $V_{\mathrm{PEBB,nom}} = 650\,\mathrm{V}$ will be the realistic limit to avoid damage. Thus, the theoretical maximum DC-link voltage is up to 4 kV as a 7-Level FCC or 2.6 kV as a five-Level FCC. The theoretical output power of the inverter is about 350 kW with an AC output voltage of up to 2.4 kV for the 7-Level FCC.

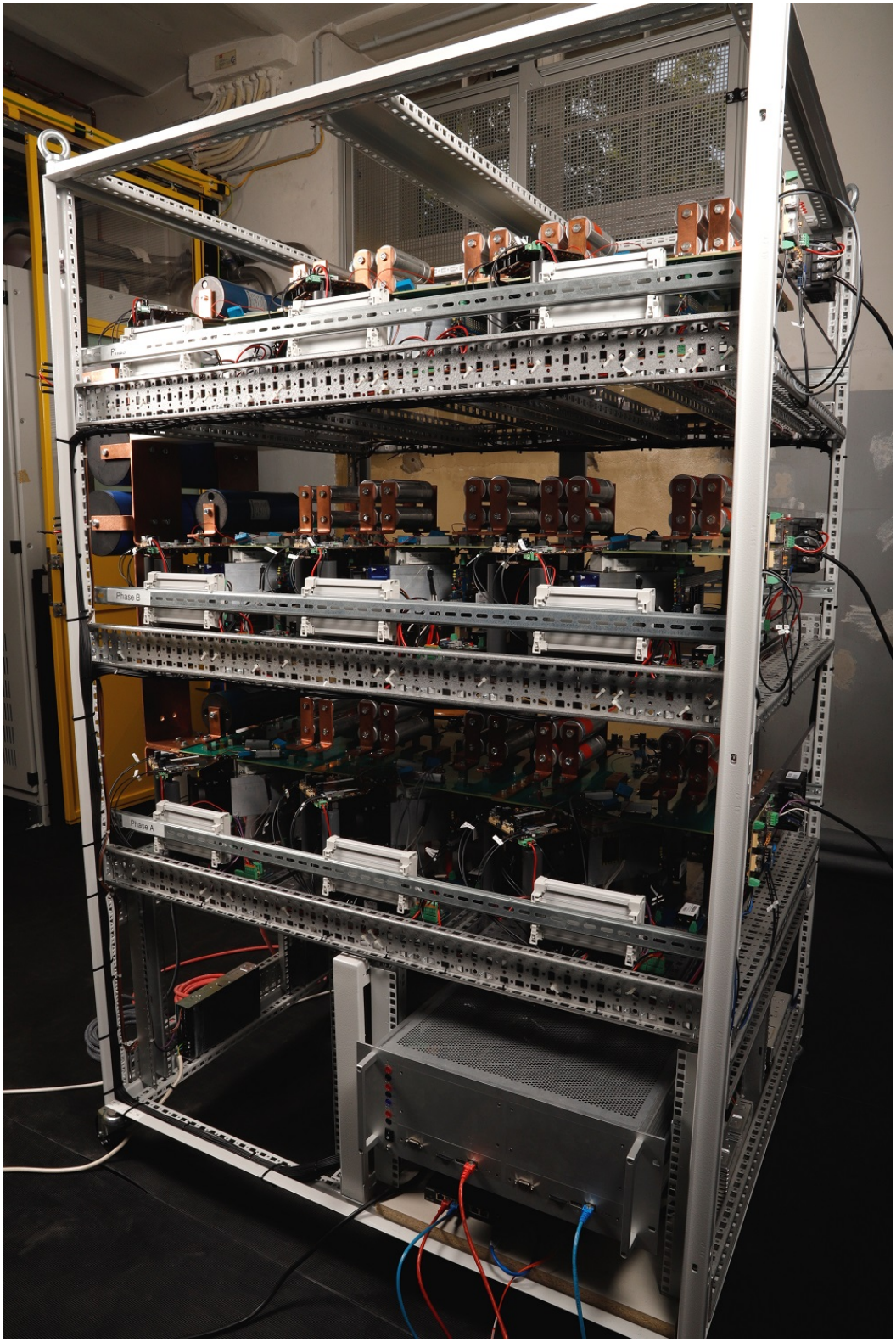


Figure 9. Picture of the three-phase seven-level flying capacitor converter.

4.3. Test Setup

The converter is used in a test setting that has as little influence as possible on the operation of the converter. The FCC is supplied by a DC source, which generates a galvanically isolated medium voltage from low voltage. A three-phase choke is used as the load with 5 mH inductance per phase. The structure is shown in Figure 10. In order

to operate the converter, the capacitors must be pre-charged so that the distribution of the DC-link voltages results in the calculated semiconductors block voltages according to Equation (2). The pre-charging algorithm presented in [13] is used for all three phases simultaneously. The pre-charging of the flying capacitors is done together with the DC-link capacitors. Pre-charging works in such a way that, in the first step, all necessary semiconductors are switched on (so that all capacitors are connected in parallel). Then, the voltage of the DC-link voltage is ramped up and the capacitors are charged. When the voltage of the capacitors has reached the nominal value of the capacitor with the lowest set-point, the according semiconductors are switched off and the other capacitors are charged. The algorithm always switches off the respective semiconductors when the capacitor voltage has reached the set point of the respective capacitor. After all capacitors have reached their nominal voltages, the control structure from Figure 4 starts immediately.

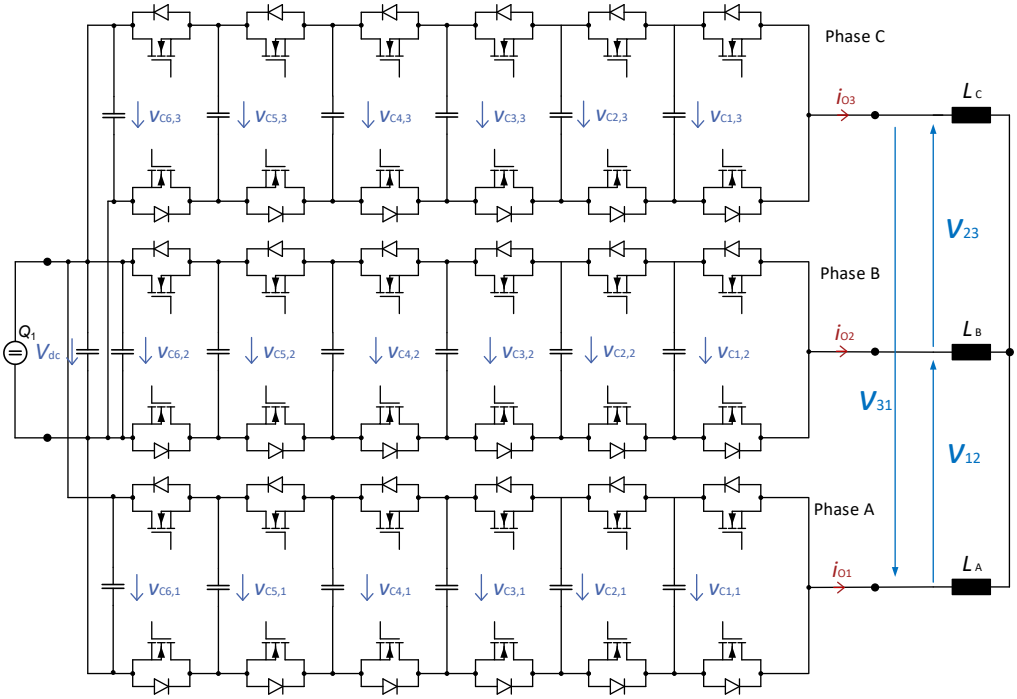


Figure 10. Three-phase test-setup.

5. Measurements

For the validation of the simulation investigations, different measurements were executed with the converter system in the test setup. First, a low-voltage measurement of the FCC was performed to analyze the influence of the different modulation schemes on the output characteristics of the FCC, the switching behavior of the semiconductors, and the voltage balancing of the cells. The influences of the different methods of balancing on the AC output voltage and AC output current were investigated. Subsequently, measurements were performed during the operation of the FCC in the medium-voltage range. Especially the overvoltage and the voltage transients were examined in more detail. Furthermore, the influence of the frequency of the output current was investigated during measurements in the medium voltage. To ensure that not only steady-state measurements but also the dynamic characteristics of the Q2O were investigated, the set points of the output current and the DC-link voltage were changed during operation. In the measurements, an output frequency of 100 Hz was used so the inductance of the load choke would result in a larger voltage drop. The larger voltage drop required a larger output voltage, so a wider range of duty cycles was used.

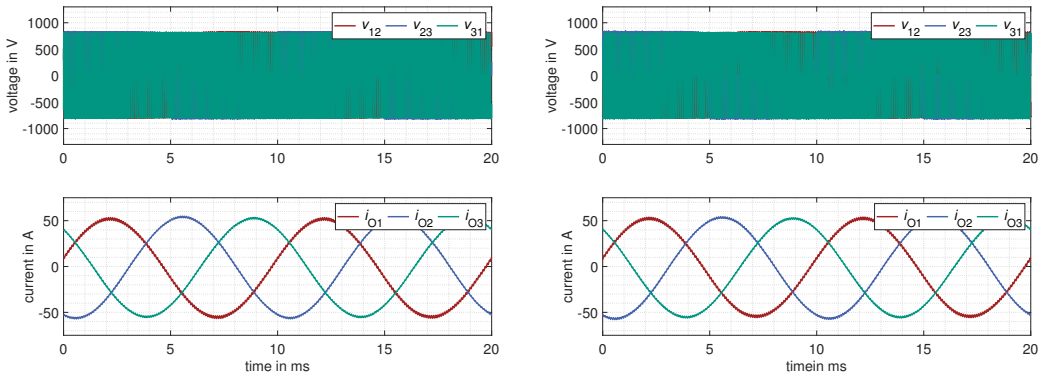
5.1. Low-Voltage Measurements

For the low-voltage measurements, the nominal semiconductor blocking voltage $V_{\mathrm{PEBB,nom}}$ is set to 200 V, which results in $V_{\mathrm{DC}} = 800\,\mathrm{V}$. With this small voltage, the influences are easier to identify. The set point of the output current for the low-voltage measurements was 50 A. Further, the minimum plateau time $t_{\mathrm{p,min}} = 400\,\mathrm{ns}$ and the maximum plateau time $t_{\mathrm{p,max}} = 800\,\mathrm{ns}$ were selected for the algorithm of method one—fixed switching sequences and variable plateau time t_{p}. For the algorithm of method two—variable switching sequences and fixed plateau time $t_{\mathrm{p,fix}} = 400\,\mathrm{ns}$ was selected. The influence of larger plateau times t_{p} was also tested. Since this change results in a deteriorated performance, those measurements are not presented. Longer plateau times t_{p} do not result in smaller overvoltages or lower $\mathrm{d}v/\mathrm{d}t$, because they do not affect the switching speed of the semiconductors. In addition, a longer plateau time provides larger capacitor voltage deviations because the output current flows through the capacitors for a longer time. The shortest possible plateau time t_{p}, which is slightly longer than t_{s}, is to be preferred.

5.1.1. Three-Phase Output Voltage and Output Current

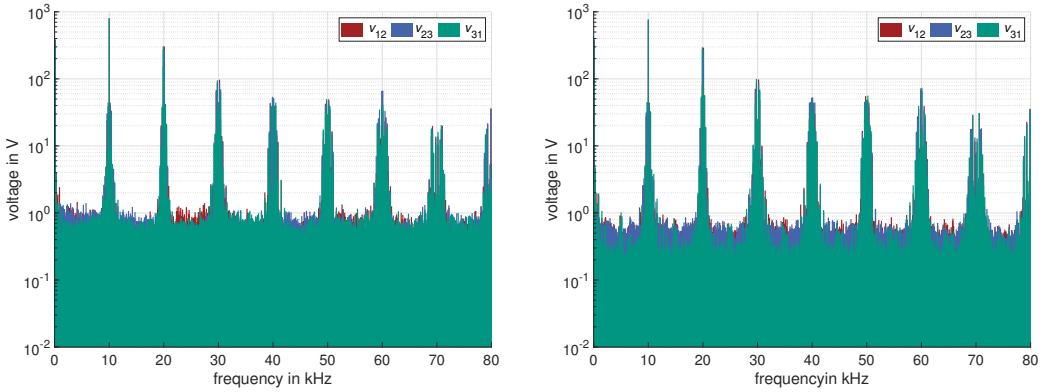
In Figure 11, the three-phase output voltage and output current of the FCC are shown with both balancing methods. The frequency spectra of the output voltages are shown in Figure 12. For the output current, the frequency spectrum is shown in Figure 13. For comparison, the THDs of the output voltage and the output current were calculated for both balancing methods. The first method shows an output voltage WTHD of 13.05% and an output current THD of 22.47%. Compared to that, the THD of the second method is 9.47% for the output voltage and 20.26% for the output current. The quality of the output current does not differ and the difference in the output voltage does not have a great effect. The spectrum of the output current shows slight differences at the higher frequencies, which could be measurement inaccuracies. In general, the measurements do not differ from a conventional 2-level converter, when considering whole AC periods.

In addition to whole AC periods, the time domain of modulation periods was also investigated more in detail. Here, the FCC shows significantly different behavior depending on the balancing method. The three-phase voltages and currents are represented in Figure 14. It can be clearly seen that the variation in switching sequences if the second balancing method is used has a negative effect on the overvoltage. The overvoltage is constantly small for the first balancing method with fixed switching sequences. This is probably the reason for the differences in the spectrum of the output current at the higher frequencies. The variation of the overvoltage is caused by the different characteristics of the commutation cells depending on the selected switching sequence. The different PEBBs have different types of capacitors and the electrical connections within the PEBB power boards differ slightly. It is surprising, however, how big the difference in overvoltage is. It cannot be ruled out that there could be a resonance in the converter system itself. The FCC in low-inductive design with the low-impedance small capacitance is a highly oscillatory system. The fast-switching of the semiconductors generates a very wide range of possible excitation for resonances in the converter system.



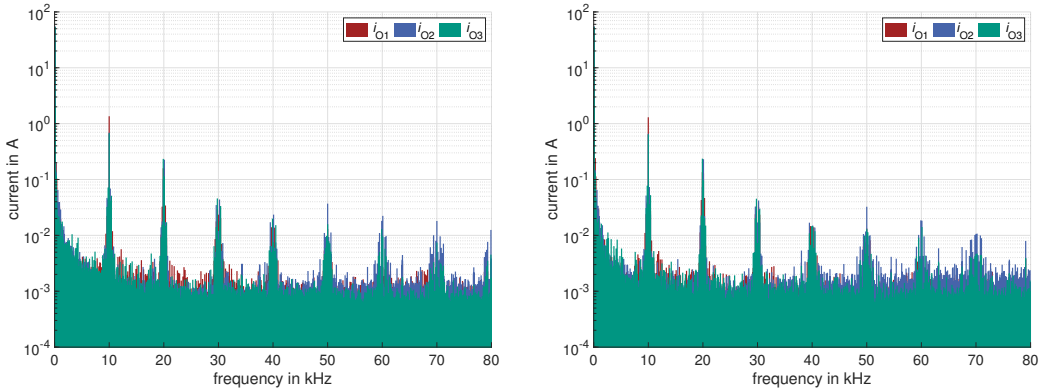
(a) (b)

Figure 11. Three-phase output voltage and output current waveforms with the same output current and DC-link voltage set point. (**a**) Measurements results of the first method [4] balancing algorithm—fixed switching sequences and variable plateau time t_p. (**b**) Measurements results of the second method [2] balancing algorithm—variable switching sequences and fixed plateau time t_p.



(a) (b)

Figure 12. Three-phase output voltage frequency spectrum with the same output current and DC-link voltage set point. (**a**) Measurements results of the first method [4] balancing algorithm—fixed switching sequences and variable plateau time t_p. (**b**) Measurements results of the second method [2] balancing algorithm—variable switching sequences and fixed plateau time t_p.



(a) (b)

Figure 13. Three-phase output current frequency spectrum with the same output current and DC-link voltage set point. (**a**) Measurements results of the first method [4] balancing algorithm—fixed switching sequences and variable plateau time t_p. (**b**) Measurements results of the second method [2] balancing algorithm—variable switching sequences and fixed plateau time t_p.

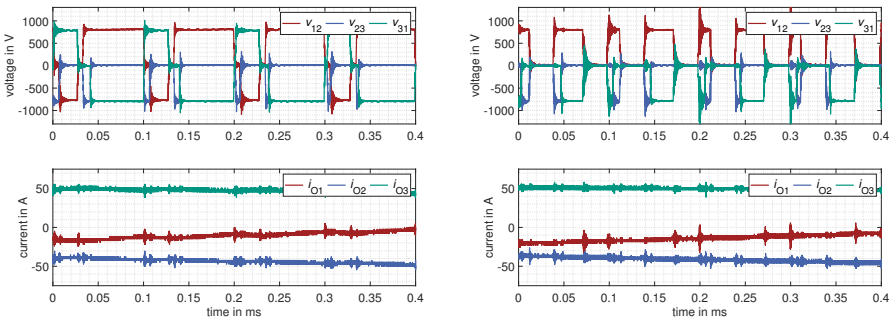


Figure 14. Three-phase output voltage and output current waveforms with the same output current and DC-link voltage set point. (**a**) Measurements results of the first method [4] balancing algorithm—fixed switching sequences and variable plateau time t_p. (**b**) Measurements results of the second method [2] balancing algorithm—variable switching sequences and fixed plateau time t_p.

5.1.2. Capacitor Voltage Balancing

For the operation of the FCC, the balancing of the flying capacitor is crucial. Hence, the voltages of the single capacitors are measured and shown in Figure 15. The capacitor voltage deviations are larger for balancing method two. With both implemented methods, the capacitor voltage deviations are kept within the permissible voltage ranges of ±20 % of $V_{PEBB,nom}$. The mean value of each capacitor does not exactly match the nominal value, since none of the used algorithms achieve 'stationary' due to the variations of the output current.

Another interesting effect of the different balancing methods is the AC stress on the capacitors. In Figure 16, the frequency spectra of the capacitor voltages are shown. For comparison, the THD of the capacitor voltage was also calculated here. The DC component was taken as the reference value. At the first balancing method, the THD of the capacitor voltage is 53.27%. The THD of the capacitor voltage at the second method is 97.23%. The switching frequency of 10 kHz and its multiples can be clearly seen in the results of the first balancing method. By balancing with the second method, the spectrum of the capacitor voltages includes many other frequencies. The additional frequencies in the second method result in the aforementioned difference in the THD. For the selection of the capacitors, the frequency-dependent AC load capacity must be taken into account.

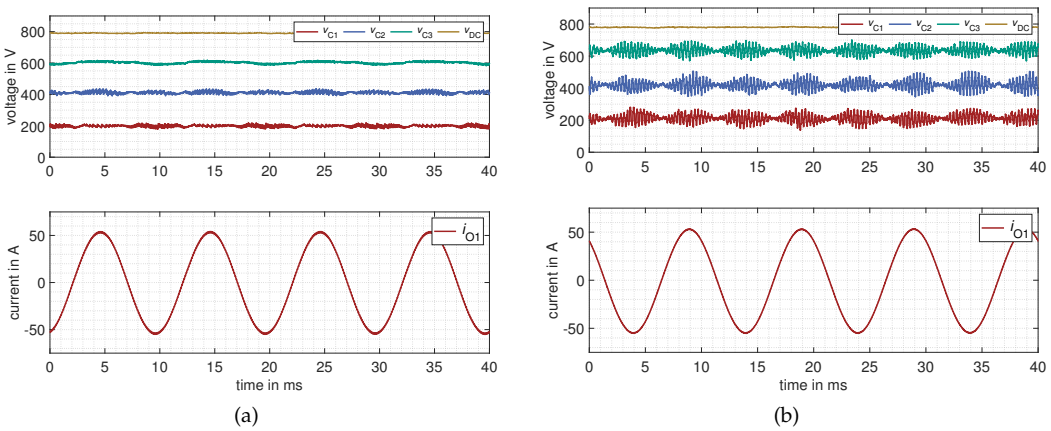


Figure 15. Single phase capacitor voltage, output voltage, and output current waveforms with the same output current and DC-link voltage set point. (**a**) Measurements results of the first method [4] balancing algorithm—fixed switching sequences and variable plateau time t_p. (**b**) Measurements results of the second method [2] balancing algorithm—variable switching sequences and fixed plateau time t_p.

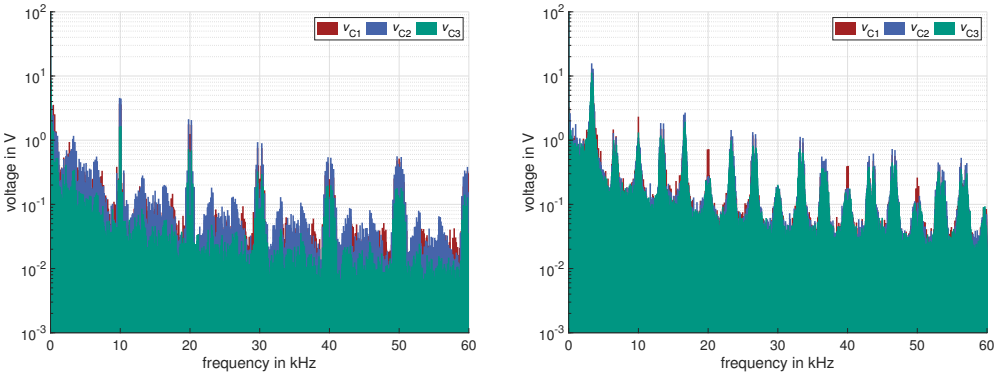


Figure 16. Single phase frequency spectrum of the capacitor voltage waveforms with the same output current and DC-link voltage set point. (**a**) Measurements results of the first method [4] balancing algorithm—fixed switching sequences and variable plateau time t_p. (**b**) Measurements results of the second method [2] balancing algorithm—variable switching sequences and fixed plateau time t_p.

5.2. Medium-Voltage Measurements

For the medium-voltage measurement, the seven-level operation of the FCC is used with the first balancing method. Thereby, the minimum and maximum plateau times ($t_{p,min}$ and $t_{p,max}$) were set to 400 ns and 800 ns, respectively. The set point of the output current was 70 A. The larger voltage deviations and larger overvoltage are why the balancing algorithm of method two was not implemented for the seven-level operation.

The medium-voltage measurements in the seven-level operation were performed according to the implemented algorithm with fixed switching sequences and variable plateau times t_p. The measurements are presented with a maximum DC-link voltage of 2.9 kV, at which a stable operation of the prototype is achieved. At higher DC-link voltages, the prototype switches off for self-protection against the destruction of the semiconductors. The presented measurements are the first measurements with DC-link voltages greater than 2 kV. These measurements can be classified as those of a full-scale medium-voltage converter.

5.2.1. Maximum DC-Link Voltage

The focus of the measurement with maximum DC-link voltage was on the specification of the overvoltage and the occurring dv/dt. In Figure 17, the same six measurement graphs are shown for the low-voltage measurements. At a higher DC-link voltage, the behaviors of the FCC's Q2O results remain the same for the low-voltage measurements. In Figure 17b, the phase output voltage is shown in the time domain of the modulation period. It can be seen that the maximum overvoltage is about 380 V, which is 13.1% of the DC-link voltage. This is very small for conventional medium-voltage converters. The maximum measured dv/dt of the phase output voltage was 3.596 kV μs^{-1}. This is also a low value compared to 2L VSC with up to 10 kV μs^{-1} [21]. Through this, the dv/dt filter can be designed to be much smaller for the same voltage stress of the load compared to conventional 2L voltage source converters. For comparison—for the low-voltage measurements, the THD of the output voltage, output current, and capacitor voltages were also calculated. The value of the WTHD is 15.78% of the output voltage. The values of the THDs are 34.45% of the output current and 25.48% of the capacitor voltage. The larger THD of the output voltage can be explained by the larger DC-link voltage with the amplitude of the 100 Hz component of the output voltage not increasing equally. The larger DC-link voltage also provides a larger current ripple and, thus, a slightly larger THD of the output current. On the other hand, the THD of the capacitor voltage has decreased due to the higher DC component. The maximum capacitor voltage deviation is still the same, which is the more important parameter for the FCC.

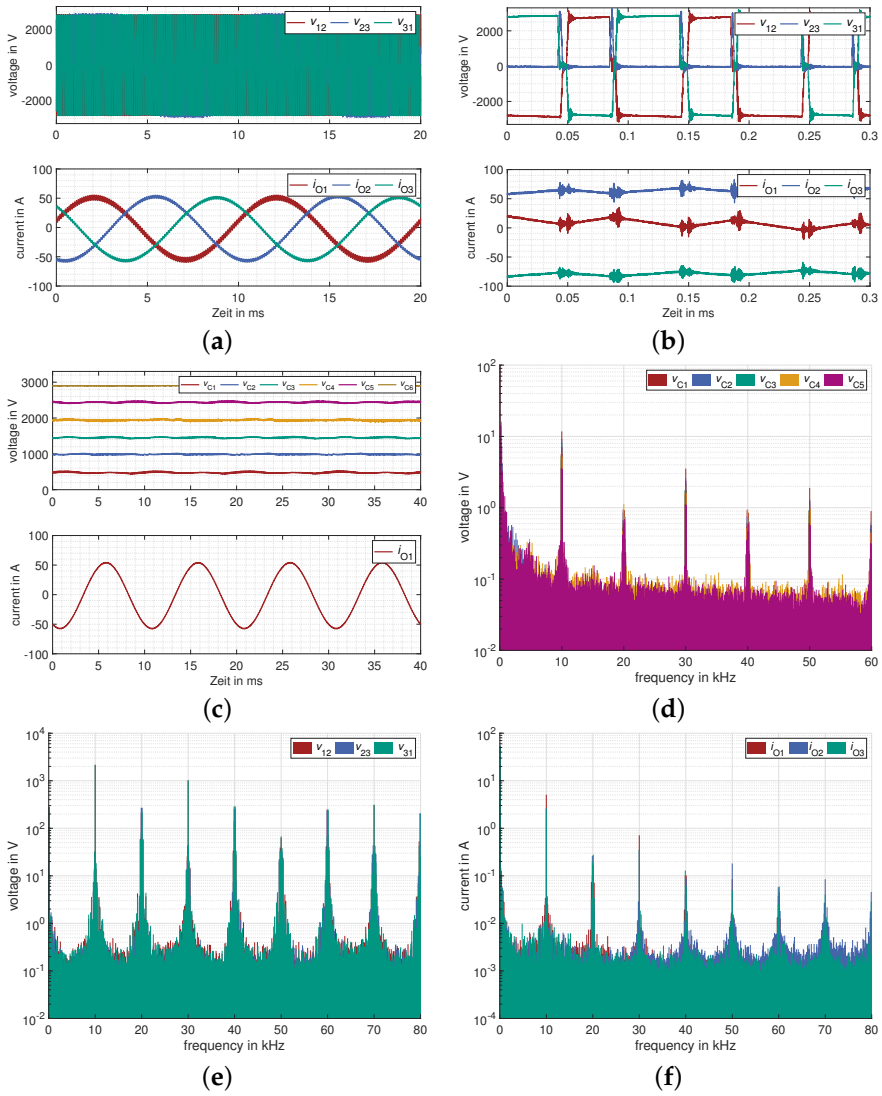


Figure 17. Measurement results at medium voltage with $V_{DC} = 2.9$ kV and 100 Hz output frequency. (**a**) Three-phase output voltage and output current waveforms. (**b**) Three-phase output voltage and output current waveforms. (**c**) Single-phase output current and capacitor voltages waveforms. (**d**) Frequency spectrum of the capacitor voltage waveforms. (**e**) Frequency spectrum of the output voltage waveforms. (**f**) Frequency spectrum of the output current waveforms.

5.2.2. Higher Frequency Output

To analyze the influence of the output frequency on the output characteristic, measurements for an output frequency of 200 Hz were made.

In Figure 18, the results of a measurement at 2.4 kV DC-link voltage are presented. For comparison with the previous measurements, the THDs were calculated again. The value of the WTHD is 5.65% for the output voltage. The value of the THD is 20.25% for the output current and 28.33% for the capacitor voltage. The smaller THD of the output voltage is because of the larger amplitude of the 200% component in the spectrum at the same output current. The THD at the output current is smaller than at the maximum DC-link voltage because the current ripple is smaller and the spectrum is more dampened. With capacitor voltages, the THD is greater because the changed output frequency results in different frequency components in the capacitor voltages. The spectrum around the switching frequencies is wider. The measurement in Figure 18c demonstrates that the capacitor voltage deviations are dependent on the output current. The maximum deviation is not dependent on the frequency of the output current. The higher frequency is clearly visible in the frequency spectra of the output voltages, output currents, and capacitor

voltages. Other frequencies are seen in the spectra, but this was expected. The frequency spectrum of the output voltages demonstrates clearly that frequencies of $n \cdot f_s \pm m \cdot f_{AC}$ can exist. The larger n and m are, the more those components are damped.

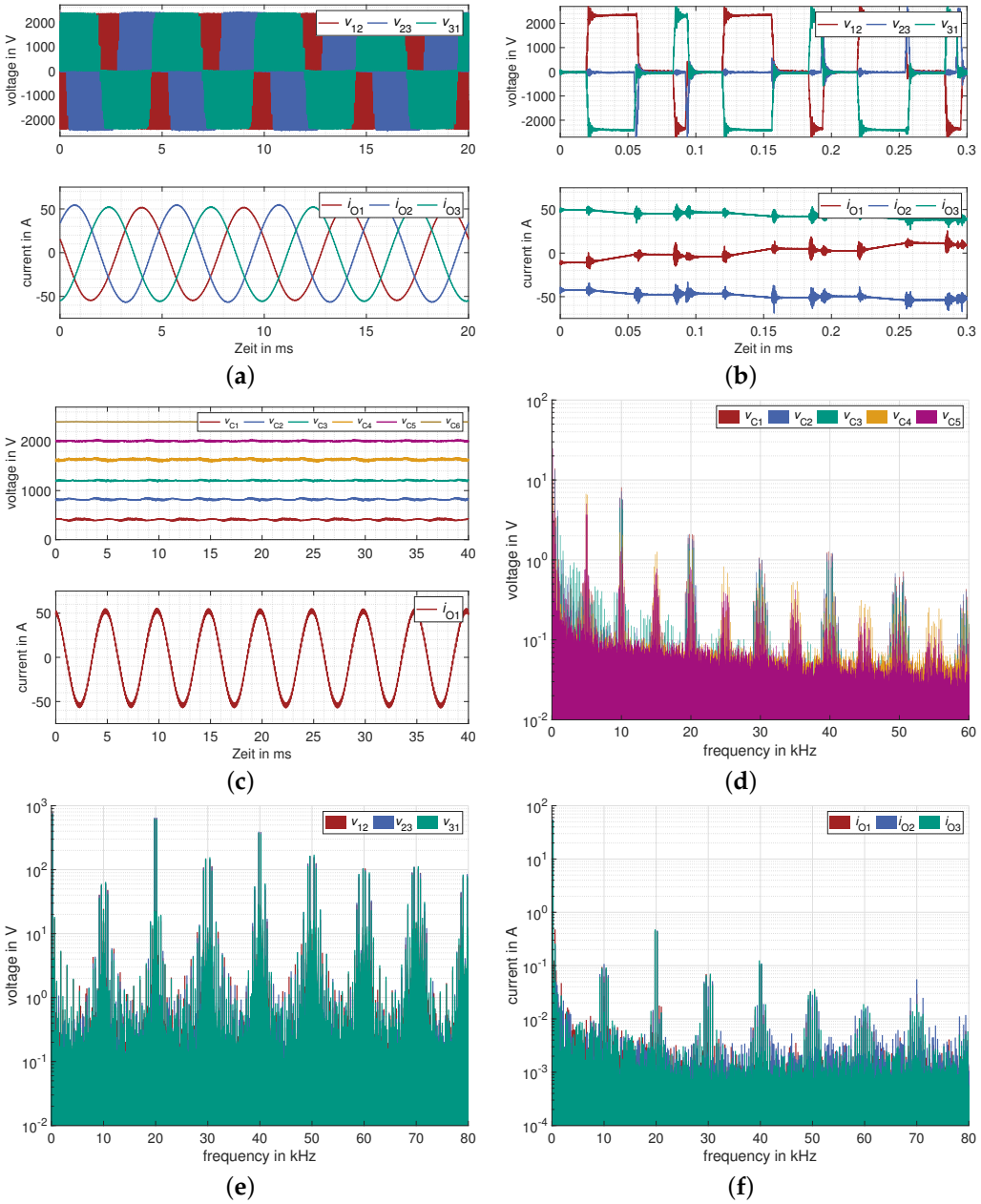


Figure 18. Measurement results at medium voltage with $V_{DC} = 2.4\,\text{kV}$ and 200 Hz output frequency. (**a**) Three-phase output voltage and output current waveforms. (**b**) Three-phase output voltage and output current waveforms. (**c**) Single-phase output current and capacitor voltages waveforms. (**d**) Frequency spectrum of the capacitor voltage waveforms. (**e**) Frequency spectrum of the output voltage waveforms. (**f**) Frequency spectrum of the output current waveforms.

5.3. Dynamic Measurements

The previous measurements were performed with a constant set-point of the output current controller and DC-link voltage. To validate the Q2O, dynamic measurements were made to verify the dynamic performance.

5.3.1. Steady-State Operation

To obtain a reference value for the dynamic measurements, the voltages of the flying capacitors are first measured for the steady-state operation. In Figure 19, the measurement results for an output current i_o of 100 A and a DC-link voltage of 2.4 kV are presented. The phase shift of the corresponding output currents can be seen in the capacitor voltage curves. The capacitor voltage waveforms for the individual phases look similar. The hardware variance of the components is noticeable here. As already discussed in Section 5.1.1, the commutation cells differ slightly in their characteristics. This also affects the comparison of the capacitor voltages of the different phases. Through the small characteristic variance, the different capacitor voltage curves on the same capacitor voltage levels occur.

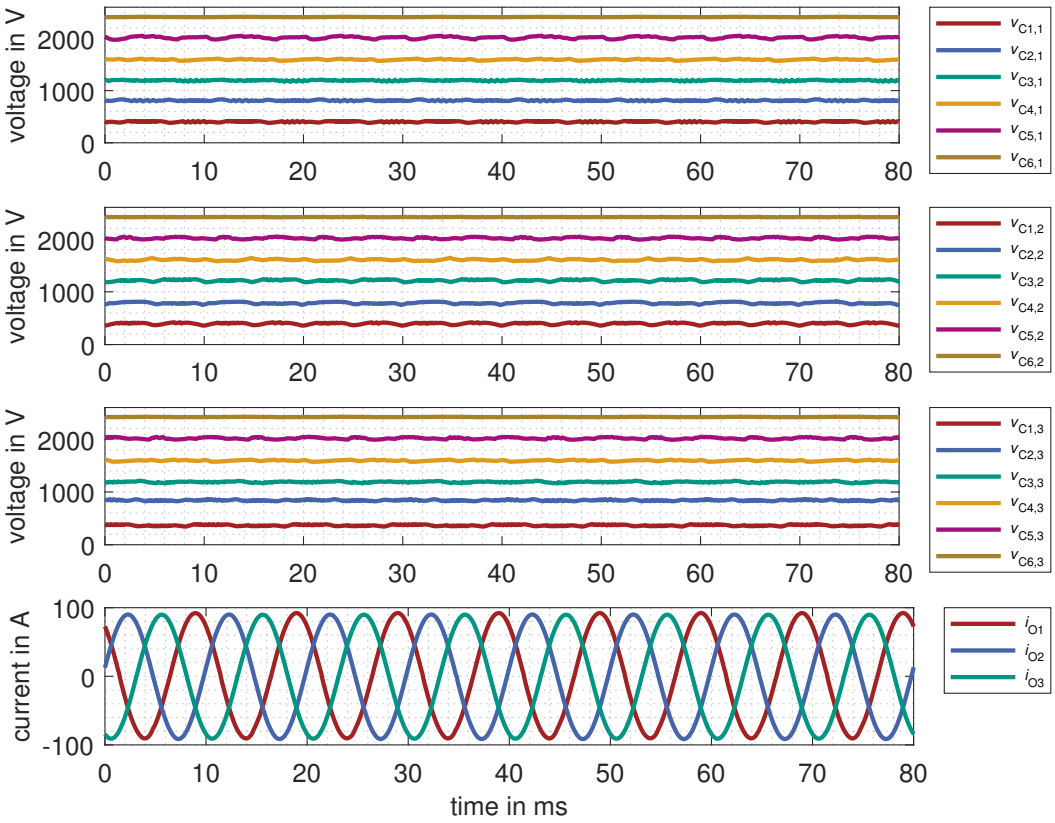


Figure 19. Steady-state measurement results at medium voltage with $V_{DC} = 2.4$ kV and 100 A.

5.3.2. Output Current Set Point Step

Even in a steady-state operation, an influence of the capacitor voltage was already noticeable [13], since the alternating current with constant amplitude cannot be compensated for by the balancing algorithm. For the balancing algorithms, an alternating current is already not a steady state, but a steady constant variation. In Figure 20, a measurement of a dynamic change of the set point for the output current is presented. The DC-link capacitor voltage waveform shows a slight voltage drop due to the higher output power. The DC power supply compensates for this with its own output dynamic, which cannot be influenced by the FCC. This voltage drop is not found in the other capacitor voltages. The balancing algorithm keeps all capacitor voltages stable within their voltage ranges. In this measurement, the direct relationship to the magnitude of the output current is evident in the maximum capacitor voltage variations. A dynamic load step is not a challenge for the Q2O.

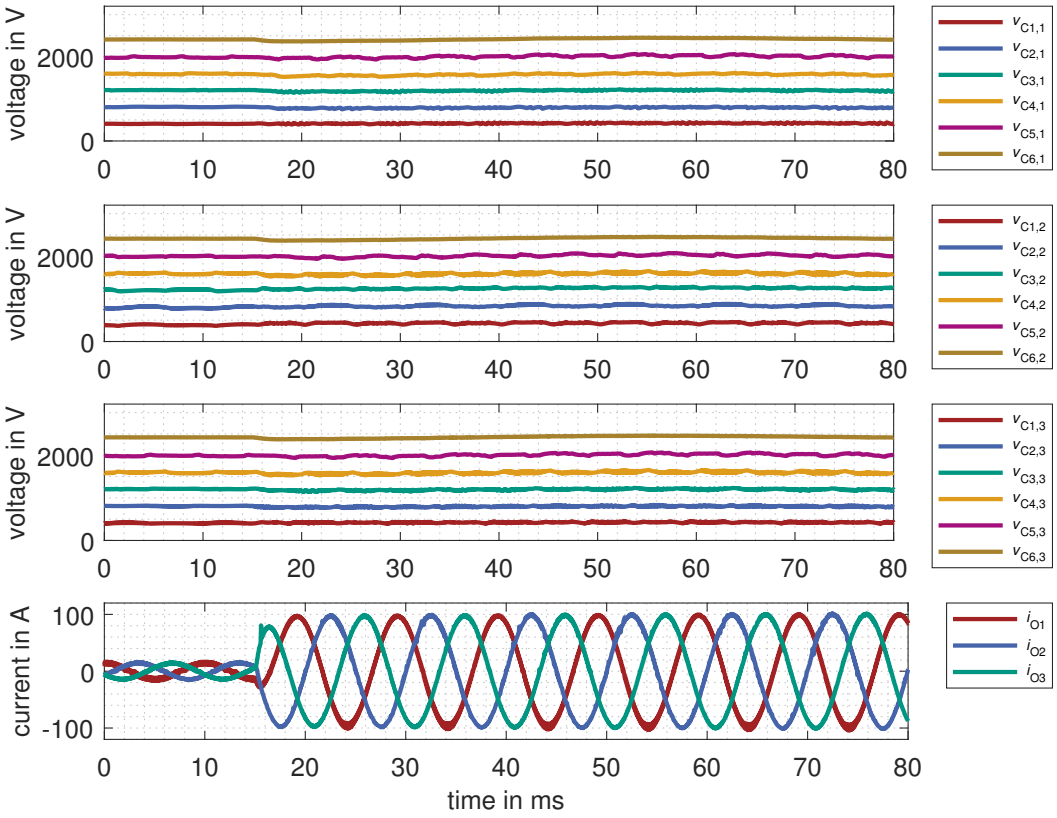


Figure 20. Output current set point step measurement results at medium voltage with $V_{DC} = 2.4\,kV$.

5.3.3. Voltage DC-Link Set Point Step

To date, only measurements with a constant DC voltage have been considered. In order to check whether the balancing algorithm in the Q2O is able to convert a change in the DC-link voltage into the respective capacitor voltages, the behavior in the case of a DC-link voltage step is analyzed. In Figure 21, the corresponding measurement results are shown. The DC-link voltage curve results from the voltage control of the DC power supply. The capacitor voltages follow the DC-link voltage proportionally and stay stable within their corresponding voltage range. The balancing algorithm is even able to follow the oscillations caused by the DC power supply. On the output current, the DC-link voltage change has no effect because the dynamic output current control compensates for it.

Thus, the balancing algorithm can correctly compensate for the DC-link voltage changes, assuming that the output current flow is sufficiently high to restore the capacitor voltages.

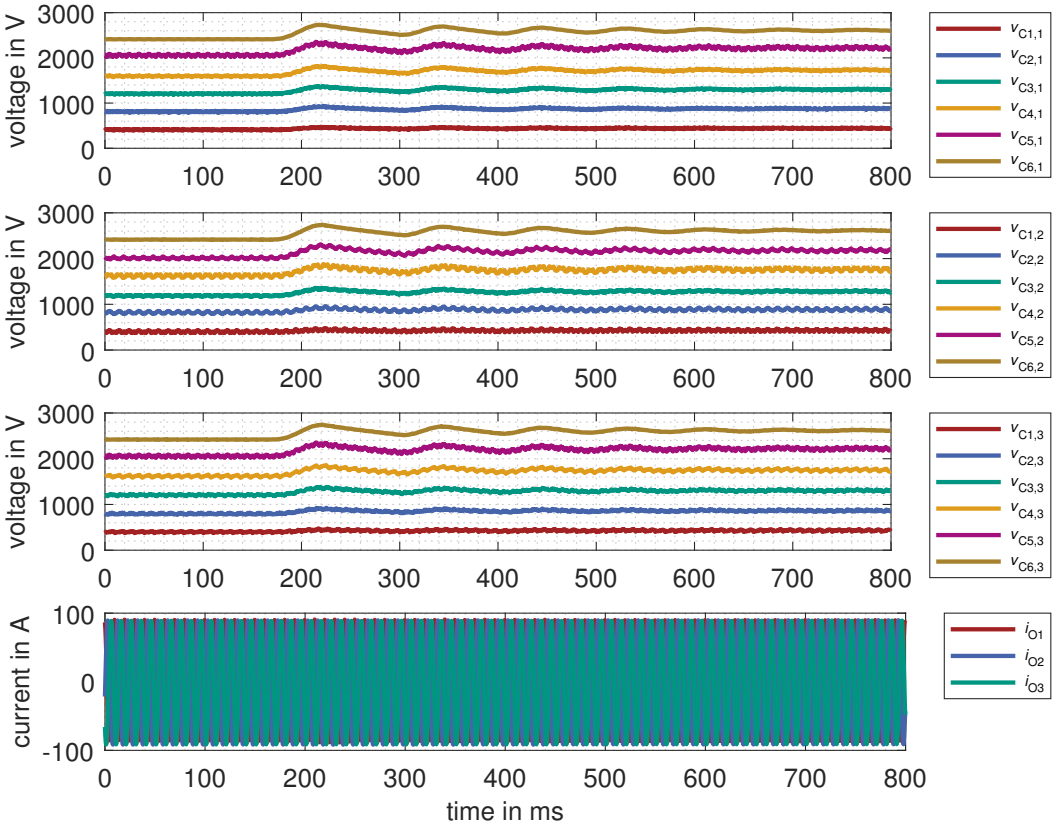


Figure 21. Voltage DC-link set point step measurement results at 100 A.

5.4. Efficiency Measurement

Efficiency is a measured variable that is important for all components in power applications. The focus of the full-scale prototype was never on optimizing efficiency. In the test setup, the efficiency was determined with a power meter. The DC active power P_{DC}, AC active power P_{AC}, and AC apparent power S_{AC} were measured.

Efficiency η_{con} is defined by Equation (4) in this measurement. Usually, the efficiency η_{con} is related to the AC active power P_{AC}, which is related to the AC apparent power S_{AC} in this test setup.

$$\eta_{con} = 1 - \frac{P_{DC} - P_{AC}}{S_{AC}} \tag{4}$$

The efficiency results are shown in Figure 22. Three different DC-link voltages were used for the measurements so that the influence of the switching losses, which are voltage-dependent, and the conduction losses, which are current-dependent, can be separated. It is clearly visible in the graphs that the switching losses are the dominant loss mechanism in the prototype. This can be seen at the measuring points with low output current at the different output frequencies. The peak efficiency also decreases with higher DC-link voltage. At 1200 V, the peak efficiency is 99.25%, at 1800 V the peak efficiency is 99.01% and at 2400 V it is 98.92%. In each of the measurements, the peak efficiency is at the peak value of the apparent power S_{AC}. The apparent output power does not increase as proportionally as the losses in the converter, which results in a slight drop in efficiency. The profile of the apparent power can be seen in Figure 22d. The graph shows the dependence of the apparent power on the output current and output frequency, which is shown here at a DC-link voltage of 2400 V. The converter can only generate a maximum amplitude of the output voltage depending on the DC-link voltage. At higher output frequencies, the maximum output current is, therefore, not reached because the voltage drop at the choke increases with the output frequency.

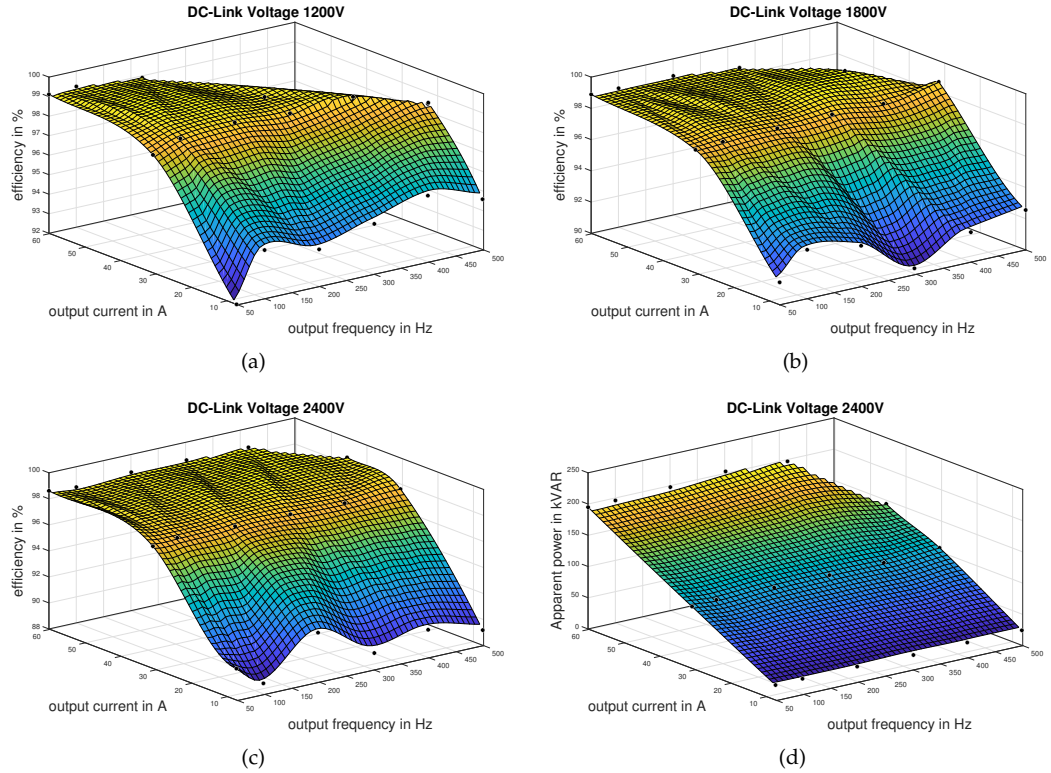


Figure 22. Efficiency measurement by different DC-link voltage set points. (**a**) Measurements results of the efficiency of the full-scale prototype by DC-link Voltage $V_{\mathrm{DC}} = 1.2\,\mathrm{kV}$. (**b**) Measurements results of the efficiency of the full-scale prototype by DC-link Voltage $V_{\mathrm{DC}} = 1.8\,\mathrm{kV}$. (**c**) Measurements results of the efficiency of the full-scale prototype by DC-link Voltage $V_{\mathrm{DC}} = 2.4\,\mathrm{kV}$. (**d**) Measurements results of the apparent power of the full-scale prototype by DC-link Voltage $V_{\mathrm{DC}} = 2.4\,\mathrm{kV}$.

6. Conclusions

This publication describes the main elements of the Q2O and its validation with a medium-voltage prototype. For validation, different measurements with low and medium voltages were performed. The analysis of the overvoltage behavior shows that a low overvoltage of 380 V is achieved at a DC-link voltage of 2.9 kV. In addition, a maximum $\mathrm{d}v/\mathrm{d}t$ of $3.596\,\mathrm{kV\,\mu s^{-1}}$ was achieved due to the short steps of the multilevel voltage, which significantly reduces the $\mathrm{d}v/\mathrm{d}t$ despite the fast-switching semiconductor.

For Q2O, an important element is the balancing of the capacitor voltages. Therefore, the comparison of the different methods of balancing algorithms for the three-phase operation was presented. It has been shown that the hardware prototype exhibits characteristics that were not so noticeable in previously published studies [13]. Thus, it obvious that to validate such a hardware-oriented algorithm, the appropriate hardware and the corresponding operation must be considered.

Further, the Q2O for the dynamic operation point variation was investigated and it showed that the balancing algorithms are also suitable for this operation. With the different experiments, it was shown that the FCC in combination with the Q2C is a usable option for medium-voltage applications.

Through the Q2O, the necessary capacitance values can significantly be reduced and, thus, the drawback of the FCC—the necessity of high capacitance values—can be compensated. At the same time, the overvoltage and $\mathrm{d}v/\mathrm{d}t$ are significantly reduced compared to a normal 2L VSC, resulting in lower stress of the load or the grid.

Furthermore, it was shown that an efficiency of about 99 % can be achieved for the FCC in the used mode of the Q2O.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	alternating current
APOD	alternative phase opposition disposition
DC	direct current
FCC	flying capacitor converter
Max	maximal value
MMC	modular multilevel converter
Mod	modulator—gate signal generation
MOSFET	metal oxide semiconductor field-effect transistor
Nom	nominal value
PEBB	power electronic building block
PD	phase disposition
Q2O	quasi-two-level operation
SiC	siliciumcarbid
SoC	system on chip
SY	balancing algorithm
THD	total harmonic distortion
VSC	voltage source converter
WTHD	weight total harmonic distortion with ω_i/ω_1
C_{Q2O}	capacity for Q2O
$\mathrm{d}v/\mathrm{d}t$	change of voltage
d_x	duty cycle of phase x
d_{xy}	duty cycle of phase x of PEBB y
G_{xy}	gate signal for phase x of PEBB y
$i_{\alpha,\beta}$	current in stator-fixed coordinate system
$i_{\mathrm{c}x}$	capacitor current
$i_{\mathrm{d},y}$	current in rotating coordinate system
$i_{\mathrm{O}x}$	output current of phase x
N	number of output voltage levels
t_{CC}	conduction time of one capacitor
t_c	changeover time
t_{m}	modulation time
t_{s}	semiconductor switching time
t_{p}	plateau time
t_{pi}	i-te plateau time
$t_{\mathrm{p,fix}}$	fixed plateau time
$t_{\mathrm{p,min}}$	minimal plateau time
$t_{\mathrm{p,max}}$	maximal plateau time
$v_{\alpha,\beta}$	voltage in stator-fixed coordinate system
$V_{\mathrm{c,nom},i}$	nominal capacitor voltage

$v_{c,i}$	actual capacitor voltage
$\Delta V_{c,max}$	permitted capacitor voltage ripple
v_{con}	converter output voltage
V_{dc}	DC-link voltage
$v_{d,y}$	voltage in rotating coordinate system
$V_{PEBB,nom}$	nominal commutation voltage
V_0	zero voltage component

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