Production Engineering
https://doi.org/10.1007/s11740-023-01200-y

PROCESSES

Enhanced chip analysis with computed tomography for estimation of chip segmentation frequency

Daniel Diaz Ocampo[1] · Jeanne Koch[1] · Germán González[2] · Frederik Zanger[2] · Michael Heizmann[1]

Received: 20 January 2023 / Accepted: 3 April 2023

Abstract
This work presents an enhancement of a method for analyzing metallic chips produced during turning processes in order to estimate the chip segmentation frequency. Therefore, the resulting 3D image of a computer tomography scan of the chip can be transformed virtually into a straight chip by describing the course of the chip in three-dimensional space by a trajectory. Along this trajectory, the chip point cloud is sliced in thin layers which can be transformed to a straight chip. To estimate the segment rate, the height course describing the segmentation of the chip is extracted on the serrated side of the point cloud by means of nearest neighbor interpolation. The resulting signals are compared with the measurements of the chip surface using an optical microscope, whereby only two straight chips could be analyzed. The comparison shows a nearly perfect match between the two signals and is confirmed by a Pearson correlation coefficient of over 86% for both signals. Furthermore, a statistical comparison with the acoustic emissions of the turning process reveals satisfying similarities for the chip segmentation frequency with respect to the compression factor.

Keywords Chip segmentation frequency · Acoustic emission · Turning · Ti-6Al-4V

1 Introduction

When machining titanium alloys, due to the formations of adiabatic shear bands caused by the prevalence of thermal softening over strain hardening, sawtooth form chips are produced [1]. The phenomenon of the sawtooth like chip formation is known as chip segmentation. The morphology of the chips has a significant influence on the thermomechanical behavior at the interface between the workpiece and the tool. This limits the material removal rates and affects the dynamic behavior of the system, cutting forces, chip-tool interface temperature, as well as the microstructure of the machined surface [2]. In order to increase productivity and tool life in machining of titanium alloys, it is necessary to study the mechanics of chip segmentation and its impact on machinability, as well as on tool life [3].

✉ Daniel Diaz Ocampo
daniel.diaz-ocampo@kit.edu

[1] Institute of Industrial Information Technology, Karlsruhe Institute of Technology, Hertzstraße 16, 76187 Karlsruhe, Germany

[2] wbk Institute of Production Science, Karlsruhe Institute of Technology, Kaiserstr. 12, 76131 Karlsruhe, Germany

As presented by Komanduri [4], the segment rate during the turning process strongly depends on the process parameters, increasing with cutting speed and decreasing with feed. Zhang and Choi [5] presented different finite element (FE) approaches for simulating the orthogonal cutting of Ti-6Al-4V. The authors concluded that a pure Langrangian formulation delivers the closest chip morphology to the experiments, compared with other FE approaches, as arbitrary Lagrangian–Eulerian and coupled Eulerian-Lagrangian. Taking into account the possibility of a strain softening phenomenon occurring from a given temperature and deformation level, as presented by Komanduri and Hou [6], new material behavior laws have been developed for the 2D-FE-modelling of the crack initiation and propagation processes, which lead to the serrated chip geometry [7]. Acoustic Emission (AE) measurements were carried out by Zanger et al. [8], and the spectral information of the AE measurements were correlated with the effects on the workpiece surface state after linear orthogonal cutting experiments of Ti-6Al-4V. For validation of the simultation results and AE measurements, an experimental analysis of the chips after the machining process is necessary. The chips from the orthogonal cutting process can be measured directly by optical measurements, as presented in Nguyen et al. [9]. However, the geometry

Published online: 24 April 2023

of the chips after the turning process is much more complex, due to the multidimensional angle of curvature. Signal processing of acoustic emission can be used to capture the chip segmentation frequency as strategy for process and tool condition monitoring, due to its high sensitivity and diverse information contained in the broad MHz frequency band [10].

Computer Tomography (CT) can be used to determine the geometry of the chips precisely. Devotta et al. [11] used CT for the characterization of the chip shape obtained from 2D orthogonal turning experiments of AISI 1045 in order to validate 3D-FE simulations, using the chip curl as an evaluation criterion. However, it remains a challenge to obtain reliable information on chip segmentation frequency from CT measurements.

In this work, a method for the automatic extraction of the chip geometry and segmentation from CT-scans of Ti-6Al-4V chips is presented. First the relations between chip analysis and acoustic emission measurements is shown. Next, several steps of preprocessing are introduced before a trajectory which describes the course of the chip can be calculated. Then it is presented how the, in most cases helical chip, can be transformed into a straight chip, whereby a signal can be extracted for the analysis of the segment distances. Finally, the results are compared with optical measurements and with the measurements of acoustic emission.

2 Methods

The presented method is an enhancement of the CT-analysis method previously published in [12]. For a better understanding, the main steps of the method will be described in brief.

The chip segmentation frequency

$$f_{\mathrm{AE}} = \frac{v_{\mathrm{c}}}{\Delta_{\mathrm{AE}}} \tag{1}$$

is the frequency over time, at which the individual segments that build up one chip, separate from the workpiece [10]. This frequency can be measured by using sensors for acoustic emission [13]. The distance covered by the worktool from one produced segment to the next one in the direction of primary motion is named segmentation distance Δ_{AE} in this work. From this distance the chip segmentation frequency can be calculated, taking into account the cutting speed v_{c}. In comparison, on a produced chip the instantaneous segment rate

$$f_{\mathrm{s}} = \frac{1}{\Delta_{\mathrm{s}}} \tag{2}$$

can be measured, which is a frequency over space, as it is the inverse of the distance of a single segment in a sawtooth chip. The distance between two segments in the chip is named segment distance in this work. In Fig. 1, the geometrical relation between the segment distance Δ_{s} and the segmentation distance Δ_{AE} during the chip formation is shown schematically.

It can be seen that the distance and thus the frequency measured by acoustic sensors, respectively at a chip, are not identical and depend on the cutting parameters. Nevertheless, it is possible to get information about the chip segmentation frequency by measuring the segment rate, since they are strongly correlated by taking a compression factor

$$f_{\mathrm{AE}} = \lambda_{\mathrm{chip}} \cdot v_{\mathrm{c}} \cdot f_{\mathrm{s}} \quad \text{with} \quad \lambda_{\mathrm{chip}} = \frac{l_{\mathrm{chip}}}{l_0} \tag{3}$$

into account. To estimate the average compression factor for a single cut, the length of a produced chip l_{chip} and the length of the cut to extract the chip from the workpiece l_0, can be taken. Due to the fact that in one cut several chips are produced which break stochastically, l_0 is unknown. Assuming that the volume V_{chip} of the chip is constant and the material cannot be compressed, the original length l_0 of a produced chip can be estimated by the machined cutting area A_0 and the volume of the chip, according to

$$V_{\mathrm{chip}} = A_0 \cdot l_0 \,. \tag{4}$$

The cutting area, which is also the sectional area of the uncut chip, can be calculated analytically integrating the intersection of the surface projection of the cutting edge with the projection of the edge position at the previous revolution of the edge. This previous revolution is shifted back by the distance value of the feed F, with the height equal to the depth of cut a_{p}, as explained in [14]. In this work, the capitalized F

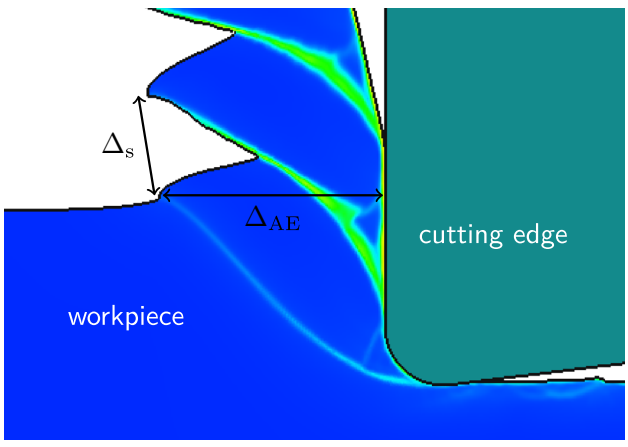


Fig. 1 Schematic relation between the measured variables, segment distance Δ_{s} and segmentation distance Δ_{AE}, during chip formation

is used as symbol for feed, which is unusual but avoids confusion between feed and frequencies. The acoustic frequency

$$f_{\mathrm{AE}} = \underbrace{\frac{A_0 l_{\mathrm{chip}}}{V_{\mathrm{chip}}}}_{=\lambda_{\mathrm{chip}}} \cdot \frac{v_{\mathrm{c}}}{\Delta_{\mathrm{s}}} \tag{5}$$

can be estimated from the segment distance by combining the Eqs. (2), (3) and (4). To determine the length and volume of the chip and the segment distances Δ_s, a CT-scan of a chip can be used. The purpose of this method is to transform and unscrew the, in most cases helical chip, virtually to a straight chip, since this is not possible with the real chip due to its brittleness.

2.1 Preprocessing

Before the transformation of the chip, several preprocessing steps have to be done. From the CT-measurement, a three-dimensional matrix $\mathbf{C}_g$ with gray scale values of dimension $I \times J \times K$ is given, which represents the intensity in the three-dimensional space containing the chip and other objects like the mounting structure or glue. Next, a binarization of the matrix entries has to be done to classify them into the two groups "chip" (1) and "background" (0). Since the chip material is titanium alloy, the values in the CT-scan, respectively in $\mathbf{C}_g$, are much higher at points representing the chip than at points representing other materials like e.g. the mounting structure. Thus, a simple thresholding is sufficient to obtain a binary matrix $\mathbf{C}_b$, which represents the chip but no other materials. To estimate the threshold with which the points are classified, a k-means algorithm is used, as described in [15]. Since in some cases single points were incorrectly classified as chip, every point which is not part of the largest volume is corrected as "background". The largest volume can be calculated by a connected-component labeling algorithm, as described in [16]. After binarization, the binary matrix can be transformed into a point cloud $\mathbf{P} = \left[\mathbf{p}_1, \ldots, \mathbf{p}_N\right]$ of dimension $3 \times N$ with $\mathbf{p}_n = \left[i \cdot \Delta_x, j \cdot \Delta_y, k \cdot \Delta_z\right]^{\mathrm{T}} = \left[x_n, y_n, z_n\right]^{\mathrm{T}}$ in the three-dimensional Euclidean space. Thereby, each point of the binary matrix that equals one is saved and transformed as follows, with Δ_x, Δ_y and Δ_z as the pixel size along the corresponding coordinate axis. Figure 2a shows an example of the point cloud of a CT-scan of a chip. Here, the chip has a helical shape, like most chips of Ti-6Al-4V generated during a turning process, however straight chips exist depending on cutting parameters.

For the estimation of the compression factor in Eq. (5), the volume

$$V_{\mathrm{chip}} = \Delta_x \cdot \Delta_y \cdot \Delta_z \cdot N \tag{6}$$

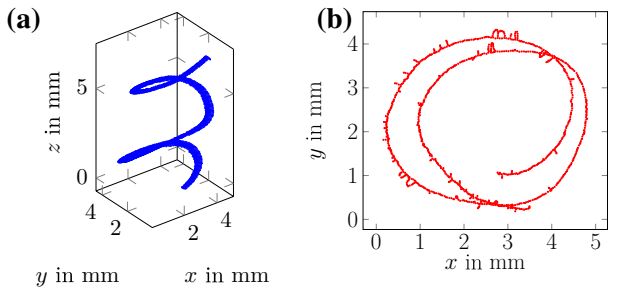


Fig. 2 Example of a chip. **a** Example of a chip point cloud. **b** *xy*-view of a chip skeleton with "barbs"

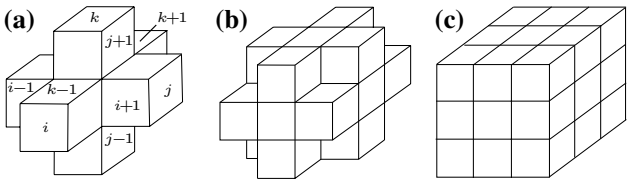


Fig. 3 The three connectivity types in the three-dimensional cubic lattice. **a** 6-neighborhood: the neighbors are connected by the faces of the voxel. **b** 18-neighborhood: the neighbors are connected by the faces and the edges of the voxel. **c** 26-neighborhood: the neighbors are connected via the faces, the edges and the vertices of the voxel. Based on [18]

is needed. It can be calculated easily at this point by multiplying the voxel volume with the amount of points in the point cloud.

2.1.1 Chip trajectory

For the analysis of the chip, a trajectory is needed, which describes the course of the chip in the three-dimensional space. In the method presented previously, the centers of the two-dimensional x-y-submatrices were used for the calculation of the trajectory. This may lead to an erroneous calculation of the trajectory if the chip has multiple parts in one horizontal plane. If the chip has been scanned while the start and endpoints are not on the topmost, respectively lowermost planes, this approach also fails. To solve this problem a method called skeletonization [17], based on mathematical morphology operations, can be used. The new method uses the erosion to successively scale down any volume until there are just lines left. In Fig. 2b the skeleton of the example chip is shown.

The erosion is an operator which uses a structural element to probe a binary matrix. If the structural element fits completely in the volume described by the binary matrix, the operator returns a "1", respectively a "0" otherwise. The used structural element presents a connectivity of 26-neighbors, as shown in Fig. 3c, based on two previous steps, where the

neighbours are connected by the faces, like in Fig. 3a, the edges, like in Fig. 3b and finally the vertices.

As can be seen in Fig. 2b, after the skeletonization, so called "barbs" exist, which are small contours from the main line to the chip surface. A minimum length of $\frac{1\text{mm}}{\Delta_x}$ for the contours can be requested to speed up the following step and delete most of the barbs.

Now, discrete three-dimensional points from which the trajectory can be calculated exist. However, in these points, loops or long barbs may exist that need to be filtered. Furthermore, at this point it is unclear where the trajectory starts, where it ends and how the points have to be sorted. For this reason, the skeleton point cloud can be interpreted as a graph, where the points are the nodes and the distances between the points are the edges. Then a shortest pathfinding algorithm can be applied to get the full course of the chip without loops or barbs.

A graph with edges between all points would lead to the direct connection between start and endpoint. To avoid this, the edges are only set to the direct neighbors of the 26-neighborhood of an arbitrary point. Since two voxels have a distance of 1 in the $I \times J \times K$-space of the binary matrix, the neighboring points are within a radius of $r = \sqrt{3}$. The search for these points is computed on the skeleton point cloud with a *kd-tree* [19], that splits data points spatially into three-dimensional subspaces along the axis of the coordinates. The shortest paths between every pair of points can be calculated by using the *Dijkstra algorithm* [20]. A good basis for the trajectory is the longest path of all shortest paths, since this path contains the maximum number of points in the skeleton without any loops.

The resulting point cloud is a subset of the chip point cloud $\mathbf{P}$. However, the points are not smooth, wherefore they need to be filtered before transforming the chip along this trajectory. They have to be smoothed, since too strong changes between two steps next to each other are undesirable in the following spatial transform. Therefore, a Savitzky-Golay filter is used, as described in [21]. An example of a smoothed trajectory point cloud $\mathbf{T} = \left[\mathbf{t}_1, \ldots, \mathbf{t}_M\right]$ of dimension $3 \times M$ with $\mathbf{t}_m = \left[x_m, y_m, z_m\right]^{\mathrm{T}}$ of a chip, is shown in Fig. 4.

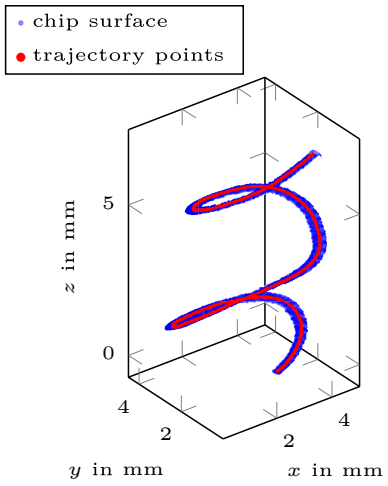


Fig. 4 Smoothed trajectory of a chip

2.1.2 Chip surface

For later tasks it is not necessary to work with the full chip, since the chip surface is sufficient, especially to reduce the number of data points and accelerate the following computations. Therefore the erosion, as described in [17], can be used. The erosion removes a point from the point cloud if one neighbor, in comparison with the shifted kernel, is not part of the point cloud. The three-dimensional erosion of the binary matrix with a kernel is computed to remove the outmost points. To obtain the surface, the difference between the eroded matrix and the original matrix is calculated. As a kernel, different binary forms can be used, which are all within a cube with an edge length of three, as shown in Fig. 3. The difference between the kernels is given by which kind of neighborhood they return, depending on the form. There are three suitable kernels, which provide the neighborhood of 6, 18 or 26, to compute the surface. Investigations have shown that the kernels for the neighborhood of 18 and 26 return many more points but lead to noisy effects in later steps of the method, so the kernel for the neighborhood of 6 is sufficient. The resulting surface point cloud $\mathbf{S}$ is a subset of the chip point cloud $\mathbf{P}$.

2.2 Chip transform

In the next step, the surface of the chip has to be transformed into a straight form to be analyzed. For this transform, the surface of the chip has to be "sliced" into thin layers, which can be rearranged as a new straight chip, as described in [12]. The layers, containing a certain set of points, are defined and stretched orthogonal to the trajectory tangent. For each of the M trajectory points $\mathbf{t}_m = \left[x_m, y_m, z_m\right]^{\mathrm{T}}$, the tangent of the trajectory is given by

$$\mathbf{n}_m = \frac{\mathbf{t}_{m+1} - \mathbf{t}_m}{\|\mathbf{t}_{m+1} - \mathbf{t}_m\|}, \tag{7}$$

which can be used as the normal vector of a plane whereby two of these planes limit the layers. Consequently, the points given by the surface point cloud $\mathbf{S}$ must fulfill the three conditions

$$\left(\mathbf{S} - \mathbf{t}_m\right)^{\mathrm{T}} \mathbf{n}_m \geq 0, \tag{8}$$

$$\left(\mathbf{S}-\mathbf{t}_{m+1}\right)^{\mathrm{T}}\mathbf{n}_{m+1}<0, \tag{9}$$

$$\text{and} \quad \|\mathbf{S}-\mathbf{t}_m\| \leq r_{\max,m} \tag{10}$$

to be classified as part of the layer $\mathbf{S}_m$, defined by the two planes by Eqs. (8) and (9) going through the trajectory points $\mathbf{t}_m$ and $\mathbf{t}_{m+1}$. Thus, every layer $\mathbf{S}_m$ is a subset of $\mathbf{S}$. The last condition, given by Eq. (10), prevents points from other chip turns from being included. For this, a maximum radius $r_{\max,m}$ is defined, which describes the largest possible contiguous surface of each layer. This radius is calculated for every layer iteratively by increasing it until the set of points no longer increases. In order to calculate the maximum radius of a layer $\mathbf{S}_m$, the layer of the full point cloud $\mathbf{P}_m$ is needed and can be calculated using the same conditions given by Eqs. (8) and (9), as for the surface point cloud $\mathbf{S}$.

Then the surface of the chip is straightened by spatially transforming each layer. To do this, each point of a layer $\mathbf{S}_m$ is transformed by

$$\mathbf{S}'_m = \mathbf{R}_m\left(\mathbf{S}_m-\mathbf{t}_m\right)+\mathbf{d}_m. \tag{11}$$

The rotation matrix

$$\mathbf{R}_m = \left[\mathbf{e}_{m,1},\ \mathbf{e}_{m,2},\ \mathbf{n}_m\right]^{\mathrm{T}}, \tag{12}$$

with the two unit vectors $\mathbf{e}_{m,1}$ and $\mathbf{e}_{m,2}$ of length $\|\mathbf{e}_{m,1/2}\|=1$, removes the individual rotation of the layers caused by the helical form of the chip. For the first layer, the unit vectors can be selected randomly, whereby both vectors must be orthogonal to each other and to the first normal vector. For the next layers, both unit vectors are calculated with

$$\mathbf{e}_{m,2} = \frac{\tilde{\mathbf{e}}_{m,2}}{\|\tilde{\mathbf{e}}_{m,2}\|} \quad \text{with} \quad \tilde{\mathbf{e}}_{m,2} = \mathbf{n}_m \times \mathbf{e}_{1,m-1} \tag{13}$$

$$\text{and} \quad \mathbf{e}_{m,1} = \mathbf{e}_{m,2} \times \mathbf{n}_m\,, \tag{14}$$

where the cross product $\times$ delivers a vector which is orthogonal to both of the others.

The translation vector $\mathbf{d}_m$ shifts each layer in z'-direction to the end of the previous layer. The first layer is not shifted and thus, the first translation vector is given by $\mathbf{d}_1 = \left[0,0,0\right]^{\mathrm{T}}$. For the next layers, the translation vector results from the sum of the distances between the previous trajectory points

$$\mathbf{d}_m = \begin{bmatrix} 0 \\ 0 \\ \sum_{l=2}^{m} \|\mathbf{t}_{l+1}-\mathbf{t}_l\| \end{bmatrix}. \tag{15}$$

Finally, all points of the subsets $\mathbf{S}'_m$ written into a matrix produce the stretched point cloud $\mathbf{S}' = \left[\mathbf{S}'_1,\ldots,\mathbf{S}'_M\right]$. After this transformation, the virtual chip is normally screwed as it can be seen in Fig. 5a.

So the chip has to be descrewed by estimating the outmost corner points of every layer, to rotate each layer of the chip. Therefore, the extreme values $x'_{m,min}$ and $x'_{m,max}$ in x-direction, and $y'_{m,min}$ and $y'_{m,max}$ in y-direction are taken for each layer. Then, the Euclidean distance between each combinations of two extreme value is calculated. The outmost corner points $\boldsymbol{\kappa}_{1,m}$ and $\boldsymbol{\kappa}_{2,m}$ are given by the two pairs of extreme values, with the largest distance to each other. Once the corner points of the first layer have been determined, the succeeding corner points must be classified in the same area as the previous ones, and so on for the next layer. The condition

$$\begin{aligned}&\left\|\left[\boldsymbol{\kappa}_{1,m}-\boldsymbol{\kappa}_{1,m-1}\middle|\boldsymbol{\kappa}_{2,m}-\boldsymbol{\kappa}_{2,m-1}\right]\right\| \\ &\quad\leq \left\|\left[\boldsymbol{\kappa}_{2,m}-\boldsymbol{\kappa}_{1,m-1}\middle|\boldsymbol{\kappa}_{1,m}-\boldsymbol{\kappa}_{2,m-1}\right]\right\|\end{aligned} \tag{16}$$

applies to the layer $\mathbf{S}_m$ and ensures that the corners match with the previous ones. The direction vector of each layer is given by the two corners and the direction angle results from its polar angle $\vartheta_m = \measuredangle(\boldsymbol{\kappa}_{1,m}-\boldsymbol{\kappa}_{2,m})$. The course of the angle is then filtered with a moving average filter to prevent discontinuities, respectively too large changes between two points next to each other. The rotation around the z-axis of each layer can be realized by multiplying the points of the layer with a rotation Matrix

$$\mathbf{S}''_m = \begin{bmatrix} \cos\vartheta_m & -\sin\vartheta_m & 0 \\ \sin\vartheta_m & \cos\vartheta_m & 0 \\ 0 & 0 & 1 \end{bmatrix} \cdot \mathbf{S}'_m. \tag{17}$$

All layers are finally combined into the point cloud $\mathbf{S}'' = \left[\mathbf{S}''_1,\cdots,\mathbf{S}''_M\right]$. Thus, the transformed chip is straight and no longer has any rotation, as can be seen in Fig. 5b.

In a next step, it is necessary to distinguish between the serrated side and the smooth side of the chip, since the segment rate can only be measured at the serrated side. Therefore, the corner points are calculated again for the descrewed chip, as described previously, since the calculation of the maxima is now more robust because of the descrewing. The points of each layer are now centered to the coordinate origin by substracting its mean value in x

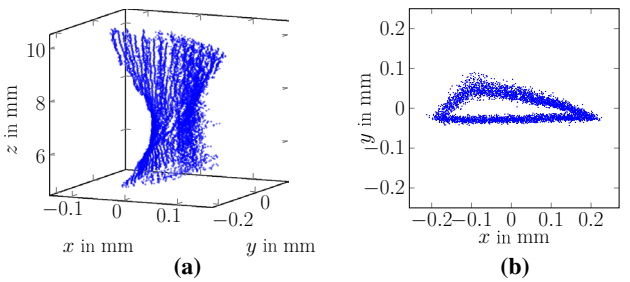


Fig. 5 Examples of the surface chip point clouds before and after descrewing

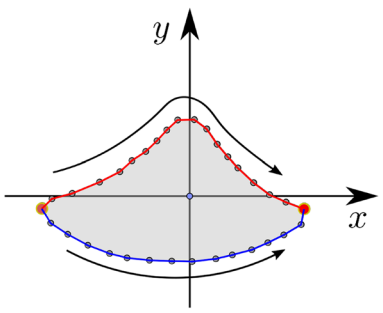


Fig. 6 Usual paths of the serrated side (depicted in red) and the smooth side (depicted in blue)

and y-direction and the points are classified by their polar angle. In Fig. 6a schematic example is shown.

After the classification has been done for every single layer, two separate subsets of point clouds $\mathbf{S}''_{\mathrm{se}}$ and $\mathbf{S}''_{\mathrm{sm}}$ are obtained, whereat it has to be decided which side is the smooth one and which side is the serrated one. Since the segments lead to a higher variation of the points in y-direction on the serrated side, the variance in y-direction can be taken as decision feature. Now a point cloud $\mathbf{S}''_{\mathrm{se}} = \left[\mathbf{p}'_1, \ldots, \mathbf{p}'_R\right]$ exists, which describes the serrated surface of the straightened chip, with which the segment rate can be analyzed.

2.3 Segment rate measurement

To analyze the segment rate, a signal has to be extracted which describes the segments with a good quality. However, the serrated surface point cloud does not have an equidistant grid after the transformation. For an optimal signal-to-noise ratio, the height course s should follow the segment peaks of the chip, which is a path along the z-axis, where the offset of the points reaches its maximum in the y-direction.

In a first step, the location of the height signal on the x-axis x_{sig} has to be estimated. Therefore, the values of the point cloud are subdivided into V bins along the x-axis, and the sum of the absolute y-values is calculated. The best signal is given where this feature has its maximum

$$x_{\mathrm{sig}} = x_v \mid \arg\max_v \left(\sum_{l=1}^{L} |y'_l| \right), \tag{18}$$

where $\mathbf{S}''_{\mathrm{se},v}$ is the binned subset of the serrated side with L points. The maximum of the feature is influenced by two properties of the sub point clouds. The first one is the offset, while a higher offset leads to a higher feature, and the second one is the number of points which ensures a better approximation of the signal at chip formation.

In the second step, an equally spaced signal s along the z-axis has to be resampled between the maxima and the minima of the chip in the z-direction with the fixed value x_{sig}. For each sampling point, the y-value of the point in the serrated side point cloud is taken as signal value, which has the nearest point in (x, z)-space to the sample point

$$s[z] = y'_r \mid \arg\min_r \left(\left\| \begin{bmatrix} x'_r \\ z'_r \end{bmatrix} - \begin{bmatrix} x_{\mathrm{sig}} \\ z \end{bmatrix} \right\| \right). \tag{19}$$

An example of the resulting signal and the original serrated side point cloud can be seen in Fig. 7.

3 Results

To validate the CT-method, it can be compared with other methods for chip analysis or with the acoustic emission. Therefore, longitudinal turning experiments with Ti-6Al-4V have been carried out by varying the feed ($F = [0.1;0.2;0.3]\,\mathrm{mm/rev}$), while all the other cutting parameters and the tool geometry were kept constant ($v_{\mathrm{c}} = 200\mathrm{m/min}, a_{\mathrm{p}} = 0.15\mathrm{mm}$). Process parameters feed F and depth of cut a_{p} were set according to the recommendation of the tool manufacturer. The cutting speed was increased up to 2.5 times the recommended value $v_{\mathrm{c}} = 80\mathrm{m/min}$, to obtain tool wear faster in order to analyze its effect on the chip morphology and the acoustic emission signals. The acoustic emissions of this experiments were recorded with a structure borne sensor, and the chip segmentation frequency has been analyzed, as described in [13]. The chips were analyzed using both the CT method and an optical microscope.

3.1 Optical comparison

At the optical method, a photography of the chip surface is created with an optical confocal microscope. To get the chip segmentation, a path is set manually over the measured surface photography and a signal along this path is extracted. The disadvantage of the optical method is that only straight chips can be analyzed, which is not the common form of the chips, while most chips have a helical

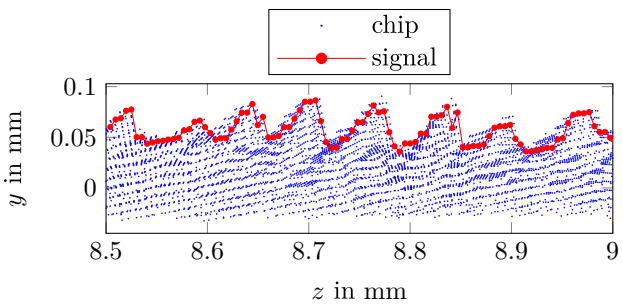


Fig. 7 Example section of a chip with its height signal depicted in red

form. Two of the chips, produced in the experiments, have a and can be analyzed with the optical microscope, too.

3.1.1 Direct comparison

After simple preprocessing, both signals can be compared. Since both methods deliver signals with varying offsets, those offsets have to be calculated by using, for example a Hanning window, as described in [22], which is subtracted from the signals. Figure 8 shows the result of one example chip.

In this figure, only the part where the signals match is shown for a better representation. The signal from the CT-method is about two to four times longer since here the whole chip can be analyzed. The region where the signals describe the same sector of the chip can be found by maximizing the Pearson correlation coefficient, described in [23], which delivers a measure in percent of how good the signals fit as well. The signals of the CT-method and the optical method are quite similar, which is also confirmed by the Pearson correlation coefficients. Merely at single points like at $z \approx 0.5$, the signals differ, but in most cases the signal from the CT-method is identical with the microscope signal. It is obvious that the signal of the CT-method is not worse, or even better, than the signal from the microscope. To get a qualitative feature of the comparison, the Pearson correlation coefficient between both signals can be taken. Since the signals have a different number of sample points at the x-axis, the signal from the CT-method has to be upsampled for the calculation of the correlation coefficient. For the two possible chips the signals match to 88 % respectively 86 %. The signals from other helical chips have been analyzed, but since the transformation in the CT-method is too strong, the microscope-signals can not be registered.

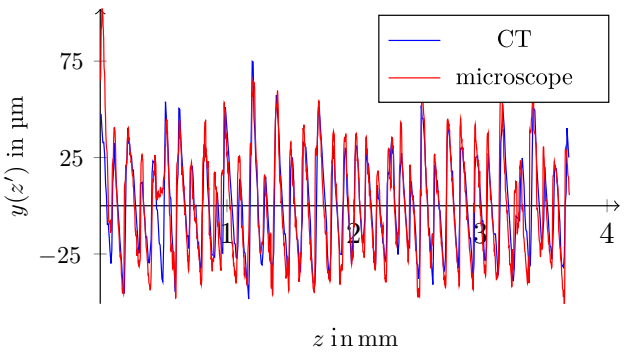
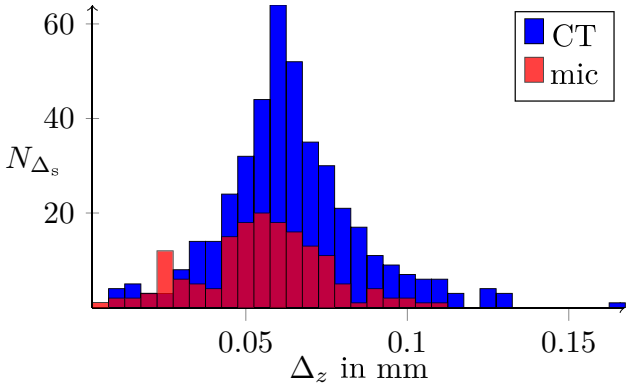
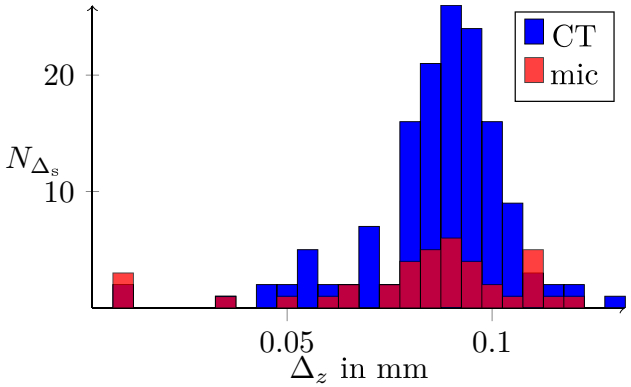


Fig. 8 Comparison of the chip signals extracted from the optical measurements (red) and the CT-method (blue)



(a) Histograms for $F = 0.1\,\mathrm{mm/rev.}$



(b) Histograms for $F = 0.3\,\mathrm{mm/rev.}$

Fig. 9 Comparison of the chip signals extracted from the CT-method and the optical measurement

3.1.2 Statistical comparison

Furthermore, it is possible to compare the statistics of the signals. This means that a histogram of the segment distances from the signals of both methods is computed and compared. For the computation of the histogram, the zero crossing rate has to be calculated, wherefore the signals have to be zero-mean, as described before [13]. Especially if the chip form is helical, this is the only way to validate the data with an optical measurement. Then, different chips from the same process can be used to get segmentation signals with the microscope.

In Fig. 9, the statistics of the segment distances, estimated by the CT-method, respectively the microscope, are shown. It can be seen that in the first examples, the statistics are quite similar. As described before, the CT-method is able to analyze the whole chip, while with optical measurement this does not work. This is the reason why, as it can be seen in Fig. 9b, the law of large numbers is not fullfilled for the microscope. If there are enough segments, like in most experiments, both statistics have a good match, whereby in some cases the CT-method

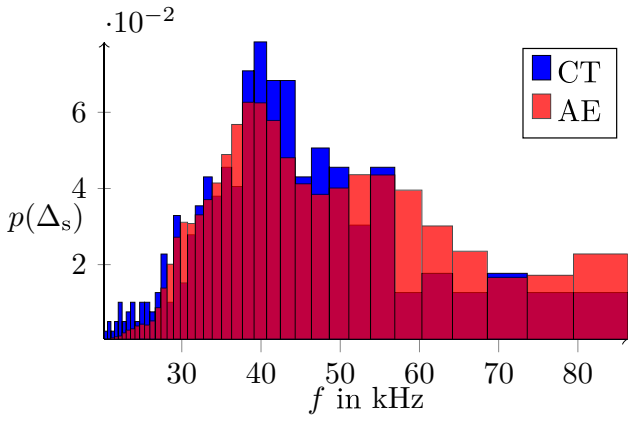


Fig. 10 Statistical comparison of the chip signal with acoustic emission by zero crossing method of process with $F = 0.1\text{mm/rev}$

provides higher values, which can be explained by the spatial transformation. In one case, a second peak appears in the CT-histogram, which is caused from a region in the chip with no distinct segmentation, so the zero crossing rate delivers untypical results.

3.2 Comparison with acoustic emission

The main objective is to get knowledge of how good the analysis of acoustic emissions works to characterize the turning process. So, it is possible to compare the statistics of the CT-method with the statistics of the acoustic emission. From the acoustic emission the chip segmentation frequency is obtained, hence the segment rate, obtained from the CT-method, has to be transformed. This can be done with Eq. (5). Since the histogram from the acoustic emission can be calculated by the whole process, the number of estimated segments is several orders higher than the number of estimated segments from the CT-method. For this reason, the histograms are normalized so that the sum of all bins equals one, and they can be interpreted as the probability density of the chip segmentation frequency. In Fig. 10, the comparison for the same helical chip, shown in Fig. 9a, is shown.

As it can be seen, the statistics of the CT-method and the statistics of the acoustic emission match really good, as well as the estimation of the compression factor λ_{chip} works. The experiments have shown that the compression depends on the process parameters and varies in the tested parameter sets between $\lambda_{\text{chip}} = 0.7$ and $\lambda_{\text{chip}} = 1.03$. Additionally, the compression compensates partly the change of the segment rate from the varying feed.

4 Conclusion

The enhancement of a method for analyzing the chip segmentation frequency of CT-scans of Ti-6Al-4V chips, has been presented. First, the relation between segment distance and segmentation distance with the compression factor has been introduced. Then, it has been shown how the grayscale matrix of the CT-scan can be transformed by means of thresholding into a point cloud, describing the chip without any distortions. Therefore, the largest connected volume is obtained. It has been described how a trajectory can be computed by means of skeletonization to obtain the course of the chip. With this trajectory the chip can be transformed into a straightened chip by slicing it in thin layers and reorder these layers. Since the straightened chip is screwed, it was shown how the chip can be descrewed by extracting the corner points of every layer. Out of this point cloud, a signal that describes the segmentation can be extracted by nearest neighbor interpolation. For validation purpose, the CT-method has been compared with optical measurements directly, which fits nearly perfectly. Additionally a statistical comparison has been done to compare helical chips, which also shows a satisfying similarity. Finally, the CT-method has been compared with the structure borne signals of the turning process, especially with regard to the compression factor, which has shown that it is possible to verify the acoustic emissions with the CT-method. The results of this work contribute to a more accurate and efficient extraction of information from the CT measurements of chips. This leads to a better understanding of the chip formation process, as well as allows to a faster creation of empirical models based on the chip segmentation frequency parameter.

With the presented improvements, current known methods can be made significantly more robust. Hence, several chips with complex forms can now be analyzed, for which known methods do not lead to any meaningful results.

Acknowledgements The scientific work has been supported by the DFG within the research priority program SPP 2086 (ZA 785/3-2 and HE 6212/1-2). The authors thank the DFG for this funding and intensive technical support.

Funding Open Access funding enabled and organized by Projekt DEAL.

Declarations

Conflict of interest The authors declare that they have no conflict of interest.

References

1. Barry J, Byrne G, Lennon D (2001) Observations on chip formation and acoustic emission in machining ti-6al-4v alloy. Int J Mach Tools Manuf 41(7):1055–1070
2. Shivpuri R, Hua J, Mittal P, Srivastava A, Lahoti G (2002) Microstructure-mechanics interactions in modeling chip segmentation during titanium machining. CIRP Ann 51(1):71–74
3. Hua J, Shivpuri R (2004) Prediction of chip morphology and segmentation during the machining of titanium alloys. J Mater Process Technol 150(1–2):124–133
4. Komanduri R (1982) Some clarifications on the mechanics of chip formation when machining titanium alloys. Wear 76(1):15–34
5. Zhang C, Choi H (2021) Study of segmented chip formation in cutting of high-strength lightweight alloys. Int J Adv Manuf Technol 112:2683–2703
6. Komanduri R, Hou Z-B (2002) On thermoplastic shear instability in the machining of a titanium alloy Ti-6Al-4V. Metall Mater Trans A 33:2995–3010
7. Calamaz M, Coupard D, Girot F (2010) Numerical simulation of titanium alloy dry machining with a strain softening constitutive law. Mach Sci Technol 14(2):244–257
8. Zanger F et al (2018) FEM simulation and acoustic emission based characterization of chip segmentation frequency in machining of Ti-6Al-4V. Procedia CIRP 72:1421–1426
9. Nguyen V, Fernandez-Zelaia P, Melkote SN (2017) PVDF sensor based characterization of chip segmentation in cutting of Ti-6Al-4V alloy. CIRP Ann 66(1):73–76
10. González G, Schwär D, Segebade E, Heizmann M, Zanger F (2021) Chip segmentation frequency based strategy for tool condition monitoring during turning of Ti-6Al-4V. Procedia CIRP 102:276–280
11. Devotta A, Beno T, Löf R, Espes E (2015) Quantitative characterization of chip morphology using computed tomography in orthogonal turning process. Procedia CIRP 33:299–304
12. Schwär D, Kunz A, Dehen S, Zanger F, Puente León F (2020) Analyse von 3d-ct-aufnahmen von spänen zur extrahierung der segmentspanbildungsfrequenz. Techn Mess 87(s1):22–27
13. Diaz Ocampo D, Gonzalez G, Zanger F, Heizmann M (2021) Schätzung der segmentspanbildungsfrequenz mithilfe von körperschallsignalen. Techn Mess 88(s1):37–41
14. Bushlya V, Schultheiss F, Gutnichenko O, Zhou J, Stahl J (2015) On the analytical representation of chip area and tool geometry when oblique turning with round tools. Part 1: chip area parameters under variation of side and back rake angle. Procedia CIRP 31:417–422
15. Liu D, Yu J (2009) Otsu method and k-means. 2009 Ninth International Conference on Hybrid Intelligent Systems 1, 344–349
16. Chowdhury AS, Bhandarkar SM (2011) Computer vision-guided virtual craniofacial surgery: a graph-theoretic and statistical perspective. Springer Science and Business Media
17. Beyerer J, Puente León F, Frese C (2015) Machine vision: automated visual inspection: theory, practice and applications. Springer
18. Jähne B (2012) Digitale Bildverarbeitung und Bildgewinnung, 7th edn. Springer, Heidelberg
19. Bentley JL (1975) Multidimensional binary search trees used for associative searching. Commun ACM 18(9):509–517
20. Dijkstra EW (1959) A note on two problems in connexion with graphs. Numer Math 1(1):269–271
21. Schafer RW (2011) What is a savitzky-golay filter? [lecture notes]. IEEE Signal Process Mag 28(4):111–117
22. Harris FJ (1978) On the use of windows for harmonic analysis with the discrete Fourier transform. Proc IEEE 66(1):51–83
23. Lee Rodgers J, Nicewander WA (1988) Thirteen ways to look at the correlation coefficient. Am Stat 42(1):59–66