Ultralow-Power W-band Low-Noise Amplifier Design in 130-nm SiGe BiCMOS

Kateryna Smirnova, Christian Bohn, Mehmet Kaynak, Ahmet Çağrı Ulusoy

***Abstract*— This paper presents a power consumption reduction aspect for a 100-GHz low-noise amplifier. Two designs implemented in 0.13-µm SiGe BiCMOS technology demonstrate state-of-the-art performance, whereas P_{DC} is reduced from 23.5 mW for the standard version to 3.8 mW for the low-power version. Two circuits exhibit a measured gain of 22 dB and 16 dB and a noise figure of 4 dB and 6.3 dB at 100 GHz. An input 1-dB compression point for the standard and the low-power version is -24.5 dBm and -26.5 dBm, respectively. The occupied IC area in both cases is 0.018 mm^2 and 0.014 mm^2 excluding the pads, which proves to be the most compact design among previously reported in the frequency range of interest.**

***Index Terms*—Low-noise amplifier (LNA), noise figure (NF), W-band.**

I. Introduction

LARGE mm-wave phased arrays are frequently used in modern communication systems [1] as well as in radar applications [2]. Containing a large number of transmit-receive channels, the arrays require a very high level of integration. As the frequency increases, spacing between antenna elements is reduced proportionally (e.g. at 100 GHz $\lambda/2 = 1.5$ mm), which becomes a limiting factor for a die size. In the case of analog beamforming and especially if a dual-polarization operation is required, the compactness of each building block becomes crucial. Besides, smaller IC area directly leads to reducing production costs, essential for large-scale employment. Additionally, the power efficiency of each Tx/Rx unit is an important aspect, as the power consumption of an array scales with the number of channels. By finding a trade-off one can save substantial power on LNA without critically sacrificing its performance, as presented in this paper. The behavior of SiGe HBTs in saturated bias regime and its impact on X- and Ku-band LNAs is previously studied in [3], [4].

In this paper, we present two W-band low-noise amplifiers implemented in IHP's SG13G2 BiCMOS technology. The first version represents a circuit designed using standard techniques without optimizing the power consumption (P_{DC} =23.5 mW). The second version is created to define trade-offs for an ultra-low-power design and to conclude what performance metrics are possible through this trade-off analysis. As a result, both versions have state-of-the-art performance and a comparable noise figure at 100 GHz, even though the low-power version dissipates only 3.8 mW, which corresponds to a reduction by six times compared to the standard version. Both versions also exhibit ultra-compact layouts of 0.018 mm^2 and 0.014 mm^2.

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II. Circuit Design

Fig. 1 presents the schematic for the standard (a) and low-power (b) LNAs. Both circuits are based on a 2-stage cascode topology. The first circuit is designed using well-established methodologies for achieving simultaneous noise and power match for the central frequency of 100 GHz. The second circuit

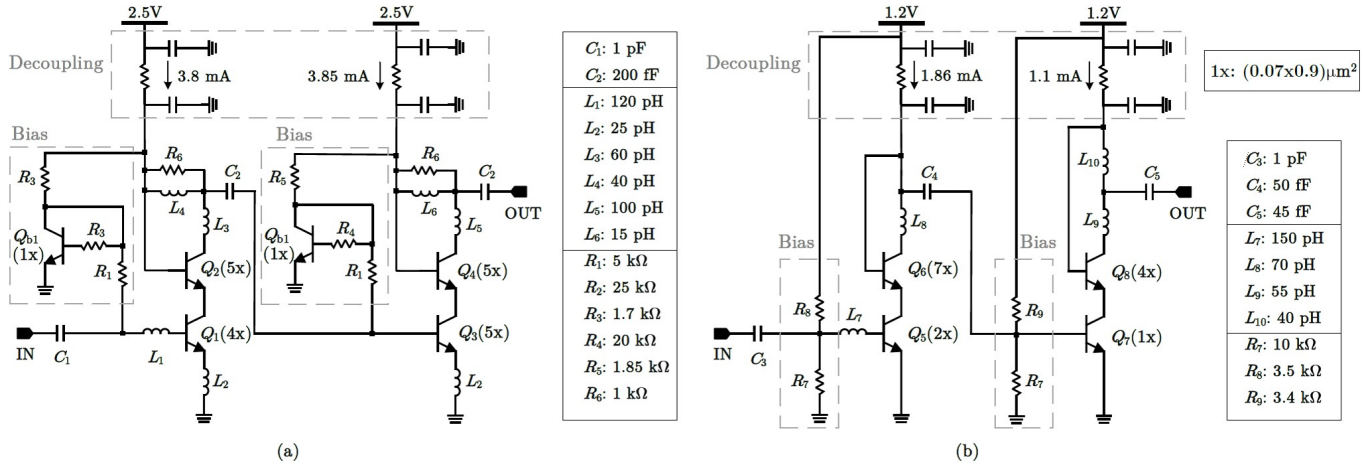

Fig. 1. Schematic of (a) standard LNA (b) low-power LNA.

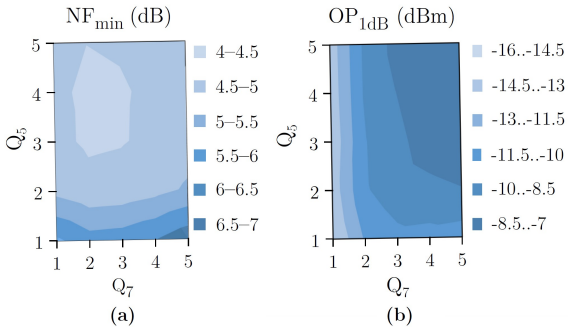

Fig. 2. Impact of CE transistors size on $NF_{\min}$ (a) and $OP_{1\text{dB}}$ (b).

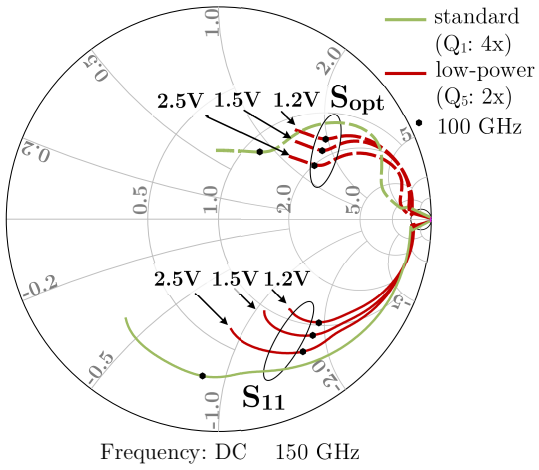

Fig. 3. Impact of Vcc on input impedance.

is designed with an additional effort to minimize DC power dissipation, while maintaining comparable performance.

An LNA design procedure requires a trade-off between NF, P_{DC} and linearity. In the low-power variant, since common-emitter transistors Q_5 and Q_7 define the current consumption, these devices were chosen with smaller emitter areas. Fig. 2 presents the impact of the size of Q_5 and Q_7 stages on $NF_{\min}$ and $OP_{1\text{dB}}$. Q_5 is chosen to be twice larger than the smallest available option (2 emitter fingers) as a trade-off between P_{DC} and NF. Fig. 2a demonstrates immediate increase of $NF_{\min}$ by 1–1.5 dB when using one-finger option for Q_5. Increasing further Q_5 emitter area in comparison to the chosen option does not improve $NF_{\min}$, unless larger Q_7 is used, as can be observed from the 4–4.5 dB zone shape. However, in this case, the circuit could no longer be considered a low-power solution.

Reducing P_{DC} directly affects the circuit linearity. Both stages of the standard version compress almost simultaneously, whereas the main contributor to the circuit non-linearity for the low-power LNA is the output stage. In this case, the power consumption of the second stage was significantly reduced, as it has negligible impact on NF in comparison to the first stage, which can be observed from horizontal behavior of different $NF_{\min}$ zones for small Q_5 (Fig. 2a). However, it has a negative impact on the linearity because of Q_7 compressing by the signal previously amplified by the first stage that is demonstrated by almost vertical pattern of

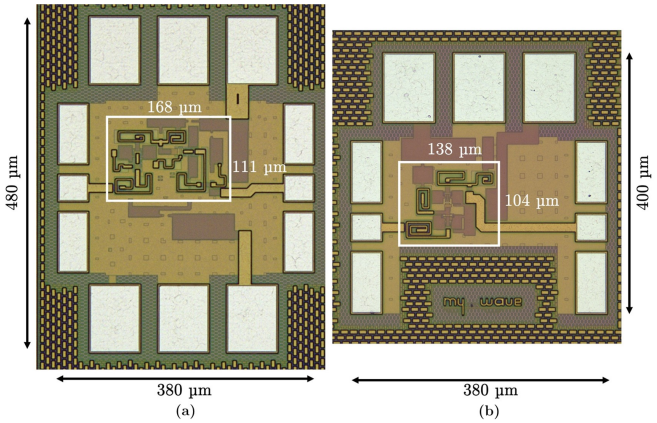

Fig. 4. Chip photograph of standard (a) and low-power (b) LNA.

$OP_{1\text{dB}}$ for small Q_7 (Fig. 2b). Increasing the size of Q_7 would immediately improve linearity of the circuit, however, in this work, achieving comparable NF for lower P_{DC} was prioritized.

Decreasing Vcc also belongs to the main changes made for the low-power design (Fig. 3). For the chosen size of Q_5, Vcc reduction from 2.5 V to 1.2 V leads to S_{11} shift towards 50 Ω circle that corresponds to an increase in C_{in} by approximately 4 fF. This is mainly due to the reduced Vbc, which results in a larger C_{bc}. This effect makes the emitter degeneration unnecessary in contrast to the standard version, also presented in the figure for comparison. Additionally, the Vcc reduction leads to a slight improvement in S_{opt} by increasing its real part.

The size choice of Q_6 and Q_8 is to a certain extent based on the impedance matching simplification. The use of the much larger device for Q_6 (7x) leads to an increase in its collector-base capacitance that eventually contributes to the interstage matching, thus allowing the use of smaller L_8 and C_4. The size of Q_8 (4x) helps to bring the high Re(S_{22}) to the 50 Ω circle and makes the output matching easier. The bias network consists of two voltage dividers in order to reduce the additional power needed in comparison to the conventional current mirror, used in the standard version.

The active circuit core of the standard LNA occupies 0.018 mm^2 of the IC area. The core of the low-power LNA occupies 0.014 mm^2 and the chips photograph is shown in Fig. 4. The compact layout is achieved by adjusting the shape and orientation of spiral inductors individually depending on empty areas available and by common-base device sizing as previously described.

III. Experimental Results

The measurements have been carried out with the Agilent N5251A broadband system using an N5247B PNA-X in a 2-port configuration. In Fig. 5a, simulated and measured S-parameters of the standard LNA are shown. The measured gain at 100 GHz is 22.2 dB with a 3-dB bandwidth of 24 GHz (86 – 110 GHz). Solid and dashed lines in all figures of this section correspond to measured and simulated data, respectively.

TABLE I
PERFORMANCE SUMMARY

	Technology	P_{DC}, mW	S_{21}, dB	Frequency, GHz	BW, GHz	NF, dB	$IP_{1\mathrm{dB}}$, dBm	Area, mm^2	FoM1	FoM2
[5]	65-nm CMOS	42	21.9	96	22.1	4.9	–13.2	0.127	57	13.1
[6]	22-nm CMOS	16	18.2	92	31	5.8	–22.8	0.435	5.7	1.9
[7]	40-nm CMOS	23.4	18.5	84	16.1	5.7	–19	0.174	10.2	2
[8]	130-nm SiGe	12	27.5	125	35’	5.5	–33	0.39	6.6	0.8
[9]	90-nm CMOS	6.8	21.5	90	5^{+}	8.3	-30	0.1	3	0.2
This work	130-nm SiGe	23.5 3.8	22.2 16	100 100	24 >16	4 6.3	–24.5 –26.5	0.018 0.014	10 5.5	2.4 0.9

’BW with gain >20 dB; 3dB-BW estimated from the plot is 15 GHz
$^{+}$estimated from the plot

$\mathrm{FoM1} = 1000 \cdot \frac{G \cdot IP_{1\mathrm{dB}}[mW]}{(F-1) \cdot P_{\mathrm{DC}}[mW]}$ $\mathrm{FoM2} = 1000 \cdot \frac{G \cdot IP_{1\mathrm{dB}}[mW] \cdot BW_{3\mathrm{dB}}[GHz]}{(F-1) \cdot P_{\mathrm{DC}}[mW] \cdot f_c[GHz]}$

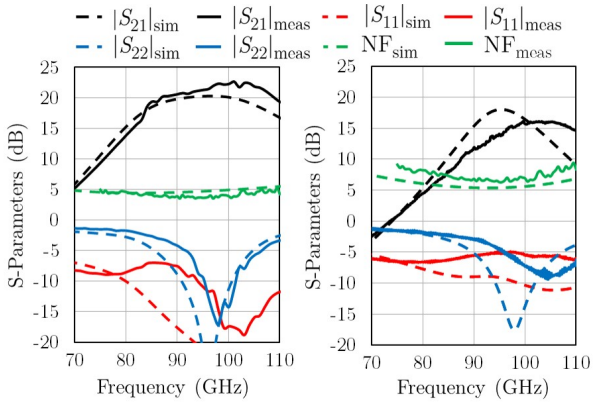

Fig. 5. S-parameters of standard (a) and low-power (b) LNA.

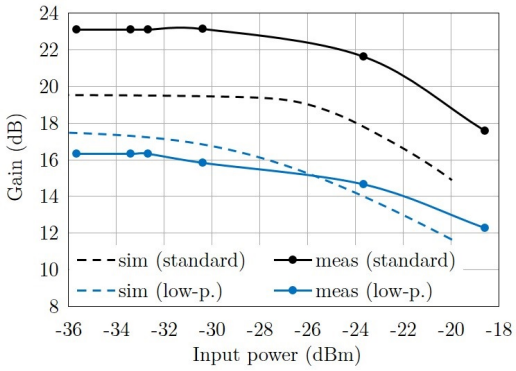

Fig. 6. Gain versus input power at 100 GHz.

S-parameters for the low-power LNA are presented in Fig. 5b. A frequency shift in the measured S_{21} curve relative to the simulation does not exceed 5% from the central frequency. The discrepancies between measured and simulated results are presumably caused by the transistor model inaccuracies since the devices are conventionally characterized for the forward-active regime, whereas in this case, transistors operate in saturation [3]. The measured 3-dB frequency range, in this case, starts from 93.8 GHz and goes beyond 110 GHz, which is not covered by the frequency extenders used. Therefore, the 3-dB bandwidth of the low-power version can only be reported to be >16 GHz. The gain of 16 dB was measured at 100 GHz.

The simulated and measured frequency dependence of NF is also presented in Fig. 5. The measurement has been carried out through Y-factor method using Agilent N8973A Noise Figure Analyzer. Measured NF values at 100 GHz for the standard and low-power versions are 4 dB and 6.3 dB, respectively. The standard LNA demonstrates higher bandwidth of the NF response in comparison to the low-power LNA.

Simulated and measured large-signal performance at 100 GHz for two circuits is presented in Fig. 6. The input power was controlled by an attenuator of the frequency extension module. For the standard LNA, the measured input 1-dB compression point of -24.5 dBm matches the simulated value of -24.7 dBm. The low-power LNA exhibits measured $\mathrm{IP}_{1\mathrm{dB}}$ of -26.5 dBm. Curve imperfections may be caused by the manual control of the attenuator that inherently introduces certain measurement inaccuracy.

IV. CONCLUSION

In this paper, we present two 100-GHz LNA designs with different power consumption to investigate its possible impact on the LNA performance. Both designs are implemented in 130-nm SiGe BiCMOS technology. An overview of previously published designs is shown in Table 1.

Several works focused on a highly linear operation, exceed the FoM presented in our paper, especially [5]. The FoM does not consider an occupied IC area, while it remains crucial for some applications, e.g. phased arrays. It is worth mentioning that our designs use five times less area than the most compact designs, listed in the table.

The power reduction inevitably leads to the gain drop and a certain NF worsening. The main purpose of this work was to study how much power is possible to save while maintaining comparable performance. In the end, after reducing 84% of P_{DC}, the LNA lost 45% of its performance (calculated from the difference in FoM1 between the standard and low-power version).

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