PROCEEDINGS OF SCIENCE

ATLASPix3 Modules for Experiments at Electron-Positron Colliders

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High-voltage CMOS detectors are being developed for application in High-Energy Physics. ATLASPIX3 is a full-reticle size monolithic pixel detector, consisting of 49000 pixels of dimension 50×150 μm^2. It has been realized in in TSI 180 nm HVCMOS technology. In view of applications at future electron-positron colliders, multi-chip-modules are built. The module design and its characterization by electrical test and radiation sources will be illustrated, including characterization of shunt regulators for serial chain powering. Lightweight long structure to support and to cool multiple-module chain are also being realized. The multi-chip-modules performance shows no degradation with respect to single-chip devices and the level of integration achieved is suitable for tracking at future e^+e^- accelerators.

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1. ATLASPix3 chip

The ATLASPix3 [1] pixel detector is a system-on-chip implemented in a 180 nm HVCMOS technology. The pixel electronics are embedded in a shallow n- and p- well. The deep n-well works as the sensor electrode and also isolates the shallow wells from the p-substrate.

The full chip has an area of 20.2×21 mm^2 and the matrix is made by 132×372 pixels of 150×50 μm^2 size. The p-type substrate has a 200 Ωcm resistivity and the deep n-well has a breakdown voltage of about 60 V respect to the substrate potential. It has a 25 ns timestamping and data can be sent off the chip with a maximum rate of 1.28 Gbit/s.

Each of the 132 columns contains 372 pixels, 372 hit digitizers (HD), 80 content addressable memory cells (CAM), and two end of column multiplexers (EoC mux). The HDs, CAMs and multiplexers are located in the chip periphery together with the readout control unit (RCU), the clock generator, configuration registers, DACs, linear regulators and IO pads. The pixels contains the analog circuits such as the charge sensitive amplifier (CSA) and the comparator. Both continuous and triggered readout are possible thanks to the two EoC-multiplexers, and, respectively, the 372 hit buffers (HDs) and the 80 trigger buffers (CAMs).

2. ATLASPix3 quad modules

A real detector system requires the aggregation of electrical services and connection for multiple modules. For this reason quad-modules for ATLASPix3 have been developed similarly to the ITk pixels layout [2]. In particular a flex hybrid has been implemented to interface 4 pixel detectors with the readout system and the software has been adapted for modules calibration.

2.1 Flex hybrid topology and characterization

The flex hybrid is a 4-layers flexible printed circuit. Fig. 1 shows the flex hybrid topology. The input lines are located in the inner layer of the stack-up and are very long with respect to the output lines, located in top layer.

The design of the flex particularly focuses on the power integrity. Fig. 2 shows a simulation for the current flow in the power layer (VDD) and the voltage drop compared to ground (GND) layer. The singular "circular" arrangement of the vias has been chosen in order to reduce the maximum current density. The maximum voltage drop is ~2.7 mV, maximum current density is ~13.9 A/mm^2 and max via current is ~137.0 mA.

The flex impedance has been measured with the use of a TDR (Time Domain Reflectometer). As an example, the input CkExt line and one of the output DataOut line are shown in Fig. 3. In both cases the measured impedances match the design value of 100 Ω.

Finally Fig. 4 shows the Eye diagram for the same CkExt and DataOut lines for signals at 100 and 500 Mbit/s. The CkExt line has a marginal opening for the high frequency signal but this does not represents an issue, since this line carries a clock of ~160 MHz maximum frequency.

2.2 Module calibration and operation

ATLASPix3 has a test signal circuit in the chip periphery regulated by a 8-bit on-chip DAC. The pixels also contain a circuit for the fine tuning of the thresholds regulated by a 3-bit DAC. They

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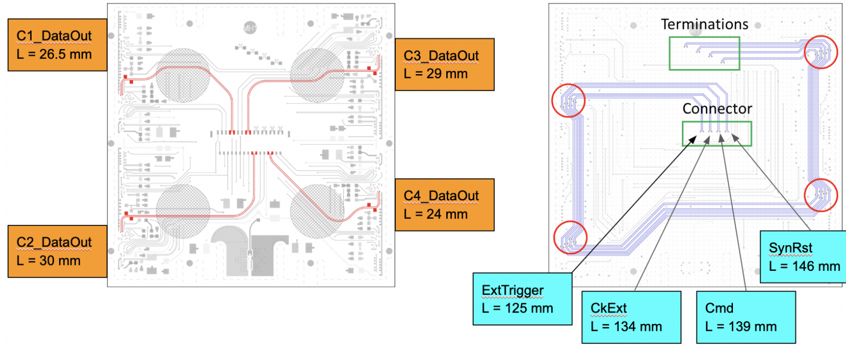

Figure 1: Flex topology. Output lines on the left and input lines on the right. Output LVDS lines, on the left, connect directly the 1.28 Mbps serial output to the communication cable, input LVDS lines distributes signals to the 4 chips and are terminated at the end of the loop.

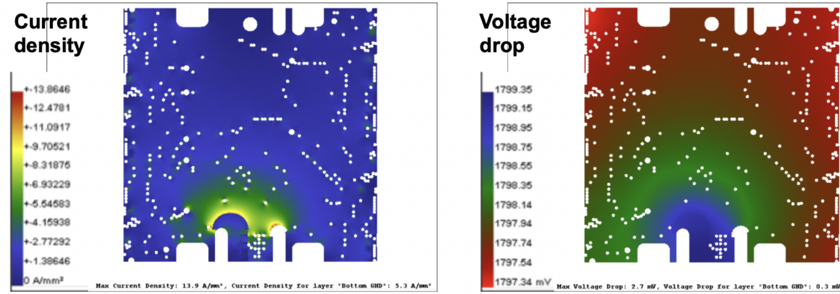

Figure 2: Power integrity simulation for VDD (GND as reference). The maximum voltage drop is ~2.7 mV, maximum current density is ~13.9 A/mm^2 and max via current is ~137.0 mA.

can be used for measuring noise and thresholds of the quad modules and for tuning the thresholds. Fig. 5 shows the obtained results. The threshold dispersion across the matrix is reduced by a factor of about five, from σ~100 mV to ~20 mV, while the measured noise is ~20 mV (~340 e^-) for a chosen thresholds of ~870 mV (~7400 e^-).

The operation of the modules has been tested with an X-ray tube [3], as shown in Fig. 6(a). Two modules have also been brought to a testbeam at DESY in April 2022 and tested with electron beams up to ~6 GeV energy. The experimental setup also included two ATLASPix3 telescopes built by KIT and the UK groups [7, 8]. The operation of quad-modules has been demonstrated also in this case, as shown in Fig. 6(b).

3. Serial Powering

The version ATLASPix3.1 of the chip includes a modification of two shunt/low-dropout regulators, which allow to bias the chips with a constant current. This provides the possibility for serial powering of multiple modules, reducing the number of supply cables and power loss between the power supplies and the detector. These regulators supply voltages for the digital and analog part of the chip and give the possibility to use a single current power supply for all the 6 biases needed to operate the chip. Input and output voltages of the regulators can be regulated by 3-bit DACs.

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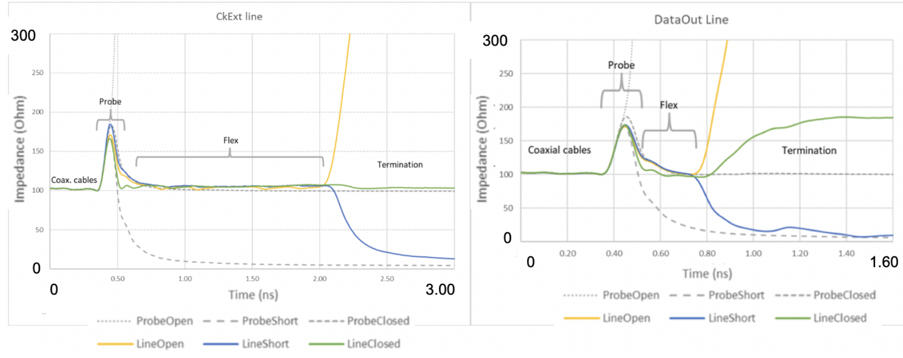

Figure 3: TDR measurements of the impedance for CkExt line and DataOut line. Three different terminations (open ciruit, short and 100 Ω) have been used to measure the length of the lines. The short DataOut line is a slightly distorted by the reflections due to the probe impedance mismatch.

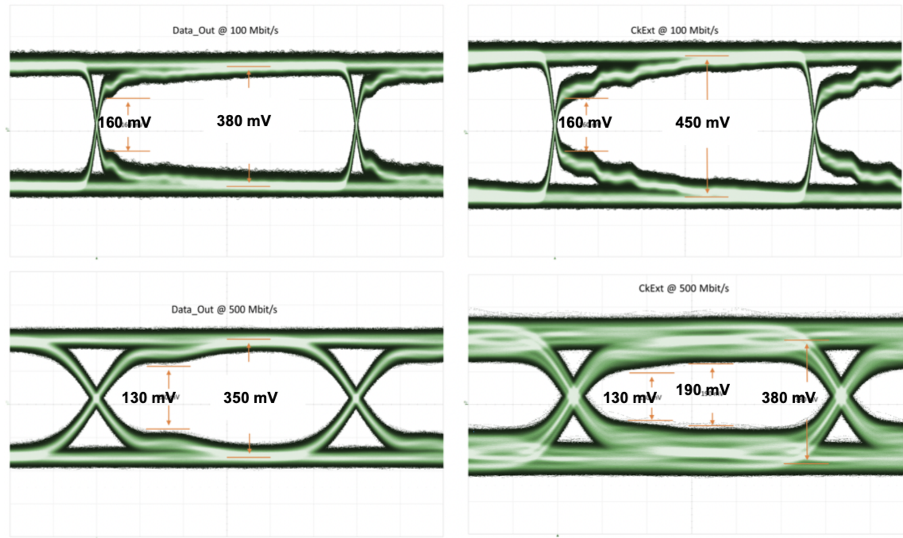

Figure 4: Eye diagrams of the LVDS lines CkExt and DataOut, for signals of 100/500 Mbit/s and 400 mV amplitude.

The regulators have been tested on a pair of ATLASPix3.1 chips mounted on single chip carrier PCB, by using different external resistive loads. Fig. 7 shows the regulators input and output voltages as a function of the bias current i_{input}. The linear part after the power-on has been fitted with a linear function

$$V = R_{\text{eff}} i_{\text{input}} + V_{\text{off}} \tag{1}$$

in order to extrapolate the effective resistance R_{eff} and the offset voltage V_{off} of the regulators. Tab. 1 reviews the obtained values and the nominal values. The agreement is acceptable, the input values, slightly larger than nominal, are mainly due to the voltage drop in the resistive path between the test point on the PCB and the ATLASPix input pads of $\sim$0.3 Ω.

Finally the chip has been biased from the output of the regulators. This gives an idea of the power consumption of the chip when using regulators, that is about 175 mW/cm^2 (690 mW/chip).

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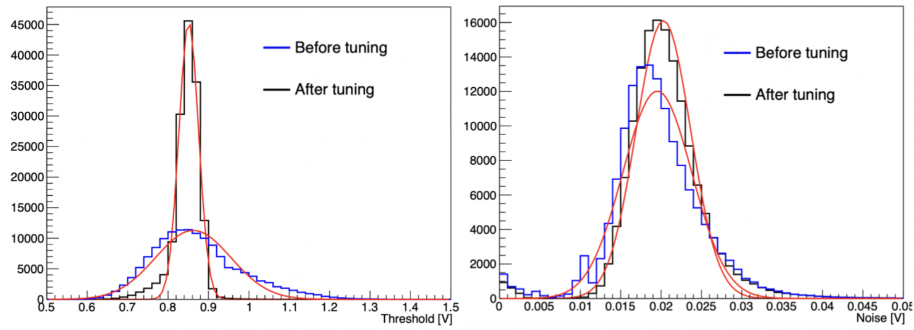

Figure 5: Threshold (left panel) and noise (right panel) distribution of the pixels of one quad module before and after threshold tuning.

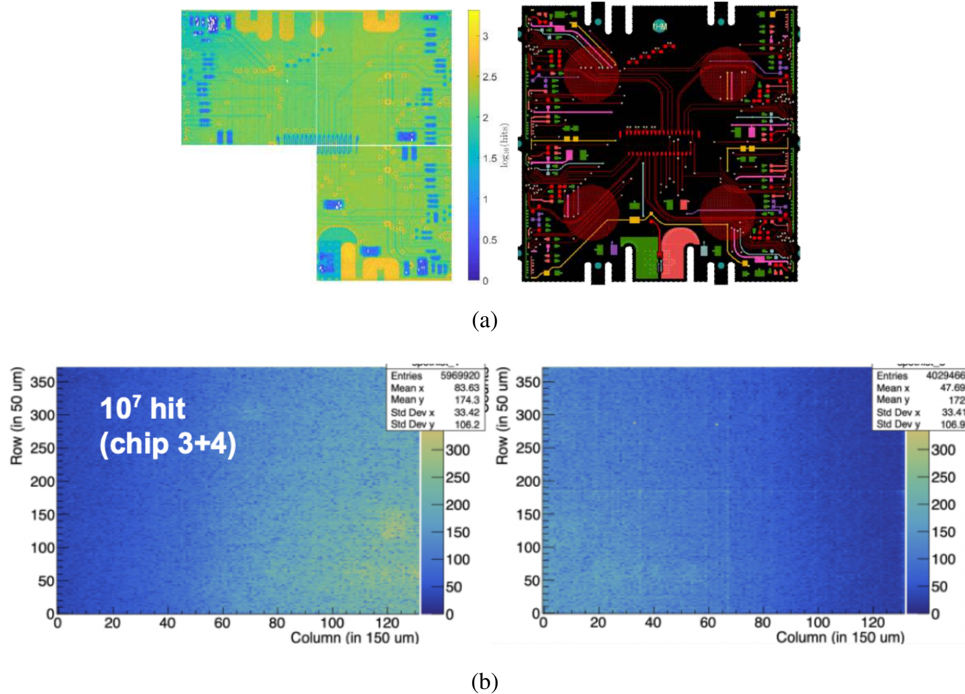

Figure 6: X-ray test of quad modules (a). The components on the PCB are clearly visible. Hitmaps of two chips of one quad module (b) from the testbeam.

4. Detector system

The high precision physics program of future experiments at e^+e^- colliders sets stringent requirements on the tracking system of future detectors [4, 5]. In order to fulfill these requirements all the future colliders, such as FCC-ee and CEPC, use a similar approach, based on an high resolution pixel vertex detector and either a full silicon tracker or a central gas chamber with a silicon wrapper around it. The CEPC CDR baseline and the IDEA detector designs both uses this second approach. In particular ATLASPix3 is suitable for the internal silicon layer in front of the central gas chamber and for the silicon wrapper. The two designs use a different mechanical approach for the internal silicon layer and they will be described in the following.

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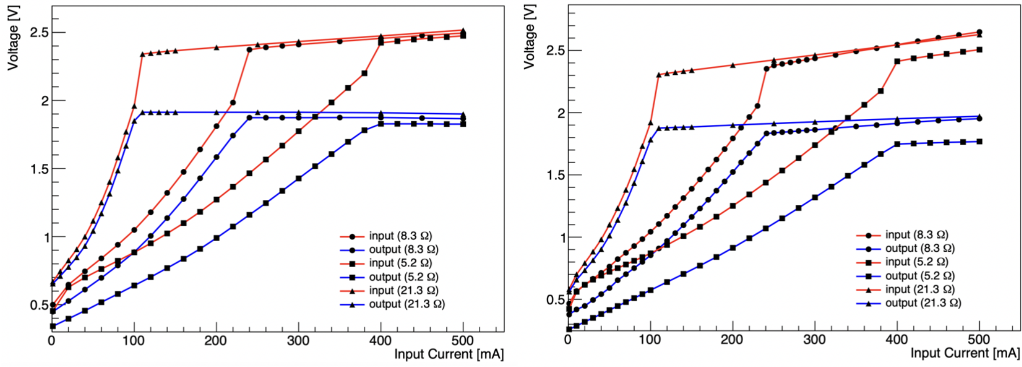

Figure 7: Turn-on curves (voltage as function of the bias current) for the ATLASPix3.1 digital and analog regulators with different external resistive loads. The linear part is fitted with the linear function of Eq. 1.

INPUT	Nominal	Analog	Digital	**OUTPUT**	Nominal	Analog	Digital
R_{eff} [Ω]	0	0.43-0.51	0.8-1.1	R_{eff} [Ω]	0	0	0.8-1.1
V_{off} [V]	2.1	2.22-2.30	2.05-2.22	V_{off} [V]	1.8	1.84-1.92	1.67-1.85

Table 1: Results of the linear fit of Fig. 7 with Eq. 1 for input and output voltages. The range obtained with the different loads is indicated.

4.1 System considerations

The mechanical structure of the detector must provide enough room for all the services (data and power connections) and cooling capacity to sustain the detector power dissipation. The area covered by ATLASPix3 in the complete system (5-10% by the internal silicon layer and the rest by the silicon wrapper) is about 90 m^2, for a total of about 225000 chips hence 56000 quad modules. Such a large number makes the aggregation of several modules for data and services distribution essential.

The data rate is constrained by the inner tracker and it is expected to be 10^{-4}-10^{-3} particles $cm^{-2}event^{-1}$. Assuming two-pixel hits per particle and 96 bits/hit for ATLASPix3, links of 640 Mbit/s for quad modules provide an ample operational margin and the data output of 16 quad modules can be aggregated into 10 Gbit/s fast links, for a total of 3500 links.

Triggerless and triggered readout are both possible, but triggered readout would help in reducing the bandwidth occupancy.

Finally considering a serial powering scheme and the power consumption measured in section 3, the total power consumption should be around 175 kW plus an additional 2 W/link.

4.2 Mechanical systems for internal silicon layer

As outlined before, the CEPC CDR baseline and the IDEA design use two different mechanical approaches for the mechanics of the internal silicon layer.

The CEPC CDR baseline uses a very long stave structure, about 1330 mm long, with a triangular truss shape manufactured by water jet cutting, similar to the developments for the Belle II upgrade [6]. It is made to accommodate 32 quad modules, distributed all along the stave.

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Fig. 8 shows the truss structure. It is made by gluing together three single structures. Fig. 9(a) shows a simulation of the structure rigidity, for which a gravitational sag of about 100 μm is obtained. Two different cooling solutions have been studied, one with 2 water pipes and one with 4. Fig. 9(b) shows the simulation results, when using 4 pipes the temperature gradient is lower but the material budget increase. A prototype of this stave is actually in construction.

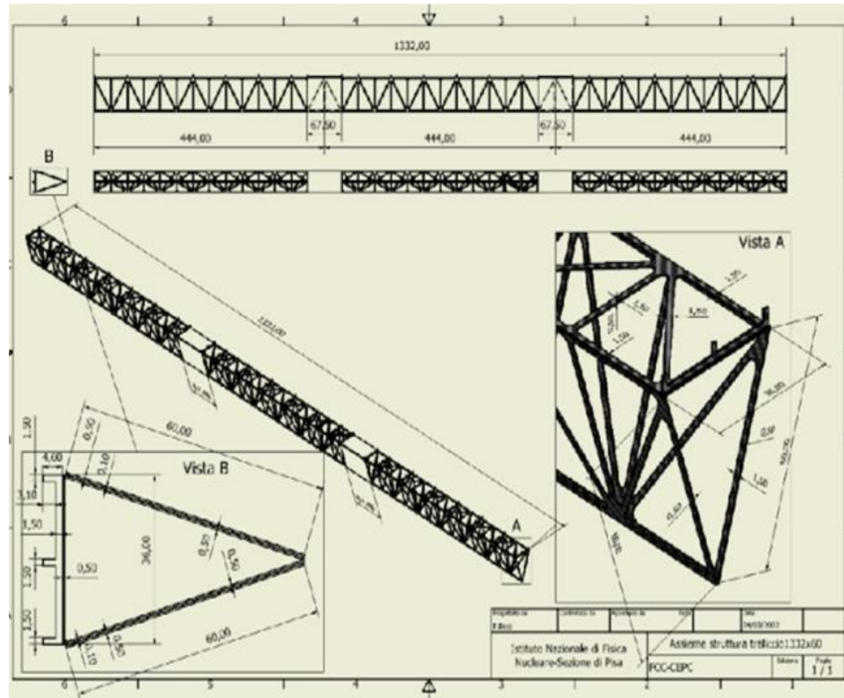

Figure 8: Truss structure for the CEPC CDR baseline stave. It has a triangular shape and is made by gluing together three single structure for a total length of about 1330 mm.

Fig. 10 shows the IDEA stave design. In this case the stave structure is shorter with a rectangular truss shape. The quad modules can be distributed in two layers for a total of 32 modules, 16 in each layer. The cooling is made with 4 water pipes per stave. The design is actually being finalized.

In both cases the outer barrel structure should be made of 48 staves with a mean distance of 30 cm from the beam axis. The whole structure should be supported by the central gas chamber. The designed power budget of ~2.63 kW is lower than the one required for the current version of ATLASPix3.

5. Conclusions and outlook

ATLASPix3 is a full size detector providing most of the features needed by e^+e^- experiments. Deployment on a real detector system requires the aggregation of data and services, for this purpose multi-chip modules have been realized and successfully tested.

Further integration requires chaining of multiple modules using the same serial powering concept developed for the silicon trackers for HL-LHC. Early tests on the shunt regulators implemented on the ATLASPix3.1 chips are encouraging and make possible to proceed to a redesign of a module

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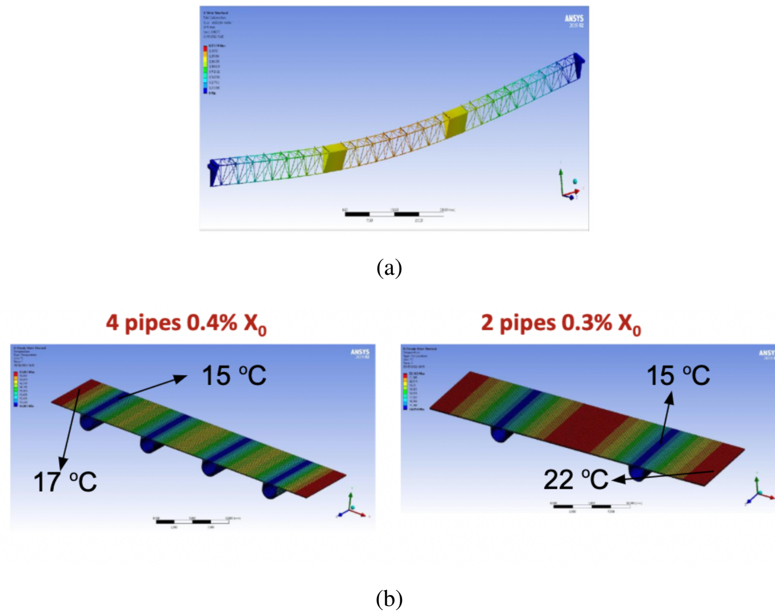

(a)

(b)

Figure 9: Structure rigidity (a) and cooling (b) simulations. a gravitational sag of about 100 μm is obtained. Two possible cooling solution are simulated, one with 2 water pipes and one with 4 water pipes.

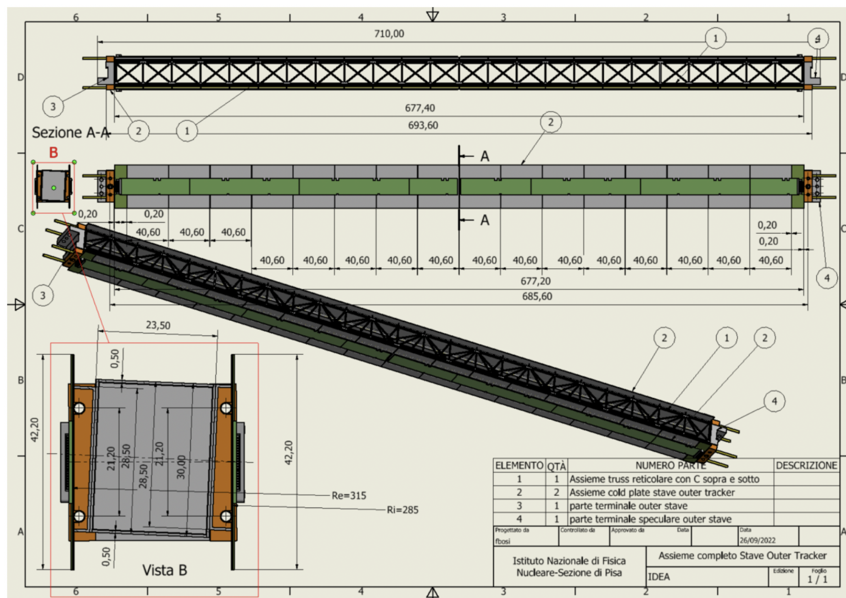

Figure 10: IDEA stave design. The truss has a rectangular shape and the quad modules can be disposed in two layers.

concept based on serial powering and the building of multi-module chains suitable for CEPC and FCC-ee accelerators.

Different detector concepts, such as CEPC CDR baseline and IDEA, are under study. They use a different mechanical approach for the internal silicon layer and a prototype for CEPC CDR baseline is actually is in construction.

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Improved sensors prototypes are also under study. The designers are trying to implement a smaller pixel pitch, a lower power consumption and different types of comparator and amplifier. Design using alternative HVCMOS in 55 nm process is also being implemented.

A design for a chip to chip data transmission is being studied. It could be used in quad modules and would permit to further reduce material for the aggregations of the chips.

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