

# Multi-Rate Discrete Domain Modeling of Power Hardware-in-The-Loop Setups

FARGAH ASHRAFIDEHKORDI <sup>ORCID</sup> (Graduate Student Member, IEEE), DUSTIN KOTTONAU <sup>ORCID</sup>, AND GIOVANNI DE CARNE <sup>ORCID</sup> (Senior Member, IEEE)

Institute for Technical Physics, Karlsruhe Institute of Technology, 76344 Karlsruhe, Germany

CORRESPONDING AUTHOR: FARGAH ASHRAFIDEHKORDI (e-mail: fargah.ashrafidehkordi@kit.edu)

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**ABSTRACT** Power Hardware-in-the-Loop (PHIL) facilitates the testing of novel power engineering solutions in the lab, allowing a flexible testing environment while keeping the high testing fidelity of real hardware. Due to the analog/digital intersection of the PHIL setup, selecting simply continuous or single-rate discrete-time domain fails to model such a hybrid system accurately. This article proposes a multi-rate discrete-time modeling approach of a PHIL setup that can estimate the mixed analog and digital nature of the PHIL accurately, resulting in accuracy improvement over a wide range of frequencies. The proposed approach applies two different sampling times, a large one connected to the digital simulator and a small one for modeling the analog-hardware part. Dynamics and delays of interfaces, such as analog-to-digital converters, the power amplifier, the sensor, and the low-pass filter, have been accurately modeled and validated by means of experimental results.

**INDEX TERMS** Power Hardware In the Loop, digital real-time simulations, power hardware in the loop stability, multi-rate discrete-time sampling.

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## I. INTRODUCTION

Testing new energy solutions in realistic conditions before their introduction in the market is vital to understand the performance and to address timely any constructive issues. However, testing them in the actual field is usually costly, not flexible, and with a high risk of customer disruption. Laboratory testing, on the other hand, can provide a safer testing environment, but it limits the testing flexibility (e.g., limited line and load configurations). A candidate solution to solve this problem is to connect the hardware under test (e.g., converters, loads, renewable sources) with a digitally real-time simulated system (e.g., grid model) by means of dedicated power interfaces. This solution, named Power Hardware-in-the-Loop (PHIL) [1], [2], [3], allows changing the flexible testing environment by modifying the simulated model in the digital real-time simulator (DRTS) [4] while achieving accurate testing results, due to the testing of the real hardware component known as hardware under test (HuT) [1], [5].

Due to the hybrid digital/analog nature of the PHIL, developing accurate modeling of the PHIL and choosing

an appropriate time domain, i.e., continuous-time (CT) or discrete-time (DT), can be challenging. CT-based modeling has been widely adopted in literature [5], [6], [7], [8], whereas other works [9], [10] demonstrated that the CT domain for stability assessment is not reliable since numerical discretization and holding effects of real-life setup can be captured better in the discrete domain. Several discretization techniques, i.e., step-invariant (also known as zero-order-hold), ramp-invariant (first-order-hold), and adaptive discretization based on input in [11] and trapezoidal approximation (bilinear method) in [9] are used to discretize the CT transfer functions. However, the sampling time in the single-rate discrete (SDT), where the simulator time-step is chosen as the discretization step for the analysis, may fail to represent the analog HuT accurately. In other words, to deal with this dual nature of the PHIL, a possible solution is to treat the CT part in the discrete-time domain but with a relatively small sampling time (at least one magnitude order smaller than the DRTS time step), building the model in a multi-rate discrete-time domain (MDT). MDT is employed and developed to enhance stability

by using a relatively small time step at the hardware-software intersection in [12]. However, the accuracy analysis over a wide range of frequencies is overlooked. In prior work of the authors [13], the accuracy of a PHIL setup with a switching mode amplifier is improved compared to CT and SDT over a wide range of frequencies. Nevertheless, the approach has never been validated experimentally and with more test cases.

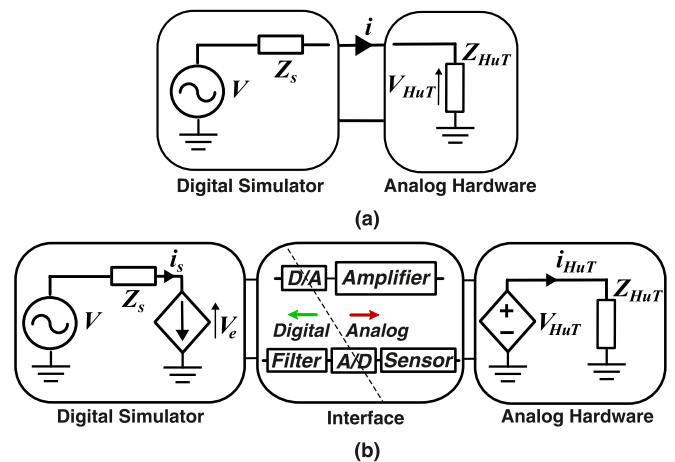
This article uses the MDT technique to improve modelling of a realistic PHIL setup with an ITM interface algorithm using a linear power amplifier with passive loads. The paper's novelty and contribution with respect to state of art can be summarized as follows:

- Comparison between the proposed Multi-Rate Discrete-Time modeling approach and existing modeling techniques, such as the Continuous-Time and Single-Rate Discrete-Time. The comparison has been quantitatively validated with the proposed indexes.
- Experimental validation of the accuracy of the aforementioned modeling approaches with a Power Hardware-in-the-Loop setup under two test cases, i.e., an RL and an RLC load.
- Assessment of the measurement uncertainty and validation of the performed experimental accuracy analysis.

This article is structured as follows: Section II gives a general introduction to the PHIL concept. In Section III, three modeling approaches, namely, CT, SDT, and MDT, are linearized and modeled through the transfer functions. A mathematical definition of accuracy is proposed in Section IV based on the closed-loop transfer function of each model. Simulink/MATLAB simulative results have been realized in Section V, to reference the accuracy analysis with respect to the standard modeling approach. Experimental results have been provided in Section VI, to validate the accuracy analysis of the simulation findings and prove the improved accuracy of the proposed MDT model. Finally, the conclusions are drawn in Section VII.

## II. POWER HARDWARE-IN-THE-LOOP CONCEPT

In order to interface the digital and hardware side of the test, a power interface and an interface algorithm are needed. This introduces an environmental difference between the “natural coupling” between DRTS and HuT (Fig. 1(a)), where the real hardware is connected to the real grid and the PHIL testing environment. As can be seen in Fig. 1(b), to connect actual power hardware, the measured signal in the DRTS must be converted to analog with a digital-to-analog (D/A) converter and amplified through a power amplifier. A sensor is required to measure the introduced voltage/current signal in the hardware and feed it back to the digital simulator. The measured analog signal (current in the figure) needs to be translated for DRTS with analog-to-digital (A/D) converter. Also, a low-pass filter is typically designed to reject high-frequency measurement noises, enhancing the stability of the loop. All the aforementioned conversion stages and delays inevitably cause inaccuracies and deteriorate the system stability [14]. Approaches such as phase lead compensators in [15] and



**FIGURE 1.** Generic scheme of PHIL: (a) Ideal scheme, (b) existing scheme with voltage-type ideal transformer method.

predictive control (Smith predictor) in [16] to cope with loop-delay consequences, leading to stability improvement.

Several interface approaches have been studied to improve loop stability. Standard interface algorithms proposed in the literature are the ideal transformer method (ITM), the damping impedance method (DIM), time-variant first-order approximation (TFA), the transmission line model (TLM), and partial circuit duplication (PCD). Selecting the proper algorithm is a research-goal-oriented decision, along with the facility constraints in the labs. Although there is no unique optimal interface for all power analyses, the ITM is understood as a straightforward interface algorithm in which the stability criterion is defined based on the simulated and hardware impedance ratio [6]. Although simple, this interface algorithm results in low stability issues. A low-pass filter in the feedback path has been proposed to improve the loop stability [17]. However, this filter compromises the accuracy by adding phase lag. An optimal feedback compensator has been proposed in [18] to deal with this phase error. Further stability and accuracy solutions based on synthesizing optimal controller and delay differential equations are presented in [19] and [20], respectively. The voltage-type ideal transformer method (V-ITM) shown in Fig. 1(b) is selected as the interface algorithm in this article. In the V-ITM, the amplifier applies the voltage to the HuT ( $V_{HuT}$ ), and the current ( $i_{HuT}$ ) is feedback through the sensor.

## III. MODELING OF POWER HARDWARE-IN-THE-LOOP

This section focuses on obtaining the closed-loop transfer function of each CT, SDT, and MDT modeling. The equivalent block diagram of each is shown in Figs. 2, 3, and 4, respectively. Two different sampling times are chosen for the software and hardware sides of the PHIL in the MDT method. The primary time step ( $T_{s1}$ ) is assigned to the software side of the PHIL, and the secondary time step ( $T_{s2}$ ), closer to the continuous-time domain, represents the hardware side.

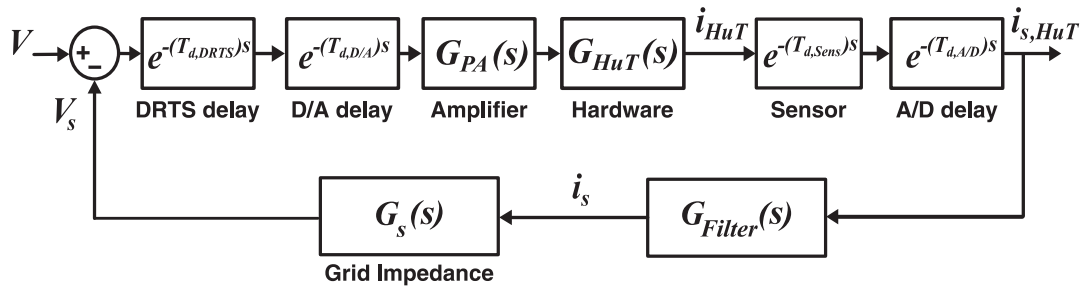


FIGURE 2. Continuous-time modeling block diagram.

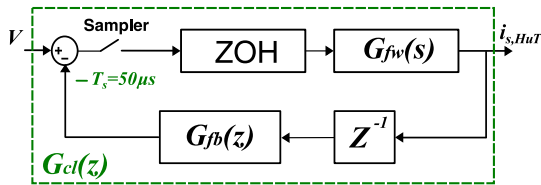


FIGURE 3. Single-rate discrete modeling block diagram.

Thevenin model with an RL impedance is chosen as the simulated grid, and RL and RLC impedances are employed as HuT in two different case studies. Delays of the A/D and D/A conversions, sensors, and DRTS are considered in addition to the PA and low-pass filter dynamics.

### A. CONTINUOUS-TIME MODELING

According to Fig. 2 the closed-loop transfer function of the system,  $G_{cl}(s)$ , implies the loop admittance driven by the measured current in DRTS  $i_{s,HuT}$ , over the input voltage  $v$ . The transfer function of each unit to attain  $G_{cl}(s)$  is defined in the following equations:

$$G_{cl}(s) = G_{fw}(s)/(1 + G_{fb}(s) \times G_{fw}(s)) \quad (1)$$

Where  $G_{fb}(s)$  is the feedback transfer function and  $G_{fw}(s)$  is the transfer function of the forward path from input to  $i_{s,HuT}$ .  $G_{fw}(s)$  is defined by the following relation:

$$G_{fw}(s) = G_{PA}(s) \times G_{HuT}(s) \times e^{-(T_d)s} \quad (2)$$

Where:

$$G_{PA}(s) = e^{-(T_{d,Amp})s} / ((1/\omega_0)s^2 + (2D/\omega_0)s + 1) \quad (3)$$

$$G_{HuT}(s) = 1/Z_{HuT}(s) \quad (4)$$

$$T_d = T_{d,DRTS} + T_{d,D/A} + T_{d,Sens} + T_{d,A/D} \quad (5)$$

The transfer function of linear power amplifier,  $G_{PA}(s)$ , consists of a resonant frequency  $\omega_0$  and damping factor  $D$  [21].  $T_d$  is the whole loop delay and  $T_{d,DRTS}$ ,  $T_{d,D/A}$ ,  $T_{d,A/D}$ ,  $T_{d,Sens}$ , and  $T_{d,Amp}$  are delays introduced by DRTS, A/D and D/A conversions, sensor measurements, and power amplifier respectively. The impedance of the hardware,  $Z_{HuT}(s)$ , for the RL and RLC cases are respectively:

$$Z_{HuT,RL}(s) = R_{HuT} + L_{HuT}s \quad (6)$$

$$Z_{HuT,RLC}(s) = Z_{HuT,RL}(s) + 1/(C_{HuT}s) \quad (7)$$

Accordingly,  $G_{fb}(s)$  in (8) contains the  $G_s(s)$  as simulated grid impedance, and  $G_{filter}(s)$  as low-pass filter with  $\omega_c$  as cut-off frequency:

$$G_{fb}(s) = G_{Filter}(s) \times G_s(s) \quad (8)$$

$$G_{Filter}(s) = \omega_c / (s + \omega_c) \quad (9)$$

$$G_s(s) = L_s s + R_s \quad (10)$$

### B. SINGLE-RATE DISCRETE-TIME MODELING

The step-invariant transformation, also known as the zero-order hold (ZOH) discretization technique, has been chosen to model more accurately the holding effects originating from DRTS during the D/A conversion [10]. Fig. 3 represents the discretized model of the system. The ZOH transformation can be described analytically as follows:

$$G_{ZOH}(s) = (1 - e^{-(T_s)s})/s \quad (11)$$

Applying (11) to the derived  $G_{fw}(s)$  from Section III-A and performing the  $s$  to  $z$  mapping with the given sampling time,  $T_s$ , the  $G_{fw,SDT}(z)$  becomes:

$$\begin{aligned} G_{fw,SDT}(z) &= Z\{G_{ZOH}(s) \times G_{fw}(s)\} \\ &= (1 - z^{-1})Z\{\mathcal{L}^{-1}\{G_{fw}(s)/s\}\}_{T_s} \end{aligned} \quad (12)$$

It is to be noted, the real-time simulator delay is handled with ZOH transform, and the delay of the amplifier is considered with its transfer function in (3) and therefore the forward delay shown in (5) here is updated as:

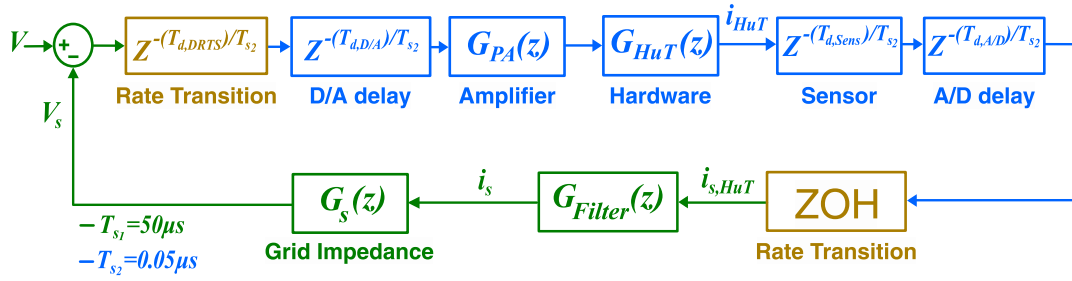
$$T_d = T_{d,D/A} + T_{d,Sens} + T_{d,A/D} \quad (13)$$

To avoid excessive modeling of the holding effect and to introduce unintentional additional unit delay, instead of the ZOH transform, the bilinear transform method (BLT) is picked to transform the  $G_{fb}(s)$  to its discrete counterpart. The approximate relation between  $s$  and  $z$  in the bilinear method is [22]:

$$s \approx 2(1 - z^{-1}) / (T_s(1 + z^{-1})) \quad (14)$$

Applying (14) to (8), the  $G_{fb,SDT}(z)$  is obtained, but due to the complexity, the full representation is avoided here:

$$G_{fb,SDT}(z) = Z_{BLT}\{G_{fb}(s)\}_{T_s} \quad (15)$$



**FIGURE 4.** Multi-rate discrete modeling block diagram.

Therefore, the closed-loop SDT transfer function of the system considering the sampling delay in the feedback is achievable as:

$$G_{cl,SDT}(z) = \frac{G_{fw,SDT}(z)}{(1 + G_{fw,SDT}(z) \times G_{fb,SDT}(z)/z)} \quad (16)$$

### C. MULTI-RATE DISCRETE-TIME MODELING

In the MDT approach, the system is partitioned with two different sampling times. The sampling time of the Section III-B is kept for the digital part of the setup but renamed as  $T_{s1}$ , and a smaller sampling time  $T_{s2} \ll T_{s1}$  (blue line in Fig. 4) is assigned to hardware section. The goal is to decouple the two system dynamics to represent the analog part of the circuit as an extremely fast-sampled discrete-domain model (e.g., up to 2-3 magnitude orders faster).

Accurate modeling of delays minimizes transfer function phase errors and improves the overall model's accuracy. In the MDT modeling, it is possible to model delays that are smaller than  $T_{s1}$ , for example, with a sampling time of  $T_{s2} \ll T_{s1}$ , and thus approximate better the phase frequency dependency.

Similarly, the closed-loop transfer function of the system in the  $z$  domain is attainable as follows:

$$G_{cl,MDT}(z) = G_{fw}(z)/(1 + G_{fw}(z) \times G_{fb}(z)) \quad (17)$$

Where  $G_{fb}(z)$  describes the feedback path and  $G_{fw}(z)$  is the transfer function of the forward path from input to  $i_{s,HuT}$ . Due to the different sampling rates, two rate transition blocks, shown in yellow in Fig. 4 are added. According to the definition of rate-transition block, the slow-to-fast transition rate block acts as a unit delay (in this case, it represents the DRTS delay), and the fast-to-slow transition rate block act as the ZOH of the A/D sampling. In the forward path, transfer functions with  $T_{s2}$  sampling time are multiplied as follows:

$$G_{fw,T_{s2}}(z) = G_{PA}(z) \times G_{HuT}(z) \times z^{-(T_d/T_{s2})} \quad (18)$$

The same approach as explained for  $G_{fb}(z)$  in Section III-B, BLT is used here to obtain the discrete transfer functions of the power amplifier and HuT:

$$G_{PA}(z) = Z_{BLT}\{G_{PA}(s)\}_{T_{s2}} \quad (19)$$

$$G_{HuT}(z) = Z_{BLT}\{G_{HuT}(s)\}_{T_{s2}} \quad (20)$$

The sampling time of the transfer function  $G_{fw,T_{s2}}(z)$  is yet to be transitioned to  $T_{s1}$  so the forward path from input to  $i_{s,HuT}$  is completed. As discussed above, the rate-transition block acting as ZOH handles fast-to-slow rate differences. However, instead of direct resampling of  $G_{fw,T_{s2}}(z)$  to  $G_{fw,T_{s1}}(z)$ , which causes losing excessive information,  $G_{fw,T_{s1}}(z)$  is achieved in two stages:

- 1)  $G_{fw,T_{s2}}(z)$  is transformed back to continuous using bilinear transform using:

$$z = e^{sT_{s2}} \approx (1 + sT_{s2}/2)/(1 - sT_{s2}/2) \quad (21)$$

And:

$$G_{FW}(s) = Z_{BLT}^{-1}\{G_{fw,T_{s2}}(z)\} \quad (22)$$

Where  $Z_{BLT}^{-1}$  represents the discrete-to-continuous transform.

- 2) Then  $G_{FW}(s)$  is sampled with  $T_{s1}$  using ZOH. Similar to (12):

$$G_{fw,T_{s1}}(z) = (1 - z^{-1})Z\{\mathcal{L}^{-1}\{G_{FW}(s)/s\}\}_{T_{s1}} \quad (23)$$

Since the calculated  $G_{fw,T_{s1}}(z)$  has the same sampling time as  $G_{fb}(z)$ , (17) is now resolvable. Following is the calculation of  $G_{fb}(z)$  using the bilinear method to achieve the discrete transfer functions of the low-pass filter and equivalent grid shown as  $G_{Filter}(z)$  and  $G_s(z)$ , respectively:

$$G_{fb}(z) = G_{Filter}(z) \times G_s(z) \quad (24)$$

$$G_{Filter}(z) = \omega_c / ((2/T_{s1}) \left( \frac{(1 - z^{-1})}{(1 + z^{-1})} \right) + \omega_c) \quad (25)$$

$$G_s(z) = L_s 2 (1 - z^{-1}) / (T_{s1} (1 + z^{-1})) + R_s \quad (26)$$

### IV. DEFINITION OF ACCURACY

Based on the calculated closed-loop transfer functions in the previous section, the accuracy of a PHIL model can be defined as the proximity of the models' gain, and phase values to a reference value (e.g., a benchmark model or experimental results) at each frequency [8]. The relative percentage error is measured at each frequency, and the mean of all measured

errors has been employed for accuracy comparison purposes:

$$AVG_{gain} = \sum_{i=1}^N \frac{|G_{ref}(j\omega)| - |G_{model}(j\omega)|}{|G_{ref}(j\omega)|} \times 100 \quad (27)$$

$$AVG_{phase} = \sum_{i=1}^N \frac{\angle G_{ref}(j\omega) - \angle G_{model}(j\omega)}{\angle G_{model}(j\omega)} \times 100 \quad (28)$$

Where  $|G_{ref}|$ , and  $\angle G_{ref}$  are the gain and phase of the closed-loop reference, which is the simulated MDT system in Simulink/MATLAB in the simulation Section V and experimental measurements in Section VI.  $G_{model}$  implies the closed-loop transfer function of the calculated CT, SDT, and proposed MDT model in Section III. Following the same procedure in [13], the weighted average error is defined as:

$$WAVG_{gain} = \sqrt{\sum_{i=1}^N \frac{|\frac{1}{f_i} (|G_{ref}(j\omega)| - |G_{model}(j\omega)|)|^2}{|G_{ref}(j\omega)|^2}} \times 100 \quad (29)$$

$$WAVG_{phase} = \sqrt{\sum_{i=1}^N \frac{|\frac{1}{f_i} (\angle G_{ref}(j\omega) - \angle G_{model}(j\omega))|^2}{|\angle G_{ref}(j\omega)|^2}} \times 100 \quad (30)$$

In the following section, the  $G_{ref}$  is chosen to be the MDT closed-loop implemented in Simulink, and through the accuracy error indexes, the validity of the linearized MDT modeling in Section IV-C is verified.

## V. SIMULATION RESULTS

The goal of this section is to verify the analytical part of MDT, specifically the formulated rate transition blocks with the Simulink model. Furthermore, it gives an overall insight into the CT and SDT behaviors compared to MDT.

To validate the MDT modeling accuracy, a comparison between the analytical modeling in Section III and the simulated model in Simulink/MATLAB has been carried out. The reference is set to be the implemented MDT V-ITM PHIL model in Simulink in two different HuT cases, an RL and an RLC load, respectively. The reference model is implemented in the Simulink as follows:

- All the delays are modeled as shown in Fig. 4.
- Series RL branches for grid impedance and series RL/RLC branches are used as HuT.
- $G_{Filter}$  shown in Fig. 4, in the feedback is implemented using (22).
- Two rate transition blocks shown in Fig. 4 are implemented for changing the sampling time.
- For the transfer function of the amplifier (16) is employed.

Results of all three MDT, CT, and SDT methods shown in this section are modeled based on the equations represented in Section III. The bode diagram is then calculated considering

TABLE 1. PHIL Simulation Parameter

Setup	Value	Unit	Setup	Value	Unit
$T_{s1}, T_{d,DRTS}$	50	$[\mu s]$	$T_{s2}$	0.05	$[\mu s]$
$T_{d,Amp}$	3.1	$[\mu s]$	$T_{d,Sens}$	0.8	$[\mu s]$
$T_{d,D/A}$	3	$[\mu s]$	$T_{d,A/D}$	2	$[\mu s]$
$\omega_c/2\pi$	2	$[kHz]$	$C_{HuT}$	7.5	$[\mu F]$
$L_s$	0.8	$[mH]$	$L_{HuT}$	8	$[mH]$
$R_s$	1	$[\Omega]$	$R_{HuT}$	1	$[\Omega]$
$\omega_0/2\pi$	180	$[kHz]$	$D$	0.9	—

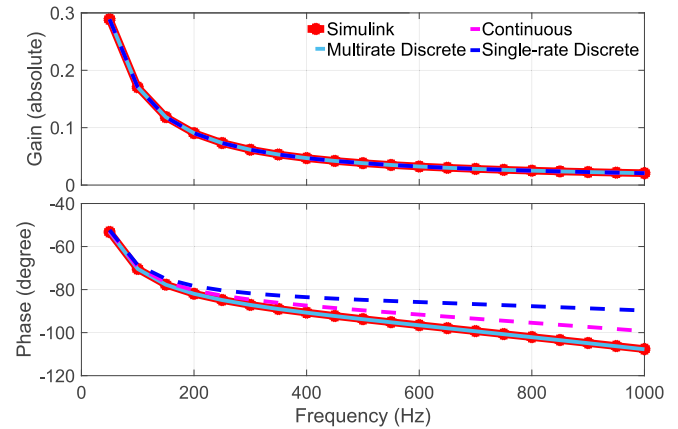


FIGURE 5. Frequency response comparison using RL as HuT.

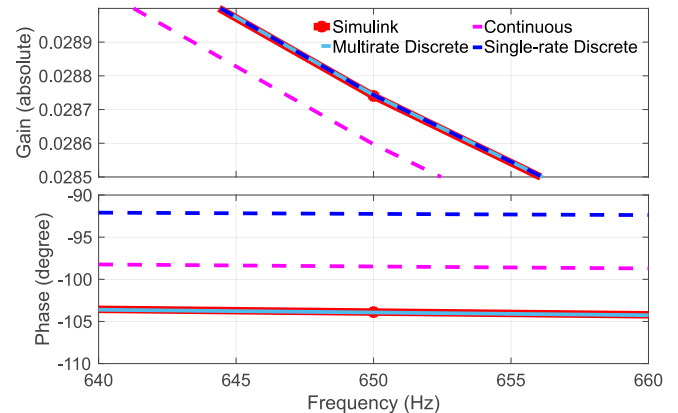


FIGURE 6. Zoomed frequency response using RL at 650 Hz.

the three linearized modeling approaches and compared with the frequency sweep results of the Simulink model over a frequency range of 50-1000 Hz with a step of 50 Hz each. The PHIL setup parameters are given in Table 1.

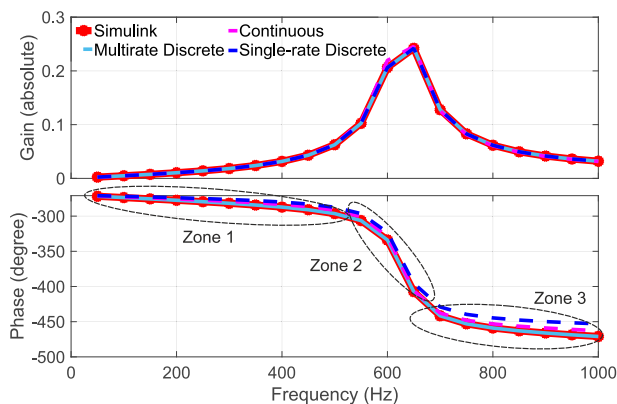
### A. RL LOAD

This section validates the modeling of the RL load via simulation. According to Fig. 5 and its zoomed plot at 650 Hz (Fig. 6), the linearized MDT model shows a higher accurate approximation of the Simulink model during the whole range with respect to the other models. As the frequency increases,



**TABLE 2. RL Accuracy Calculation Based on Simulations**

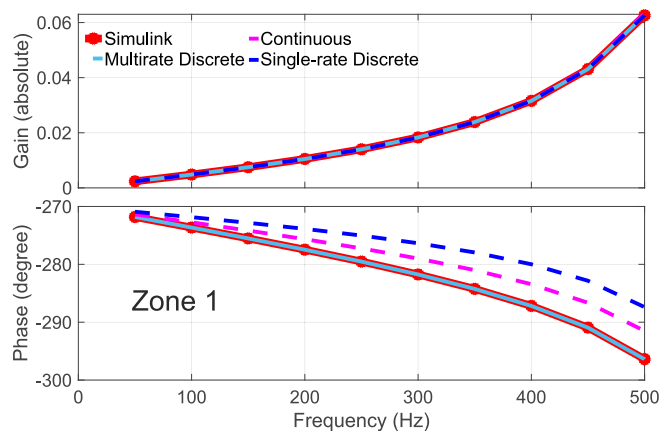
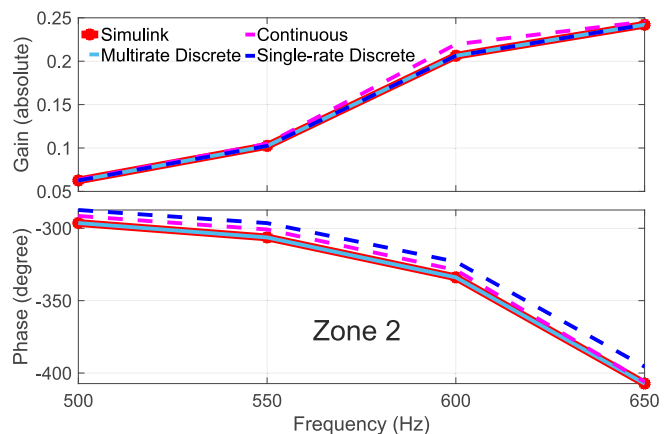
Model	Index	Error(%)	Index	Error(%)
CT	$AVG_{gain}$	0.4451	$WAVG_{gain}$	0.0055
SDT		0.0039		0.0001
MDT		<b>0.0039</b>		<b>0.0001</b>
CT	$AVG_{phase}$	4.2291	$WAVG_{phase}$	0.0391
SDT		9.1196		0.0872
MDT		<b>0.0399</b>		<b>0.0004</b>


**FIGURE 7. Frequency response comparison using RLC as HuT.**

phase deviations in the CT and SDT model increase as well, whereas the MDT modeling follows the reference throughout the frequency spectrum. It can be seen that the CT and SDT model s underestimate the phase values concerning the Simulink model. In addition to the bode diagrams, the accuracy is also calculated using the indexes formulated from (27) to (30), and compared in Table 2. As can be noted for phase indexes, the MDT achieves relatively negligible errors of at least 2 orders of magnitude smaller than the other two modeling approaches, confirming the accuracy of the proposed multi-rate discrete modeling approach.

### B. RLC LOAD

For further analysis regarding the accuracy of the MDT approach, it has also been examined considering the RLC load. The reason behind this testing lies in the fact that the RLC load has a certain resonance frequency, that in this case lies around 650 Hz, where any modeling errors may be amplified. Diagrams in Fig. 7 demonstrate the frequency behaviors of the PHIL system, where the spectrum range is divided into three main areas, smaller, around, and bigger than the resonance frequency shown in Figs. 8, 9, and 10, respectively. In the analyzed frequency range, the MDT model overlaps with the simulator output. On the other side, it can be noted that the CT and SDT models diverge from the reference for frequencies smaller and bigger than the resonance frequency of the RLC testing system. Gain and phase graphs are shown at the resonance frequency in Fig. 11.


**FIGURE 8. Frequency response using RLC as HuT, Zone 1.**

**FIGURE 9. Frequency response using RLC as HuT, Zone 2.**
**TABLE 3. RLC Accuracy Calculation Based on Simulations**

Model	Index	Error(%)	Index	Error(%)
CT	$AVG_{gain}$	1.2297	$WAVG_{gain}$	0.0133
SDT		0.0033		3.28e-05
MDT		<b>0.0045</b>		<b>4.02e-05</b>
CT	$AVG_{phase}$	1.1097	$WAVG_{phase}$	0.0119
SDT		2.4933		0.0245
MDT		<b>0.0013</b>		<b>1.31e-05</b>

The same as bode diagrams, Table 3 accredits the accuracy of the described analytical MDT modeling. Both phase error indicators in the table prove that the presented linear MDT is well-formulated and reproduces similar behaviors as the MDT Simulink model.

## VI. EXPERIMENTAL RESULTS

As shown in Fig. 12, a PHIL setup consisting of the real-time digital simulator (RTDS) and a linear power amplifier in the Energy Lab2.0 at Karlsruhe Institute of Technology (KIT) has been built-up to verify the accuracy of the proposed modeling approach. The grid model and low-pass filter in Fig. 1(b),

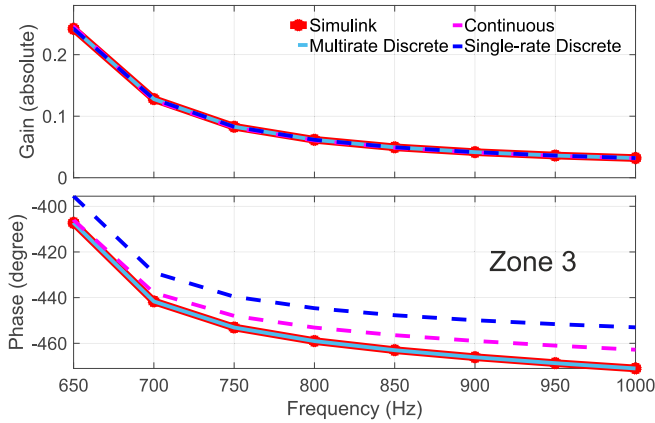


FIGURE 10. Frequency response using RLC as HuT, Zone 3.

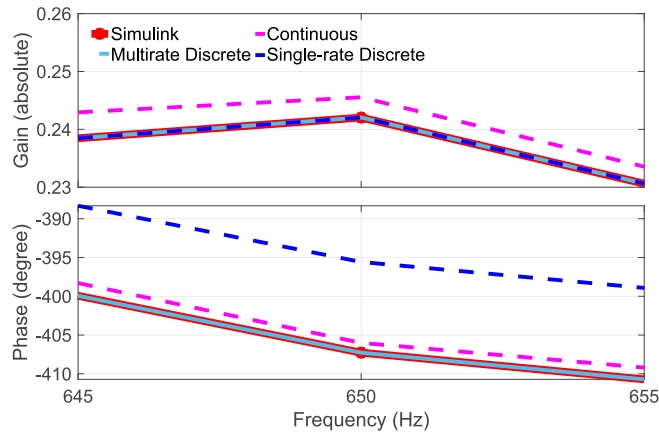


FIGURE 11. Zoomed frequency response using RLC as HuT.

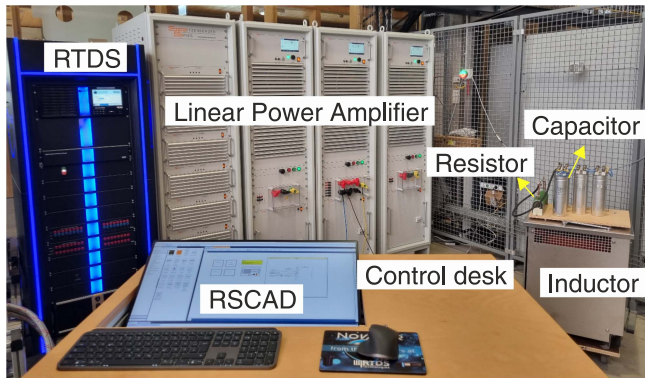


FIGURE 12. PHIL setup at the Energy Lab2.0, KIT.

are implemented in RSCAD to be compiled on the RTDS. The bilinear (trapezoidal) method explained in (14) is used in RSCAD for discretizing the first-order low-pass filter [23]. Through the small form-factor pluggable (SFP) connectors, RTDS communicates with the 15 kVA APS 15000 4-quadrant amplifier Spitzenberger & Spies (single phase) to provide the

TABLE 4. PHIL Experiment Parameter

Setup	Value	Unit
$V_s(rms)$	40	[V]
$T_{s1}, T_{d,DRTS}$	50	[ $\mu s$ ]
$T_{d,Conv}$	4	[ $\mu s$ ]
$\omega_c$	2	[kHz]
$C_{HuT}$	7.5	[ $\mu F$ ]
$L_s$	0.8	[mH]
$L_{HuT}$	$f_L(F)$	[mH]
$R_s$	1	[ $\Omega$ ]
$R_{HuT}$	$1 + f_R(F)$	[ $\Omega$ ]

TABLE 5.  $L_{HuT}$  Frequency Sensitivity

Frequency (Hz)	$L_{HuT}$ (mH)	$r_{HuT}$ ( $\Omega$ )
50	8.01	0.1288
60	8.0027	0.1436
75	7.992	0.1686
100	7.99761	0.2195
120	7.9636	0.2687
150	7.945	0.3559
180	7.9241	0.4598
200	7.9095	0.5368
250	7.8702	0.7355
300	7.827	1.008
360	7.7716	1.3455
400	7.7328	1.5870
450	7.683	1.9020
500	7.633	2.23
600	7.5331	2.902
720	7.418	3.716
750	7.391	3.917
800	7.347	4.25
900	7.264	4.903
1000	7.189	5.55

desired power to the connected loads. Delays of A/D and D/A conversions can be considered negligible with respect to the digital time step (i.e., 50  $\mu s$  due to the use of SFP connections). The rest of the delays (e.g. amplifier, sensor) are considered unitary as  $T_{d,Conv}$ , originating from the PA cabin. The parameters specifications for the experiment are provided in Table 4. Using the power components for relatively low-voltage/current operation, the temperature of the resistor does not considerably affect the resistivity. However, the values of the employed inductor (REO, 8mH /111 A, NPT-LD 100-111-8-150000) vary at different frequencies, whereas the used resistor (TE1000B1R0J) and capacitors (6 of KOMET C's 1,7 kV / 47  $\mu F$ , in series) remain relatively constant within the 50-1000 Hz range. Inductance and resistivity ( $r_{HuT}$ ) characteristics of  $L_{HuT}$  are then measured at different frequencies with the R&SHM8118 LCR-Messbrücken-/Messer LC meter and the results are provided in Table 5, to facilitate the reproducibility of the results. To verify the measurement accuracy

of the data in Table 5, the impedance of the  $L_{HuT}$  at each frequency is calculated using a Meatest M-142 multi-function generator as a current source and measuring the voltage of the  $L_{HuT}$ , showing a good match between datasheet data and experimental results. Based on these measurements,  $f_L(F)$  and  $f_R(F)$  are defined in (31) and (32) as functions of frequency to estimate actual values of  $L_{HuT}$  and  $r_{HuT}$  at each frequency.

$$f_L(F) = (5.9291e - 10)F^3 - (9.7235e - 07)F^2 - 0.00046659F + 8.0371 \quad (31)$$

$$f_R(F) = (3.7209e - 12)F^4 - (1.2197e - 08)F^3 + (1.4196e - 05)F^2 - (0.00028625)F + 0.11441 \quad (32)$$

### A. MEASUREMENT UNCERTAINTY

According to the uncertainty propagation of the used current/voltage transducers, the uncertainty of magnitude measurements is given in Table 8.

Then the uncertainty error of the gain measurements can be obtained as:

$$Y = I/V$$

$$dy = Y\sqrt{(di/I)^2 + (dv/V)^2} \quad (33)$$

Where  $Y$  is the loop admittance gain and  $dy$  is the gain error propagated by current and voltage sensors uncertainties, depicted as  $di$  and  $dv$ , respectively. As an example in the RL case, if a voltage equal to  $V = 40$  V is applied at a frequency of 50 Hz, the current  $I$  results to be equal to 11.3 A, where the gain uncertainty,  $dy$ , is equal to  $\pm 0.0034$  S. Likewise, in the RLC case,  $I$  is approximately 0.01 A, and  $dy$  is calculated as  $\pm 0.0035$  S.

### B. ACCURACY COMPARISON

Similar to Section V, the gain and phase of the loop admittance are obtained by measuring the amplitude and phase of induced current at each frequency up to 1000 Hz with a step of 50 Hz over that of the applied voltage. Results are shown in Figs. 13–16, where different modeling are compared with respect to the experimental reference. The experimental measurements shown in red color here are replaced with the simulated PHIL response in the previous section. Uncertainty bandwidth is also added to the gain subplot. The phase subplots of Figs. 13 and 15 for both HuTs graphically reveal that the proposed MDT modeling is verified to be the most accurate to the reference in the group of studied models. More illustrative plots to judge gain measurements are shown in Figs. 14 and 16.

Analytical accuracy calculation results are given in Tables 6 and 7. Beginning with Table 6, the smallest  $AVG_{gain}$  error among the considered approaches is equally achieved with SDT and MDT at 1.93%. However, all achieved  $AVG_{gain}$  errors can be considered acceptable since they are within

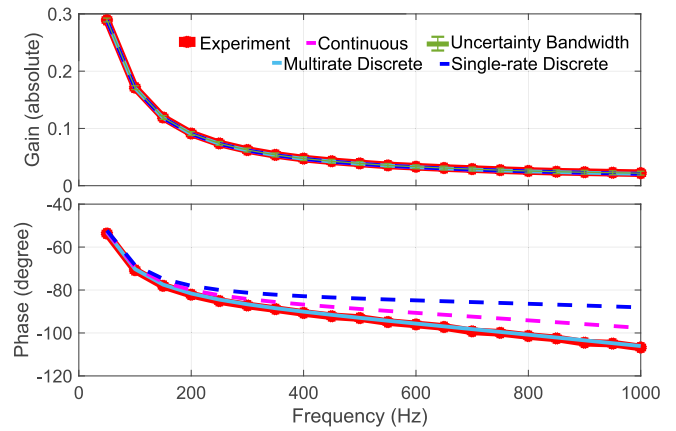


FIGURE 13. Frequency response comparison using RL as HuT.

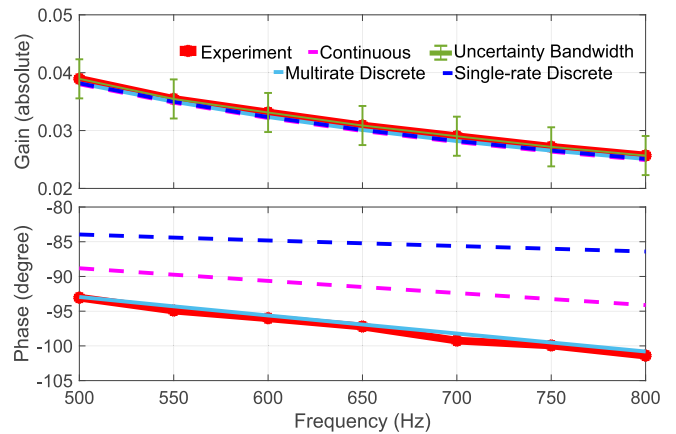


FIGURE 14. Zoomed frequency response using RL as HuT.

TABLE 6. RL Accuracy Calculation Based on Experiments

Model	Index	Error(%)	Index	Error(%)
CT		2.4409		0.0215
SDT	$AVG_{gain}$	1.9349	$WAVG_{gain}$	0.0164
MDT		<b>1.9349</b>		<b>0.0164</b>
CT		5.0939		0.0576
SDT	$AVG_{phase}$	10.3394	$WAVG_{phase}$	0.1077
MDT		<b>0.6033</b>		<b>0.0220</b>

the uncertainty error of  $\pm 1.22\%$  ( $dy = 0.0034$  S). However, considering the phase accuracy with the  $WAVG_{gain}$  index, MDT achieves the smallest weighted errors. The phase-related index reveals that MDT is around ten times more accurate in  $AVG_{phase}$  and at least 2.5 times better in  $WAVG_{phase}$  than the other two methods, achieving the best phase match with the experimental response. This implies a better representation of the system delays, which is fundamental to estimating the stability of the PHIL system.

In Table 7, where the experiment has been repeated with the RLC load, the MDT shows errors lower than 1% in  $AVG_{phase}$



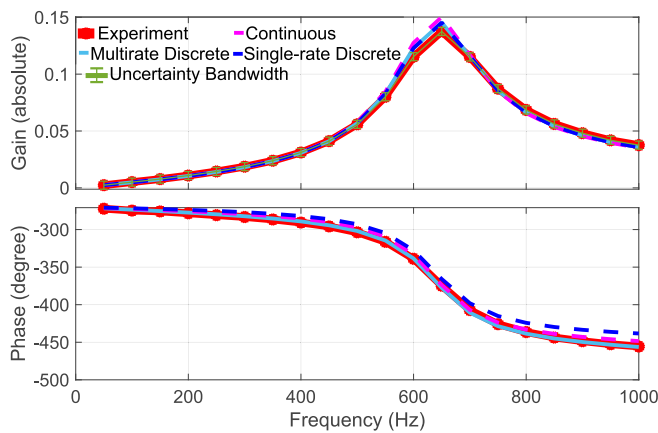


FIGURE 15. Frequency response comparison using RLC as HuT.

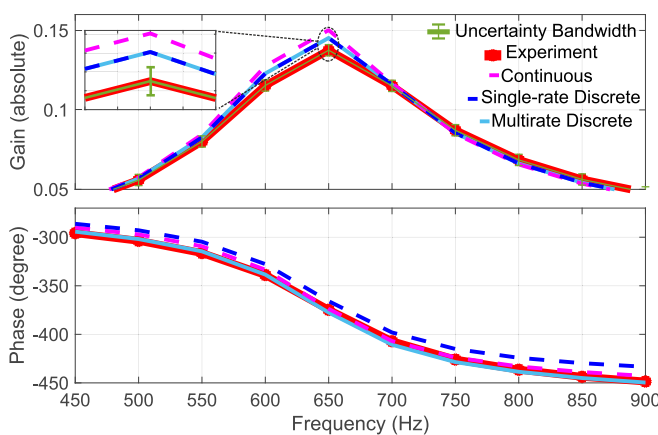


FIGURE 16. Zoomed frequency response using RLC as HuT.

TABLE 7. RLC Accuracy Calculation Based on Experiments

Model	Index	Error(%)	Index	Error(%)
CT	$AVG_{gain}$	3.7050	$WAVG_{gain}$	0.0612
SDT		2.9292		0.0599
MDT		<b>2.9295</b>		<b>0.0599</b>
CT	$AVG_{phase}$	1.2171	$WAVG_{phase}$	0.0177
SDT		2.6379		0.0297
MDT		<b>0.4030</b>		<b>0.0073</b>

TABLE 8. Uncertainty of Magnitude Measurements [21]

Parameter	Range	Error	Unit
$I(rms)$	$\pm 51$	$\pm 0.15$	[A]
$V(rms)$	$\pm 650$	$\pm 0.39$	[V]

and 0.01% in that of  $WAVG$ . This proves a better phase accuracy of the MDT model with respect to the currently proposed models.

Therefore, considering the performed experimental accuracy investigations, the MDT approach shows higher accuracy for both examined HuTs.

## VII. CONCLUSION

This article examines the accuracy of a voltage-type ideal transformer method (V-ITM) power hardware-in-the-loop (PHIL) modelings by testing RL and RLC loads as hardware under test (HuT). In addition to classical approaches, namely, continuous-time (CT) and single-rate discrete-time (SDT) modeling methods, a multi-rate discrete-time method (MDT) is proposed. The MDT method uses a relatively short sampling time to model the analog hardware section of the setup and a larger time step for modeling the real-time simulated models. Accuracy is assessed with defined error indexes based on the closed-loop transfer function, which describes the admittance of the loop. The frequency response of the proposed linearized MDT model is verified with its Simulink model using bode plots and error indexes. To further validate the modeling approach, experimental results with PHIL evaluation have been obtained, also considering the uncertainty bandwidth of the gain measurements. In both HuT cases, the proposed MDT modeling outperforms the primarily used CT and SDT modelings, showing increased accuracy, particularly for the system phase.

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**DUSTIN KOTTONAU** received the B.Eng. degree in mechatronics and the M.Sc. degree in electrical engineering from the University of Duisburg-Essen, Duisburg, Germany in 2013 and 2018, respectively, and the Ph.D. degree in electrical engineering with the prestigious Karlsruhe Institute of Technology, Karlsruhe, Germany in 2022. His research interests include real-time simulation and optimization within power hardware in the loop methodology. His current research interests revolve around implementing and enhancing real-time simulation techniques, aiming to improve the efficiency, and performance of power systems.



**GIOVANNI DE CARNE** (Senior Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the Polytechnic University of Bari, Bari, Italy, in 2011 and 2013, respectively, and the Ph.D. degree from the Chair of Power Electronics, Kiel University, Kiel, Germany, in 2018. He was a Postdoctoral Fellow with Kiel University, working on HVdc control and services until 2019. He is currently a Tenure-Track Professor with the Institute for Technical Physics with the Karlsruhe Institute of Technology, Karlsruhe, Germany, where he leads the Real Time System Integration Group and he is the head of the Power Hardware In the Loop Lab. In 2020, he was the recipient of the Helmholtz Young Investigator Group for the project Hybrid Networks: a multi-modal design for the future energy system. He has authored and coauthored more than 80 peer-reviewed scientific papers. His research interests include power electronics integration in power systems, solid-state transformers, real-time modelling, and power hardware in the loop. He is an Associate Editor for the *IEEE Industrial Electronics Magazine* and IEEE OPEN JOURNAL OF POWER ELECTRONICS. He is the Chairman of the IEEE PES Task Force on Solid State Transformer Integration in distribution grids.

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**FARGAH ASHRAFIDEHKORDI** (Graduate Student Member, IEEE) received the B.Sc. degree in electrical engineering degree from the Babol Noshirvani University of Technology, Babol, Iran, in 2016, and the M.Sc. degree in electrical engineering from the Amirkabir University of Technology, Tehran, Iran, in 2019. He is currently working toward the Ph.D. degree in stability and accuracy analysis of the Power Hardware-in-the-Loop setups with the Real Time System Integration group, EnergyLab 2.0 with the Karlsruhe Institute

of Technology, Karlsruhe, Germany. His research interests include power electronics integration in power systems, grid-tied converters control, stability analysis, real-time simulations, and power hardware in the loop.