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Test Structures for the Characterization of the Gate Resistance in 16 nm FinFET RF Transistors

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Abstract: The gate resistance is a parasitic element in transistors for RF and millimeter-wave circuits that can negatively impact power gain and noise figure. To develop accurate device models, a reliable measurement methodology is crucial. This article reviews the standard measurement methodology used in the literature and proposes also an additional method, which is evaluated using suitable test structures in a 16 nm FinFET process. The advantages and disadvantages of the two approaches are discussed along with their respective application scenarios.

Keywords: gate resistance; characterization; de-embedding; radio-frequency MOSFETs (RF MOSFETs); FinFET

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1. Introduction

Following the emergence of several new applications in the radio frequency (RF) and millimeter-wave (mmW) frequency range in the last decades, a huge effort was put into the implementation of fully integrated transceivers in CMOS processes. As a result, CMOS has evolved from a purely digital technology to a competitive candidate for high-frequency analog circuits. This was made possible by the continuous downscaling and layout optimization, which has allowed values of unity gain frequency f_t and maximum oscillation frequency f_{max} close to 400 GHz [1,2] to be reached. To this day CMOS has become in many ways competitive as RF technology with the higher-performance III-V semiconductor processes like GaN [3], but with the advantage of higher yield, ease of mass production and much lower cost.

The gate resistance R_g is a key parasitic parameter for RF transistors, as it has a significant impact on f_{max} and on the noise performance [4,5]. From the analog circuit perspective, this translates into a severe limitation mainly for power amplifiers (PA) and low-noise amplifiers (LNA). In order to keep R_g low, circuit designers have to select a suitable geometry for the active devices [6], and to do so it is crucial that the behavior of R_g be correctly captured in the compact models of the transistors. In the last few years much research work has been published on this topic, achieving very good results [7–11]. Since the target of any model is to reproduce measurement results as closely as possible, using the best-known measurement methodology is a fundamental pre-requisite for accurate modeling. The measurement methodology is the main focus of this article.

One key aspect in device characterization at mmW frequencies is the de-embedding of the on-chip interconnect parasitics, which are caused mainly by the pads and feedlines. Most of the traditional de-embedding methods are based on a lumped representation of the parasitics and make use of one or more auxiliary structures to eliminate their contributions and extract the behavior of the device under test (DUT). The most popular is the open-short method [12], which is used as reference in this article. The main limitation of the lumped methods is that they neglect the distributed nature of the interconnects at high frequency. In order to partially take this effect into account, some more refined

methods have been devised [13,14], which achieve higher accuracy but require additional de-embedding structures.

In the analyzed literature the standard common-source structure with open-short de-embedding is consistently used. In this article we consider also an alternative structure with the transistor connected in capacitor mode, called "capacitor-like" structure, which requires only the open de-embedding step. The article is organized as follows: in Section 2 the physical origin of the various contributions of the gate resistance is briefly explained. In Section 3 the main features of the two measurement methodologies are presented along with a list of fabricated test structures in a 16 nm FinFET process. In Section 4 the measurement setup is described and some of the figures of merit utilized throughout the paper are introduced. In Section 5 the capacitor-like structure is analyzed in detail and some design guidelines are derived to achieve accurate measurement results. In Section 6 the standard and capacitor-like structures are compared and finally in Section 7 the conclusions of this study are presented.

2. The Gate Resistance: Physical Origin and Modelling

The gate resistance R_g is particularly detrimental for analog applications, in which the metal oxide semiconductor (MOS) transistor is typically used as common-source amplifier. In the case of PAs, R_g causes a significant drop of the already scarce power gain, whereas in the case of LNAs it leads to increased thermal noise and degradation of the noise figure (NF) [15]. The origin of R_g can be easily understood looking at the physical structure of the gate stack of the MOS transistor, which includes the metal and oxide layers. The gate stack plays a fundamental role in that it controls the on/off state of the device in digital applications and sets its bias point in analog applications. Over the years it has undergone several developments, with a major breakthrough being achieved in the first decade of the 2000s with the transition from the SiO_2 oxide layer with polysilicon gate electrode to the high-k dielectrics with metal gate electrode [16,17]. The physical implementation of the gate stack has a strong impact on the threshold voltage V_t and on the gate leakage current. The highest influence on R_g comes from the gate material, with the lower-resistivity metal gate providing significant benefit over the polysilicon one.

The modeling of R_g is a rather complicated topic due to the multiple contributions involved and the non-trivial dependency on the transistor geometrical parameters. In CMOS technologies a multi-finger layout is normally used for RF transistors to achieve the desired device width while keeping R_g low. Considering the relatively simple case of a planar technology, the input resistance presented by a single gate finger can be modeled by means of a distributed resistive-capacitive (RC) network, as shown in Figure 1. The main contributions are the bias-independent electrode resistance, which can be decomposed into a horizontal ($r_{el,h}$) and a vertical component ($r_{el,v}$), and the bias-dependent channel resistance $r_{ch}(V_g)$, which is connected to the electrode through the oxide capacitance c_{ox} [7,8,10,18].

Unfortunately this distributed representation of the MOS structure cannot be easily integrated in a compact model of the transistor, where it is preferable to use only one node for each terminal to prevent long simulation times at circuit level. For this reason the distributed network is typically simplified into a single lumped resistance R_g placed at the input of the equivalent circuit [19], which can be written in the form:

$$R_g = R_{el,h} + R_{el,v} + R_{ch} \tag{1}$$

where $R_{el,h}$, $R_{el,v}$ and R_{ch} are lumped equivalent resistances which absorb the contributions of the elementary resistances of Figure 1. In terms of the device parameters, $R_{el,h}$ is proportional to W/L_g, whereas $R_{el,v}$ is proportional to L_g/W [20], where W is the finger width and L_g the gate length. Since each component of the model has to be bias-independent, the dependency of R_{ch} on V_g is normally sacrificed, and the value at one typical V_g operating point is chosen.

In FinFET technologies the structure of the gate electrode is more complicated due to the inhomogeneous profile of the gate finger resulting from the presence of the fins [21,22].

This gives rise to additional components of R_g, so that careful optimization of the transistor is required to limit R_g to acceptable values. This is one of the main reasons behind the choice of the 16 nm FinFET process for this research work.

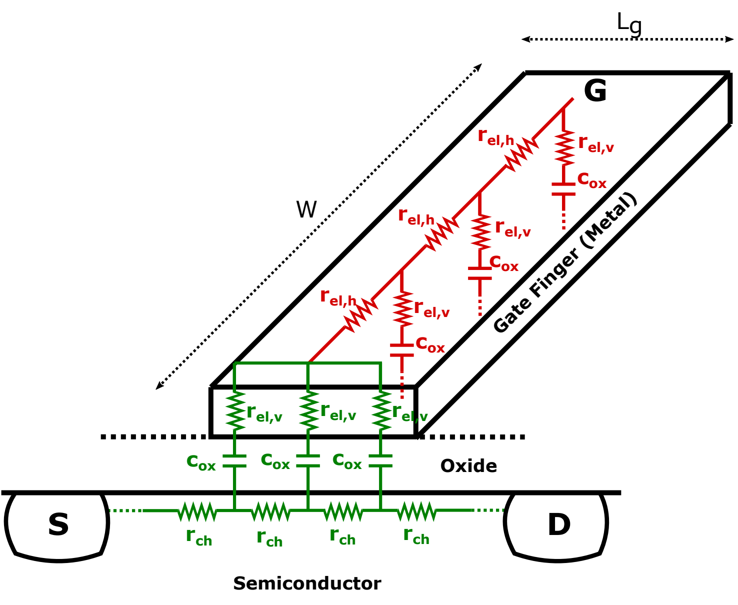


Figure 1. Distributed model of the input resistance of a single gate finger, including the gate electrode, the oxide and the channel resistance contributions.

3. Measurement Structures for the Gate Resistance

The standard method for the measurement of the gate resistance is based on the structure in Figure 2, which consists of an RF transistor in common-source configuration routed to RF ground-signal-ground (GSG) pads. This is the structure which is commonly used to extract R_g as well as the other equivalent-circuit parameters of the MOS transistor, and requires open and short structures to de-embed the pads and feedline parasitics. Using the small-signal equivalent circuit of the MOS transistor, the gate resistance can be extracted from the two-port Y-parameters using the formula $R_g = Re(1/Y_{11})$ [10], under the assumption that the source and drain parasitic resistances R_s and R_d are negligible with respect to R_g.

The alternative capacitor-like structure in Figure 3 consists of an RF transistor with the gate connected to both the input and output pads, and source and drain shorted to ground. The naming is due to the fact that in this configuration the channel is shunted out and the transistor behaves as a capacitor C_{gg} in series with R_g, where C_{gg} is the total capacitance on the gate of the transistor.

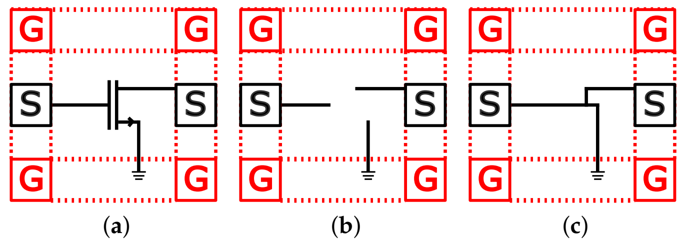


Figure 2. Standard structures for R_g measurement. (**a**) Main structure. (**b**) Open structure. (**c**) Short structure.

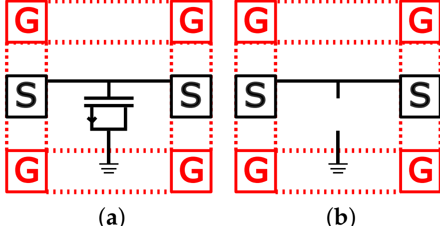


Figure 3. Capacitor-like structures for R_g measurement. (**a**) Main structure. (**b**) Open structure.

One key advantage of this structure is that it requires only the open de-embedding step. Indeed, once the shunt parasitic components of the pads is removed with the open de-embedding, one is left with a T-network formed by the feedlines and the DUT, as shown in Figure 4. Taking Z_{21} of this network automatically excludes the contribution of the feedlines (Z_{fl}) and no additional de-embedding step is required. Based on considerations very similar to those done for the standard structure, it is found that $R_g = Re(Z_{21})$, again under the assumption that $R_s, R_d \ll R_g$. It should be noted that this concept can not be used in a one-port configuration, as it would require both the open and short de-embedding steps.

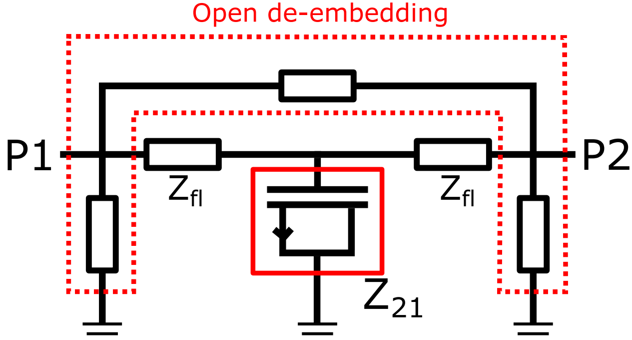


Figure 4. Illustration of the gate resistance extraction methodology using the capacitor-like structure.

For this study 18 test structures utilizing both the standard and capacitor-like concept were fabricated in a 16 nm FinFET process. The various structures differ in the geometrical parameters of the transistor, which are the number of fins N_{fins}, the number of gate fingers N_{fing}, the gate length L_g and the multiplicity M, that is, the number of devices in parallel. A graphical representation of all these parameters is provided in Figure 5.

The list of all the available test structures with the related geometrical features is presented in Table 1. All the devices are RF transistors with the lowest threshold voltage (V_t) available in the process design kit (PDK). The focus is on N_{fins}, L_g and M because they have the largest impact on R_g, whereas N_{fing} is kept constant because of its weaker influence. In addition to several instances of the capacitor-like structure, three standard structures with different values of M (1, 4, 8) were fabricated for comparison. For both types of structures, the on-chip interconnections are de-embedded up to the third level of metallization (M3).

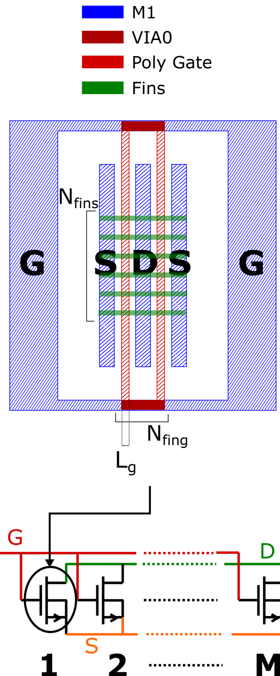


Figure 5. Graphical representation of the main geometrical parameters of a FinFET transistor (N_{fins}, N_{fing}, L_g, M).

Table 1. List of DUTs on the 16 nm FinFET testchip.

DUT	Structure Type	N_{fins}	N_{fing}	L_g[nm]	M
1	Capacitor-like	6	10	20	1
2	Capacitor-like	10	10	20	1
3	Capacitor-like	16	10	20	1
4	Capacitor-like	20	10	20	1
5	Capacitor-like	6	10	20	4
6	Capacitor-like	10	10	20	4
7	Capacitor-like	16	10	20	4
8	Capacitor-like	20	10	20	4
9	Capacitor-like	6	10	20	8
10	Capacitor-like	10	10	20	8
11	Capacitor-like	16	10	20	8
12	Capacitor-like	20	10	20	8
13	Capacitor-like	20	10	16	8
14	Capacitor-like	20	10	18	8
15	Capacitor-like	20	10	24	8
16	Standard	20	10	20	1
17	Standard	20	10	20	4
18	Standard	20	10	20	8

4. Measurement Setup, Simulation Setup and Figures of Merit

The measurement setup consists of a FormFactor Elite 300/AP-0011 Probe Station for 300 mm wafers, a Keysight N5227A PNA Vector Network Analyzer (VNA) with frequency range from DC up to 67 GHz and FormFactor Infinity RF GSG probes for on-wafer probing with frequency range from DC up to 110 GHz. In order to be able to measure the S-parameters up to 110 GHz, the frequency range of the VNA is extended using a Keysight N5250CX10 millimeter-wave module for each port. The output of the mmW module and the input of the RF probes are connected using 1 mm coaxial cables for higher-order mode suppression. For the two-port S-parameter measurement the VNA was calibrated up to the probe tips using a standard two-port short-open-load-thru (SOLT) method. A block-diagram and a picture of the measurement setup are shown in Figure 6a,b respectively.

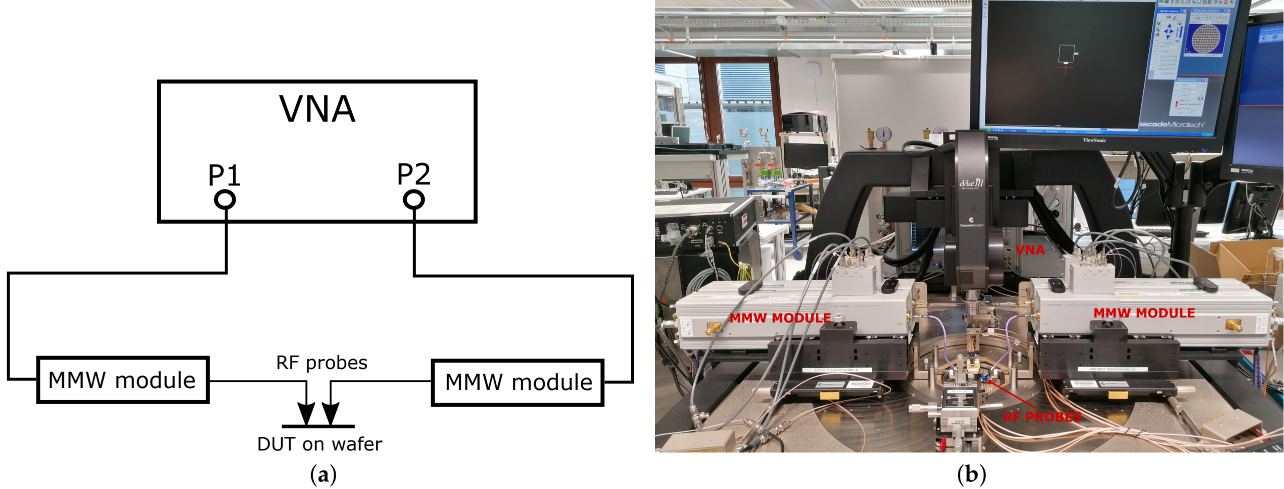


Figure 6. Block-diagram and photograph of the measurement setup. (**a**) Block-diagram. (**b**) Photograph.

The measurement was carried out with RF input power $P_{in} = -20$ dBm at both ports, for values of the gate bias voltage V_g ranging between 0 V and 0.8 V. Only for the standard structure was a drain bias voltage $V_{DD} = 0.8$ V used.

The simulation setup consists of a standard two-port S-parameter analysis with frequency range from DC up to 110 GHz, which is carried out using the Spectre simulator and the RF transistor models from the PDK.

In order to assess the quality of the measurement, the relative deviation ΔR_g of the measured gate resistance ($R_{g,meas}$) from the simulated one ($R_{g,sim}$) was used:

$$\Delta R_g = \frac{R_{g,meas} - R_{g,sim}}{R_{g,meas}} \tag{2}$$

One issue with this figure of merit is that the details of the device model from the foundry are not known, therefore using $R_{g,sim}$ as reference for the measurements could be questionable. For this reason, as a preliminary step, it was verified that $R_{g,sim}$ follows the expected scaling law with respect to N_{fins} and M [23], given by:

$$R_g = \frac{R_{conn} + R_{el,v}/N_{fins} + R_{el,h} \times N_{fins}}{M} \tag{3}$$

where R_{conn} is a constant which includes end resistances, contact resistances and interconnects up to M3. This result, shown in Figure 7, justifies the usage of the foundry model as reference to assess the quality of the measured data.

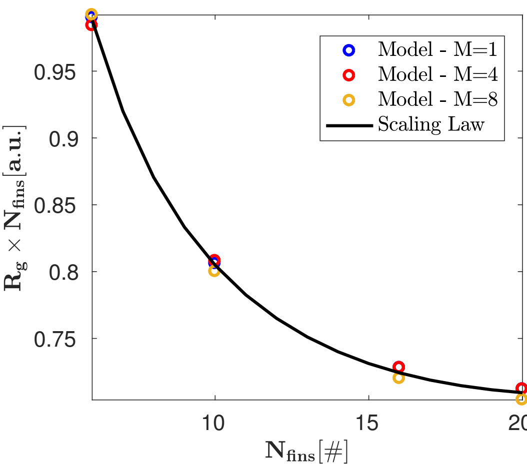
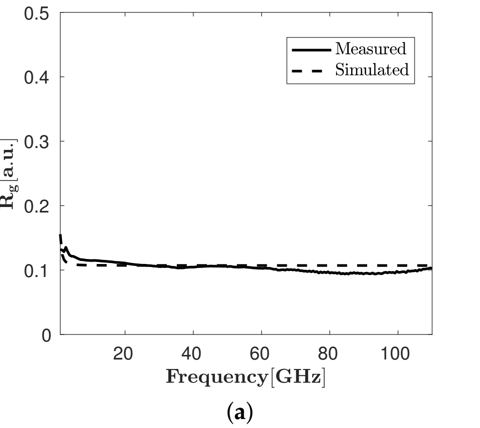


Figure 7. Scaling behavior of gate resistance vs. N_{fins} and M obtained from foundry model and from scaling law ((3) with $R_{el,v} = 155.4\,\Omega$, $R_{el,h} = 0.3\,\Omega$, $R_{conn} = 21.7\,\Omega$) for an RF transistor with $N_{fing} = 10$, $V_g = 0.4\,\text{V}$ at $f_0 = 50\,\text{GHz}$.

5. Capacitor-like Structures

This section focuses on the analysis of the capacitor-like structure. The plot of R_g vs. frequency for $V_g = 0.4\,\text{V}$ in Figure 8a shows very good agreement with the foundry model over the entire frequency range. On the other hand the plot of $|\Delta R_g|$ over frequency for different bias conditions in Figure 8b shows that the best agreement between measurement and simulation is obtained for $V_g = 0.4\,\text{V}$. The reason is that, as explained in Section 2, the dependency of R_{ch} on V_g is neglected in the model, and a single value at a "convenient" V_g is taken. Based on these data, the chosen bias point seems to be $V_g = 0.4\,\text{V}$, which is a reasonable choice, as it was observed to be the bias condition which optimizes f_t. In practice, since the RF transistor is biased most of the times either exactly at $V_g = 0.4\,\text{V}$ or at a value close to it, the error introduced by this approximation is small.



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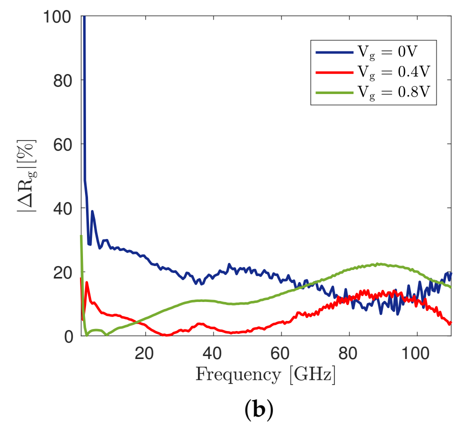


(**b**)

Figure 8. R_g at $V_g = 0.4\,\text{V}$ (measured and simulated) and $|\Delta R_g|$ for different values of V_g as a function of frequency for DUT12. (**a**) Measured and simulated R_g vs. frequency on DUT12 for $V_g = 0.4\,\text{V}$. (**b**) $|\Delta R_g|$ vs. frequency of DUT12 for different values of V_g.

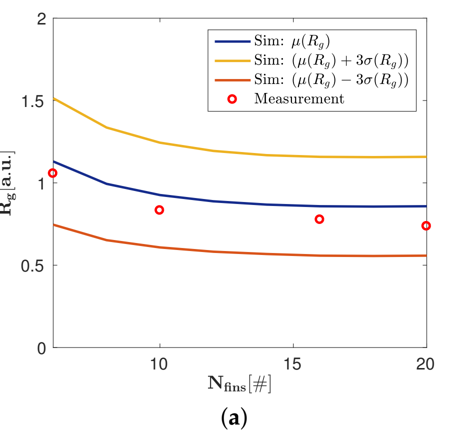
Table 2 reports the values of ΔR_g for different DUTs at $V_g = 0.4\,\text{V}$ and $f_0 = 50\,\text{GHz}$. The value $f_0 = 50\,\text{GHz}$ is chosen because it is approximately in the middle of the analyzed frequency range. It can be observed that a minimum total device width is required to achieve good agreement between measurement and simulation. The reason is that, for the smallest devices like DUT1, the total gate capacitance C_{gg} of the transistor is smaller or comparable to the pad capacitance $C_{pad} \sim 25\,\text{fF}$, which results in a large numerical error in

the open de-embedding step. This phenomenon can be also observed simulating the de-embedding process using an approach similar to that of [24]. Based on these considerations, a large value of M should be used if the width of the transistor is small. This is instead not necessary if the width of the device is large enough, as in the case of $N_{fins} = 20$.

Table 2. ΔRg in % at $f_0 = 50\,\text{GHz}$ with $V_g = 0.4$ V for capacitor-like structures using transistors with various combinations of N_{fins} and M.

M	N_{fins}			
	6	10	16	20
1	−52	−18.3	−5.6	3.9
4	9	3.8	4.2	−1.6
8	1.7	−1.8	−4.2	−1.7

In Figure 9 the measured R_g is compared to simulations as a function of the geometrical parameters N_{fins} and L_g. In order to capture the device-to-device (mismatch) variations and the die-to-die, wafer-to-wafer and lot-to-lot (process) variations, Montecarlo simulations with 2000 samples are run for each set of parameters. The results are displayed in three different curves: the mean value $\mu(R_g)$ of the gate resistance and the so-called $\pm 3\sigma$ curves, i.e., the quantities $\mu(R_g) \pm 3\sigma(R_g)$, where $\sigma(R_g)$ is the variance of R_g. These are relevant because they define the interval in which R_g falls with a probability of 99.7%, and therefore provide a good estimation of the process and mismatch variation. The measured data show very good correlation with $\mu(R_g)$ and lie completely in the interval delimited by the $\pm 3\sigma$ curves. Based on these simulation results, an overall R_g fluctuation of up to 55% above or below the mean value is expected. One interesting observation from Figure 9b is that the spread of R_g becomes tighter for large values of L_g. This is expected because L_g is one of the transistor parameters which is mostly affected by the process variation. Since the fluctuation δL_g is independent of L_g, its impact decreases as L_g becomes larger.



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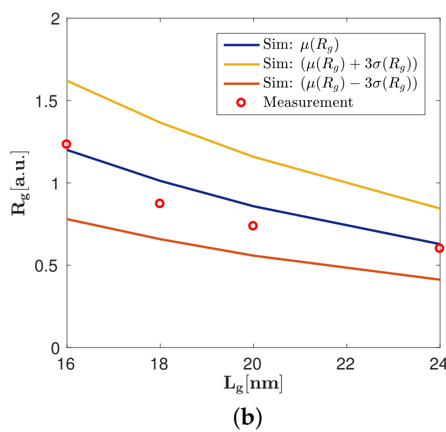

(**b**)

Figure 9. Measured and simulated R_g from capacitor-like structures with $M = 4$ at $f_0 = 50\,\text{GHz}$ and $V_g = 0.4\,\text{V}$ as a function of N_{fins} and L_g. (**a**) Gate Resistance vs. N_{fins} ($L_g = 20\,\text{nm}$, $N_{fing} = 10$). (**b**) Gate Resistance vs. L_g ($N_{fins} = 20$, $N_{fing} = 10$).

6. Comparison between Standard and Capacitor-like Structures

In order to make an effective comparison between the two types of structure, standard DUTs 16, 17 and 18 have been included in the testchip, having the same transistor parameters as capacitor-like DUTs 4, 8 and 12 respectively. Comparing ΔR_g of the three pairs of structures, it is found that the standard structure gives the best results for $M = 1$, as shown in Table 3. Larger values of M (4 and 8) lead to larger deviations and should be avoided. In this specific case the capacitor-like structure is not very sensitive on M due to the large device width ($N_{fins} = 20$), but in general it shows the opposite behavior, as discussed in

Section 5. Unlike the capacitor-like structure, in the standard structure R_g is not connected in parallel with C_{pad}, therefore the higher C_{gg} resulting from the larger M does not bring any advantage to the measurement. On the contrary, the larger number of devices in parallel exacerbates the error caused by the two-step de-embedding methodology. Therefore the design recommendation is to keep M as low as possible, which is excatly the opposite as in the case of the capacitor-like structure. All in all, the achievable ΔR_g with the two structures is comparable if the recommended value of M is used in each case.

Table 3. ΔRg in % at $f_0 = 50\,\mathrm{GHz}$ with $V_g = 0.4\,\mathrm{V}$ for standard and capacitor-like structures with $N_{fins} = 20$, $N_{fing} = 10$, $L_g = 20\,\mathrm{nm}$ and different values of M.

Structure Type	*M*		
	1	**4**	**8**
Standard	1.7	16.4	21
Capacitor-like	3.9	−1.6	−1.7

The second important comparison criterion is the stability of the measured R_g over frequency, which could be potentially influenced by the de-embedding structures. It can be quantified by means of the normalized standard deviation over frequency $\hat{\sigma}_{R_g}/\overline{R_g}$, where $\overline{R_g}$ and $\hat{\sigma}_{R_g}$ are respectively the mean value and the standard deviation of R_g over frequency, defined as:

$$\overline{R_g} = \frac{1}{N}\sum_{i=1}^{N} R_g(f_i) \tag{4}$$

$$\hat{\sigma}_{R_g} = \sqrt{\frac{1}{N}\sum_{i=1}^{N}(R_g(f_i) - \overline{R_g})^2} \tag{5}$$

with N being the number of frequency points. The normalized standard deviation is plotted in Figure 10 as a function of V_g for the standard and capacitor-like structures with different values of M. It can be observed that the measurements performed with the two structures show a variation over frequency between 2% and 10%. In most cases the variation is between 2% and 5%, with the exception of the capacitor-like structure with $M = 1$ and the standard structure with $M = 8$, which show up to 7% and 10% deviation respectively. This shows that the standard structure with large M and the capacitor-like structure with small M represent the worst case not only in terms of agreement with the model, as discussed in Sections 5 and 6, but also in terms of frequency stability.

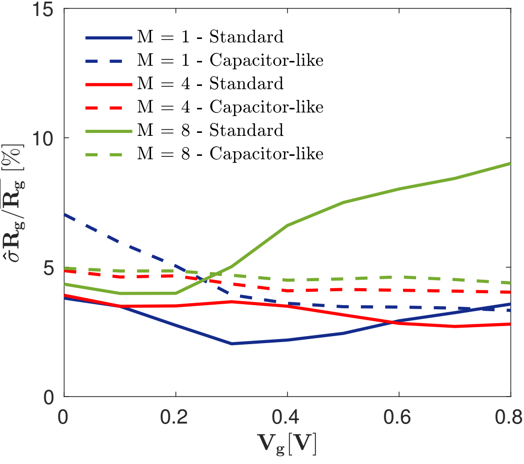

Figure 10. Normalized variance of R_g over frequency as a function of V_g for standard (DUT 16, 17, 18) and capacitor-like (DUT 4, 8, 12) structures.

7. Conclusions

This article provided an overview of the physical origin of the gate resistance in MOS transistors and discussed its impact on the performance of analog circuits. It discussed two different methodologies for the characterization of the gate resistance itself, based on the standard and capacitor-like structures, which were analyzed and compared with the aid of fabricated test structures in a 16 nm FinFET process. It was found that the design guidelines to achieve best accuracy in the two types of structure are somehow opposite: for the standard structure there is a constraint on the maximum transistor size, whereas for the capacitor-lilke structure there is a constraint on the minimum size. Following these guidelines, the two methods achieve overall similar agreement with the foundry model and similar variation over frequency. For the capacitor-like structure, a process and mismatch variation study based on Montecarlo simulations was performed, showing that the gate resistance can fluctuate up to 55% above and below the average value.

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