Time Domain Modeling of Zero Voltage Switching behavior considering Parasitic Capacitances for a Dual Active Bridge

Fabian Sommer[1*], Nikolas Menger[1], Tobias Merz[1], Nils Soltau[2], Shiori Idaka[2], Marc Hiller[1]
1 Elektrotechnisches Institut, Karlsruhe Institute of Technology, Karlsruhe, Germany
2 Mitsubishi Electric Europe B.V., Ratingen, Germany
*E-mail: fabian.sommer@kit.edu

***Abstract*—To increase the switching frequency in DC/DC converters, soft switching is necessary to limit switching losses. In case of the Dual Active Bridge (DAB), Zero Voltage Switching (ZVS) is used to reduce switching losses. Since the ZVS behavior of the DAB depends on multiple parameters, an accurate model is necessary to ensure operation with minimal losses by applying ZVS. This paper presents an accurate capacitance based time domain (CTD) model for the resonant commutation which enables the calculation of the minimal necessary current, the optimal deadtime as well as the voltage error caused by the nonideal commutation. The parasitics and therefore nonideal behavior of the MOSFETs are considered to further increase accuracy. The model can be used for all operating points commonly applied in single (SPS) and triple phase shift (TPS) modulation. Measurement results obtained with a 500 kW DAB prototype proves the high accuracy of the model.**

***Keywords*—Dual Active Bridge, Zero Voltage Switching, DC/DC Converter, Soft Switching**

I. Introduction

The ongoing development of wide bandgap semiconductors, especially for high current and high blocking voltage ratings enables new applications for galvanically isolated DC-DC converters. One of these converters is the Dual Active Bridge (DAB) first introduced in 1991 in [1]. The main advantages of the DAB are a wide operation range, bidirectional power transfer, high switching frequencies enabled by soft switching while maintaining high efficiency and a reduced effort for passive components [2]. In recent years, the power level of such DABs is constantly rising which results in an increasing impact of parasitic influences and nonideal behavior as shown in [3]- [5]. The most important effect that is affected by these influences, concerning proper operation and minimal switching losses, is the resonant Zero Voltage Switching (ZVS) behavior of the DAB. Therefore, to increase the efficiency at all operating points, the nonideal ZVS commutation must be taken into account. Additionally, the finite gradient of the voltage in case of the resonant ZVS commutation can influence the operation of the DAB under light load significantly [6]. There are many approaches to model the resonant commutation as well as ZVS operation of the DAB. The easiest and most common modeling approach is to assume that solely negative current through the turned-on MOSFET always leads to a ZVS turn-on event [7]. However, this method does not consider the parasitic components responsible for nonideal ZVS. A more accurate approach is the current-dependent charge-based (CDCB) ZVS modeling [8], [9]. For this method the energy stored in the magnetic field of the inductor $E_{\mathrm{L}\sigma} = \frac{1}{2} L_\sigma i_{\mathrm{sw}}^2$ is compared to the energy E_{Coss} necessary to charge and discharge the capacitances C_{OSS} of the MOSFETs. With this approach, an accurate statement about the ZVS limits can be made. Nevertheless, no information about the necessary deadtime and voltage on the secondary side is taken into account. However, there are more advanced charge-based models which include the secondary side voltage without including the time course of the voltage $v_{\mathrm{AC},1/2}$ and current i_{AC} as shown in [10]. In this paper, a capacitance based time domain (CTD) model, which was introduced in [6], is presented and improved to describe the ZVS behavior more accurately. It enables the calculation of the optimal deadtime $T_{\mathrm{dt,opt}}$, the minimum necessary switching current $I_{\mathrm{sw,min}}$, the voltage time area error Φ_{error} caused by the commutation as well as the voltage $v_{\mathrm{AC},1/2}$ and current i_{AC} time course for all operating points possible in a DAB. Furthermore the nonlinear behavior of the MOSFET capacitances is also considered [11]. The model is validated using measurements of different operating points on a $500\,\mathrm{kW}$ DAB prototype first introduced in [5].

Figure 1 shows the typical waveforms for Single Phase Shift (SPS) modulation and Triangular Current Modulation (TCM), which is a special case of the Triple Phase Shift (TPS) modulation. These are the most commonly used modulation schemes for a DAB. SPS is used for similar DC-link voltages $V_{\mathrm{DC1}} \approx V_{\mathrm{DC2}}$ whereas TCM is used for different voltage transfer ratios $V_{\mathrm{DC1}} \neq V_{\mathrm{DC2}}$ [12]. For SPS, all switching events should ideally utilizing ZVS to reduce switching losses, whereas TCM will have four zero current switching events and two ZVS transistions as shown in fig. 1.

II. Nonlinear MOSFET Capacitance C_{OSS}

Caused by the p-n junction structure of the vertical power MOSFET shown in fig. 2 (a), unavoidable parasitic capacitances are formed. These capacitances and the respective representation in an equivalent circuit diagram are shown in fig. 2. For soft switching applications and

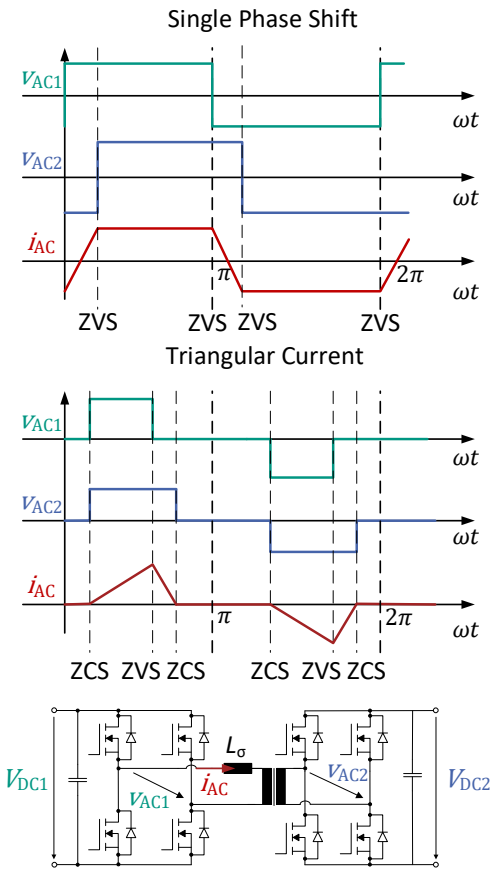


Fig. 1: Waveforms for single phase shift and triangular current modulation for a DAB

ZVS modelling the output capacitance C_{OSS} presented in (1) is the most relevant one since this parasitic capacitance must be charged and discharged for ZVS operation. Therefore, only the Drain-Source C_{DS} and Gate-Drain C_{GD} capacitances are considered [13]. Both C_{DS} and C_{GD} are highly dependent on the thickness and width of the depletion region. Since the depletion region is defined by the applied Drain-Source voltage V_{DS} the capacitances are also a function of this voltage and therefore strongly nonlinear. With a decrease of V_{DS} the internal surface of the n+ to p+/gate region is increasing as well as the spacing of the p-n junction in the depletion region is decreasing, subsequently both capacitances are increased as shown for C_{OSS} in fig. 3 (a) [14].

$$C_{\mathrm{OSS}}(V_{\mathrm{DS}}) = C_{\mathrm{DS}}(V_{\mathrm{DS}}) + C_{\mathrm{GD}}(V_{\mathrm{DS}}) \tag{1}$$

The voltage dependent capacitance shown in fig. 3 (a) is taken from the applied 1200 V/1200 A SiC MOSFET module from *Mitsubishi Electric*. Since calculations with this nonlinear capacitance are difficult, an equivalent capacitance is introduced to reduce the complexity of the model. It is possible to calculate an equivalent capacitance $C_{\mathrm{Q,eq}}$ with equal charge Q_{OSS} or an equivalent capacitance $C_{\mathrm{E,eq}}$ with equal energy E_{OSS} at a given voltage level V_{DS} compared to the nonlinear $C_{\mathrm{OSS}}(V_{\mathrm{DS}})$

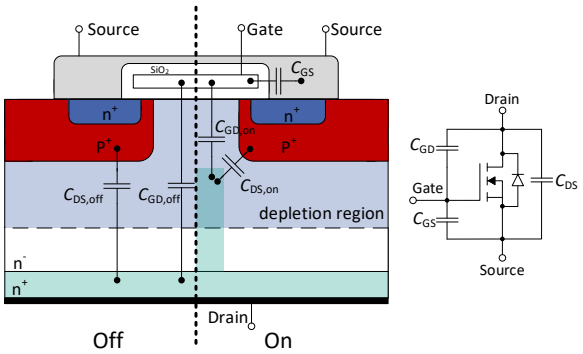


Fig. 2: (a) Cross section of a vertical power MOSFET with parasitic capacitances in off (left side) and on (right side) state (b) equivalent circuit diagram with parasitic capacitances of a MOSFET

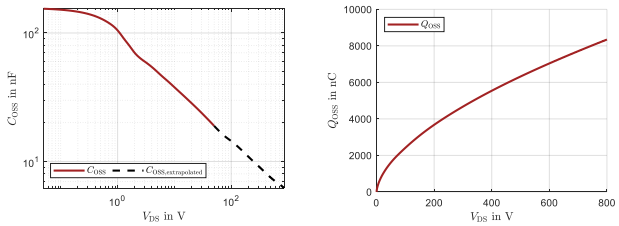
[9]. The resulting equations are given in (2) and (3). The charge Q_{OSS} as well as the equivalent capacitances $C_{\mathrm{Q,eq}}$ and $C_{\mathrm{E,eq}}$ are shown in fig. 3 (b) and fig. 3 (c), respectively. By using this, the capacitance $C_{\mathrm{OSS}}(V_{\mathrm{DS}})$ can be expressed as an equivalent constant value at one specific DC-link voltage V_{DC} and the voltage dependency for the charging and discharging process is eliminated. However, this is a simplification which can lead to inaccuracy in the modelling process, especially if the time course of the voltage v_{DS} is considered. Because of the nonlinear voltage dependency the charge and energy equivalent capacitances are not equal and differ by a factor of about $\frac{C_{\mathrm{E,eq}}}{C_{\mathrm{Q,eq}}} \approx 1.5$ which makes it necessary to specify the used equivalent capacitance for ZVS modelling. For analyzing the ZVS behavior the charge equivalent capacitance $C_{\mathrm{Q,eq}}$ has to be considered, since this specific charge has to be delivered from the inductor L_σ to charge or discharge the capacitances in order to achieve full ZVS operation.

$$C_{\mathrm{Q,eq}}(V_{\mathrm{DS}}) = \frac{\int_0^{V_{\mathrm{DS}}} C_{\mathrm{OSS}}(v)\, dv}{V_{\mathrm{DS}}} \tag{2}$$

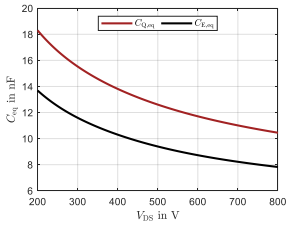
$$C_{\mathrm{E,eq}}(V_{\mathrm{DS}}) = \frac{2 \cdot \int_0^{V_{\mathrm{DS}}} v \cdot C_{\mathrm{OSS}}(v)\, dv}{V_{\mathrm{DS}}^2} \tag{3}$$

III. Capacitance Based Time Domain Model

In this chapter, the CTD model based on the nonlinear MOSFET capacitance C_{OSS} is presented. Using this model, the possible ZVS cases are explained. Based on these possible ZVS cases, the optimal deadtime and ZVS boundary are calculated and explained. At the end, a brief introduction to the resulting voltage error caused by the commutation is given. In this paper, the commutation process of the full bridge on DC1 side is considered. Both full bridges use the same MOSFETs and a transformer with a winding ratio of $1:1$ is assumed, if not stated otherwise. Therefore, the equivalent capacitances $C_{\mathrm{Q,eq}}$ are equal on either DC side. However, an adaption to



(a) (b)



(c)

Fig. 3: (a) Extrapolated nonlinear drain source capacitance $C_{\mathrm{OSS}}(V_{\mathrm{DS}})$ (b) Drain Source charge $Q_{\mathrm{OSS}}(V_{\mathrm{DS}})$ (c) Equivalent capacitances $C_{\mathrm{Q,eq}}$ and $C_{\mathrm{E,eq}}$

different transformer ratios and commutation processes is easily possible by transforming all values on one transformer side using the winding ratio. All calculation and simulation results are according to the parameter of the hardware setup presented in table II.

A. Modelling in Time Domain

In order to model the ZVS behavior of the DAB the equivalent circuit diagram shown in fig. 4 is considered. Under the condition that only the commutation process within the deadtime is observed, the nonlinear components, namely the MOSFETs and the diodes, can be neglected for the analysis. The result is an oscillating circuit with the stray inductance L_σ and the equivalent capacitance C_{eq} which depends on the MOSFETs and the operating point. If no switching occurs on the secondary side within the deadtime, the secondary side can be simplified as a constant voltage source v_{AC2}. For a switching event on the secondary side within the deadtime, a piecewise calculation, with and without overlap, is necessary to calculate accurate voltages and currents. Figure 5 shows different capacitance networks that have to be considered to acquire the equivalent capacitance C_{eq} depending on the different switching event cases. Figure 5 (a) shows a switching event for T1 and T2 which is a half bridge (HB) commutation, fig. 5 (b) a full bridge (FB) commutation for the DC1 side and fig. 5 (c) for an overlapping full bridge switching event on DC1 and DC2 side. If the transistor capacitances $C_{\mathrm{T1-T8}}$ are calculated according to (2) and all of them are equal as well as $C_{\mathrm{DC}} \gg C_{\mathrm{Q,eq}}$, the constant equivalent capacitances C_{eq} in table I can be assumed.

Using this linear model from fig. 4, the equation for the AC current $i_{\mathrm{AC}}(t)$ during the commutation process can be deduced:

$$i_{\mathrm{AC}}(t) = I_{\mathrm{sw}} \cdot \cos\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) + \sqrt{\frac{C_{\mathrm{eq}}}{L_\sigma}}(V_{\mathrm{sw}} - v_{\mathrm{AC2}}) \sin\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) \quad (4)$$

The resulting AC voltage v_{AC1} can be obtained by integrating the current from (4) and dividing by C_{eq}:

$$v_{\mathrm{AC1}}(t) = -\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \cdot I_{\mathrm{sw}} \cdot \sin\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) + (V_{\mathrm{sw}} - v_{\mathrm{AC2}}) \left(\cos\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) - 1\right) + V_{\mathrm{DC1}} \quad (5)$$

Using (5) gives the corresponding transistor voltage $v_{\mathrm{T,on/off}}$ of the turned-on/off MOSFET:

$$\begin{aligned} v_{\mathrm{T,on}}(t) &= \frac{1}{2}\left[-\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \cdot I_{\mathrm{sw}} \cdot \sin\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) + (V_{\mathrm{sw}} - v_{\mathrm{AC2}}) \left(\cos\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) - 1\right)\right] + V_{\mathrm{DC1}} \\ v_{\mathrm{T,off}}(t) &= -\frac{1}{2}\left[-\sqrt{\frac{L_\sigma}{C_{\mathrm{eq}}}} \cdot I_{\mathrm{sw}} \cdot \sin\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) + (V_{\mathrm{sw}} - v_{\mathrm{AC2}}) \left(\cos\left(\frac{t}{\sqrt{L_\sigma C_{\mathrm{eq}}}}\right) - 1\right)\right] \end{aligned} \quad (6)$$

The equations (4), (5) and (6) are describing a resonant oscillation between the equivalent capacitance C_{eq} and the AC inductance L_σ which are the defining parameters for the system behavior in case of ZVS. I_{sw} and V_{sw} represent the starting condition of the resonant oscillation for $t = 0$. For the different switching cases, namely half bridge switching and full bridge switching, only the equivalent capacitance C_{eq} has to be changed. This makes it possible to calculate all ZVS cases and therefore all DAB operating points with only the presented three equations. It is important to note, that these equations only hold within the deadtime and are not valid for hard switching. Additionally, equations (4) - (6) are only valid until the diodes start to conduct at $T_{\mathrm{d,con}}$. After that the behavior of the resonant commutation becomes nonlinear. The resulting voltages $v_{\mathrm{T,on/off}}$ and the current i_{AC} is shown in (7) and (8). The resulting AC voltage v_{AC1} depends on the switching event that occurs and is equal to the DC link voltage $v_{\mathrm{AC1}} = \pm V_{\mathrm{DC1}}$ (for FB commutation) or equal to zero $v_{\mathrm{AC1}} = 0\,\mathrm{V}$ (for HB commutation).

$$\begin{aligned} v_{\mathrm{T,on}} &\approx 0\,\mathrm{V} \\ v_{\mathrm{T,off}} &\approx V_{\mathrm{DC1}} \end{aligned} \quad (7)$$

$$i_{\mathrm{AC}} = \frac{v_{\mathrm{AC1}} - v_{\mathrm{AC2}}}{L_\sigma} t + I_{\mathrm{L}}(t = T_{\mathrm{d,con}}) \quad (8)$$

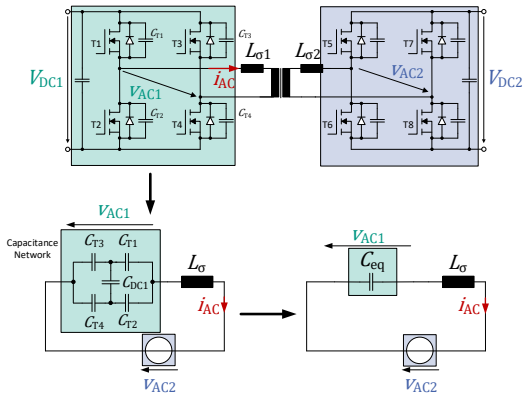


Fig. 4: Equivalent circuit diagram for the resonant commutation of DC1 side with full bridge commutation

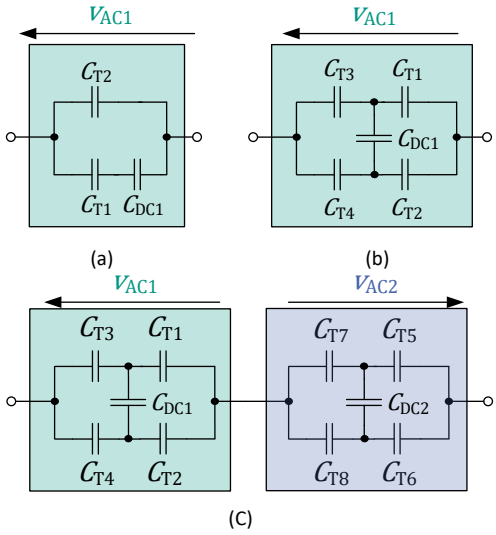


Fig. 5: The resulting capacitance networks for (a) half bridge commutation, (b) full bridge commutation and (c) full bridge commutation on both sides at the same time

B. ZVS cases

By analyzing (4) and (5)/(6) three different ZVS cases can be distinguished:

1) incomplete ZVS due to Current (iZVS-C) due to insufficient energy stored in the inductor L_σ to charge/discharge the equivalent capacitor C_{eq}
2) incomplete ZVS due to Deadtime (iZVS-D) due to a nonoptimal deadtime to achieve minimal switching losses
3) complete ZVS (cZVS)

For both iZVS cases, the voltage at the turned-on MOSFET after the deadtime is not zero. This fact leads to turn-on losses which are reduced compared to fully hard switching but are not zero as expected for ZVS operation. The corresponding AC voltage v_{AC1} and AC currents i_{AC} are shown in fig. 6 for the different cases. For the following ZVS analysis, v_{AC1} is used because it consists of the combination of all transistor voltages $v_{\mathrm{T},x}$ for a commutation process. Looking at the waveforms in fig. 6, the most important parameter to achieve cZVS and therefore minimal switching losses are the switching current at the start of the commutation I_{sw} (equivalent to the energy stored in the inductance L_σ) and the deadtime T_{dt} which has to be sufficiently long to charge/discharge the capacitance C_{eq} but short enough to avoid recharging of the capacitance.

TABLE I: Equivalent capacitances C_{eq} for different switching events with $C_{\mathrm{DC}} \gg C_{\mathrm{Q,eq}}$

	half bridge	full bridge	full bridge + half bridge	full bridge + full bridge
C_{eq}	$2 \cdot C_{\mathrm{Q,eq}}$	$C_{\mathrm{Q,eq}}$	$\frac{2}{3}C_{\mathrm{Q,eq}}$	$\frac{1}{2}C_{\mathrm{Q,eq}}$

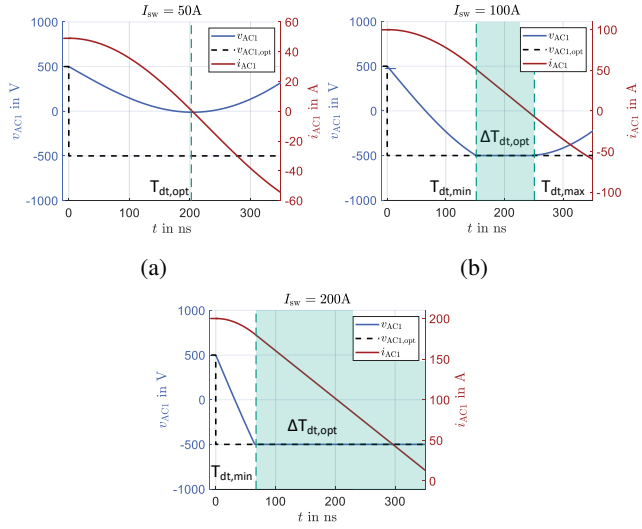


Fig. 6: Different ZVS cases with minimal, maximal and optimal deadtime for equal voltage $v_{\mathrm{AC1}}(t = 0) = v_{\mathrm{AC2}}(t = 0)$ (a) iZVS-C (b) iZVS-D (c) cZVS

C. Optimal Deadtime

As mentioned earlier, the deadtime T_{dt} is a critical parameter to achieve cZVS. Because of that, a detailed investigation on the optimal deadtime $T_{\mathrm{dt,opt}}$ is necessary. To calculate the minimal necessary deadtime $T_{\mathrm{dt,min}}$, the minimum of the AC voltage v_{AC}, calculated in (5), in case of iZVS-C or the point where the AC voltage gets clamped by the diodes $v_{\mathrm{AC}} = -V_{\mathrm{DC}}$ for cZVS has to be calculated (cf. fig. 6). The resulting equations are shown in (9)-(11). It has to be noticed, that the equation for FB (10) and HB (9) commutation are different because of the different necessary AC voltage ($v_{\mathrm{AC}} = -V_{\mathrm{DC}}$ for FB, $v_{\mathrm{AC}} = 0$ for HB) at the end of the commutation to achieve cZVS. The resulting minimal/optimal deadtime

and maximum deadtime is shown in fig. 7 for different operating points. For DABs in a generic triple phase shift operation, four relevant cases for ZVS behavior can occur:

1) $V_{\mathrm{DC1}} \approx v_{\mathrm{AC2}}$ (red)
2) $V_{\mathrm{DC1}} < v_{\mathrm{AC2}}$ (blue)
3) $V_{\mathrm{DC1}} > v_{\mathrm{AC2}}$ (green)
4) $v_{\mathrm{AC2}} < 0$ (black)

The optimal deadtime has vastly different behavior for these four cases. Case 1 is shown in fig. 6 with equal voltages. This leads to a optimal deadtime according to (11) which denotes the minimum of the resonant oscillation. After reaching enough current for cZVS, (9) and (10) have to be considered depending on the switching event. At this point the deadtime shown in fig. 7 (a) is the minimum necessary deadtime $T_{\mathrm{dt,min}}$ and in fig. 7 (b) is the maximum permissible deadtime $T_{\mathrm{dt,max}}$ between which cZVS is achieved. At higher deadtimes, cZVS is lost due to the zero crossing of the current i_{AC} and thus the voltage swinging back (cf. fig. 6). Case 2 works in similar manner compared to case 1 with the exception, that because of the high secondary side voltage, the current is decreasing faster and the zero current crossing of i_{AC} happens much earlier for iZVS. Therefore, the maximum deadtime $T_{\mathrm{dt,max}}$ has to be much smaller to avoid recharging. For cZVS the behavior is similar to case 1. Case 3 has an inverted behavior compared to Case 2. The reason for that is, that the secondary side is injecting a bit of energy in the AC circuit and thus supports the commutation. This leads to a delayed zero crossing of i_{AC} and a longer optimal deadtime rage $\Delta T_{\mathrm{dt,opt}}$. Case 4 can always achieve cZVS because the secondary side always helps with the commutation process. This leads to a small minimal necessary deadtime $T_{\mathrm{dt,min}}$. The maximum possible deadtime $T_{\mathrm{dt,max}}$ for cZVS is much higher compared to all other cases and therefore does not have to be considered.

$$T_{\mathrm{dt,HB,cZVS}} = \pm\sqrt{b} \arccos\left(\frac{\pm\sqrt{a^2 I_{\mathrm{sw}}^4 - 4aI_{\mathrm{sw}}^2 V_{\mathrm{sw}} v_{\mathrm{AC2}}} - V_{\mathrm{sw}}^2 + v_{\mathrm{AC2}}^2}{aI_{\mathrm{sw}}^2 - V_{\mathrm{sw}} v_{\mathrm{AC2}} + V_{\mathrm{sw}}^2 + v_{\mathrm{AC2}}^2}\right) \tag{9}$$

$$T_{\mathrm{dt,FB,cZVS}} = \pm\sqrt{b} \arccos \left[\frac{\pm\sqrt{a^2 I_{\mathrm{sw}}^4 - 2aI_{\mathrm{sw}}^2 V_{\mathrm{sw}} v_{\mathrm{AC2}} + aI_{\mathrm{sw}}^2 V_{\mathrm{sw}}^2}}{aI_{\mathrm{sw}}^2 - 2V_{\mathrm{sw}} v_{\mathrm{AC2}} + V_{\mathrm{sw}}^2 + v_{\mathrm{AC2}}^2} - \frac{V_{\mathrm{sw}} v_{\mathrm{AC2}} + v_{\mathrm{AC2}}^2}{aI_{\mathrm{sw}}^2 - 2V_{\mathrm{sw}} v_{\mathrm{AC2}} + V_{\mathrm{sw}}^2 + v_{\mathrm{AC2}}^2}\right] \tag{10}$$

$$T_{\mathrm{dt,iZVS}} = \sqrt{b}\left(\pi + \arctan\left(\frac{I_{\mathrm{sw}}\sqrt{a}}{V_{\mathrm{sw}} - v_{\mathrm{AC2}}}\right)\right) \tag{11}$$

$$\text{with } a = \frac{L_\sigma}{C_{\mathrm{eq}}} \text{ and } b = L_\sigma C_{\mathrm{eq}}$$

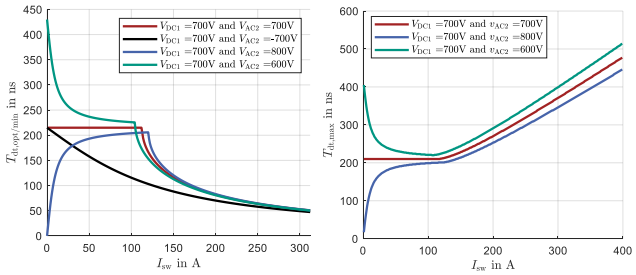
D. cZVS boundary

To achieve cZVS a minimum amount of energy stored in the inductor is necessary, otherwise the equivalent capacitor C_{eq} can not be fully charged/discharged. The minimum current at the start of the switching event $I_{\mathrm{sw,min}}$ can be calculated from (6) and (11) by using (12). This denotes the point where iZVS is changing into cZVS and the voltage v_{T} is equal to zero for the first time.

$$v_{\mathrm{T}}(T_{\mathrm{dt,iZVS}}) \leq 0 \tag{12}$$

Simplifying (12) leads to:

$$I_{\mathrm{sw,min}} = \frac{2 \cdot \sqrt{L_\sigma \cdot C_{\mathrm{eq}} \cdot V_{\mathrm{sw}} \cdot v_{\mathrm{AC2}}}}{L_\sigma} \tag{13}$$



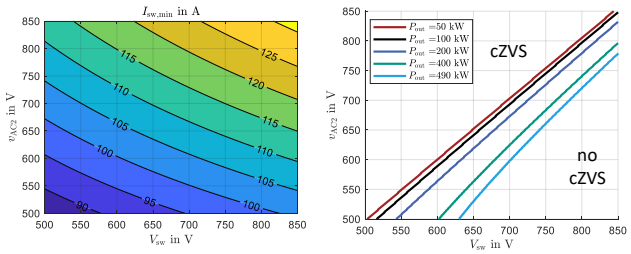
(a) (b)

Fig. 7: (a) Minimal/optimal deadtime (b) maximum deadtime

It can be observed that the minimal necessary switching current $I_{\mathrm{sw,min}}$ depends on the switching voltage V_{sw} at the start of the commutation as well as the secondary side voltage v_{AC2}. $I_{\mathrm{sw,min}}$ is shown in fig. 8 (a) for different voltages. If the difference between the voltage on the switching side and the other side $V_{\mathrm{sw}} - v_{\mathrm{AC2}}$ is increasing the minimal necessary current $I_{\mathrm{sw,min}}$ is decreasing. This is due to the fact, that the voltage v_{AC2} can also provide some energy for the equivalent capacitance to charge/discharge if it is lower then the switching side V_{sw}. For negative $v_{\mathrm{AC2}} < 0$ this will lead to cZVS at all operating points even for negative switching current I_{sw} with subject to the restriction that the deadtime T_{dt} is long enough. Figure 9 shows the necessary deadtime for cZVS with negative voltage $v_{\mathrm{AC2}} < 0$ for different stray inductances L_σ. It can be observed that for negative currents I_{sw}, cZVS is theoretically possible but the deadtime has to be high compared to positive currents and therefore is not practical. Only for small inductances L_σ this can be feasible and a way to optimize the converter modulation. The resulting cZVS range for SPS modulation at the DC1 side is shown in fig. 8 (b) for different power level P_{out} of the DAB. It can be observed that for boost operation $V_{\mathrm{sw}} < V_{\mathrm{DC2}}$ the cZVS region is larger because the DC2 side is helping with the resonant commutation. The DC2 side can theoretically always achieve cZVS because of the negative AC voltage v_{AC1} as discussed earlier (cf. fig. 9).

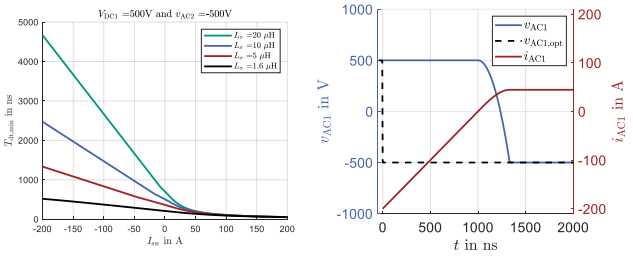
E. Voltage time area error due to commutation

As shown in (5) the AC voltage v_{AC} for the commutation depends on the operating point of the DAB, namely



(a) (b)

Fig. 8: (a) Minimal necessary switching current $I_{\mathrm{sw,min}}$ to achieve cZVS assuming optimal deadtime (b) DC1 side cZVS boundary for SPS at different power ratings



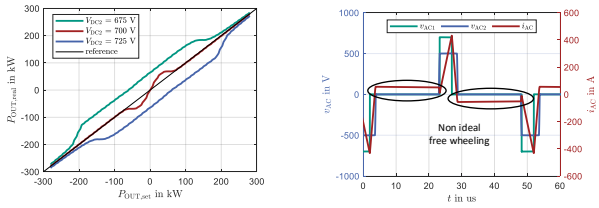
(a) (b)

Fig. 9: (a) Minimum deadtime for $I_{\mathrm{sw}} < 0$ and different L_σ (b) voltage v_{AC} and current i_{AC} for starting current $I_{\mathrm{sw}} = -200\,\mathrm{A}$, $L_\sigma = 5\,\mu\mathrm{H}$ and $V_{\mathrm{sw}} = -v_{\mathrm{AC2}} = 500\,\mathrm{V}$

the switching current I_{sw} and the DC2 side voltage v_{AC2}. Because of that, the error of the Voltage Time Area (VTA) of the AC voltage Φ_{error} caused by the deadtime T_{dt} is also dependent on the operating point. From this follows, that the commonly used compensation by checking the current direction and adding or subtracting the deadtime T_{dt} from the switching time is not sufficient for a DAB. Therefore, a more advanced approach has to be used. By using (5) the VTA error Φ_{error} can be calculated with (14). Using this, a compensation with the same voltage time area is possible $\Phi_{\mathrm{comp}} = -\Phi_{\mathrm{error}}$. In this case $v_{\mathrm{AC,opt}}$ is the optimal AC voltage with infinite fast commutation shown in fig. 6.

$$\Phi_{\mathrm{error}} = \int_0^{T_{\mathrm{dt}}} v_{\mathrm{AC,opt}}(t) - v_{\mathrm{AC}}(t)dt \qquad (14)$$

Figure 10 shows the impact of the voltage error Φ_{error} for SPS and triangular modulation. In case of SPS, the transfer characteristic is getting highly nonlinear for iZVS which can reduce the performance of the controller and can lead to unstable operating points. Depending on the voltages V_{DC1} and V_{DC2} the impact on the transfer characteristic differs (shown in fig. 10 (a)). This is mainly a challenge for low power operation until cZVS is achieved on both sides of the DAB. After that the voltage error Φ_{error} can be neglected, since the voltage error on the DC1 side is compensated by that of the DC2 side. For TCM the transfer characteristic does not change significantly but the free wheeling states are changing as



(a) (b)

Fig. 10: (a) nonlinear transfer characteristic for SPS at $V_{\mathrm{DC1}} = 700\,\mathrm{V}$ (b) nonideal behavior for TCM for $P_{\mathrm{out}} = 25\,\mathrm{kW}$

TABLE II: Hardware Setup Parameter

Symbol	Meaning	Value
	DAB parameter	
$L_{\sigma,\mathrm{prim}}$	AC inductance prim	700 nH
$L_{\sigma,\mathrm{sec}}$	AC inductance sec	700 nH
$C_{\mathrm{Q,eq}}$	Charge based capacitance @700 V	11 nF
$V_{\mathrm{DC1/2}}$	In- Output voltage range	500 V-850 V
f_{sw}	Switching frequency	20 kHz
P_{out}	Nominal output power	500 kW
T_{dt}	Inverter deadtime	$<1\,\mu\mathrm{s}$
	Transformer parameter	
n	Transfer ratio	1 : 1
$L_{\sigma,\mathrm{T}}$	Leakage inductance	200 nH
$L_{\mathrm{h,T}}$	Magnetizing inductance	250 µH
	Transformer volume	56.1 l

shown in the simulation results from fig. 10 (b). This will lead to inefficient operation of the DAB because of higher switching losses (ZCS is not achieved anymore) and higher conduction losses due to the non-zero current free wheeling. In addition, this VTA error Φ_{error} can have significant impact on advanced dynamic control schemes where an accurate compensation might be necessary [15].

IV. Measurement Results and Validation

To validate the CTD model and the presented implications of the nonlinear ZVS behavior the test bench shown in fig. 11 has been constructed. The DAB has a nominal output power of $P_{\mathrm{out}} = 500\,\mathrm{kW}$ and a switching frequency of $f_{\mathrm{sw}} = 20\,\mathrm{kHz}$ to avoid acoustic noise. The resulting relevant parameters of the system are shown in table II. In order to measure switching behavior and switching losses the setup shown in fig. 12 (a) is used. Since for ZVS switching events, a considerable part of the energy is oscillating between the turned on and the turned off MOSFET, both E_{on} and E_{off} have to measured at the same switching event. That is the reason why a single pulse testing shown in fig. 12 (b) is used. The resulting half bridge switching energy $E_{\mathrm{sw,HB}}$ can be calculated according to (15) and represents the full switching losses of a half-bridge for one switching event and mainly occurs in the turned off MOSFET.

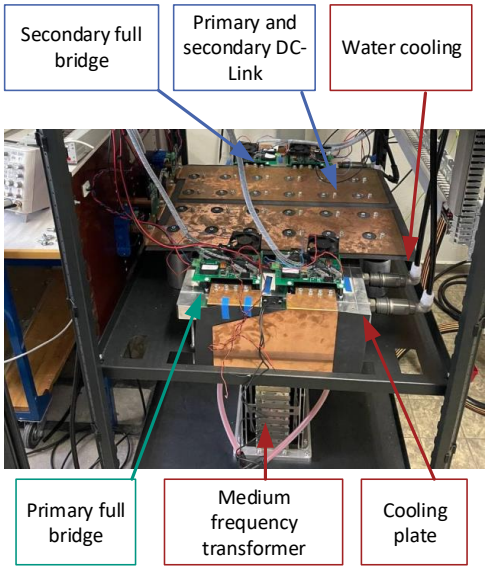
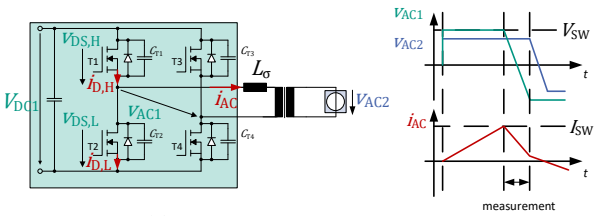


Fig. 11: DAB testbench

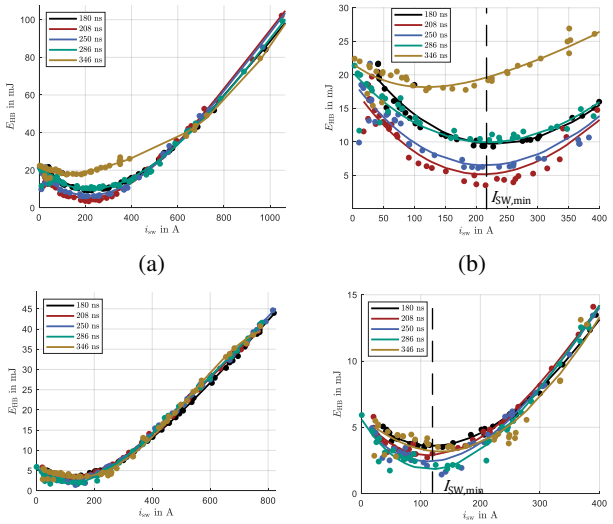


(a) (b)

Fig. 12: (a) DAB test setup (b) waveform for single pulse testing

$$E_{\mathrm{sw,HB}} = E_{\mathrm{on}} + E_{\mathrm{off}} = \int_{t_{\mathrm{start}}}^{t_{\mathrm{end}}} v_{\mathrm{DS,L}} \cdot i_{\mathrm{D,L}} \mathrm{d}t + \int_{t_{\mathrm{start}}}^{t_{\mathrm{end}}} v_{\mathrm{DS,H}} \cdot i_{\mathrm{D,H}} \mathrm{d}t \quad (15)$$

The resulting switching energy $E_{\mathrm{sw,HB}}$ for different deadtime T_{dt} is shown in fig. 13 for $V_{\mathrm{sw}} = 800\,\mathrm{V}$ in (a,b) and $V_{\mathrm{sw}} = 500\,\mathrm{V}$ in (c,d). It can be seen, that for high switching currents $I_{\mathrm{sw}} \gg I_{\mathrm{sw,min}}$ the deadtime does not influence the switching energy and the total losses are similar to the turn off energy E_{off} of a single MOSFET since the turn on happens with cZVS (cf. fig. 6 (c)). For low currents $I_{\mathrm{SW}} < 2I_{\mathrm{sw,min}}$, the difference can be higher than a factor of $\approx 2-4$, especially for $V_{\mathrm{sw}} = 800\,\mathrm{V}$ (cf. fig. 6 (a) and (b)). The minimum of the shown halfbridge losses denotes the boundary between iZVS and cZVS and thus the minimum necessary switching current $I_{\mathrm{SW,min}}$. The resulting measured and calculated optimal deadtime T_{dt} and $I_{\mathrm{sw,min}}$ to achieve cZVS are shown in table III for different switching voltages. It can be observed, that the model and the measurements fit very well. To evaluate the model further, measured waveforms are compared with calculated ones for the output current i_{AC} and voltage v_{AC}. Figure 14 shows the waveforms for iZVS due to a long deadtime $T_{\mathrm{dt}} > T_{\mathrm{dt,max}}$ and fig. 15 due to insufficient current $I_{\mathrm{sw}} < I_{\mathrm{sw,min}}$. For both cases the calculation fit very well with the measurement even for the nonlinear behavior due to the clamping of the diodes. Additionally the nonlinear transfer characteristic for SPS of the DAB is compared between calculations and measurements in fig. 16 at $V_{\mathrm{DC1}} = V_{\mathrm{DC2}} = 500\,\mathrm{V}$ and $V_{\mathrm{DC1}} = V_{\mathrm{DC2}} = 700\,\mathrm{V}$. For both cases the transfer characteristic matches very well.



(a) (b) (c) (d)

Fig. 13: half bridge switching energy $E_{\mathrm{sw,HB}}$ for a full bridge commutation at (a,b) $V_{\mathrm{sw}} = v_{\mathrm{AC2}} = 800\,\mathrm{V}$ (c,d) and $V_{\mathrm{sw}} = v_{\mathrm{AC2}} = 500\,\mathrm{V}$

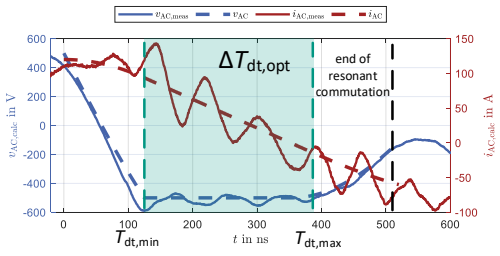


Fig. 14: Voltage v_{AC} and current i_{AC} for measurement and CTD model in case of iZVS-D caused by a long deadtime $T_{\mathrm{dt}} > T_{\mathrm{dt,max}}$

TABLE III: Comparison of optimal deadtime T_{dt} and minimal necessary switching current I_{sw} to achieve cZVS for measurement and CTD model

V_{sw}	$T_{\mathrm{dt,calc}}$	$T_{\mathrm{dt,meas}}$	$I_{\mathrm{sw,calc}}$	$I_{\mathrm{sw,meas}}$
500 V	272 ns	286 ns	145 A	141 A
600 V	260 ns	250 ns	167 A	161 A
700 V	250 ns	208 ns	189 A	180 A
800 V	240 ns	208 ns	210 A	212 A

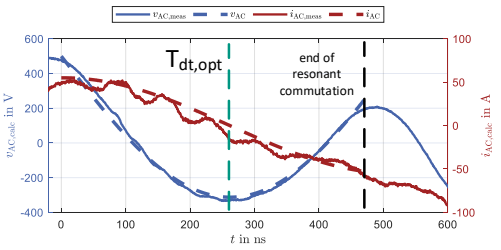
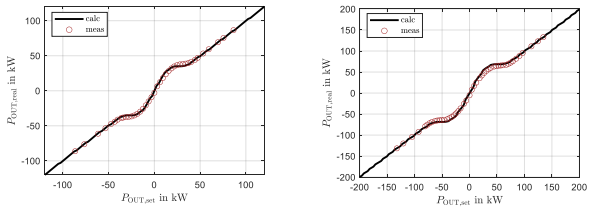


Fig. 15: Voltage v_{AC} and current i_{AC} for measurement and CTD model in case of iZVS-C due to insufficient current $I_{\mathrm{sw}} < I_{\mathrm{sw,min}}$



(a) (b)

Fig. 16: (a) Transfer characteristic for $V_{\mathrm{DC1}} = V_{\mathrm{DC2}} = 500\,\mathrm{V}$ (b) for $V_{\mathrm{DC1}} = V_{\mathrm{DC2}} = 700\,\mathrm{V}$

V. CONCLUSIONS

In this paper, a capacitance based time domain (CTD) model for the resonant commutation in case of zero voltage switching (ZVS) is presented. The modeling of the nonlinear MOSFET output capacitance C_{OSS} is presented and a constant charge based equivalent capacitance $C_{\mathrm{Q,eq}}$ is derived. Based on this, a linear model is presented to calculate the time course of the voltages $v_{\mathrm{DS},x}$ and v_{AC} as well as the current i_{AC} of the DAB in case of resonant commutation. Based on this calculation, the optimal deadtime $T_{\mathrm{dt,opt}}$ and minimal necessary switching current $I_{\mathrm{sw,min}}$ to achieve complete ZVS (cZVS) are deduced. It is shown, that the cZVS condition is highly dependent on the operating point of the DAB namely the starting current I_{sw} and the difference between the AC side voltages $v_{\mathrm{AC1}} - v_{\mathrm{AC2}}$. Furthermore, the error of the voltage time Φ_{error} caused by the nonlinear behavior of the ZVS operation of a DAB is calculated and presented. This modeling is decisive for achieving maximum efficiency and optimal control over a wide operation range. The analytical model is confirmed using measurements from a $500\,\mathrm{kW}$ DAB prototype. It is shown that calculations and measurements fit very well. Real time implementation of the model is possible with state-of-the-art control.

REFERENCES

[1] R. W. A. A. De Doncker, D. M. Divan and M. H. Kheraluwala, "A three-phase soft-switched high-power-density DC/DC converter for high-power applications," in IEEE Transactions on Industry Applications, vol. 27, no. 1, pp. 63-73, Jan.-Feb. 1991, doi: 10.1109/28.67533.

[2] F. Krismer and J. W. Kolar, "Efficiency-Optimized High-Current Dual Active Bridge Converter for Automotive Applications," in IEEE Transactions on Industrial Electronics, vol. 59, no. 7, pp. 2745-2760, July 2012, doi: 10.1109/TIE.2011.2112312.

[3] G. Fortes, P. Ladoux, J. Fabre and D. FIumian, "Characterization of a 300 kW Isolated DCDC Converter using 3.3 kV SiC-MOSFETs", PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics Intelligent Motion Renewable Energy and Energy Management, pp. 1-8, 2021.

[4] R. Haneda and H. Akagi, "Design and Performance of the 850-V 100-kW 16-kHz Bidirectional Isolated DC–DC Converter Using SiC-MOSFET/SBD H-Bridge Modules," in IEEE Transactions on Power Electronics, vol. 35, no. 10, pp. 10013-10025, Oct. 2020, doi: 10.1109/TPEL.2020.2975256.

[5] F. Sommer, N. Menger, T. Merz, N. Soltau, S. Idaka and M. Hiller, "Design and Characterization of a 500 kW 20 kHz Dual Active Bridge using 1.2 kV SiC MOSFETs," 2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia), 2022, pp. 1390-1397, doi: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807023.

[6] F. Sommer, N. Menger, T. Merz and M. Hiller, "Accurate Time Domain Zero Voltage Switching Analysis of a Dual Active Bridge with Triple Phase Shift," 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), 2021, pp. 1-9, doi: 10.23919/EPE21ECCEEurope50061.2021.9570684.

[7] S. S. Shah, V. M. Iyer and S. Bhattacharya, "Exact Solution of ZVS Boundaries and AC-Port Currents in Dual Active Bridge Type DC–DC Converters," in IEEE Transactions on Power Electronics, vol. 34, no. 6, pp. 5043-5047, June 2019, doi: 10.1109/TPEL.2018.2884294.

[8] J. Everts, F. Krismer, J. Van den Keybus, J. Driesen and J. W. Kolar, "Charge-based ZVS soft switching analysis of a single-stage dual active bridge AC-DC converter," 2013 IEEE Energy Conversion Congress and Exposition, 2013, pp. 4820-4829, doi: 10.1109/ECCE.2013.6647349.

[9] M. Kasper, R. M. Burkart, G. Deboy and J. W. Kolar, "ZVS of Power MOSFETs Revisited," in IEEE Transactions on Power Electronics, vol. 31, no. 12, pp. 8063-8067, Dec. 2016, doi: 10.1109/TPEL.2016.2574998.

[10] Y. Yan, H. Gui and H. Bai, "Complete ZVS Analysis in Dual Active Bridge," in IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1247-1252, Feb. 2021, doi: 10.1109/TPEL.2020.3011470.

[11] D. Costinett, D. Maksimovic and R. Zane, "Circuit-Oriented Treatment of Nonlinear Capacitances in Switched-Mode Power Supplies," in IEEE Transactions on Power Electronics, vol. 30, no. 2, pp. 985-995, Feb. 2015, doi: 10.1109/TPEL.2014.2313611.

[12] Schibli, N, "Symmetrical multilevel converters with two quadrant DC-DC feeding," dissertation Ecole polytechnique fédérale de Lausanne, 2000

[13] M. Escudero, M. -A. Kutschak, N. Fontana, N. Rodriguez and D. P. Morales, "Non-Linear Capacitance of Si SJ MOSFETs in Resonant Zero Voltage Switching Applications," in IEEE Access, vol. 8, pp. 116117-116131, 2020, doi: 10.1109/ACCESS.2020.3004440.

[14] L. Lorenz, G. Deboy, A. Knapp and M. Marz, "COOLMOS/sup TM/-a new milestone in high voltage power MOS," 11th International Symposium on Power Semiconductor Devices and ICs. ISPSD'99 Proceedings (Cat. No.99CH36312), Toronto, ON, Canada, 1999, pp. 3-10, doi: 10.1109/ISPSD.1999.764028.

[15] N. Menger, F. Sommer, T. Merz and M. Hiller, "Transient Power Control Algorithm for a Dual Active Bridge," 2021 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), Ghent, Belgium, 2021, pp. P.1-P.8, doi: 10.23919/EPE21ECCEEurope50061.2021.9570419.