Predictive Control for Isolated Matrix Rectifier Without Current Distortion at Sector Boundary

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***Abstract*— Three phase active rectifiers are needed to supply dc loads from the ac distribution grid without introducing large distortions on the ac grid. Galvanic isolation is a requirement for many applications due to safety concerns. High frequency link power conversion topologies, based on indirect matrix converters, are an emerging solution for such applications. In this paper a predictive digital control is developed for an isolated three phase ac/dc matrix converter by combining a deadbeat controller and space vector modulation. This approach simplifies the controller design and allows for full-range soft-switching with sinusoidal input currents. Due to the discrete operating sectors of high frequency link topologies, an additional modulation mode is introduced near sector boundaries, reducing the distortion caused by sector changes. The proposed deadbeat controller is validated with PSIM simulations.**

Keywords—Isolated rectifiers, deadbeat control, matrix converters, ac/dc conversion.

I. INTRODUCTION

In recent years, there is an increasing number of dc loads and generators connected to the public ac distribution grid. Examples include, as shown in Fig. 1, electric vehicle (EV) chargers, data centers, photovoltaic panels and battery storage [1]-[4]. These loads and generators are connected to the ac distribution grid with an ac/dc converter. In the case of battery-connected applications, bidirectional operation of the converter could be required. To respect grid codes, the converter must exchange energy with sinusoidal grid currents on the ac side. For safety reasons, galvanic isolation may also be a requirement for many applications [5], [6].

An example of the conventional solution for isolated ac/dc conversion is shown in Fig. 2 (a). Two power electronic converters are connected in series. A three-phase boost power factor correction converter (PFC) is used to supply a steady dc voltage to a dc link, which is then regulated by a dc/dc converter. The dc/dc stage provides isolation with a high frequency transformer (HFT). The two converters are controlled independently, and dc link capacitors are used as an energy buffer to decouple the dynamics of the two converters. This work

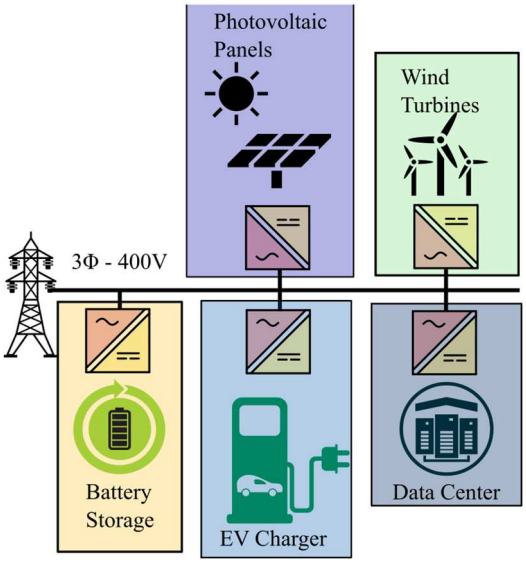


Fig. 1 dc native technologies connected to the ac distribution grid via isolated dc/ac converters.

focuses on the emerging single stage solution, shown in Fig 2 (b), that directly converts ac to dc with a HFT [7]. The advantage of this solution is that it does not require intermediate dc link capacitors, nor a corresponding voltage sensor.

Generally, grid connected inverters are controlled with two loops, an inner current loop, and an outer voltage loop. The performance of the inner loop, which controls the current, largely determines the performance of the system.

Deadbeat control has been thoroughly studied for traditional inverter systems, and offers the advantages of better dynamic performance and low total harmonic distortion (THD) [8]–[10]. Furthermore, the design of a deadbeat controller is simpler, as there is no need for a linearized model of the converter and linear controller design. Deadbeat control can be extended to high frequency link conversion for better performance and simpler design.

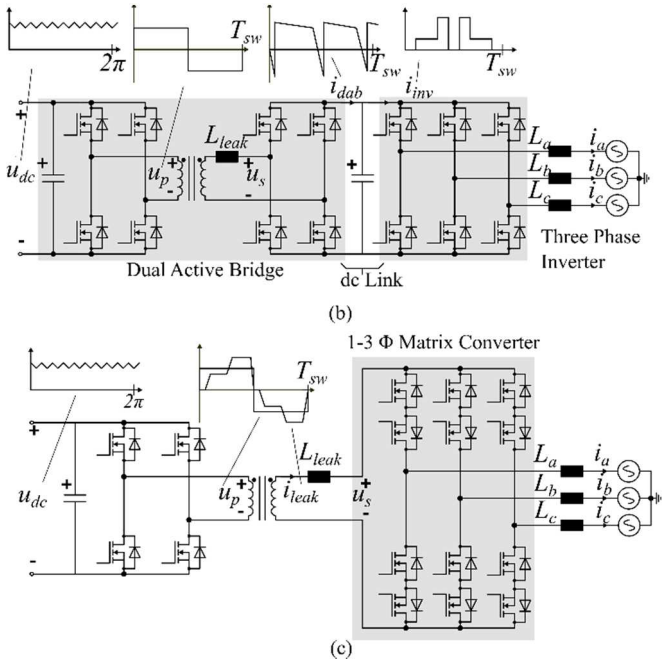


Fig. 2 Power converter topologies for high frequency ac-dc conversion and their characteristic waveforms. (a) shows the typical two-stage solution. (b) shows the emerging single stage solution.

Existing literature on matrix-type rectifiers all rely on discrete operating sectors [11]–[15], which are determined from ac voltage and current polarity. The transition between two operating sectors, which happens multiple times in a grid period, introduces distortions on the grid waveforms. To resolve this a modified operating mode which relies on discontinuous conduction mode (DCM) of the phase undergoing zero crossing is developed. The resulting controller has low THD, fast dynamic response, and eliminates the current distortion near the zero crossing.

II. Converter Operation

A. Modulation

The dc side is controlled to generate a square wave ac voltage with constant duty cycle, which is fed to the primary of the transformer. At the secondary of the transformer the matrix converter (MC) unfolds and sinusoidally modulates the square wave voltage to provide the necessary converter-side voltage vector for sinusoidal currents. The full-bridge switches on the dc side alternate with a deadtime, not only to avoid a shoot-through of the voltage source, but also to allow for zero voltage turn-ON. The soft-switching performance of all switches is described in detail in [16] and is not the focus of this paper.

The MC must block and conduct voltages and currents respectively in both directions, meaning it must be composed of four-quadrant switches. This can be achieved with anti-series connection of MOSFETs. A consequence of using these four quadrant switches at the ac side, is that there is no freewheeling path for the diodes, so the MC switches must be controlled in such a way that there is always a path for the inductor current, or else they will discharge over the switches, potentially damaging the converter. To ensure that the phase legs are commutated

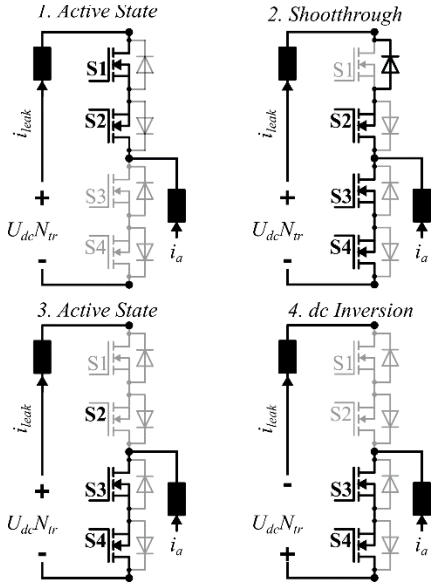


Fig. 3 Commutation scheme for phase leg of converter operating in rectifier mode. Only one leg is shown for simplicity. The dc side voltage is used to redistribute the current during the leg commutation, allowing for ZCS.

safely, there must be an shoot-through state during which the current is redistributed from the top arm to bottom arm and vice versa. This commutation scheme was first developed by [17] and is shown in Fig. 3. It is described below for rectifier operation.

1. Switches S_1, S_2 are conducting, connecting the phase leg to the top rail of the HFT. The converter is in an active state, transferring power from the ac side to the dc side. S1 is operating in synchronous rectification mode.
2. Switches S_3, S_4 turn on. S_1 is turned OFF, but continues to conduct through its body diode. This puts the transformer in a shoot-through state, wherein the transformer voltage is applied to the leakage inductance, and the output at the secondary terminals of the transformer is clamped to zero. This causes the current in the top arm to redistribute to the bottom, limited by the leakage inductance.
3. Once the current has fully redistributed, S_1 undergoes reverse recovery and begins blocking the voltage. The secondary of the transformer is no longer clamped and power flows through the converter again. Switch S_2 can now be turned OFF with zero current switching (ZCS).
4. The final state occurs after the dc side commutation, the converter is ready to repeat the process by commutating the MC leg in the opposite direction.

The shoot-through period of the current source MC is analogous to the deadtime of the voltage source full-bridge (FB). Due to this necessary shoot-through period, the duty cycle of the MC switches is also fixed at a value above 0.5. The shoot-through period for the redistribution of current between arms in a leg is depends on the leakage inductance of the transformer and the current to be redistributed, t_{comm} is calculated as

$$t_{comm} = \frac{i_{ac,x} L_{leak}}{U_{dc}} \tag{1}$$

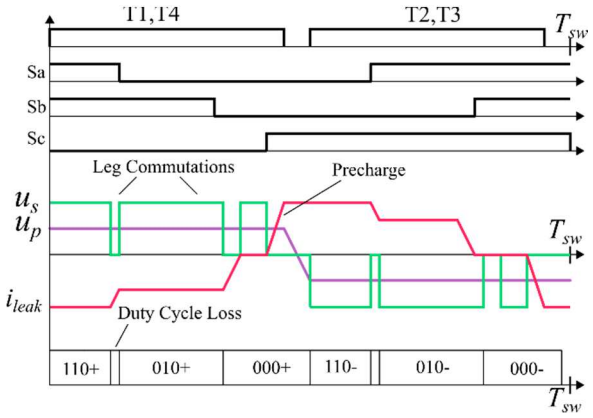


Fig. 4 Generalized representation of one switching period during rectifier operation. T_1,T_4, and T_2,T_3 represent the full bridge switches on the dc side, applying a positive and negative voltage respectively. Each voltage vector is symmetrically applied twice in the switching period.

The constant duty cycle square wave voltage impressed by the FB ensures that there is no need for dc blocking capacitors on the transformer, as used in [14]. Furthermore, as shown in Fig 4, due to the constant duty cycle, each voltage vector applied by the MC is essentially applied twice in a switching period, for both the positive and negative voltage impressed on the primary. In fact, the matrix converter can be seen as two traditional inverters placed 180º out of phase, operating with opposite input polarities in an interleaved fashion. Therefore, the ripple frequency seen on the capacitors and inductors is double the switching frequency. The precharge shown in Fig. 4 is a deliberate shoot-through state to increase the current in the transformer before the dc side commutation, so that it matches the load current.

B. Deadbeat Control with SVM

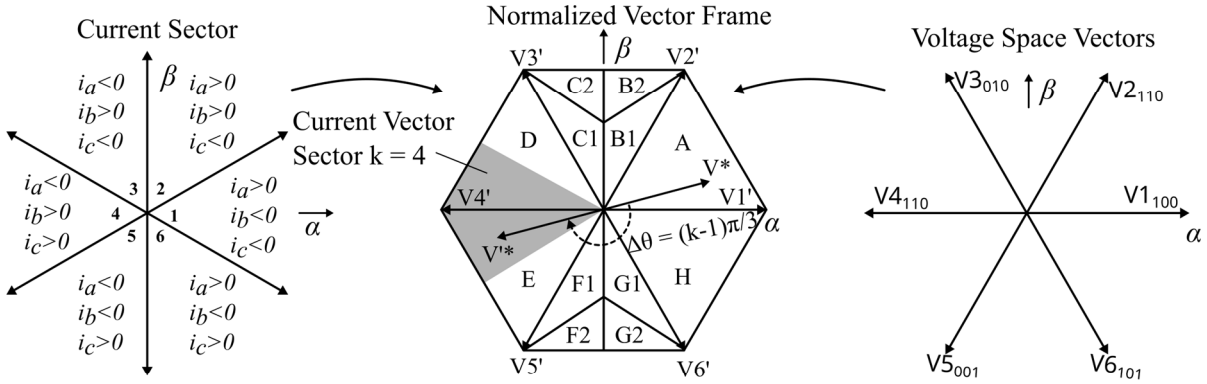
The optimal commutation scheme for HFLCs was first derived for the non-isolated high frequency link inverter in [18]. A three vector sequence modulation scheme with maximized zero voltage vector is applied, with the final vector being suppressed by being placed at the end of the switching interval. The soft leg commutation described in Fig. 3 is only possible with a certain sequence of vectors, which depends on the reference voltage sector and phase current polarities. The process of determining the idea vector sequence is shown in Fig. 5. A normalized stationary reference frame is used, and the reference voltage vector is rotated by $\Delta\theta = (k-1)\pi/3$, where k is the current sector. Note that in rectifier operation, the rotated reference voltage will always find itself in the D or E sectors.

Once the vector sequence in the normalized vector frame is found, the normalized vectors are transformed back to the real vectors and the duty cycles are calculated. This calculation can be quite computationally burdensome, as it requires the inversion of a 3x3 matrix, however it an be simplified by preloading the inverted matrice values in a look-up table.

The deadbeat controller is used to generate an appropriate V^* reference for the desired currents. Some deadbeat controls

Optimized 3 vector sequence in Normalized Reference Frame

	A	B1	B2	C1	C2	D	E	F1	F2	G1	G2	H
$\mathbf{V_x}$	V7’	V4’	V4’	V3’	V3’	V4’	V4’	V5’	V5’	V4’	V4’	V7’
$\mathbf{V_y}$	V2’	V7’	V3’	V0’	V2’	V3’	V5’	V0’	V6’	V7’	V5’	V6’
$\mathbf{V_z}$	V1’	V2’	V2’	V1’	V1’	V0’	V0’	V1’	V1’	V6’	V6’	V1’



Normalized Space Vectors

	V0’	V1’	V2’	V3’	V4’	V5’	V6’	V7’
k=1	V0	V1	V2	V3	V4	V5	V6	V7
k=2	V7	V2	V3	V4	V5	V6	V1	V0
k=3	V0	V3	V4	V5	V6	V1	V2	V7
k=4	V7	V4	V5	V6	V1	V2	V3	V0
k=5	V0	V5	V6	V1	V2	V3	V4	V7
k=6	V7	V6	V1	V2	V3	V4	V5	V0

Duty Cycle Calculation

$$\begin{bmatrix}\delta 0\\ \delta 1\\ \delta 2\end{bmatrix} = \begin{bmatrix}V'_{x,\alpha} & V'_{y,\alpha} & V'_{z,\alpha}\\ V'_{x,\beta} & V'_{y,\beta} & V'_{z,\beta}\\ 1 & 1 & 1\end{bmatrix}^{-1}\begin{bmatrix}V'^{*}_{\alpha}\\ V'^{*}_{\beta}\\ 1\end{bmatrix}$$

Fig. 5 Space vector modulator for high frequency link converter. The optimized 3 vector sequence depends on the current sector and reference voltage sector and allow for all legs to undergo safe commutation.

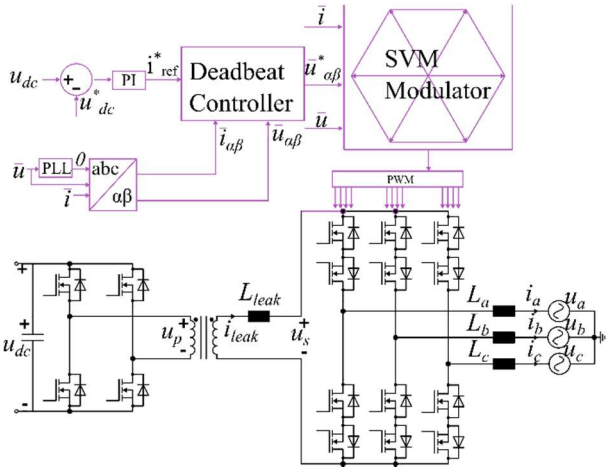


Fig. 6 Converter control scheme. The dc side control (constant duty cycle square wave) is not shown.

(holmes, martin) sample the system twice in a single switching period, for both turn on and off of the switches, to partially compensate for the digital delay. As the isolated HFLC is controlled with fixed duty cycles on the primary and secondary, the control routine only needs to be executed once per switching period, reducing the computational effort.

The calculations are performed in the alpha-beta frame, so they can be used directly with the space vector modulator. The system is assumed to be balanced and symmetric. The change in current in one sampling period can be calculated by the volt-second balance applied to the inductor.

$$i(k+1) = \frac{1}{Lf_{sw}}\left(u_{inv}(k) - u_g(k)\right) + i(k) \qquad (2)$$

where $i(k)$ is the current, L is the inductance of the grid inductor, f_{sw} is the switching frequency, $u_{inv}(k)$ is the voltage generated by the converter and $u_g(k)$ is the grid voltage. The reference voltage to generate the desired currents is:

$$u_{inv}(k+1) = Lf_{sw}\left(i^*_{ref}(k) - i(k)\right) + 2u_g(k) - u_{inv}(k) \qquad (3)$$

C. Discontinuous Conduction Mode

A problem arises when the reference current is less than the current ripple on the inductor, i.e., operation near the zero crossing of the phase current. In this case the current will change polarity during the active state (state 1 in Fig. 3), and switch S_1 will be working in forward conduction instead of synchronous rectification. When the switch is turned OFF the inductor current will have no path and discharge on the switches, potentially damaging them. This hard switching results in increased device stress. Furthermore, the phase current is distorted near the zero crossing.

If the synchronous rectification switches are turned OFF near the zero crossing, hard switching is avoided. However, the lowest achievable average current is half the value of the inductor ripple. This is also true immediately after the sector change, with inverted polarity. Therefore, the average value of the current will jump from positive to negative of half the ripple value, resulting in significant distortion near the zero crossing.

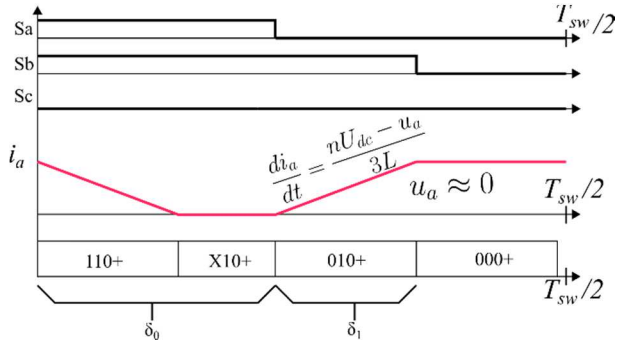


Fig. 7 Converter operation in discontinuous conduction mode. Half of a switching period is shown. Before the first leg commutation the current in phase a falls to zero, disconnecting the phase.

In order to achieve the desired average currents with no hard switching and minimum current distortion, the modulation will be modified when the reference current is less than half the inductor ripple. The converter will operate in DCM on the phase leg undergoing a zero crossing. This mode introduces an additional converter operating state, shown in Fig. 7. Before the first leg commutation, the current in phase A falls to zero. Given that synchronous rectification is disabled in this phase during the zero crossing, the diode undergoes reverse recovery and begins blocking, essentially disconnecting the phase from the system, which is reconnected after the leg commutation. The objective during the DCM operating mode is to generate an average current during the switching period equal to the current reference. The voltage phase to neutral u_{an} is

$$u_{an} = \frac{nU_{dc}}{3}\left(2*S_a - S_b - S_c\right) \qquad (4)$$

Near the zero crossing v_a is negligible, so $u_{La} \approx u_{an}$ is an acceptable approximation. During δ_1, when the current is increasing, the current derivative in phase a is

$$\frac{di_a}{dt} = \frac{nU_{dc}}{3L} \qquad (5)$$

The total change in current is found by multiplying the derivative by $\delta_1 T_{sw}/2$, as δ_1 refers to only half of a switching period,

$$\Delta i_a = \frac{nU_{dc}\delta_1 T_{sw}}{6L} \qquad (6)$$

During the freewheeling (000) state, with the simplification of $u_a = 0$, the current in phase a does not change. After the dc side commutation, the converter is again in the 110 state, and the derivative of the current in phase a is the same as calculated in a with opposite sign.

TABLE I
SIMULATION PARAMETERS

Line to line voltage	400V RMS
dc side voltage	400V
Grid inductance	1.3 mH
dc capacitance	10 µH
Turns ratio	1.8
Switching Frequency	50 kHz

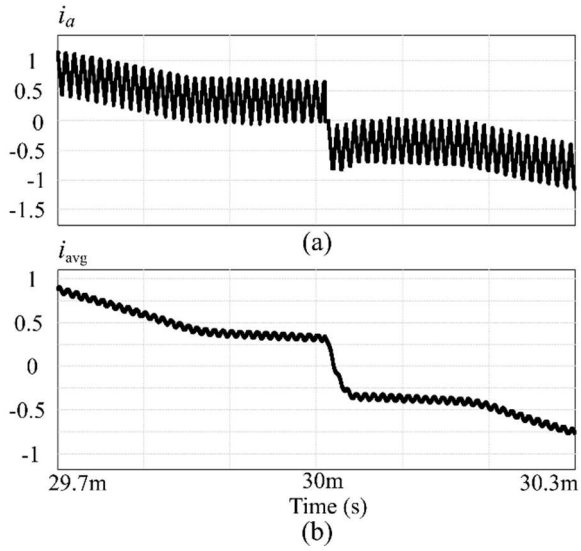


Fig. 8 Sector change with continuous conduction (a) shows the current of phase a, (b) shows the average value of the current.

The average current of the discontinuous conduction mode phase is.

$$i_{avg} = \frac{T_{sw} n U_{dc}}{6L}\left(\delta_1^2 + \delta_1\delta_2\right) \tag{7}$$

δ_2 is calculated as before, shown in Fig. 5. δ_1 is calculated to achieve the desired average current, δ_0 can be obtained from the other two duty cycles

$$\begin{cases} \delta_1 = \dfrac{-\delta_2 + \sqrt{\delta_2^2 + \dfrac{24 I_{ref}^* F_{sw} \mathrm{L}}{\mathrm{nU}_{dc}}}}{2} \\ \delta_0 = 1 - \delta_1 - \delta_2 \end{cases} \tag{8}$$

III. Simulation Results

The proposed control and discontinuous conduction mode are verified by simulation on PSIM. The parameters of the simulation are given in Table I

The performance of the converter with and without the discontinuous conduction mode were compared. Fig. 8 (a) shows the phase current during the sector change in continuous conduction mode (CCM). The average value of the current shown in Fig. 8 (b) is unable to fall to zero, and can only go as low as half the value of the ripple current, about 0.3. It switches polarity at the sector change, introducing distortion in the current shape.

Instead, Fig. 9 (a) shows the phase current during the sector change with discontinuous conduction mode. Once the reference current falls below a certain value, a controlled train of pulses is generated to achieve the reference current. The average does not have any step during the sector change, and the distortion is greatly reduced. The THD on phase currents reduces from 2.52% to 2.19% .

Fig 10 shows the FFT of the dc capacitor voltage in (a) CCM and (b) DCM. By eliminating the current distortion at zero

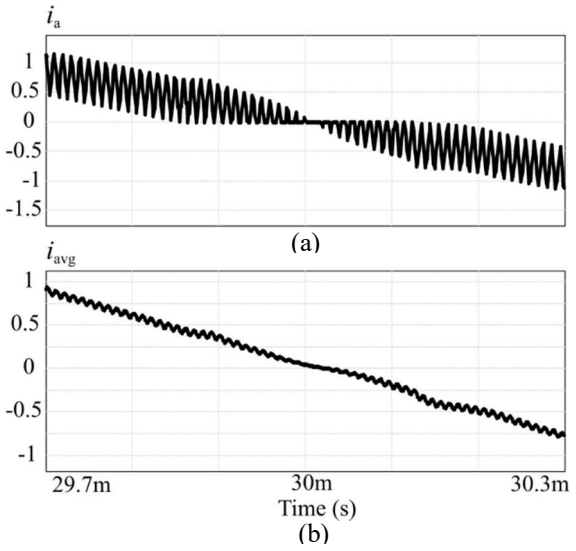


Fig. 9 Sector change with discontinuous conduction (a) shows the current of phase a, (b) shows the average value of the current.

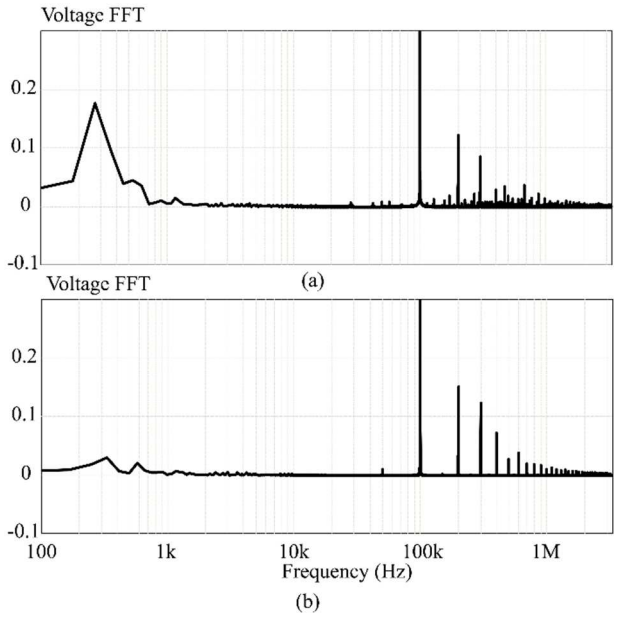


Fig. 10 FFT of dc capacitor voltage (a) in CCM and (b) in DCM.

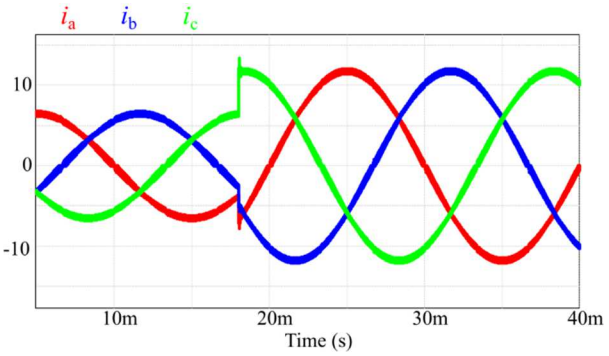


Fig. 11. Response to step change in reference currents. The reference current steps from 6A to 12A in amplitude.

crossing, the low order harmonics in the voltage are greatly reduced. Note that, despite a switching frequency of 50 kHz, the

first switching harmonic is seen at 100 kHz, because of the doubling of the ripple frequency described in Fig. 4.

Fig. 11 shows the response to a step in the current reference. As expected, the dynamic response of the deadbeat controller is very good, however there is still minor overshoot due to sampling delay between measurements and PWM output.

IV. Conclusions

HFLCs are a promising solution for integration of dc technologies in the existing ac distribution grid with isolation. The deadbeat control developed in this paper gives fast dynamic response, low THD, a simple design procedure, and inherent compatibility with SVM. The problem of operation at the boundary between sectors is resolved with the introduction of DCM operation, which is able to accurately track low current references. The resulting controller has reduced THD.

Acknowledgment

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