Auxiliary Resonant Commutated Pole Inverter (ARCPI) with SiC MOSFETs for efficient Vehicle-to-Grid (V2G) charging

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Abstract

The need for energy storages is growing with an increasing share of renewable energy sources in the electricity grid. The roll-out of electric vehicles into the mass market will bring huge battery storage capacities into the grid, which have remained largely unused so far but could be used to temporarily store energy. One key enabler for this is low-cost, efficient and compact power electronics, like the Auxiliary Resonant Commutated Pole Inverter (ARCPI), which is a promising topology for bidirectional AC/DC converters in battery chargers. In this paper, we present the principle of operation and a simulation of the ARCPI. In addition, we provide first results from an ARCPI prototype using SiC MOSFETs designed for a power of up 22 kW, DC link voltages of up to 920 V and peak efficiencies beyond 99 %.

Introduction

Many countries are increasingly using renewable energy for electricity generation to reduce CO_2 emissions to tackle climate change. In order to effectively integrate a high proportion of fluctuating energy sources, e.g. electricity coming from solar and wind, into the grid, additional energy storages, sector coupling and flexibilities in electricity demand are essential.
For the decarbonization of the transport sector, electric vehicles (EVs) are one of the most promising solutions in terms of overall cost and primary energy consumption. Although charging a large number of EVs in future grids can be a challenge in itself, flexible EV charging or even discharging (Vehicle-to-Grid, V2G) could contribute to making electricity grids more sustainable and cost-effective, but still stable and reliable. While some studies state that V2G is not economical in most cases today or in the past [1], [2], recent improvements in battery lifetime [3] and cost as well as inexpensive power-electronics could make V2G more attractive in the near future. The increasing need for energy storage, which can lead to stronger electricity generation price fluctuations, could be another driver for the adoption of V2G. A sharp drop in EV prices due to very high volumes and a high degree of automation in production could even make V2G a competitive alternative to stationary storages in the future, not only for EV drivers but also from the point of view of distribution grid operators or industrial facilities.
The vast majority of today's battery electric vehicles (BEVs) include an on-board charger (OBC) comprising power electronics for AC/DC conversion to allow unidirectional AC charging with a simple wallbox or regular power outlets. While the cost of the OBC slightly increases if it is designed for bidirectional charging, using bidirectional OBCs for V2G is still significantly cheaper than using a dedicated stationary V2G charger in addition to the OBC, since the power electronics would be required twice.
In addition to cost, the efficiency, performance and reliability are important metrics for EV charging electronics. While highly efficient resonant converter topologies oftentimes require additional passive components and semiconductors when compared to hard switching topologies, they can also decrease thermal stress and necessary cooling efforts or increase the switching frequency and therefore allow using smaller filters. In partial load range, where switching losses are one of the main causes of losses,

resonant converters are particularly beneficial. This is not only attractive for powertrain inverters, but also for EV chargers, which oftentimes offer an option to operate with a smaller charging current to increase battery lifetime, and for V2G chargers, which may adjust the charging or discharging current depending on the availability of renewable energy or electricity cost.
A promising resonant AC/DC converter topology to enable bidirectional V2G charging with high efficiency and performance at moderate cost is the Auxiliary Resonant Commutated Pole Inverter (ARCPI). In this paper, we present the principle of operation of an ARCPI and how the transistor control schemes discussed in previous literature [4], [5], [6] can be adapted to be operated efficiently with fast switching wide-bandgap semiconductor switches. After evaluating the switching behavior in a simulation, we introduce an ARCPI prototype designed to operate as a 22 kW bidirectional V2G charger in conjunction with a galvanically isolated DC/DC converter. We discuss the actual switching behavior and provide first insights into the inverter efficiency at different points of operation that have been explored so far.

Theory

Principle of operation

A simplified schematic of a grid-connected Auxiliary Resonant Commutated Pole Inverter is shown in Fig. 1. This implementation of the ARCPI is based on a voltage-source two-level inverter using a B6 topology with six "main" MOSFETs (LS/HS-FETs on branches A/B/C). In addition, there are 3 additional switches that consist of two antiparallel "auxiliary" MOSFETs (AX1/2, BX1/2 and CX1/2). Each auxiliary switch is connected to the center-point of one of the three main half-bridges (A/B/C in Fig. 1) and a resonant inductor ($L_{resA/B/C}$) which themselves are connected to the center point of a split DC-link capacitor ($C_{1/2}$). The resonant capacitors (C_{res}) next to the main MOSFETS in the schematic represent both the parasitic C_{DS} capacitance of the MOSFETs, C_D of the diodes and additional discrete capacitors in parallel to the MOSFETs. In this realization, the inverter is equipped with an LCL-Filter at the AC output, which can be supplemented with a common mode filter (not shown).

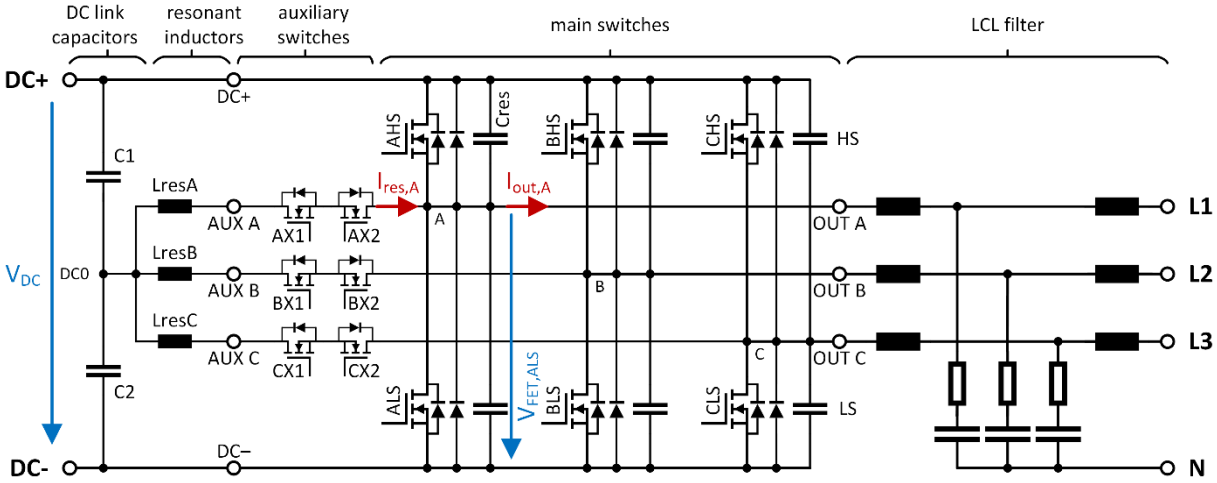

Fig. 1: Simplified schematic of a grid-connected Auxiliary Resonant Commutated Pole Inverter

The main MOSFETs can be controlled almost like in a conventional hard-switching voltage-source two-level inverter, for example by using PWM signals generated by a space vector modulation. The main differences are the transitions between switching states and the exact timings of the main MOSFET turn-offs and turn-ons. An ARCPI enables zero-voltage switching (ZVS) with the aid of the auxiliary switches and resonant components, which transition the potential of the mid-points of the half-bridges (A/B/C) towards the opposite side during the dead time. Depending on the direction and intensity of the half-bridge output current I_{out} at the OUT terminal and on the direction of the half-bridge transitions (from HS- to LS-FET or from LS- to HS-FET), six different cases determine the use of the auxiliary switches to achieve soft-switching. Three of those cases, which apply to the transition from a conducting LS-FET to a conducting HS-FET and use auxiliary FET AX1 (herein called 1.1, 2.1, 3.1), are shown in Fig. 2. The transitions from HS- to LS-FET (cases 1.2, 2.2, 3.2) follow a similar pattern but use the other auxiliary switch AX2 as the polarity of the resonant current $I_{res,A}$ is reversed.

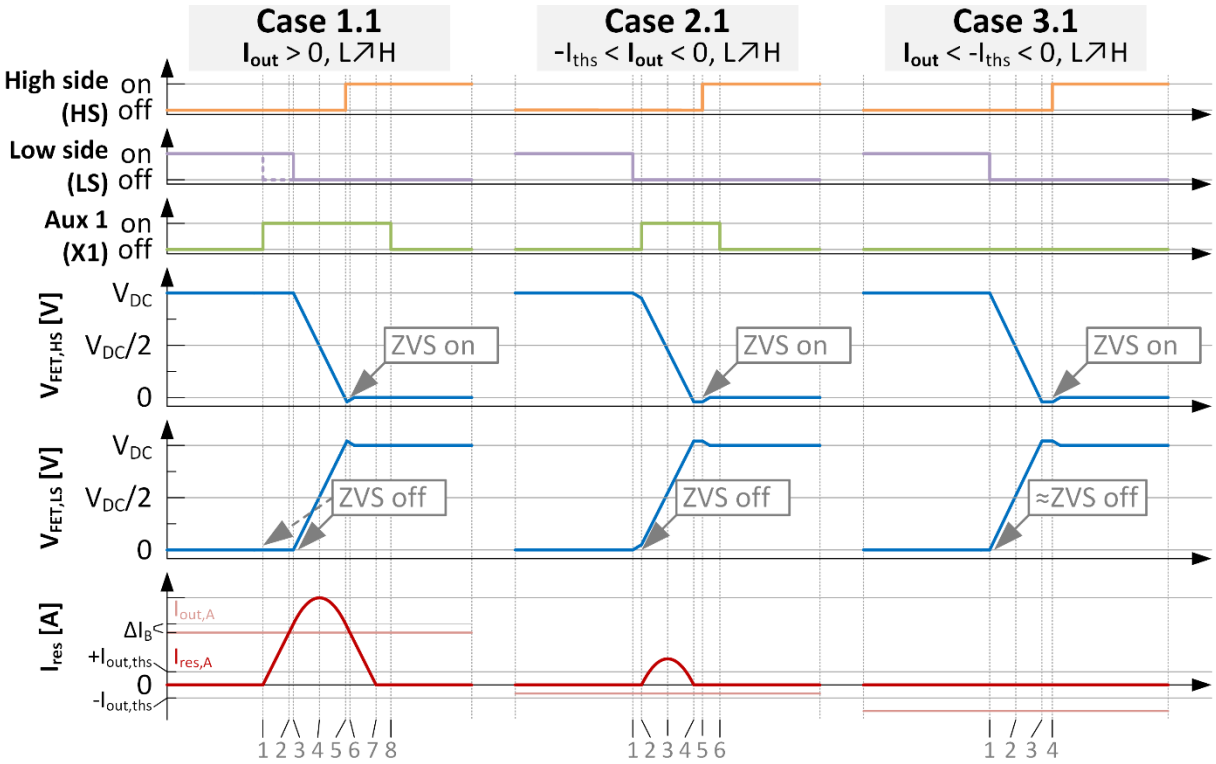

Fig. 2: Switching transition timing with states of high-side, low-side and one of the auxiliary switches (top), HS and LS FET V_{DS} voltages (middle) and resonant current through auxiliary switches (bottom)

To explain the switching transitions, we focus on half-bridge A. Low-side FET ALS is turned on and conducting at the beginning of all cases in Fig. 2. Auxiliary switches AX1 and AX2 as well as high side switch AHS are turned off. We assume that the DC link voltage is split equally by C1 and C2.
In case 1.1, the output current $I_{out,A}$ (as shown in Fig. 1) is positive, so at the beginning, a current is flowing from source to drain of the LS-FET. To initiate the switching transition to the high-side FET AHS, the auxiliary switch AX1 is turned on at t_1 (marker "1" at the bottom of case 1.1 in Fig. 2). Since the voltage between DC0 and DC- is positive and ALS and AX1 are turned on, a positive current $I_{res,A}$ starts to build up through the resonant inductor L_{resA} and the body diode of AX2. $I_{out,A}$ is approximately constant during the observed timeframe because the left LCL-filter inductor prevents rapid current changes. As the HS-FET is still non-conducting, the current through the LS-FET becomes smaller while $I_{res,A}$ rises. After t_2, as soon as $I_{res,A}$ is larger than $I_{out,A}$, the output current is entirely taken over by the auxiliary FET current and the current through the low-side FET reverses polarity. Shortly afterward, the LS-FET is turned off at t_3. Since the current through the LS-FET is relatively low at turn-off and the resonant capacitors limit the dV_{DS}/dt rate, the turn-off losses are comparatively small. The additional current margin between $I_{res,A}$ and $I_{out,A}$ at the time of LS-FET turn-off is called "boost current" I_B in the literature (e.g. [4], [5]). According to [4], this boost phase assures that the resonant inductor is charged with additional energy so the resonant current can carry out a complete voltage transition despite the losses in the resonant inductor and the FETs. The boost current can also be used to balance the two DC link capacitors C1 and C2. In the following period between t_3 and t_5, the resonant current charges the capacitance C_{res} (including $C_{res,ext}$, $C_{DS,FET}$ and $C_{D,diode}$) of the low side and discharges the capacitance of the high-side. The body diode of the high-side FET starts to conduct when the voltage transition finishes, i.e. the low-side FET V_{DS} passes the DC link voltage. The HS-FET should be turned on between t_5 and t_6 since the half-bridge output voltage would otherwise start to fall again once $I_{res,A}$ is smaller than $I_{out,A}$ after t_6. Since the voltage across the FET was already small before turn-on, ZVS turn-on is achieved. As the resonant tank current falls to 0 A until t_7, the HS-FET picks up the output current. AX1 can be turned off as soon as the current in the resonant tank safely declined.
Unlike described in many previous publications (e.g. [4], [5], [6]), it is also conceivable to exclude the boost phase in normal operation and instead turn off the LS-FET before $I_{res,A}$ passes $I_{out,A}$ or even before turning on AX1 (dashed line in LS timing in Fig. 2). In this case, the body diode of the LS-FET will pick up the current and naturally turn off as soon as $I_{res,A}$ passes $I_{out,A}$ (or shortly afterward, considering

diode recovery). Even though the HS-FET may not turn on with a perfect ZVS condition, the vast majority of its turn-on switching losses can be reduced compared to hard switching. More importantly, the advantage is a much lower resonant current, which in turn reduces the losses in the resonant inductor as well as the auxiliary switches and decreases their necessary current capabilities. Since the average current of the auxiliary switches is low, their package can be smaller as long as they withstand the peak current during the transition in case 1.1 with maximum output current.
In case 2.1, the same switching transition is shown, but this time with a negative output current with a small amplitude ($-I_{out,ths} < I_{out} < 0$). At t_1, the low side FET ALS turns off to initiate the switching transition. Since the output current is negative, the output current charges the low-side C_{res} and discharges the one of the high-side, potentially allowing for a natural change of the half-bridge output voltage towards the positive rail. Again, the dV_{DS}/dt rate of the LS-FET is limited. The turn-off losses are relatively small, if ALS quickly turns off, which is the case for typical SiC MOSFETs. AX1 is turned on at t_2 shortly after the ALS turn-off to speed up the voltage transition which finishes at t_4. At this point, the body diode of AHS starts to conduct and the HS-FET is turned on at t_5 with ZVS. AX1 can be turned off after the current of the resonant tank completely declined.
Case 2.3 is similar to 2.2, but this time the output current is larger in amplitude. Since the negative output current changes the output voltage quickly enough on its own, the auxiliary circuit is not needed for the ZVS turn-on of AHS. As the amplitude of the current through ALS is large and therefore its V_{DS} voltage rises comparatively quick, neither zero-current nor zero-voltage switching turn-off can be achieved in the LS-FET. A quick turn-off of ALS is critical to reduce switching losses in this case.

Strengths and weaknesses

A disadvantage of the Auxiliary Resonant Commutated Pole Inverter compared to a voltage-source two-level inverter is its increased complexity. For a three-phase inverter, six additional semiconductor switches including six gate drivers and at least three isolated power supplies, three resonant inductors and typically six resonant tank capacitors are required, which increases cost in the first place. In addition, the DC link capacitor has to be split into two halves and the center voltage should be monitored to assure symmetrical operation. The auxiliary switches might need snubbers and either a circuit to detect the level of the half-bridge output voltage to properly trigger the switching or a look-up table in the controller that determines the switching pattern timing based on DC link voltage and half-bridge output current. The auxiliary switches and their high requirements on exact timing make controlling more complicated. For very high switching frequencies, an advanced PWM generation module in the microcontroller, an FPGA or even a dedicated ASIC might be desirable. The complexity could also negatively impact reliability because more components could fail during operation. The lower dV/dt rates of the half-bridge outputs due to the resonant tank capacitors increase the proportion of time in which the output voltage is not equal to one of the DC rails but lies in between. Especially in inverters with very high switching frequency, this decreased output amplitude might have to be accounted for by the space-vector modulation to improve controller performance and may also impact maximum achievable output voltage magnitude or conversely a higher minimum necessary DC link voltage.
On the other hand, the elimination of the vast majority of switching losses can greatly improve efficiency. It also allows increasing the switching frequency compared to a hard-switching topology, in particular when using SiC MOSFETs, which have smaller turn-on and especially turn-off times compared to Si IGBTs [7]. For grid-connected inverters like EV chargers or PV inverters, the AC filter components can have a much smaller value and size for increased switching frequencies. This decreases cost, volume and weight, which is very important for on-board EV chargers. When using MOSFETs, the switching losses are approximately linear and the conduction losses quadratic to the current [8]. Therefore, for the light-load operation of hard-switching topologies, switching losses tend to dominate over conduction losses. The ARCPI eliminates the majority of switching losses. In light-load conditions, the average currents through the auxiliary switches are low as well, allowing for very high efficiencies even at small loads. This is not only beneficial for EV chargers, which may rarely operate in full-load condition if the owner chooses a small charging power, e.g. to minimize battery aging, but also for EV motor inverters, which operate in part- or even light-load conditions most of the time.
A higher efficiency not only saves electricity cost in operation but may also save cost because of decreased necessary cooling efforts that come with lower power losses. The ARCPI may decrease thermal stress on the semiconductors and the occurring voltage and current overshoots while switching. This can

increase the reliability and lifetime of the inverter, which may compensate for the decreased reliability because of the higher number of components. Smoother switching transitions with reduced dV/dt rates and lower overshoots have the opportunity to greatly improve EMI issues, which can be challenging for hard-switching high-power EV chargers.

Simulation

Simplified models of MOSFETs using ideal switches are often used to increase simulation speed. Such models cannot be paralleled with capacitors and do not properly reproduce resonant switching transitions. On the other hand, more representative models that allow the simulation of resonant circuits and ZVS significantly slow down simulations. Therefore, high-level simulations that run in the timescale of milliseconds to seconds (e.g. to optimize the controller) were performed without the auxiliary circuit using idealized FETs in Simulink and PLECS whereas simulations in a timescale of nano- to microseconds to analyze and optimize the resonant circuit and switching timing were carried out in LTspice.
The switching cases described in Fig. 2 were simulated in LTspice and are shown in Fig. 3. Cree CPM3-1200-0013A SiC MOSFETs were used for the main switches, paralleled by CPW5-1200-Z050B SiC diodes. Cree CPM3-1200-0075A or CPM3-0900-0065A SiC FETs were used as auxiliary switches. The semiconductor models were supplied by Cree. All gate drivers were modeled using exponential output voltage curves with $\tau = 30$ ns and a series resistor. Only one half-bridge leg was simulated and the output current was modeled by a constant current source between half-bridge output and DC-.
With $L_{res} = 900$ nH, $C_{res} = 1$ nF (excluding parasitic MOSFET and diode capacitances), a DC link voltage of 800 V and output currents between +45 and -45 A (peak currents at 32 A_{rms} AC output), switching times in the range of 100 to 400 ns could be realized. Shorter switching times can be achieved with smaller resonant component values. However, they make it harder to turn on and off the MOSFETs at the right moment as typical gate driver and MOSFET turn-on and turn-off times are almost in the order of magnitude of the complete switching transition. On the other hand, longer switching times decrease the usable on-time for the PWM which is targeted to run at 100 kHz.
The simulation, which included ohmic losses in the resonant components, showed that nearly a complete transition of the half-bridge output voltage is possible even without a boost phase. In fact, the boost current significantly increased the resonant current and therefore conduction losses in the auxiliary path.

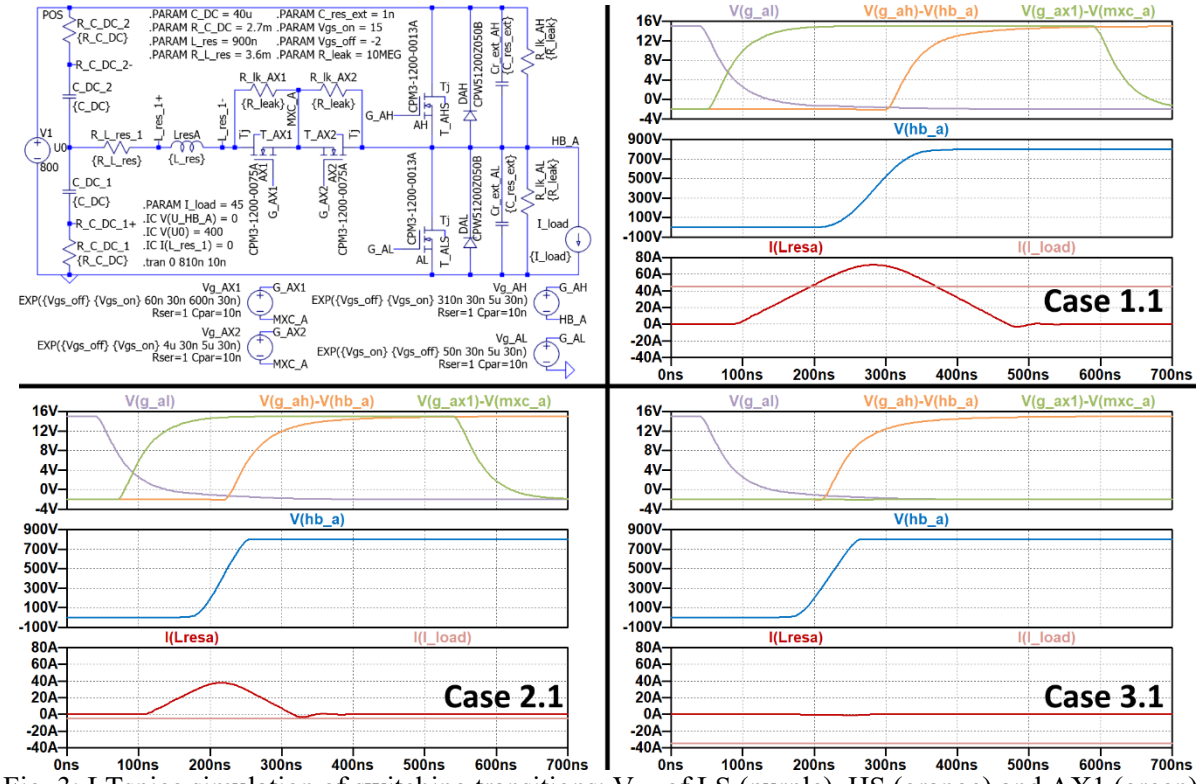

Fig. 3: LTspice simulation of switching transitions: V_{GS} of LS (purple), HS (orange) and AX1 (green) FET, V_{DS} of LS-FET (blue), resonant inductor current $I_{res,A}$ (red) and output current $I_{out,A}$ (light red)

Prototype

Description of hardware and software

We developed an ARCPI prototype, shown in Fig. 4, which is designed to operate at up to 22 kW and with a switching frequency of 100 kHz. This bidirectional AC/DC converter shall operate with a flexible DC link voltage of 360 – 920 V (depending on the grid connection, single- or three-phase) to charge a li-ion battery together with an isolated DC/DC converter. The inverter includes sufficient DC-link capacitance to assure a stable DC-link voltage even in single-phase operation as well as grid-side relays, overvoltage protection and an AC filter designed to allow for a direct grid connection.
We developed and manufactured custom power modules for the inverter that comprise six Cree CPM3-1200-0013A SiC MOSFETs as main and six CPM3-0900-0065A SiC FETs as auxiliary switches. Some versions of the module include additional Cree CPW5-1200-Z050B SiC freewheeling diodes and/or additional high-temperature SMD capacitors for each half-bridge. A PT1000 temperature resistor from Heraeus is sintered into all modules to monitor the temperature close to the dies. Six additional pins in the center of the module for the low-side switches enable a compact design into an Infineon EconoPACK 2 housing. Pressureless copper sintering was used to attach the large WBG-semiconductors on the bare copper surface of a Si_3N_4-AMB substrate. The sintering process was performed under an H2-atmosphere at a peak temperature of 260 °C and a peak time of 10 minutes. The copper sinter paste is a prototype paste provided by Showa Denko Materials Co., Ltd., Japan. After the sintering, the top side of the dies was connected by 200 µm Al-wires. The complete module was encapsulated by a soft silicone gel.

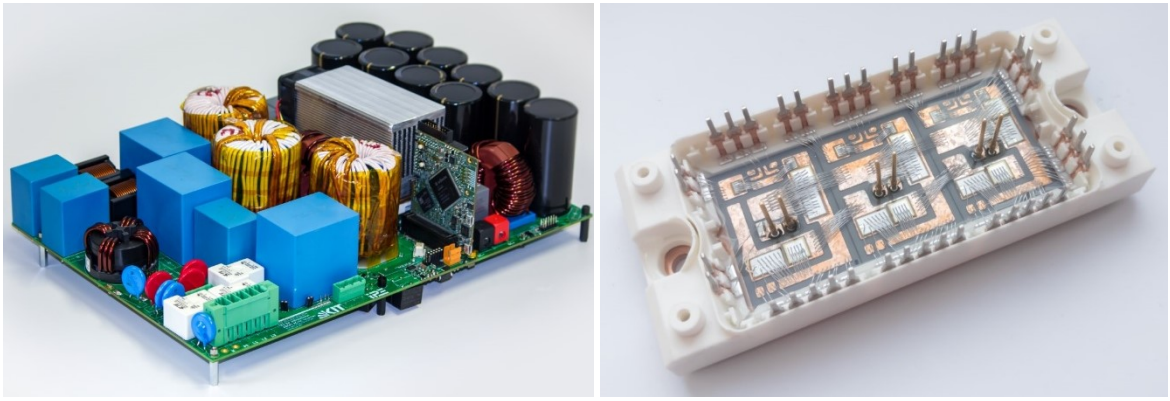

Fig. 4: Photo of the ARCPI prototype (left) and its custom power module (right)

Because of the relatively high switching frequency, short resonant switching times and to increase flexibility in the prototype, a Xilinx Spartan-7 FPGA (XC7S50 series) was chosen to control MOSFET switching, acquire measurement values from ADCs and process derived measurement values like direct/quadrature voltages and currents as well as grid frequency and phase. We used the TASKING TriCore Software Development Toolset to develop software for an Infineon Aurix TriCore TC275 microprocessor that is used in parallel to the FPGA. It is used to calculate the PWM duty cycles in order to control voltages and currents as well as for high-level controlling (e.g. adjusting AC power depending on the grid frequency) and communication with other components of the battery charger (e.g. DC/DC converter, user interface and energy management system). Redundant monitoring of critical measurement values and detection of fault states in both FPGA and microcontroller ensure increased reliability and safety. The data transfer between FPGA and microcontroller is secured with a CRC8 checksum and power conversion is stopped in case one of the two controllers freezes or sends implausible values.
The size of the prototype is 353.0 x 248.5 x 90.5 mm with a weight of 8.78 kg, including all DC and AC filters, AC relays, precharge resistors and forced air cooling, but excluding housing and external cables. With a maximum power of 22 kW, the power density results in 2.77 kW/dm³ and 2.51 kW/kg. The vast majority of space and weight is used for AC filtering.

Switching behavior

In order to make use of soft-switching wherever possible, the timing of the auxiliary and main FET on- and off-times have to be determined depending on the operation point at each switching period. As

already mentioned in the theory of operation, the transition speed of each half-bridge output voltage depends on the polarity and magnitude of the momentary current at its output. It also depends on the values of the discrete resonant inductors and capacitors as well as the voltage-dependent, non-linear MOSFET and diode capacitances. The DC link voltage itself also influences transition time, because, for a given output current, more charge has to be transferred between LS and HS capacitances.
In the prototype, a half-bridge output mid-voltage detection circuit was implemented using comparators to notify the FPGA when the drain-source voltage of a MOSFET passes half the DC voltage during a switching transition. This was intended to allow for a dynamic dead time estimation during the switching transition without further knowledge of the exact operating point. However, so far it was also sufficient to store a fixed MOSFET timing look-up table (LUT) into block read-only memory (BROM) sections of the FPGA and determine the switching timing of the MOSFETs based on the DC link voltage and the momentary half-bridge output current, which is measured in addition to the filtered grid current for safety and reliability reasons. Since the resonant tank values and the semiconductor capacitances are known and delays of the gate driver circuit can be determined in advance as well, the LUT method which does not make use of the mid-voltage detection circuit is a cheaper solution, especially if the half-bridge output current is measured anyway.
Before each switching period begins, the FPGA starts the timing calculation with reference turn-on and turn-off times derived for each of the three PWM duty cycle values requested by the microcontroller (see Fig. 5, also compare to t_4 of case 1.1 in Fig. 2). Depending on the latest DC link voltage and half-bridge output current measurement, four timing values are read from the BROM for each transition: $t_{aux,on,prepone}$ and $t_{main,off,prepone}$, which are subtracted from the reference timing point, as well as $t_{aux,off,postpone}$ and $t_{main,on,postpone}$, which are added to the reference timing point.

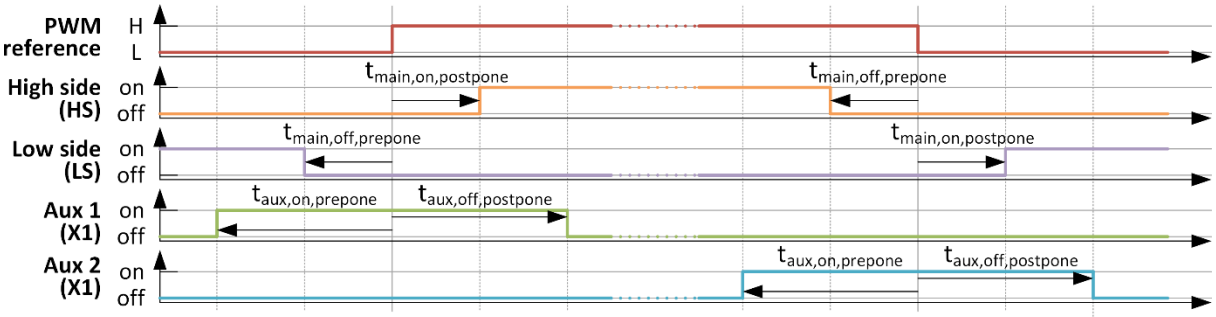

Fig. 5: Turn-on and turn-off timing of auxiliary and main MOSFETs relative to the ideal PWM edges

The timing was calculated for each combination of discretized DC link voltage and half-bridge output current values considering the non-linear MOSFET and diode capacitances, the external resonant capacitor and inductor values as well as estimated delays, turn-on and turn-off times of the gate driver. The temperature, saturation and manufacturing tolerance of the resonant inductor were not taken into account yet, but may also be incorporated. The timing was evaluated and optimized in the simulation and during measurements on the inverter. The LUT used at the moment is visualized in Fig. 6: In area 1, the auxiliary FETs are used for the switching transition (cases 1.1, 1.2, 2.1 and 2.2). Cases 3.1 and 3.2 are lying in area 2. In area 3, a soft switching transition would take relatively long in comparison to the PWM period and thus hard switching is used instead. However, this only affects operating conditions with low DC link voltages and high currents which are not relevant for regular operation in the grid.
The actual soft switching behavior measured at the inverter is shown in Fig. 7: Digital signals coming from the FPGA are shown in the upper half while the lower half shows analog measurements of the power circuit, namely the DC link voltage and the voltage V_{DS} across the ALS MOSFET (green curve). The light-red area in the V_{DS} graphs between markers 1 and 2 shows the dead time area in which the gate drivers of both the low-side and the high-side FETs are turned off (already considering the gate driver signal propagation delay from FPGA to the gate side of the gate driver). Since the MOSFETs turn off in less than 150 ns from point 1 and they start to turn on at point 2, zero-switching turn-off and turn-on can be achieved in all cases with a smooth voltage transition in between. However, marker 3 in case 1.2 shows that actually no perfect zero-switching is achieved, but a small voltage is still present when the MOSFET turns on in cases 1.1 and 1.2. In this example, approximately 11 V are still present at turn-

on, i.e. less than 4 % of the DC link voltage. This is because unlike proposed in the literature, this inverter usually doesn't use a boost phase to decrease auxiliary switch and resonant tank current (compare chapter "Principle of operation"). The inverter only includes a boost phase when balancing of the two DC link halves is required, i.e. when the upper and lower DC link voltage vary by more than 3 V. Boosting is only performed for switching transitions that push the DC link center voltage into the right direction and if the output current is not higher than a certain limit (to limit the resonant tank current and decrease losses). In this case, the respective auxiliary FET is turned on up to 70 ns earlier and the corresponding main FET turns off up to 70 ns later to increase the resonant tank current for balancing.

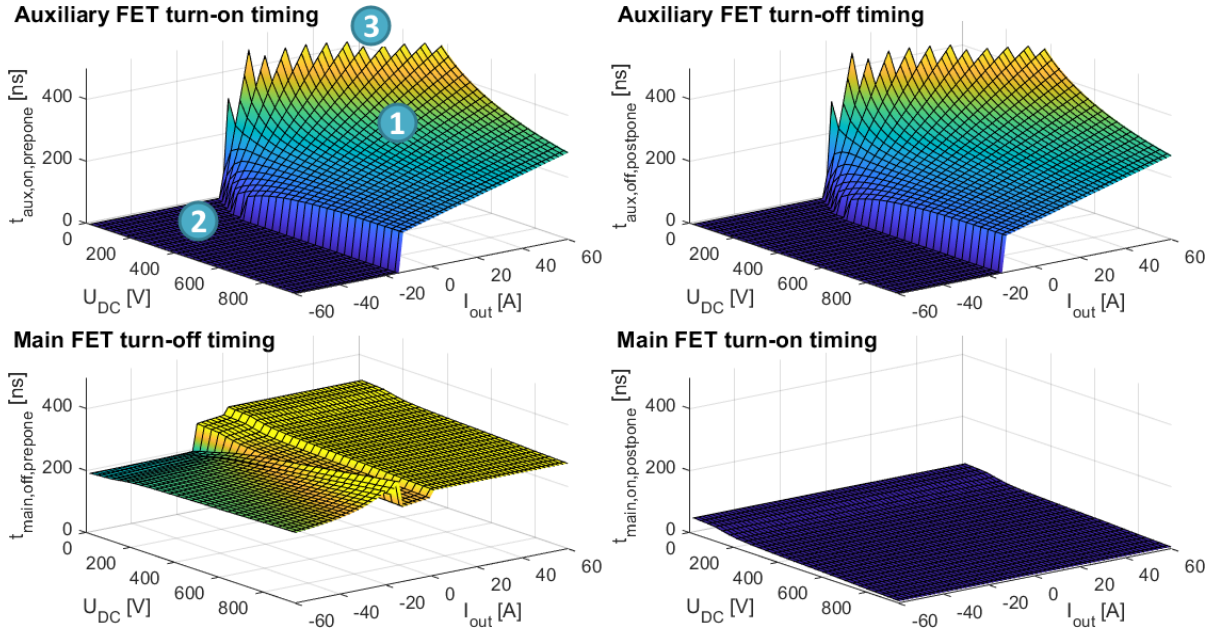

Fig. 6: FET timing values of the look-up-table based on DC link voltage and half-bridge output current

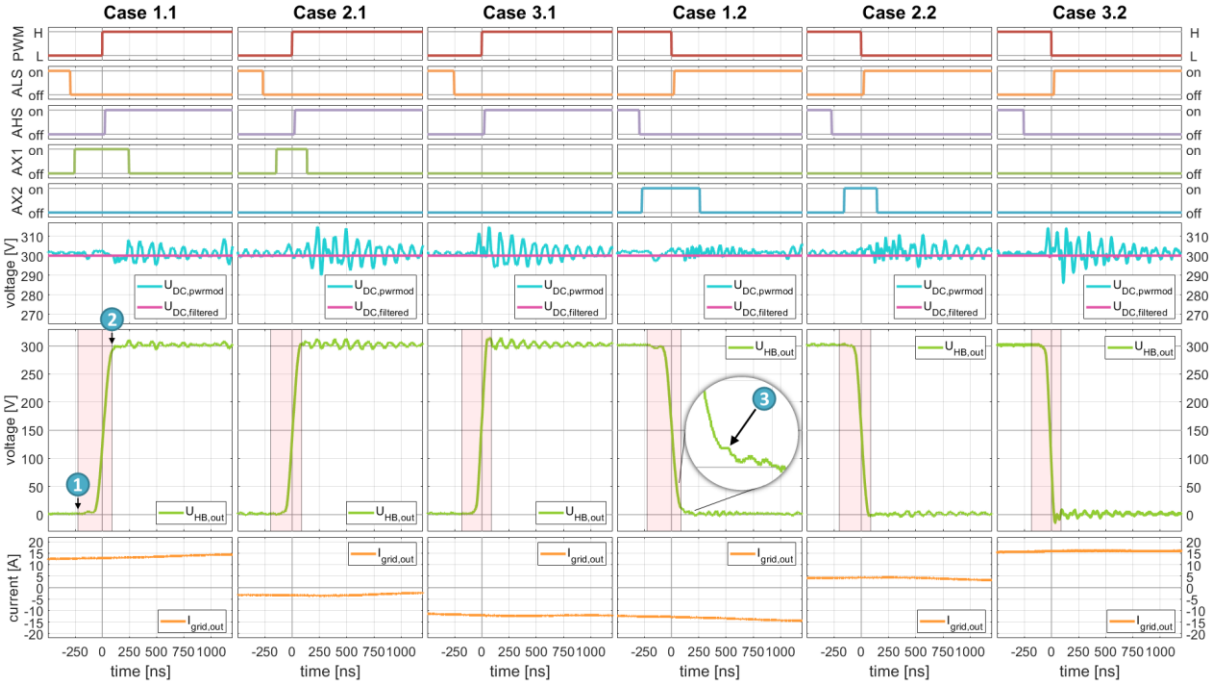

Fig. 7: Measurements of all switching transition cases taken at one phase of the prototype – from top to bottom: PWM reference signal (red), signals to gate drivers of low side (orange), high side (purple), auxiliary switch 1 (green) and 2 (blue), DC link voltage measured at the power module (cyan) and the inverter DC terminal (pink), voltage V_{DS} of the low-side MOSFET (green), grid output current (orange)

Less than 5 % overshoot and ripple are present in the unfiltered DC link voltage and the MOSFET drain-source voltages. Less than 0.5 % ripple exists in the filtered DC voltage connected to the power supply. The maximum voltage gradient of V_{DS} measured at a DC link voltage of 300 V is approximately 3 kV/µs in cases 3.1 and 3.2. This gradient can be controlled by choosing different resonant tank capacitor values. The half-bridge output voltages pass through half of the DC link voltage with a deviation of ±25 ns from the ideal PWM reference signal, which results in PWM duty cycle errors of less than 0.25 %.
Even though the half-bridge output current looks very smooth, the voltages across the auxiliary FETs and between power module pins AUX A/B/C and DC- (see Fig. 1) show significant oscillations after each voltage transition, in which auxiliary FETs are used, finishes. In the left side of Fig. 8, a measurement of the half-bridge output voltage (OUT A to DC-) and the voltage between AUX A and DC- is shown for V_{DC} = 500 V during an LS to HS FET transition with a small negative output current (case 2.1). The oscillations are capped by protection diodes connected between AUX A/B/C and DC+/-. For a better understanding, the same operating point is simulated in LTspice (plot in the center of Fig. 8).
While we have not yet fully identified the cause and the implications of the oscillations, we suspect that the reverse recovery charge Q_{rr} of the auxiliary FET body diode used in the transition (here: AX2) poses an issue when the current I_{res} passes 0 A at t ≈ 400 µs and turns off the body diode. The charge then excites another resonant circuit after the complementary auxiliary FET AX1 is turned off. This resonant circuit is formed by L_{res} and C_{DS} of one auxiliary FET (depending on the current direction) and is damped by the voltage drop over the body diode. Even though the oscillations do not noticeably influence the in- or output voltages and currents of the inverter or its efficiency, they could cause EMI problems and possibly harm the auxiliary FETs, which is why they should be eliminated in the future. Using different MOSFETs with a lower Q_{rr} could be a possible solution. A simulation of the same operating point with a CPM3-1200-0075A auxiliary FET shows significantly improved behavior (right side of Fig. 8).

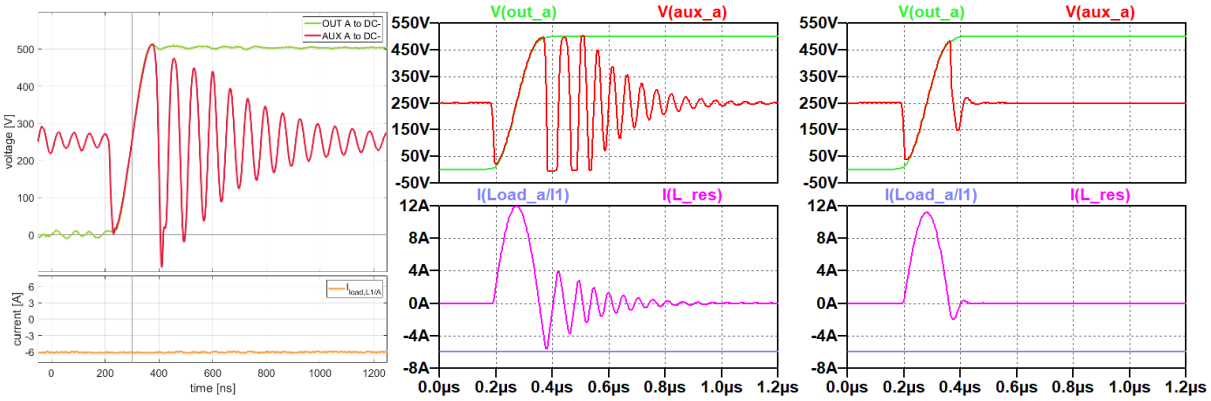

Fig. 8: Detailed view of the half-bridge output voltage “OUT A” and the voltage between power module pins “AUX A” and “DC-“ (see Fig. 1) at V_{DC} = 500 V measured in the prototype using CPM3-0900-0065B auxiliary FETs (left) and the same operating point in the simulation using the same FETs (center) and a CPM3-1200-0075A as a replacement for the auxiliary FETs (right)

Output characteristics, efficiency and losses

So far, the inverter has only been tested in vehicle-to-load mode, i.e. transferring power from a DC supply to an AC load, with a DC link voltage of up to 500 V and output powers of up to 11 kW. Further measurements with DC link voltages of up to 920 V, AC voltages of up to 255 V, powers of up to 22 kW and other operating modes have yet to be carried out. Output voltages of all three phases L1/L2/L3 and the current of L1 in DC to AC operation mode at V_{DC} = 210 V and $V_{AC,RMS}$ = 50 V using 10 Ω load resistors for each phase are shown in Fig. 9 (left). The AC current ripple is smaller than ±0.1 A and the voltage ripple smaller than ±1 V in this operating point. All efficiency measurements taken to this point are shown in Fig. 9 (right side, blue points). The efficiency does not include the power consumption of the controller and relays (ca. 9.5 W) as well as the air cooling. For powers >1 kW, the efficiency is well above 95 % with a peak efficiency of 99.2 % measured at V_{DC} = 400-450 V, $V_{AC,RMS}$ = 160-180 V, $I_{AC,RMS}$ = 16-18 A and P_{AC} = 9-11.5 kW. We performed a loss calculation that matches the measured losses by ±6 W and extended the efficiency plot to other operating points with higher voltages and output powers (dashed lines). We expect efficiencies of more than 97 % in most typical operating points. The

main contributors to losses are the conduction and core losses of the AC inductors, the conduction losses of the main MOSFETs followed by PCB conduction losses but also conduction losses in the auxiliary FETs. Instead of using the body diode of one of the auxiliary FETs during switching transitions, both FETs could be turned on to further reduce losses. The inverter shall be operated together with a bidirectional resonant DC/DC converter [9] in the future and dynamically adjust the DC link voltage based on the battery and grid voltages and currents to maximize efficiency and performance.

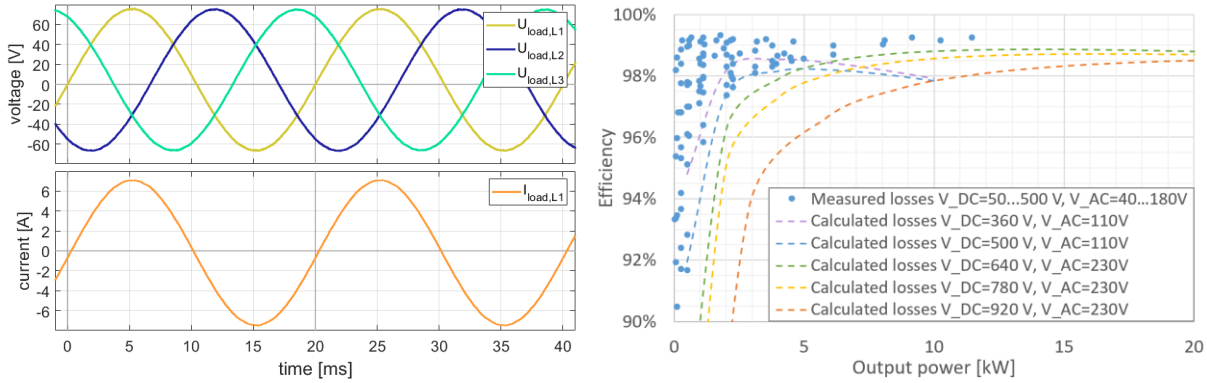

Fig. 9: Measured AC output voltages and current of L1 at V_{DC} = 210 V, $V_{AC,RMS}$ = 50 V, $R_{load,AC}$ = 10 Ω (left), measured (points) and calculated (lines) efficiencies for power transfer from DC to AC (right)

Conclusion and outlook

Vehicle-to-Grid is a promising solution for the intermediate storage of energy to cost-effectively increase the share of renewable energy sources in the electricity grid. In order to deploy V2G in the mass market, inexpensive, reliable, powerful and efficient bidirectional power electronics is required for battery chargers. The Auxiliary Resonant Commutated Pole Inverter (ARCPI) is a bidirectional resonant AC/DC converter that could be used in such a V2G charger. In this paper, we described its principle of operation and validated the switching behavior in an LTspice simulation. We demonstrated the operation of the ARCPI on a 22 kW prototype and presented first results of its efficiency and switching behavior. The peak efficiency measured so far is more than 99.2 % and we expect a typical efficiency of more than 97 % in relevant operating points. The converter is yet to be tested with higher voltages and powers, and the oscillations in the resonant circuit shall be reduced in the future as well.

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