Karlsruhe Institute of Technology

Development of CMOS Sensors for Scientific and Industrial Applications

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Doctor Thesis

At the Fakultät für Elektronik
Institut für Prozessdatenverarbeitung und Elektronik (IPE)

Reviewer:	Prof. Dr. Ivan Perić
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Duration:	18. September 2017 – 25. September 2023
Submission:	Karlsruhe, 25. September 2023

Entwicklung von CMOS-Sensoren für wissenschaftliche und industrielle Anwendungen

Zur Erlangung des akademischen Grades eines
DOKTORS DER INGENIEURWISSENSCHAFTEN (Dr.-Ing.)

von der KIT-Fakultät für Elektrotechnik und Informationstechnik des
Karlsruher Instituts für Technologie (KIT)
angenommene

DISSERTATION

von

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Tag der mündlichen Prüfung:	25. September 2023
Hauptreferent:	Prof. Dr. Ivan Perić
Korreferent:	Prof. Dr. Ahmet Cagri Ulusoy

I declare that I have developed and written the enclosed thesis completely by myself, and have not used sources or means without declaration in the text.

Karlsruhe, the October 18, 2023

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(**Horacio Mateos**)

Abstract

Radiation detection is important for many applications. Existing pixel sensor technologies are not suitable for high energy particle detection. Customized image sensor chips are therefore needed. This thesis proposes two novel particle pixel sensor chip designs.

Within my PhD work, I have developed monolithic pixel sensor based on High Voltage COMOS (HVCMOS) technology for electron microscopy and monitoring of ion beams. HVCMOS technology allows implementation of low voltage transistors and high voltage devices on the same substrate. It is possible to implement readout electronics and sensor diodes biased with high voltage on the same chip.

The main projects, described in this thesis, are the HINT sensor, developed for beam monitoring in a radiation therapy center, and the HPIXEL sensor, designed to be used as an image sensor for electron microscopy. I also developed test systems for two chips (SWITCHER and DCD) for the Belle II experiment.

HINT was developed in TSI Semiconductor high voltage CMOS 180 nm technology. Novel integrator has been implemented that can measure the signal charge in wide dynamic range with linear response (from 12 fC up to 3000 fC), with low noise (0.8 fC), without saturating the integrator. HINT has demonstrated that charge integration is an effective method for high-intensity beam diagnostic purposes. The sensor design included several enclosed transistors for improved radiation hardness since the application requires it. I developed a test system and performed measurements on the chip.

The second theme of my work was the development of the pixel sensor for electron microscopy - HPIXEL. I have developed test systems and performed measurements. In the first iteration of the sensor showed insufficient radiation tolerance, I modified the design to improve radiation tolerance.

As third part of my work I have developed the test system for two ASICs for Belle II experiment (DCD and SWITCHER) and tested ∼350 chips in total.

Zusammenfassung

Die Erkennung von Strahlung ist für viele Anwendungen wichtig. Bestehende Pixelsensortechnologien sind für Nachweis hochenergetischer Teilchen nicht geeignet. Es werden daher maßgeschneiderte Pixelsensorchips benötigt. In dieser Arbeit werden zwei neuartige Chips für Teilchennachweis vorgeschlagen.

Im Rahmen meiner Doktorarbeit habe ich monolithische Sensorchips in HVCMOS-Technologie für die Elektronenmikroskopie und die Überwachung von Ionenstrahlen entwickelt. Die Hochspannungs-CMOS (HVCMOS) Technologie ermöglicht die Implementierung von Niederspannungstransistoren und Hochspannungsbauteilen auf demselben Substrat. Es ist möglich, Ausleseelektronik und die Sensordioden mit hoher Vorspannung auf demselben Chip zu implementieren.

Die wichtigsten Projekte, die in dieser Arbeit beschrieben werden, sind der HINT-Sensor, der für Beam-Monitoring in einem Ionenstrahltherapiezentrum entwickelt wurde, und der HPIXEL-Sensor, der als Bildsensor für die Elektronenmikroskopie eingesetzt werden soll. Außerdem habe ich Testsysteme für zwei Chips für das Belle II Experiment entwickelt.

HINT wurde in TSI-Semiconductor Hochspannungs-CMOS 180 nm Technologie entwickelt. Es wurde ein neuartiger Integrator implementiert, der die Signalladung in einem großen dynamischen Bereich mit linearem Ansprechverhalten (von 12 fC bis 3000 fC) und geringem Rauschen (0,8 fC) messen kann, ohne dass der Integrator in die Sättigung geht. HINT hat gezeigt, dass die Ladungsintegration eine wirksame Methode für die Diagnose mit hochintensiven Strahlen ist. Ringförmige Transistoren wurden benutzt, um die Strahlungshärte zu verbessern, da die Anwendung dies erfordert. Ich habe ein Testsystem entwickelt und Messungen auf dem Chip durchgeführt.

Das zweite Thema meiner Arbeit war die Entwicklung des Pixelsensors für die Elektronenmikroskopie - HPIXEL. Ich habe ebenfalls hier Testsysteme entwickelt und Messungen durchgeführt. Die erste Iteration des Sensors hatte eine unzureichende Strahlungstoleranz. Ich habe ein verbessertes Design vorbereitet.

Als dritten Teil meiner Arbeit habe ich das Testsystem für zwei ASICs für das Belle II Experiment (DCD und SWITCHER) entwickelt und insgesamt ∼350 Chips getestet.

Contents

1 Introduction

The theme of this thesis are semiconductor sensors for heavy particles, electrons, and gamma-ray detection. The use of silicon semiconductors for this application is not new, the discovery of the electron-hole pair production in germanium by the hit of alpha particles dates back to the early 1950s [51]. Later in the 1980s, the innovations in sensor manufacturing allowed the technology to be scaled up and used in the field of high-energy physics, with the first silicon detector used at CERN in 1983 [30]. From there the development just continued to evolve.

Today, the use of silicon detectors for radiation detection is widely adopted, since they have several advantages compared to other devices (such as gas-filled detectors and scintillators). They can achieve good energy resolution, stability, time resolution, and simplicity of operation [38].

This dissertation is structured as follows:

In sections 1.1 and 1.2, a brief introduction of mechanism of radiation detection, as well as an overview of the CMOS sensors topologies are presented.

Chapter 2 explains the working principle of a sensor called HPIXEL, designed for electron microscopy. The building blocks of sensor HPIXEl will be explained, as well as the test system (FPGA, software and firmware). Finally, the measurement results are presented.

Chapter 3 describes the sensor called HINT. This chip was developed for radiation detection of protons and carbon ions and the working principle will be explained as well as the main building blocks of the sensor. The setup (FPGA, software and firmware) used to control the sensor will be described, and the measurements presented.

Chapter 4 gives an introduction to the Belle II experiment, and the test setup for the SWITCHER and DCD ASICs.

Chapter 5 shows the work done for the ADL group by wire bonding the sensors developed.

Chapter 6 presents an evaluation and conclusion of this work from the author's point of view. It also throws some light on the prospects of this research.

1.1 Detection of charged particles

When charged particles, such as alpha particles, beta particles, or protons, pass through a material, they interact with the atoms of the material. These interactions cause the particles to lose energy, which results in the slowing down, or stopping, of the particles. The amount of energy lost by the particles, and thus the amount they are slowed down, depends on the properties of the material and the energy and type of the particles. The stopping power of a material is defined by The International Commission on Radiation Units and Measurements (ICRU) as the average energy loss by ionizing radiation in the material per unit path length of travel of travel of the radiation in the medium [31].

Silicon semiconductors has several advantages over gas-filled detectors. Due to the higher density of silicon, the stopping power of the sensor is much larger compared to gaseous detectors, and the average energy necessary to ionize silicon is much smaller than in gases (around four times less) [38, 60].

In this section, I will present the interaction of charged particles with matter, as well as different ways to measure the energy deposited by the particles in the silicon substrate.

Energy loss by a charged particle

When a charged particle passes through a silicon semiconductor, it will loose a part of its energy due to the interaction (mostly by Coulomb interaction at lower speeds [54]) between the particle and the electrons of silicon, resulting in the generation of electron-hole pairs along the track of the particle. The average energy required for production of an electron-hole pair is called *ionization energy*, and for silicon is equal to $\sim$3.6 eV [38].

The amount of energy lost by each interaction between the charge particle and an electron in silicon is relatively small, but thanks to the high density of the material, there is a large cumulative energy loss. The average energy loss of a charged particle per unit path length (also called stopping power) was calculated by Bethe and Bloch [45] (eq 1.1).

$$-\frac{dE}{dx} = 2\pi N_a r_e^2 m_e c^2 \rho \frac{Z}{A}\frac{z^2}{\beta^2}\left[ln\left(\frac{2m_e\gamma^2\upsilon^2 W_{max}}{I^2}\right) - 2\beta^2 - \delta - 2\frac{C}{Z}\right] \tag{1.1}$$

where

$2\pi N_a r_e^2 m_e c^2$:	0.1535 MeVcm^2/g
r_e :	classical electron radius = 2.817×10^{-13} cm
m_e :	electron mass = 9.109×10^{-31} kg
N_a :	Avogadro's number = 6.022×10^{23} mol^{-1}
I :	mean excitation potential
Z :	atomic number of absorbing material
A :	atomic weight of absorbing material
ρ :	density of absorbing material
z :	charge of incident particle in units of e
β :	υ/c of the incident particle
γ :	Lorenz factor $1/\sqrt{1-\beta^2}$
δ :	density correction
C :	shell correction
W_{max} :	maximum energy transfer in a single collision

The Bethe-Bloch formula (eq 1.1) tells us that the energy loss per length unit, at non-relativistic energies, is dominated by the $1/\beta^2$ factor, and decreases when the velocity

of the charged particle increases, until it reaches a minimum around $\upsilon \approx 0.96\,\mathrm{c}$, i.e. when the particle energy becomes about 3.6 times higher than its rest energy mc^2. As the energy increases dE/dx rises again due to the logarithmic dependence, however, this is canceled by the density correction factor δ [45]. Figure 1.1 shows the above-described shape of the Bethe-Bloch formula.

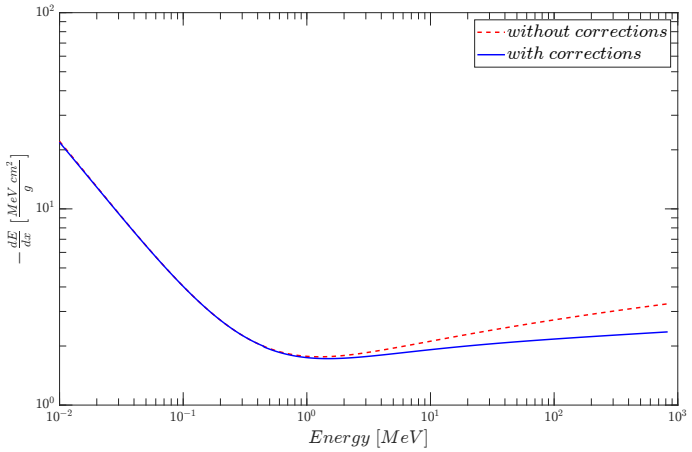


Figure 1.1: Plot of Bethe-Bloch formula for non-relativistic electron energies with and without shell and density corrections in silicon.

Electron-hole pair generation in silicon

When a charged particle travels through silicon, part of its energy will be transferred to atomic electrons. That energy can ionize the material and generate electron-hole pairs. The amount of charge that will recombine depends on the electron-hole density as well as time. If left alone, those charges will travel outward from the point of generation through the silicon by diffusion. Along the path they will scatter on silicon atoms, losing their energy until eventually, they recombine [88].

If a voltage is applied to the silicon sample, the electron-hole pairs generated will experience a force (due to the electric field) which will make them move towards the electrodes, decreasing the amount of recombined charge and creating a current proportional to the energy deposited (figure 1.2). The current generated is called drift and dominates over diffusion current. The sensors developed in this thesis use drift current as charge collection mechanism.

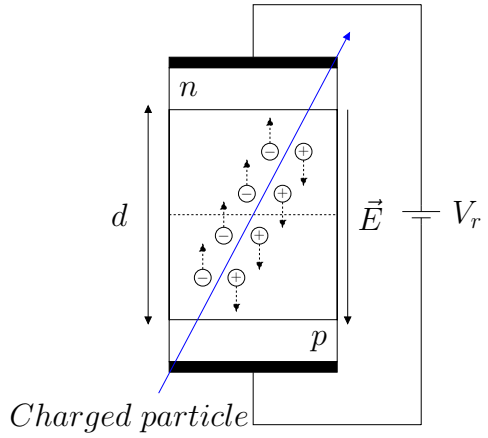


Figure 1.2: Sensor cross-section with an electron-hole pair generated by a charged particle passing through silicon.

1.2 Semiconductors

Semiconductor devices are fundamental in almost every electronic device. They are usually manufactured with silicon, in which impurities are embedded to modify, in a controlled way, the electrical characteristics.

Pure silicon is an example of a semiconductor. By itself, silicon has high resistance, which is possible to manipulate by adding atoms of a different material to the crystalline structure of silicon [66].

When silicon is doped with donor impurities, atoms with five valence electrons, four of them will bond to the electrons of silicon atoms, while the fifth electron stays unpaired and weakly bonded to the lattice. Small energy is required to dislodge it. This type of semiconductor is called n-type [66].

On the other hand, if the silicon lattice is doped with a trivalent impurity, atoms with three valence electrons, all of them will bond to the electrons of silicon atoms, and one silicon electron stays unpaired, creating a charge vacancy (hole) free to bond with an electron. This type of material is called p-type [50, 66].

pn junction in silicon

When two different semiconductor types (p and n) are put together, holes from the p-type will defuse to the n region. This will result in the recombination process and the disappearance of some free electrons from the n-type. The fixed charges of silicon atoms (missing one electron) will no longer be neutralized by free electrons. This will create a positive net charge close to the junction. On the other side, the electrons that diffuse to the p-type region will quickly recombine with the holes there, and this in turn will result in a negative net charge near the junction [4].

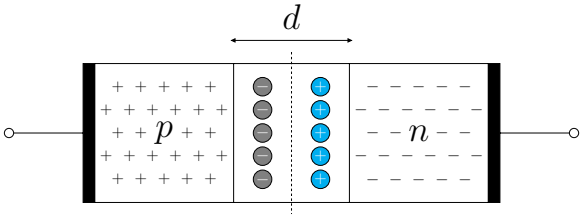


Figure 1.3: pn junction cross section. d is the width of the depleted region.

Since the fixed charge is present on each side of the junction, the depletion region in the pn junction can be modeled as a capacitor, where the capacitance will depend on depleted layer thickness (or junction thickness), as shown in equation 1.2:

$$C = \epsilon_{Si} \frac{A}{d} \tag{1.2}$$

where

ϵ_{Si} : silicon permittivity = 1.06×10^{-10} F/m
d : thickness of the depletion region
A : area of the depletion region

Reversed biased junction

While the unbiased (shorted) *pn* junction can work as a detector, the electric field generated in the depleted region will not be intense enough to provide an efficient charge collection and the small depletion width creates a larger capacitance which leads to small voltage signals or high noise. When a reverse voltage is applied to the *pn* junction, the depleted region width d increases following the equation 1.3 [5]. Figure 1.4 illustrates this process.

$$d = \sqrt{\frac{2\epsilon_{Si}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)(V_0+V_r)} \tag{1.3}$$

where

ϵ_{Si} : silicon permittivity = 1.06×10^{-10} F/m
q : electron charge = 1.602×10^{-19} C
N_A : doping concentration of the p-type
N_D doping concentration of the n-type
V_0 junction built-in voltage, for silicon at room temperature is about 0.6 V
V_r reverse voltage applied

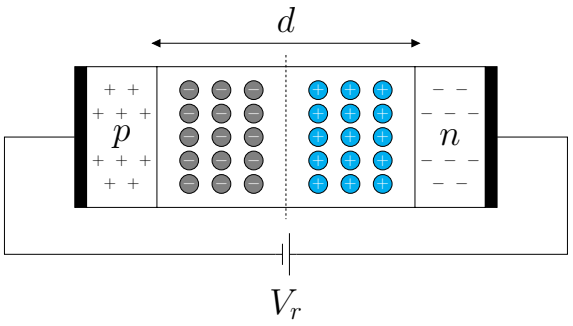


Figure 1.4: *pn* junction cross section when a reverse voltage is applied. The depleted region width d increases with the square root of the voltage applied.

As expressed in equation 1.3, the depth of the depleted region will be proportional to the square root of the substrate resistivity and the voltage applied.

$$d \propto \sqrt{\rho V_r}$$

This leads to a bigger region in which the electron-hole pair generated by the incident radiation drift towards the electrode. Therefore a thicker depletion region leads to a larger signal.

HVCMOS

High-voltage CMOS (HVCMOS) technology was originally designed to be used in the microchips for automotive application [19, 23]. The term high-voltage refers to any voltage that is significantly higher than the supply voltage (typically 1.8 V for 180 nm technology) for a typical CMOS chip [58]. The HV technology allows for low-voltage CMOS transistors to be placed in the same substrate as the HV components. In the case of monolithic

high-energy particle detectors, this allows implementation of pixels with a fill factor closer to 100% since the low voltage electronics, both pmos and nmos transistors, can be placed over the sensor diode [71].

A HVCMOS sensor is a reverse-biased pn junction, the substrate is used as p-region of the diode while the n-region is formed by deep nwell. This pn junction has an asymmetric doping profile. The depth of the depleted region is thicker towards the p side (lightly doped) compared to the n side (heavily doped) [63].

Because the depleted volume is thick (due to high reverse bias voltage) and the charge collection is fast, a HVCMOS sensor can detect not only photons but also ionizing particles if they generate enough number of electron-hole pairs to overcome the detection threshold[1].

High-voltage CMOS sensors

There are two types of radiation sensors, monolithic and hybrid. A hybrid sensor is a device that consists of two separated chips that are bump bonded together. One of them is a thick, high-resistivity silicon substrate that contains the sensing diodes while the other has all the readout electronics. Hybrid sensors are expensive and have usually larger current consumption [83]. One advantage of this approach is that the electronics can be optimized individually to better fit the requirements [13, 63].

A monolithic HV-CMOS sensor is an active pixel sensor implemented in a commercial HV-CMOS process. The sensing element is a diode created by a deep n-well in a p-type substrate. The n-well collects the electrons generated by passing particles. The pixel electronics are placed in the deep n-well. As explained before, the depleted region is increased by applying a reverse high voltage bias [71, 29]. One advantage of this type of sensor is that the costs are reduced compared to hybrid sensors (from about 2M vs. 85k per m^2 [22]).

The HV-CMOS technology has several advantages over standard CMOS process. The floating electronics is embedded inside the deep n-well that isolates the transistors from the p substrate that is biased with high voltage (figure 1.5). Furthermore, the high drift speed of the electron-hole pairs allows for a higher radiation tolerance [83], because the displaced charge can reach the collection electrode before is trapped, or recombined, in the substrate, which would lead to the creation of local voltages that change the behavior of the device or lead to charge loss [46].

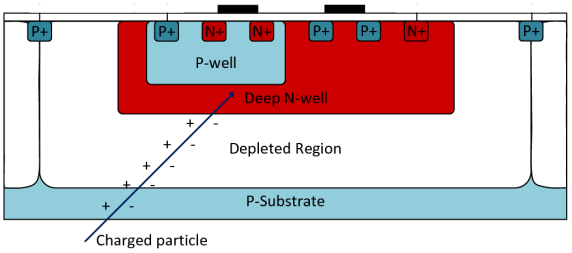


Figure 1.5: HVCMOS cross section(after [43] modified).

The sensors explained in this thesis were fabricated in HV-CMOS technology.

[1] https://adl.ipe.kit.edu/downloads/ThesisHVCMOS.pdf

Types of pixel amplifiers

Two common amplifiers implemented to acquire the charge generated by incident radiation in silicon are, the source follower and charge sensitive amplifier (CSA).

The source follower consists of a single transistor on which the gate is capacitive coupled to the diode sensor [13]. The gain of this transistor is close to the unity, however, it presents a high input impedance and a low output resistance, converting the charge acquired into a voltage and isolating the diode from the large bus capacitance [46, 4]. Figure 1.6 shows a schematic of a 3T (three transistors) pixel readout topology that implements a source follower.

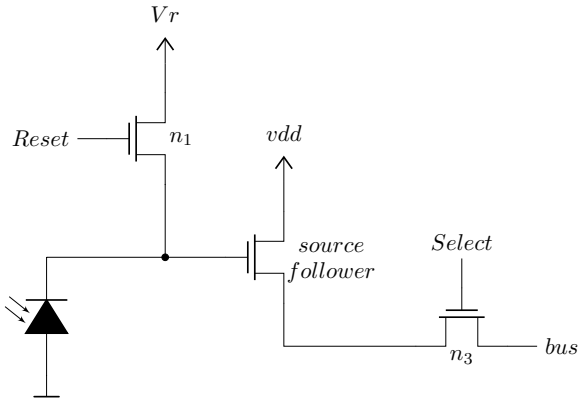


Figure 1.6: Transistor level schematic of a 3T pixel signal readout.

On the other hand, a CSA (figure 1.7) presents a more complex topology. It behaves as an ideal integrator where the charge generated by the particle in the silicon is stored in the feedback capacitor C_f. In the ideal case, the output voltage depends only on the detector charge and the value of C_f [67]. Since this type of readout works by storing the charge in a capacitor, to avoid its saturation, it is needed to provide some kind of discharge path. This can be done by a simple resistor or a switch that shortens C_f.

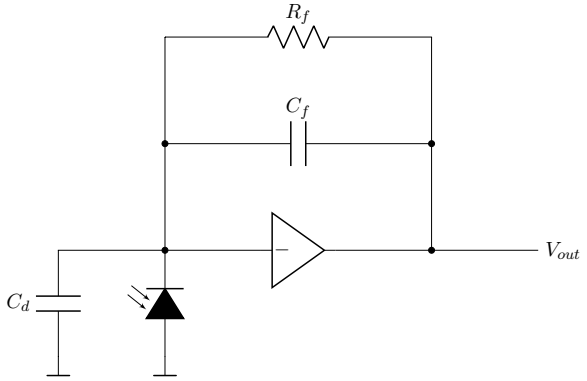


Figure 1.7: Schematic of a charge sensitive amplifier (CSA) with a feedback capacitance C_f in parallel to a discharge path through R_f. C_d corresponds to the sensor capacitance. This topology integrates the charge generated by the diode and converts it into a voltage in the node V_{out}.

Types of pixel readout

Once the charge generated by the particle is amplified, the signal needs to be processed. Two main approaches can be used, an integrating readout and single particle readout.

In order to measure large amount of charge, integrating the charge generated by one or more particles passing through the sensor is used. This approach allows to measure large amounts of charge but does not have the capability to resolve single hits. The energy of the particles can be measured as an equivalent voltage at the output of the integrator. The HINT sensor (chapter 3) developed uses integrating readout with a tweak to increase the resolution of the output from 8-bit to 16-bit.

The single particle readout, on the other hand, works by creating a voltage square pulse with a duration proportional to the charge acquired by the diode sensor. After the charge is converted to a pulse voltage, it passes through a comparator on which the output is a square pulse that lasts until the input voltage gets smaller than the threshold (figure 1.8) [87].

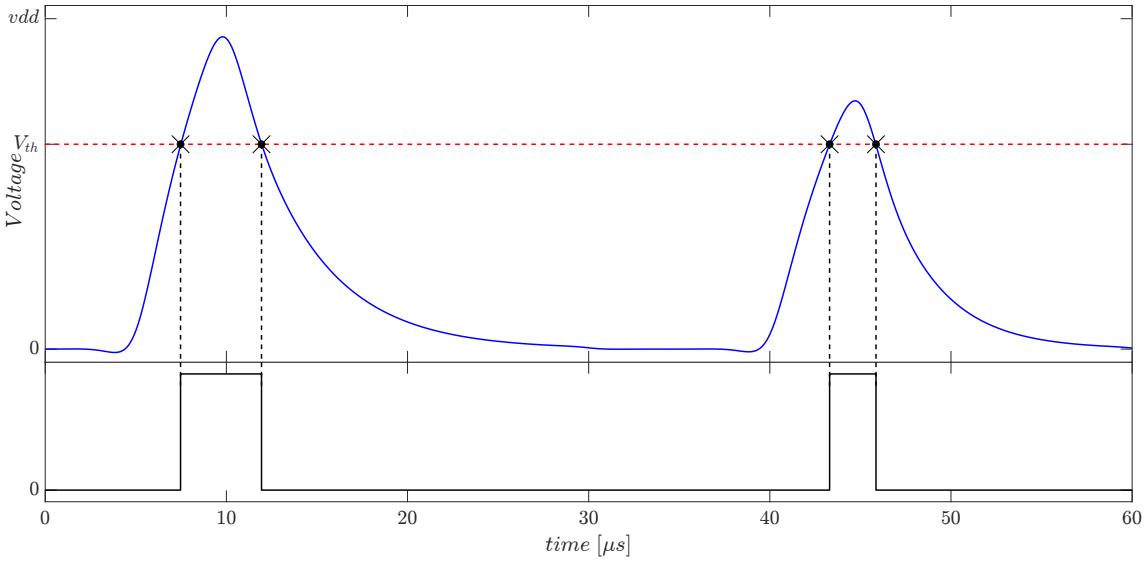


Figure 1.8: Diagram of the output signal pulse (black) when the charge to voltage converter (blue) register a hit. The width of the comparator pulse depends on signal amplitude.

As depicted in figure 1.8, when the voltage pulse (blue curve) is over the voltage threshold (red), the comparator will create a square pulse (black) that will last until the input voltage gets smaller than the threshold. By measuring the time of the comparator output, the amount of charge sensed by the diode can be measured. HPIXEL sensor (chapter 2) utilize this type of method as well as integrating.

2 HPIXEL chip for electron microscopy

Electron microscopy is a technology that allows to create images with a much higher resolution than conventional microscopes (based on light). The limit of the resolution depends on the wavelength of the particle used (photons or electrons), also called Rayleigh criteria [1], and diffraction by the microscope optics (Abbe criteria [33]). In the case of electrons, their energy determines their wavelength. For example, the practical resolution of a transmission electron microscope (TEM) at 100 kV (the acceleration voltage of the electrons, which determines their speed) is ∼500 pm [34].

There are two main methods of electron microscopy, scanning electron microscopy (SEM) and transmission electron microscopy (TEM). Both techniques require a high vacuum, to avoid the electrons to collide with gas particles and thus widen their energy spectrum. The sample is placed inside the vacuum chamber and under the electron beam. The electron beam is created by applying a high voltage to a tungsten filament, and then applying electromagnetic fields to accelerate, focus, and form a narrow beam of high-speed electrons. Then the beam penetrates the sample and depending on the absorption capability of it, more or fewer electrons will pass through the specimen and will reach the image sensor behind. Figure 2.1 shows a schematic of a TEM.

Electron counting imaging technique is mainly used in low-dose applications such as life science microscopy, where high electron flux lead to a quick sample degradation (e.g. protein denaturation). Typical use-cases of an electron counting detector are Cryo-TEM experiments such as single particle analysis which lately have gained much popularity in the life science domain: proteins can now be resolved with resolutions as high as 2 Å, which is also fundamental for drug design, and medical science [89, 36, 18].

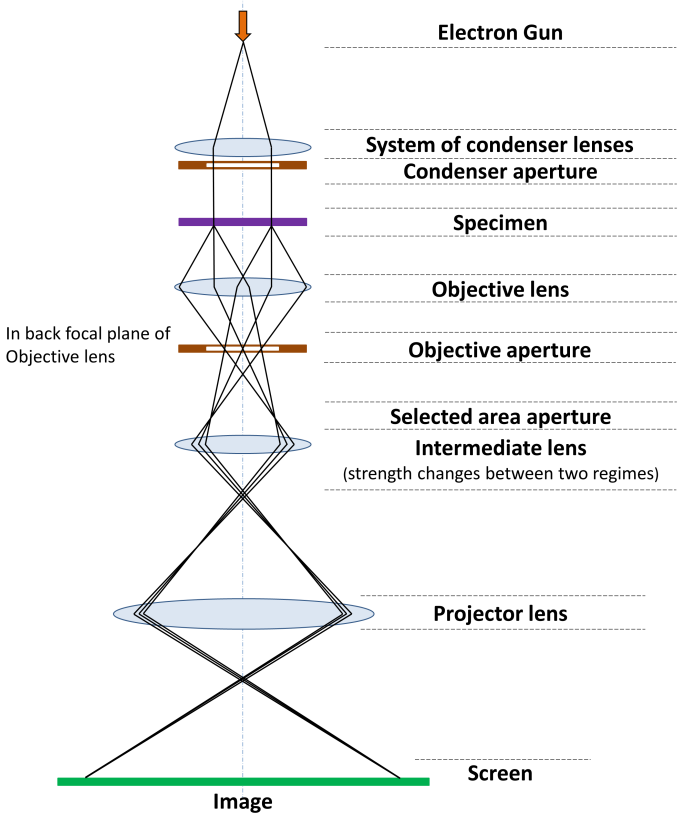


Figure 2.1: Schematic of the main parts that conform a TEM (after [44] modified).

Generally, TEM image sensors for life science consist of a pixel matrix of up to 4k×4k pixels, capable of single-electron detection, and a frame rate of at least 40 frames per second (fps). The total dose that the sensor needs to withstand in its life time is around 20 MRad[1] [26].

The performance of this imaging sensor is very important for taking good quality electron microscope pictures. Because of that, in the last ten years, CMOS monolithic active pixel sensors (MAPS) have become the preferred choice for directly detecting charged particles, particularly electrons, in TEM [17].

The sensor (called HPIXEL) was developed as a demonstrator of HV-CMOS sensor technology, and it was a collaboration with Thermo Fischer Scientific under the "Smart Sensor Technologies and Training for Radiation Enhanced Applications and Measurements" (STREAM) project[2]. All the measurements with electrons (inside the electron microscope) were carried out at Thermo Fischer Scientific facilities in Eindhoven, Netherlands with a TECNAI-F20 TEM.

In this chapter, the whole detector system will be discussed, starting from the sensor itself (sections 2.1 to 2.7). The relevant parts of the FPGA firmware and software designed to control and read out the chip are also discussed. Finally, in section 2.8, all the measurements carried out to validate the sensor will be presented. This includes calibration and testing measurements as well as results under an electron beam in an electron microscope.

[1] `https://ec.europa.eu/research/participants/documents/downloadPublic?documentIds=080166e5bd5073d4&appId=PPGMS`

[2] Smart Sensor Technologies and Training for Radiation Enhanced Applications and Measurements (STREAM) have received funding from the "European Union's Horizon 2020 Research and Innovation Programme" under the Grant Agreement No 675587

2.1 Architecture

The first prototype of the sensor was built with a matrix of 64×64 pixels with a square pixel of 25 µm length per side. Two different types of charge measure electronics inside the pixel were developed (figure 2.7). The first type, called current pixels because they integrate the current generated by the radiation, is the more complex and covers the first 48 rows of the matrix, and has the ability to use correlated double sampling mode (CDS) [80]. The second flavor pixels are called voltage pixels, because they amplify the voltage created by the radiation, and correspond to all the pixels from columns 49 to 64. The chip is controlled with an FPGA that acts as an intermediary between the PC, where the data measured is received and analyzed, and the sensor (figure 2.2).

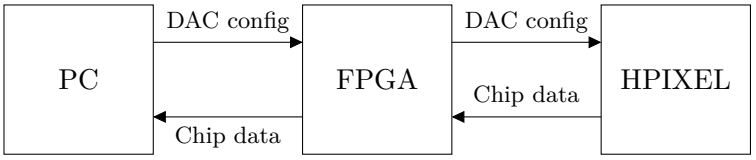


Figure 2.2: Data flow schematic for the whole setup of HPIXEL.

The HPIXEL has a total area of 2.2 mm × 2.5 mm, with a matrix area of 1.6 mm × 1.6 mm. The sensor was fabricated on a multi-project wafer, with the chip cluster (reticle) shown in figure 2.3. It was developed in 180 nm HV-CMOS technology, capable of handling up to 120 V.

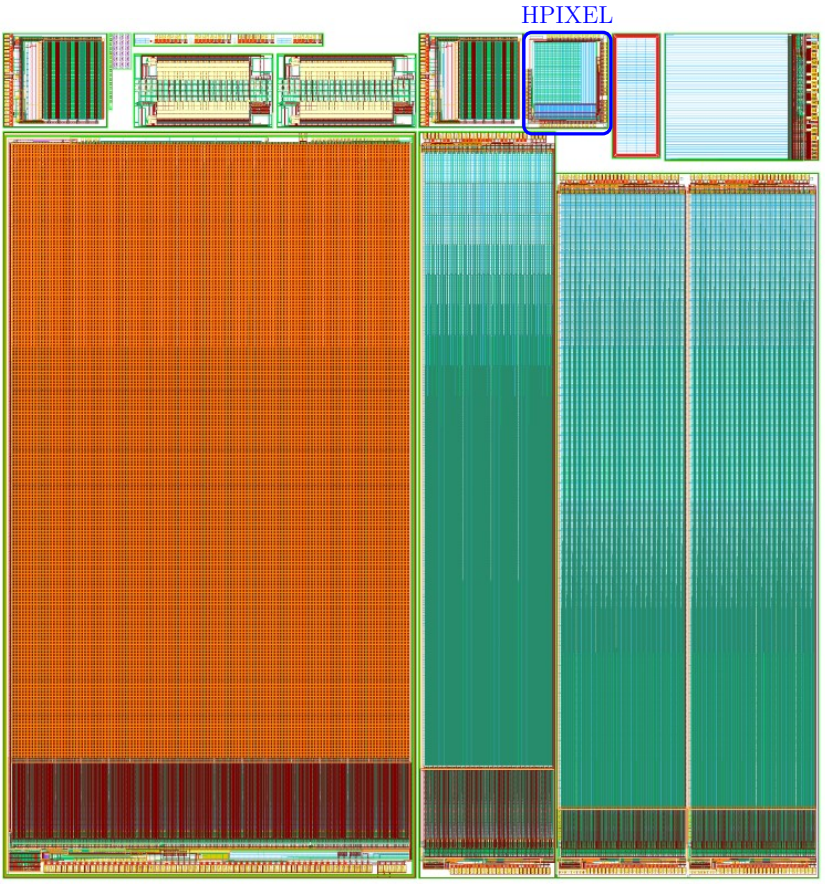


Figure 2.3: Layout of the reticle with the HPIXEL sensor position highlighted in blue.

Table 2.1 gives an overview of the main parts of the HPIXEL sensor.

Table 2.1: Main blocks of the HPIXEL sensor.

Part	Description
Pixel Matrix	64×64 pixels that form the active sensing area
64 row control blocks	Each of them controls one row of 64 pixels
Signal shaping	Controls and generates necessary signals for the correct timing of the sensor
128 amplifiers (amp-ADC)	Each of them are connected to 32 pixels. The block contains a difference-amplifier and an Analog to Digital Converter (ADC)
Bias block	Contains current-mode DACs with attached bias diodes. The DAC setting is stored locally and written by PC
8 Low-Voltage Differential Signaling (LVDS) outputs	Converts each of the 8-bit data output into 8 LVDS signals for noise reduction

The layout of the sensor is shown in figure 2.4. Input-output (IO) pads are placed at the chip edges. Each of the 64 row control-blocks (placed to the left of the matrix) controls a single row of pixels, while the 128 amp-ADC placed below the matrix.

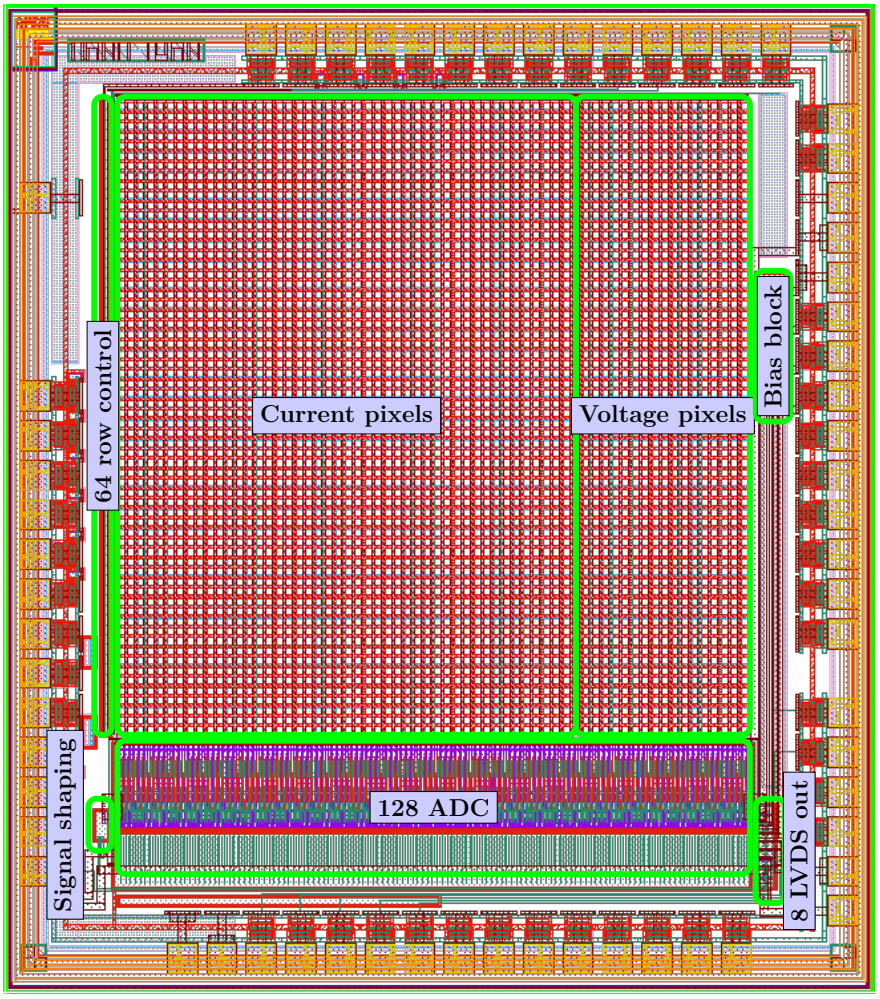


Figure 2.4: Layout of HPIXEL sensor with the main parts highlighted in green boxes.

Since there are twice the amount of ADCs compared to columns, the matrix is actually routed as if it were a 32 rows and 128 columns (rectangle shape), each of them connected to one of the 128 amp-ADC blocks (figure 2.5). The upper 32 pixels are connected to one ADC and the lower 32 pixels to the next one, increasing the speed of the sensor by a factor of two. This will be explained in section 2.3.

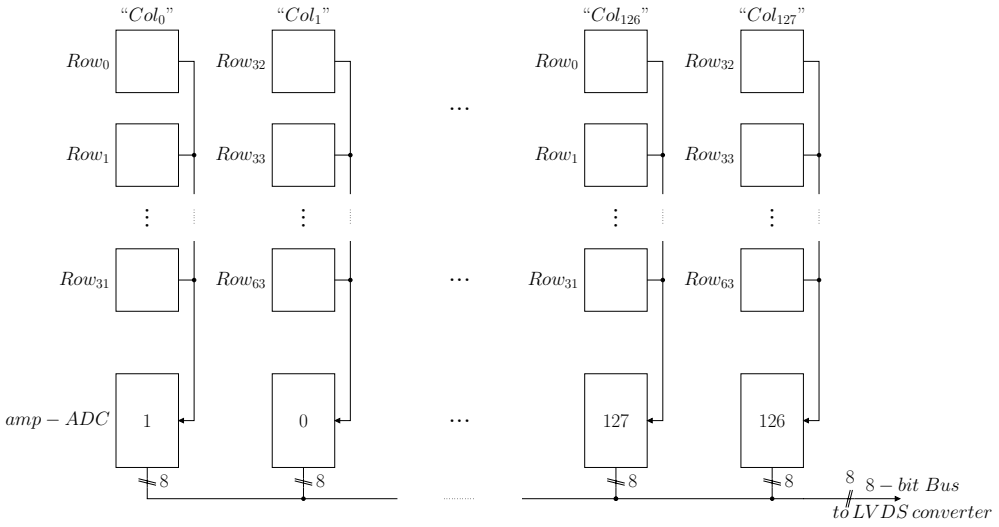


Figure 2.5: Schematic of the pixel matrix representing the routing of columns to amp-ADC blocks.

The bias block generates the necessary voltages and currents, for biasing of the analog circuits in pixels and in periphery. The 6-bit DAC values are stored locally and written from the PC. The signal shaping block generates signals for controlling of the matrix. In section 2.3 an explanation will be presented.

All the signals used in the pixels to turn on and off the different switches are generated by the row control block. This block will be discussed in section 2.3.2. The output of each pixel is sent to the amp-ADC block (explained in section 2.3.3). The amp-ADC block contains the variable gain amplifier. Signal shaping block controls the ADC (section 2.3.4). The digital output of the ADC is serialized and sent out of the chip by LVDS pads.

All of the blocks present in the sensor have several variable current sources and voltages that can be adjusted by setting a series of 6-bit DACs via the FPGA. The bias block (explained in section 2.3.1) generates the corresponding currents and voltages. Figure 2.6 shows the block diagram of the full sensor as explained above.

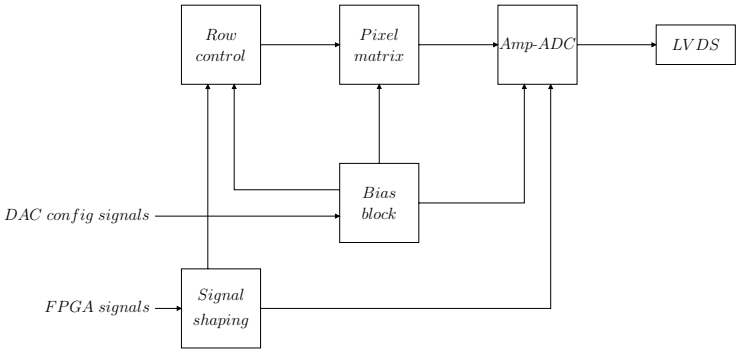
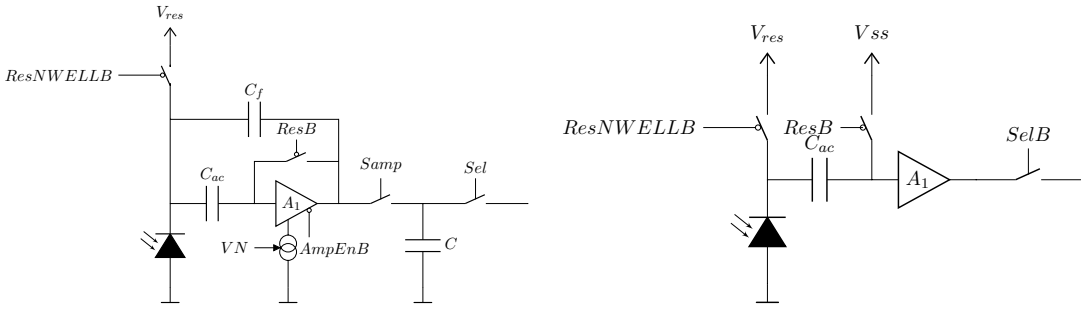


Figure 2.6: Block diagram of the HPIXEL sensor blocks and how they interconnect each other.

The sensor readout works as rolling shutter [47]. The principle of this method is to read out the data of each pixel at a time in a serpent pattern that starts at the top left corner of the matrix and goes to the top right corner, then continues with the row below, again starting from left to right.

2.2 The pixel

There are two different pixel flavors in the matrix, they are called current and voltage pixels. In this way we can test both topologies to verify which pixel is better suitable for electron detection. The schematic of both sensor type is shown in figure 2.7.



(a) Current pixel schematic. (b) Voltage pixel schematic.

Figure 2.7: Schematic of both pixel flavors, current pixels (a) and voltage pixels (b).

The main difference between both types of pixels is that the current pixels can take advantage of a CDS mechanism due to the extra electronics (capacitor C and *Sel* switch) and posses a higher gain compared to voltage pixels.

2.2.1 Current pixel

The current pixels have more complex design than the voltage pixel, has the possibility to work in CDS mode, and has a bigger gain. This pixel consists of a inversely biased photodiode, the capacitor for ac-coupling C_{ac}, a charge sensitive amplifier with adjustable bias current through VN voltage and a feedback capacitance C_f, a storage capacitor C and a series of switches (figure 2.7 (a)).

The layout of the current pixel is shown in figure 2.8, the pixel electronics are placed inside the charge collecting n-well. The transistor-level schematic of the pixel is presented in figure 2.9.

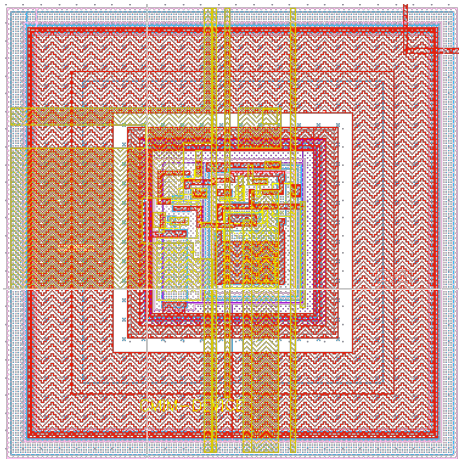


Figure 2.8: Layout of the current pixel type developed, the center square contains the electronics.

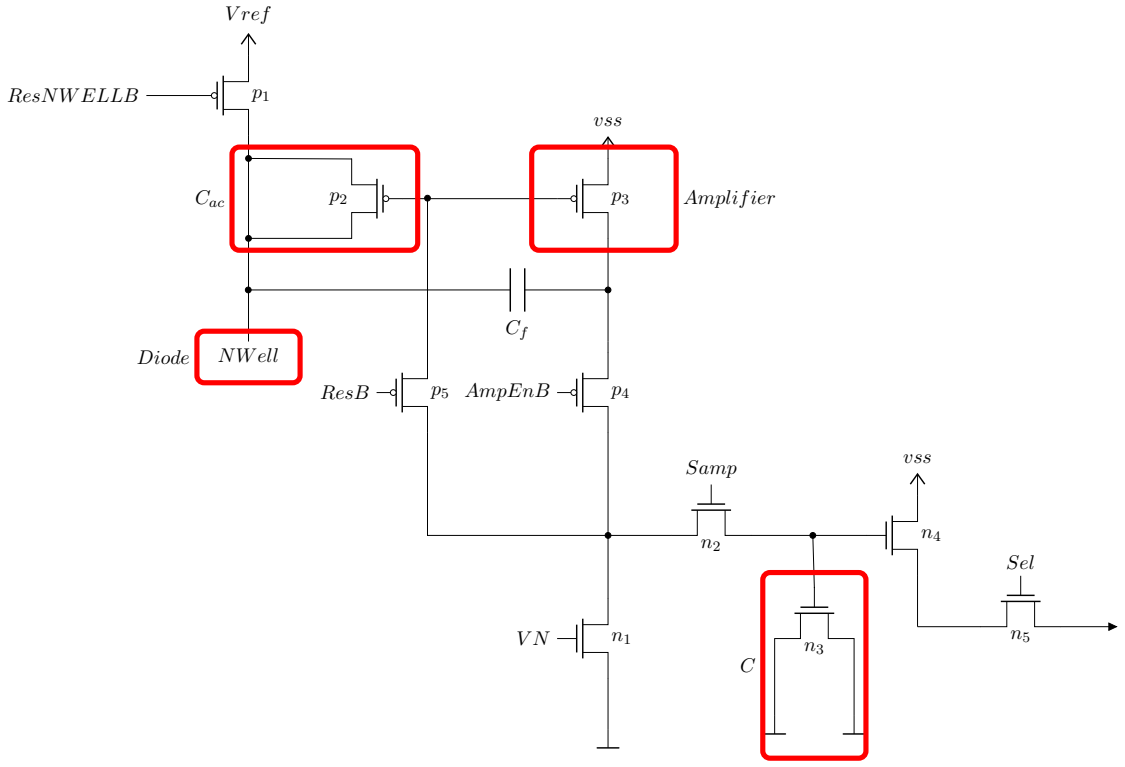


Figure 2.9: Transistor level schematic of the current pixel implemented in HPIXEL sensor.

The gain of the current amplifier can be expressed as [69]:

$$A = \frac{V_{out}}{Q_{in}} = -\frac{1}{C_f} * \frac{g_m R_S \frac{C_f}{C_{gs}+C_{gd}+C_f+C_D}}{1 + g_m R_S \frac{C_f}{C_{gs}+C_{gd}+C_f+C_D}} \tag{2.1}$$

where

C_f : feedback capacitance, equal to the parasitic capacitance bulk-drain
g_m : transconductance of the transistor
R_S : impedance at the source
C_{gs} : parasitic capacitance gate-source
C_{gd} : parasitic capacitance gate-drain
C_D : capacitance of the diode

Assuming $g_m R_S >> 1$ the gain of the charge sensitive amplifier is determined only by the feedback capacitance:

$$A = \frac{V_{out}}{Q_{in}} = -\frac{1}{C_f} \tag{2.2}$$

Simulations with Cadence ADL L tool gives a feedback capacitance of ∼2 fF.

The functioning of the current pixel has four phases, controlled by the signals sent by the FPGA:

1. During the first phase (figure 2.10) switches *ResNWELLB*, *ResB*, and *Samp* are closed. By doing this, the dc-feedback from the amplifier output to its input is activated and the reset voltage is stored in capacitor C. This phase is marked with green in figure 2.14.

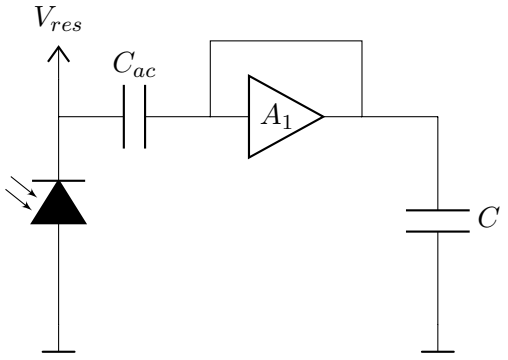


Figure 2.10: Current pixel phase 1. C stores the reset voltage.

2. In the second phase (figure 2.11) all switches are open and the photodiode collects the signal charge. During this time the amplifier is disabled. This phase is marked with yellow in figure 2.14.

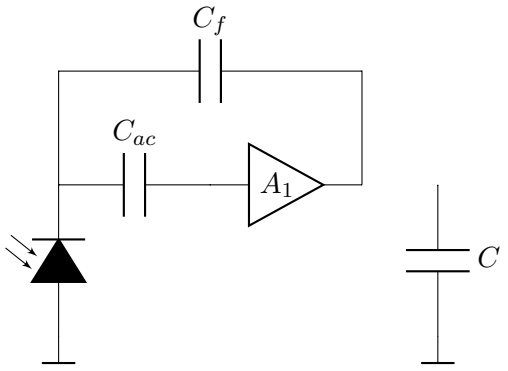


Figure 2.11: Current pixel phase 2. The charge generated by radiation flows into feedback capacitance, the voltage across C_f is proportional to the integral of the charge.

3. In the third phase, figure 2.12, the switch *Sel* is closed, allowing the reset voltage stored in the capacitor C to be read out by the amplifier placed at the periphery. This phase is marked with blue in figure 2.14.

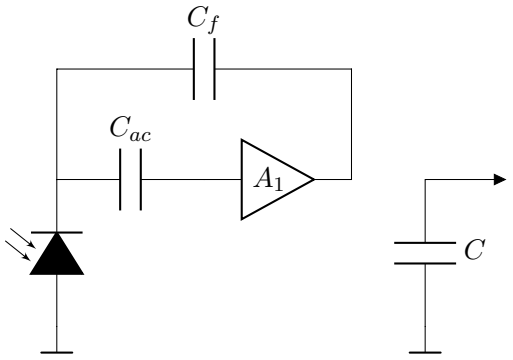


Figure 2.12: Current pixel phase 3. The reset voltage in C is sent to the amplifier placed at the periphery.

4. Finally, in the fourth phase (figure 2.13) the switches *Samp* and *Sel* are closed, and the charge sensitive amplifier is enabled, allowing the amplified voltage to be read out. This phase is marked with red in figure 2.14.

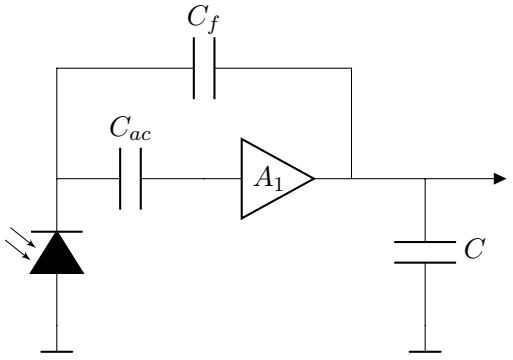


Figure 2.13: Current pixel phase 4. The amplifier is enabled, the input signal amplified and the output voltage is read out.

It is possible to adjust the current source *VN* of the amplifier, in order to control the current consumption of the amplifier A_1.

A timing diagram of the signals used for the control of the different phases is shown in figure 2.14. The time axis is expressed as a value of the counter *SmallCnt* (which has a frequency of 12.5 MHz). This counter is the reference to generate all the necessary signals in the FPGA and will be explained in detail in section 2.6. Unless explicitly expressed, the time axis will be expressed as a number of *SmallCnt*.

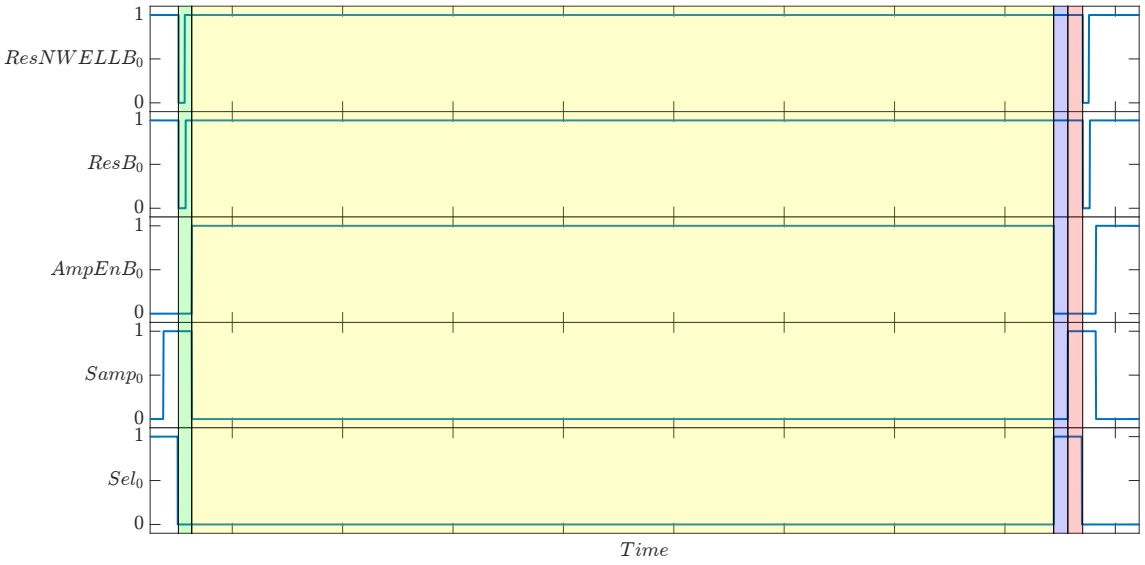


Figure 2.14: Timing diagram of the signals used to control the measurement flow in the current pixel type of HPIXEL. Phase 1 is highlighted in green, yellow corresponds to phase 2, blue to phase 3, and red is phase 4.

2.2.2 Voltage pixel

The second flavor is the voltage pixel. It is simpler than the current pixel. The voltage pixel consist of a photodiode, a signal coupling capacitor C_{ac}, a source follower transistor as amplifier, and several switches (figure 2.7 (b)).

The layout of the voltage pixel is shown in figure 2.15, the pixel electronics are also placed inside the charge collection electrode. The transistor level schematic of the pixel is shown in figure 2.16.

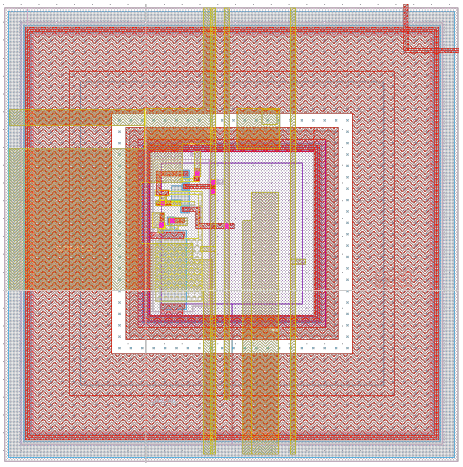


Figure 2.15: Layout of the voltage pixel.

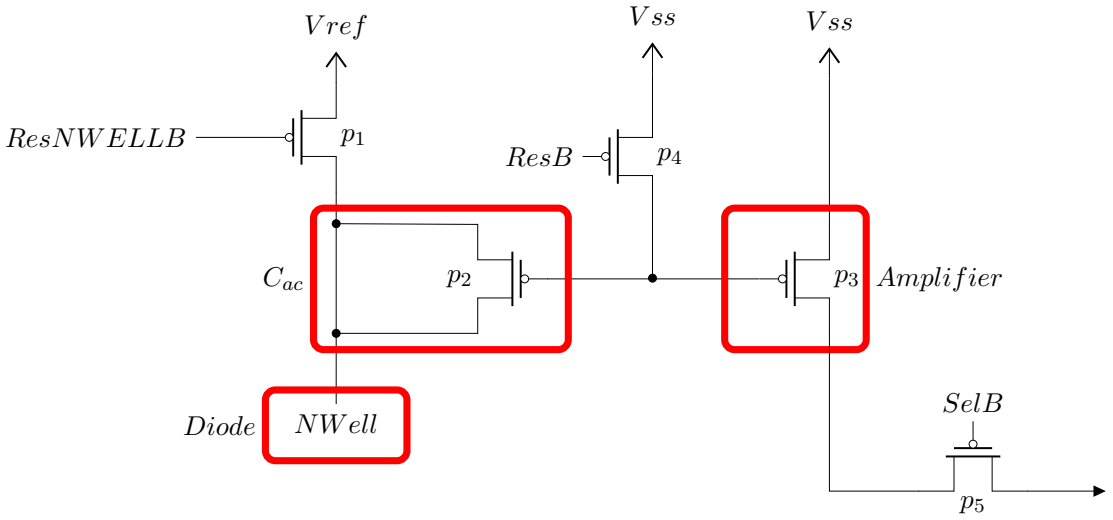


Figure 2.16: Transistor level schematic of the voltage pixel implemented in HPIXEL sensor.

The gain of the amplifier is roughly equal to 1 since it is made up of a single common-drain transistor (also known as a source-follower) [14]. The gain can be expressed as follows [4]:

$$A = \frac{V_0}{V_i} = \frac{g_m R_S}{1 + g_m R_S} \tag{2.3}$$

Where

g_m : transconductance of the transistor
R_S : impedance load connected to source

Assuming $g_m R_S >> 1$ the gain of the charge sensitive amplifier is close to unity.

The functioning of this design can be divided in three phases, controlled by the signals sent by the FPGA:

1. In the first phase, figure 2.17, the switches *ResNWELLB*, *ResB* and *SelB* are closed. In this way, the sensor and the amplifier input are re-set to defined voltages. The amplifier output is read out. This phase is marked in green in figure 2.20.

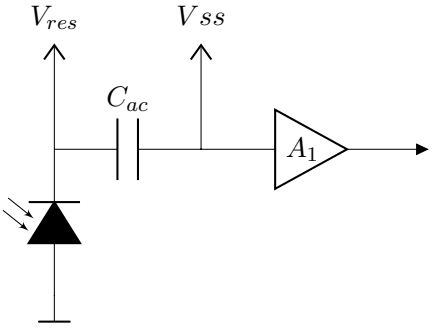


Figure 2.17: Voltage pixel phase 1. The sensor and the amplifier input are re-set to defined voltages. The amplifier output is read out.

2. In the second phase, figure 2.18, the switches *SelB*, *ResNWELLB* and *Res* are opened and the photodiode starts to accumulate the charge generated by radiation. This phase is marked in yellow in figure 2.20.

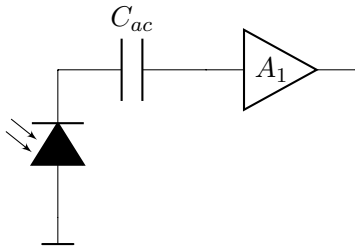


Figure 2.18: Voltage pixel phase 2. Photodiode accumulates the charge generated by radiation.

3. Finally, in the third phase (figure 2.19) the switch *SelB* will be closed. The amplified signal will be read out. This phase is marked in blue in figure 2.20.

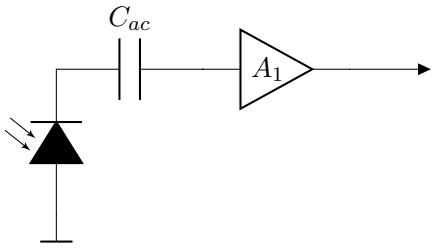


Figure 2.19: Voltage pixel phase 3. The amplified signal is read out.

A time diagram of the signals used for the control is shown in figure 2.20. The time axis is expressed as a value of the counter *SmallCnt*.

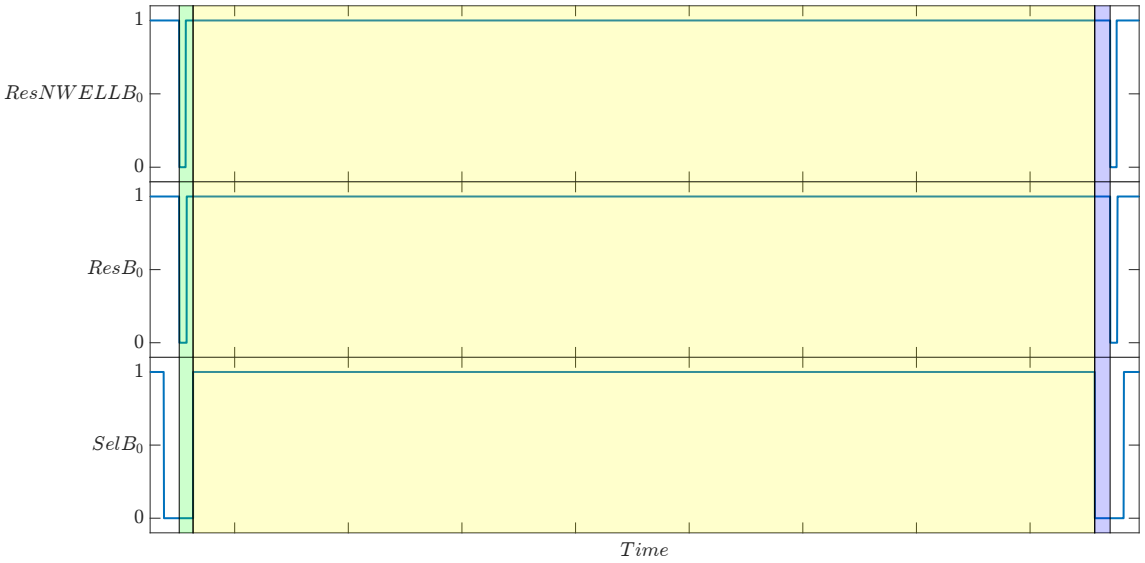


Figure 2.20: Timing diagram of the signals used to control the measurement flow in the voltage pixel type of HPIXEL. Phase 1 is highlighted in green, yellow corresponds to phase 2, and blue is phase 3.

2.3 Periphery electronics

The periphery electronics of the sensor consists of the following components:

- Bias block

- Signal shaping block
- 64 Row control blocks
- 128 amp-ADC blocks

Since the sensor readout works as a rolling shutter [47], each pixel needs to be timed to enable it at a precise moment. For that purpose, each row will have a dedicated row control clock that generates the necessary signals for each pixel. The timing of the signals will be provided by the signal shaping block which receives the main signals from the FPGA (section 2.6).

The pixel signals are amplified and digitized by the ADCs placed at the bottom of the column. The ADC output code is stored into a parallel-in/serial-out 8-bit wide shift register. Then, the 8-bit output is converted from CMOS to LVDS and transmitted off chip. The timing of the signals used in this block is also controlled by the signal shaping block.

2.3.1 Bias-block

The bias block is generating the bias voltages for current sources in pixel amplifiers, end of column amplifiers, ADCs and other circuits. The voltages are generated using current mode DACs, the output currents are converted to voltages using diode connected transistors. The DAC settings are stored in a shift register that can be written via FPGA. Figure 2.21 shows the schematic of this block.

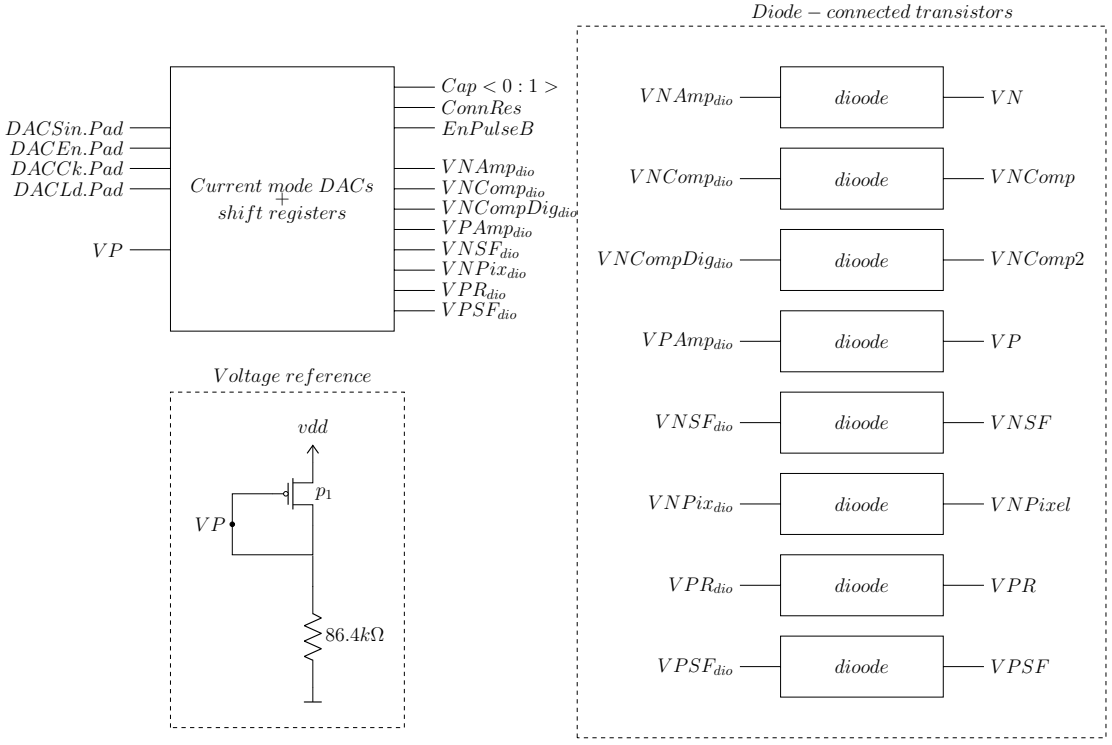


Figure 2.21: Top level schematic of the parts that form the bias-block of HPIXEL.

This block consists of three main parts:

- Current-mode DAC and shift registers
- Reference voltage generator
- Diode connected transistors

The digital serial data is sorted in the shift register. Current-mode DACs convert each 6-bit value into a current. The currents are converted to voltage using diode connected transistors. Equation 2.4 shows the formula for the output current which is in the range from 0 to 13.3 µA. In figure 2.22 the transistor level schematic of the 6-bit DAC is shown.

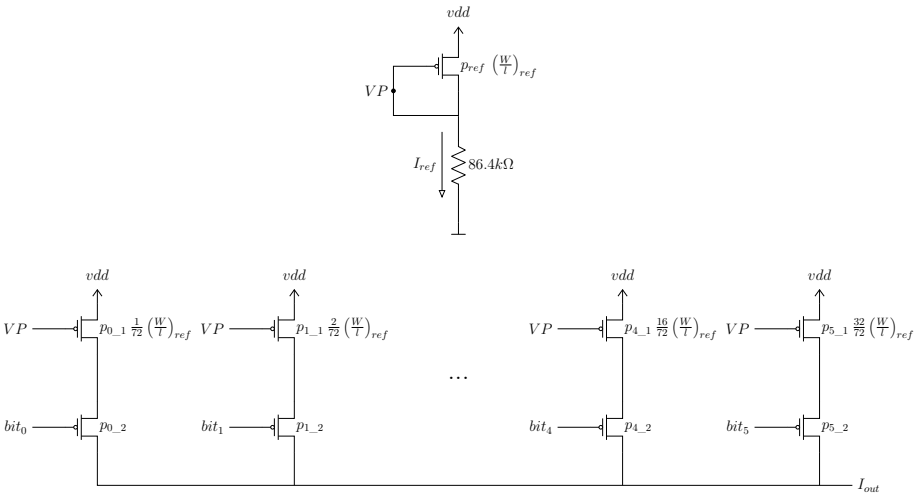


Figure 2.22: Transistor level schematic of the 6-bit DAC of the bias block of HPIXEL.

$$I_{out} = \frac{I_{ref}}{72} * \sum_{n=0}^{5} bit_n * 2^n \tag{2.4}$$

There are several bias voltages that are generated by the bias block.

- *VP* current for the load transistor in the amplifier of the amp-ADC block
- *VN* bias current for the amplifier in the amp-ADC block
- *VPR* changes the slope of the ramp that discharges the capacitor at the input of the comparator in the amp-ADC block
- *VPSF* controls the current that flows through the p-type source follower in the pixel
- *VNSF* controls the current that flows through the n-type source follower in the pixel
- *VNComp* controls the current for the comparator in the amp-ADC block
- *VNComp2* controls the current for the amplifier placed after the comparator in the amp-ADC block
- *VNPixel* controls the bias current for the amplifier in the current pixel

The digital control bits are:

- *EnPulseB* active high control bit signal that enables the NWELL reset voltage
- *Cap< 0:1 >* 2-bits that change the amplification (between three discrete values) of the amplifier in the amp-ADC block

The bias block is configured via a shift register. Its input signals are:

- *DAC Ck* clock
- *DAC Sin* serial input signal
- *DAC Ld* will load the data into the latch
- *DAC En* enables the outputs

For illustration, a diagram of the digital signals to configure the bias block is shown in figure 2.23.

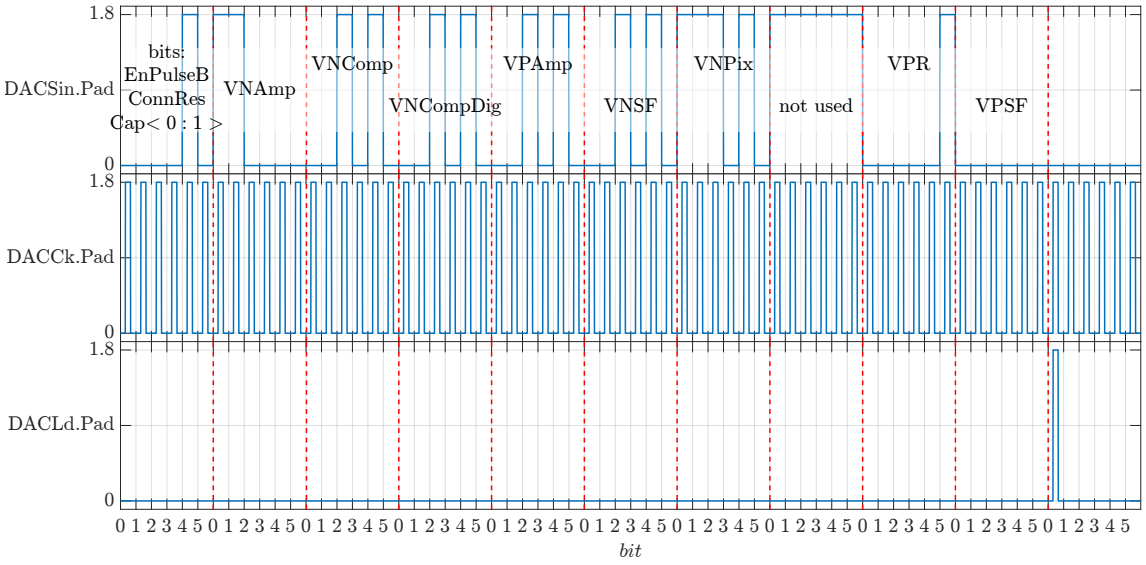


Figure 2.23: Diagram of DAC signals used to configure the currents in the bias block of HPIXEL. In the x-axis the bit number is represented, every 6 bits the counter resets since the currents are 6-bit wide.

In figure 2.23 the value of *DACSin.Pad*, *DACCk.Pad*, and *DACLd.Pad* is plotted. As shown, the packages of 6-bit each are sent sequentially through *DACSin.Pad*. A shift register receives the data and the outputs of the shift register are connected to another parallel-in register. The outputs of the parallel-in register are then connected to bias DACs. The signal *DACLd.Pad* will trigger the load of the digital data into the registers.

2.3.2 Row control

The row control is a chain of 64 row control blocks connected like a shift register. Each block generates the signals necessary to perform the readout of each row. The layout of the row control designed is presented in figure 2.24, a schematic of the interconnection of all the blocks is shown in figure 2.26, and a schematic of one block is shown in figure 2.25.

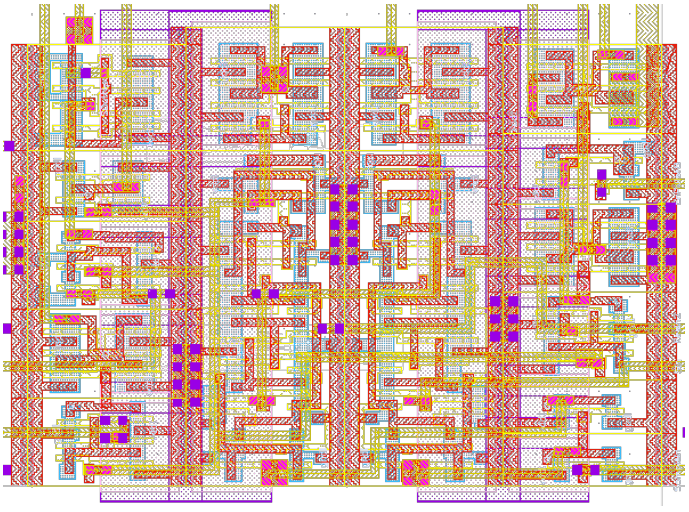


Figure 2.24: Row control layout designed for HPIXEL.

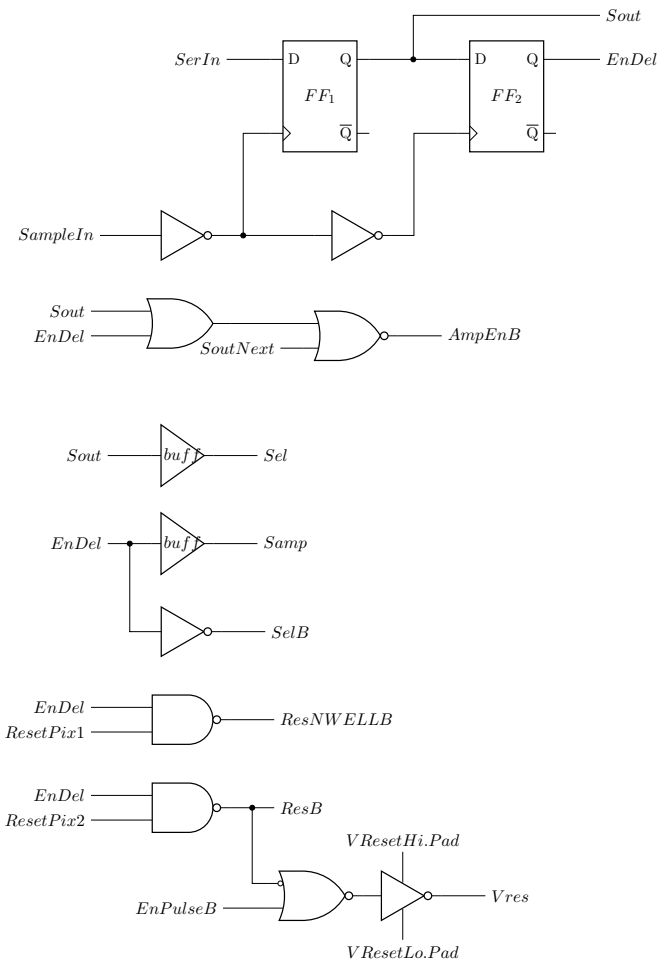


Figure 2.25: Row control schematic designed for HPIXEL.

The inputs and outputs of the row control are:

- *SerIn* is the *Sout* signal of the previous block in the chain. The interconnection is shown in figure 2.26. The first block has *Shift* as *SerIn* input, which starts the sequence of the row controls.
- *SoutNext* is the *Sout* signal of the next block in the chain. The interconnection is shown in figure 2.26
- Input signals coming through IO-pads
  - *VResetHi.Pad* is the positive reset voltage of the diode
  - *VResetLo.Pad* is the negative reset voltage of the diode
- Input signals coming from the signal shaping block
  - *ResetPix1* is used to create *ResNWELLB* to be used in the pixels
  - *ResetPix2* is used to create *ResB* to be used in the pixels
  - *SamplePix* is used to create *Samp* to be used in the current pixels
  - *Shift* is used to create *Sel* and *SelB* to be used in the current and voltage pixels
- Output signals, used to control the pixels were shown in figure 2.14
  - *AmpEnB* enables the amplifier for current pixels
  - *ResB* resets the amplifier of the pixels
  - *ResNWELLB* sets the voltage of the NWELL of the pixels to a known voltage
  - *Samp* controls the switch that connects the amplifier output to the storage capacitor C of the current pixels

  - *Sel* controls the switch that connects the storage capacitor of current pixels with the amp-ADC block through a source follower transistor (n_4 in figure 2.9)
  - *SelB* controls the switch that connects the amplifier output of voltage pixels with the amp-ADC block
  - *VRes* is the voltage to which the pixel diode is reset
  - *Sout* is the shift register signal of the block
- *EnPulseB* is a digital bit coming from the bias block to enable *VRes* (voltage to which the diode sensor will be reset) for the use of pulse reset mode.

To synchronize each row control block, the *Sout* signal of the *n+1* block is connected to the *SoutNext* input of the previous one (*n* block), while the last block (the 64$^{\text{th}}$) is connected to *vdd* as shown in figure 2.26.

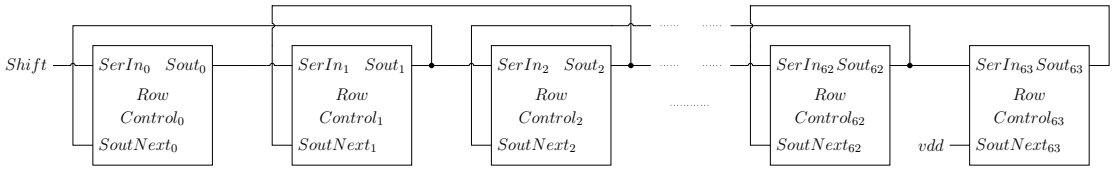


Figure 2.26: Row control blocks schematic interconnected to address each row at the precise moment.

To better understand the functioning of the blocks together as well as the input and output signals, figure 2.27 shows a timing scheme of the signals *SerIn*, *SoutNext*, and *Sout* for the first three row control blocks.

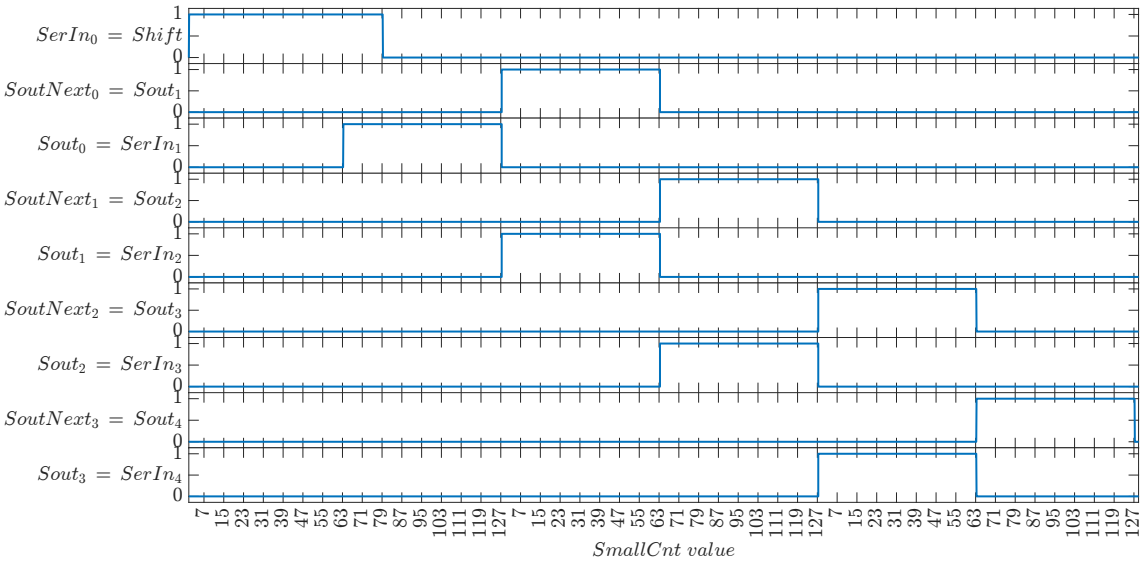


Figure 2.27: Relevant signals generated for row control block to synchronize each row. The x-axis corresponds to the value of the 7-bit counter *Smallcnt*, clocked with 12.5 MHz clock.

The $SoutNext_{n+1}$ input signal is used to enable the output $AmpEnB_n$. When $SoutNext_{n+1}$ is high ("1") $AmpEnB_n$ (active low) will be "0" regardless the value of $Sout_n$ and $EnDel_n$ (figure 2.25). However, as soon as $SoutNext_{n+1}$ becomes "0" $AmpEnB_n$ will be enabled to change. Since $SoutNext_n$ is the $Sout_{n+1}$, a sequential signal will be generated for each *AmpEnB* which will be responsible for the timing of the rolling shutter (figure 2.28). To increase the speed of the system, there is an overlapping time on which

two amplifiers are enabled. While one pixel is storing the voltage reset, the pixel in the next row is sending the signal stored in the capacitor to the amp-ADC block (figure 2.29).

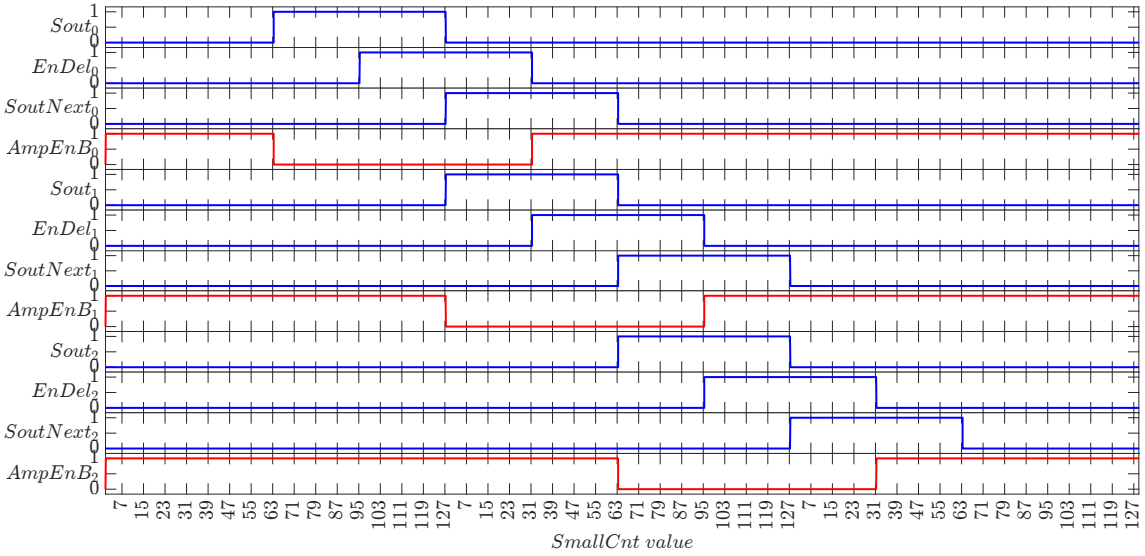


Figure 2.28: Example signals of the three first row control blocks that generate the *AmpEnB* sequence. The x-axis corresponds to the value of the 7-bit counter *Smallcnt*.

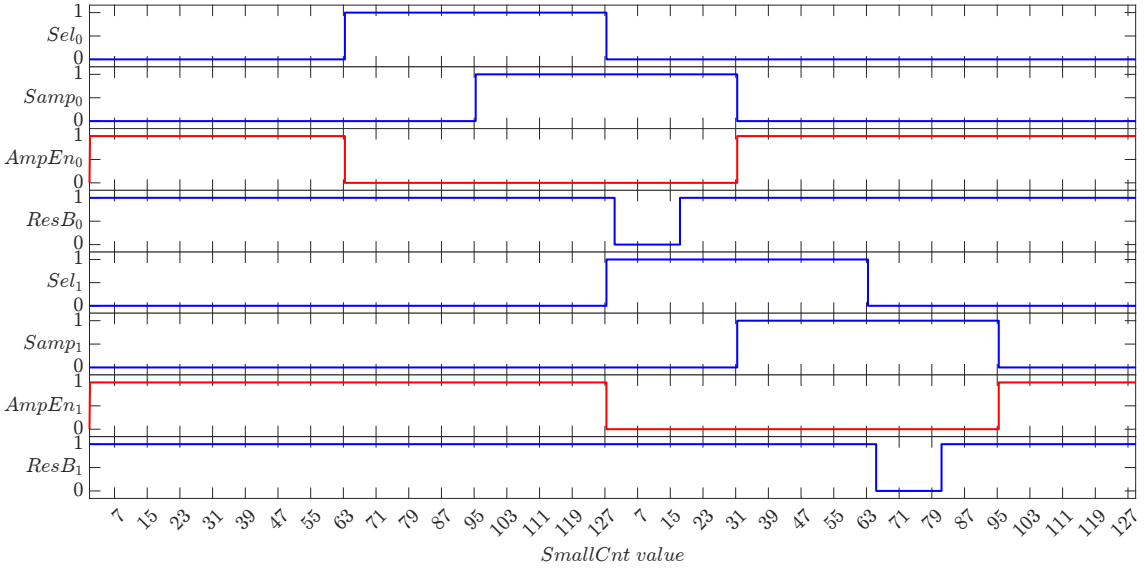


Figure 2.29: Example of the first two row control blocks that generate the signals used by the pixels. The x-axis corresponds to the value of the 7-bit counter *Smallcnt*.

2.3.3 Amplifier and ADC block

The amplifier block design consists of several components that give the sensor the ability to do CDS, as well as to increase the speed of readout and conversion. There are 128 amp-ADC blocks, and 64 columns of pixels because every 32 pixels of each column is connected to one amp-ADC block, to increase the speed of the system by a factor of two compared to a topology of one amp-ADC block for each column. The circuitry, consisting of the switches *Toggle*, and *ToggleB* and the capacitors C_1, and C_2, between the amplifier and the comparator also increases the speed by a factor of two compared to a topology in which the amplifier is directly connected to the comparator. This is further explained in this section. Figure 2.30 shows the schematic of the block.

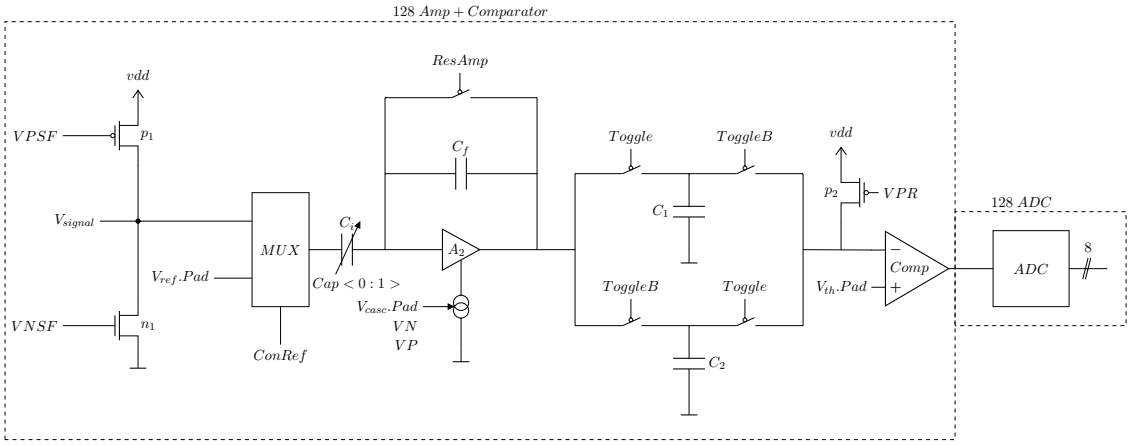


Figure 2.30: Schematic of the amp-ADC block of HPIXEL.

A list of the main components of the block is shown:

- p_1 and n_1 transistors that produce the bias currents for the source follower placed in the pixel
- MUX to multiplex, between $V_{ref}.Pad$ and voltage coming from the pixels
- Amplifier A_2 with capacitors C_i and C_f to amplify the signal
- Two capacitors to store the output signal
- Comparator
- 8-bit counter

The output signal of the pixels are connected to the current source transistors (figure 2.31), which adjust the current of the source follower placed in the pixels. Since current and voltage pixels have different current source transistor types (n-type for current pixels and p-type for voltage), it is necessary to turn on and off the corresponding n or p-type current source when using each pixel flavor.

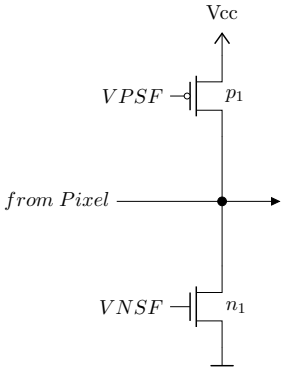


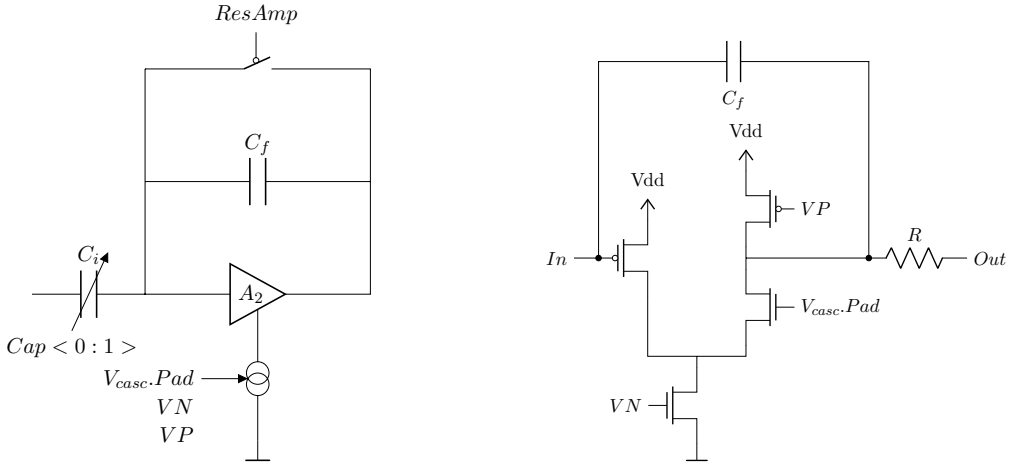
Figure 2.31: Current sources used to bias the source followers in the pixels.

At the beginning, the signal enters a multiplexer, controlled by *ConRef*, a signal sent by the signal shaping block. This multiplexer allows the system to work on two different modes:

CDS mode The multiplexer always connects the output signal that comes from the pixel to the amplifier stage after ($ConRef = 0$)

Single sampling mode The multiplexer will switch between the two inputs, sending to the amplifier first the voltage reference and then the signal that comes from the pixel ($ConRef = 1$ / 0)

The signal output of the multiplexer enters a variable gain amplifier (figure 2.32). The amplification factor can be changed setting C_i to three values via software. By adjusting the values of VN, VP, and $V_{casc}.Pad$ it is possible to change the current consumption of the amplifier, making it faster or slower. The values of VN and VP can be modified via software, while the voltage $V_{casc}.Pad$ is adjusted with a potentiometer on the interface PCB (printed circuit board).



(a) Schematic of the variable gain amplifier in the amp-ADC block of HPIXEL.

(b) Transistor level schematic of the variable gain amplifier in the amp-ADC block of HPIXEL.

Figure 2.32: Schematic of the variable gain amplifier in the amp-ADC block of HPIXEL.

The difference amplifier is implemented a switch capacitor. In reset state, the output and input of the amplifier are shorted and the output has initial potential V_{dc}. In the amplification state, the reset switch is opened and the output voltage follows the change of the input voltage with the negative gain $-C_i/C_f$. Depending on operation mode, the input voltage difference is:

- CDS mode: $V_{signal+reset} - V_{reset}$
- Single sampling mode: $V_{signal+reset} - V_{ref}$

The output voltage can be expressed with the following formula (2.5):

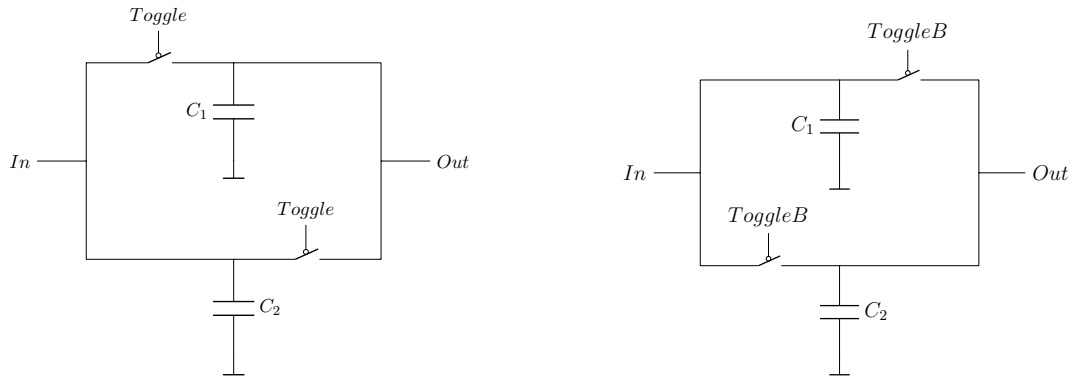
$$V_0 = (V_{signal+reset} - V)\frac{C_i}{C_f} \quad \Rightarrow \quad A = \frac{C_i}{C_f} \tag{2.5}$$

Since C_i can have three values (∼300 fF, ∼600 fF, or ∼900 fF, determined by the process) and C_f is equal to ∼100 fF, the different gains (A) are: 3, 6, or 9.

CDS is done by properly synchronizing the switch *ResAmp* and the switch *Sel* inside each pixel. During the time that the pixel sends the reset voltage, *ResAmp* is closed. In reset sate, the output and input are shorted and have initial potential V_{dc}. C_i is charged to the voltage $V_{reset} - V_{dc}$. After reset, the signal acquired by the pixel is sent to the amplifier (by closing the switch *Sel* on figure 2.32 (a)). Voltage across C_i will now change to $V_{reset+signal} - V_{dc}$. The voltage change on C_i is therefore $V_{reset+signal} - V_{reset}$. This change produces a voltage $-C_i/C_f\,(V_{reset+signal} - V_{reset})$ at the amplifier output.

In case the CDS mode is off, the voltage that is subtracted will be $V_{ref}.Pad$, a reference value that can be set by a variable resistor placed on the interface PCB. This mode is used for debug purpose or when the DC level difference between V_{reset} and V_{signal} is large.

The output of the amplifier is connected to a circuit that contains two capacitors (C_1 and C_1, both of 368 fF) and four switches. The idea is to double the speed, by storing the signal in one capacitor, while the other, which has stored the previous signal value, is connected to a comparator. In figure 2.33 both states of the circuit are shown.



(a) State in which C_1 is connected to the comparator input while C_2 is being charged by the amplifier output.

(b) State in which C_2 is connected to the comparator input while C_1 is being charged by the amplifier output.

Figure 2.33: Schematic of the sampling circuit.

When the capacitor is connected to the input of the comparator, it will be charged, from its stored voltage, to *vdd* via a constant current controlled by *VPR* (set by the 6-bit DAC) flowing through p_2 (figure 2.30). The charging speed is controlled by the current. The voltage at the capacitor is compared to a threshold $V_{th}.Pad$ (set externally via a variable resistor on the interface PCB). The comparator goes off when V_{cap} (the voltage on C_1 or C_2) exceeds V_{th}. The duration of the pulse at the comparator output will be proportional to the signal charge that the pixel sensor acquired. Figure 2.34 gives simulated waveforms.

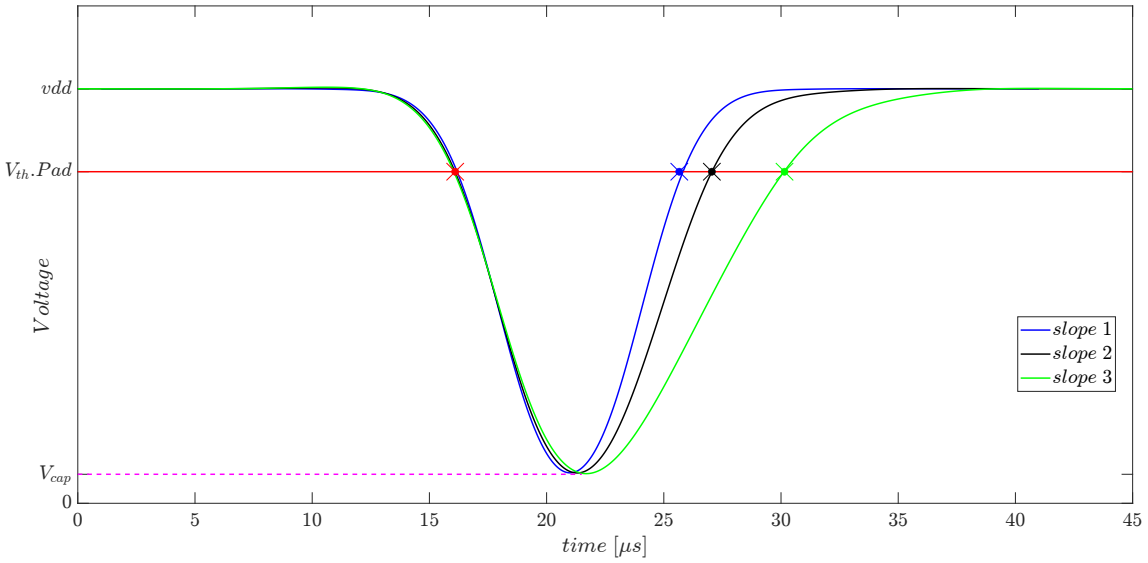


Figure 2.34: Diagram of capacitor voltage as a function of time at the comparator input for three different *VPR* values. Each *VPR* generates a different current intensity that is translated into a different slope in the voltage charge.

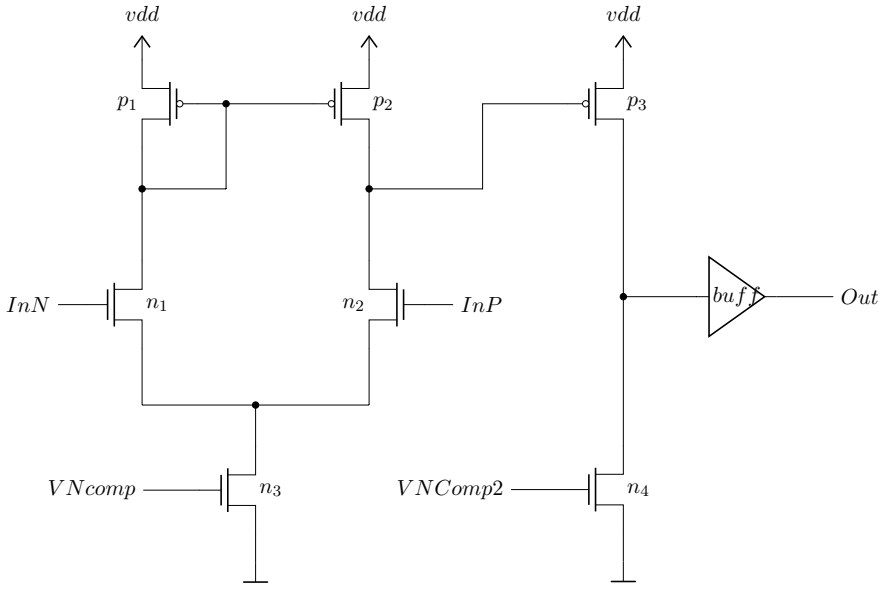


Figure 2.35: Transistor level schematic of the comparator.

In the voltage diagram of figure 2.34 three different slopes were plotted for the same voltage measured. The plot shows how the time at which the capacitor voltage crosses the $V_{th}.Pad$ increases as the slope decreases. Figure 2.36 shows how the change in the slope modifies the time that the pulse is on. In the example figure, $t_1 < t_2 < t_3$, as the slope decreases, it takes more time the current to charge the capacitor until it reaches the $V_{th}.Pad$ voltage.

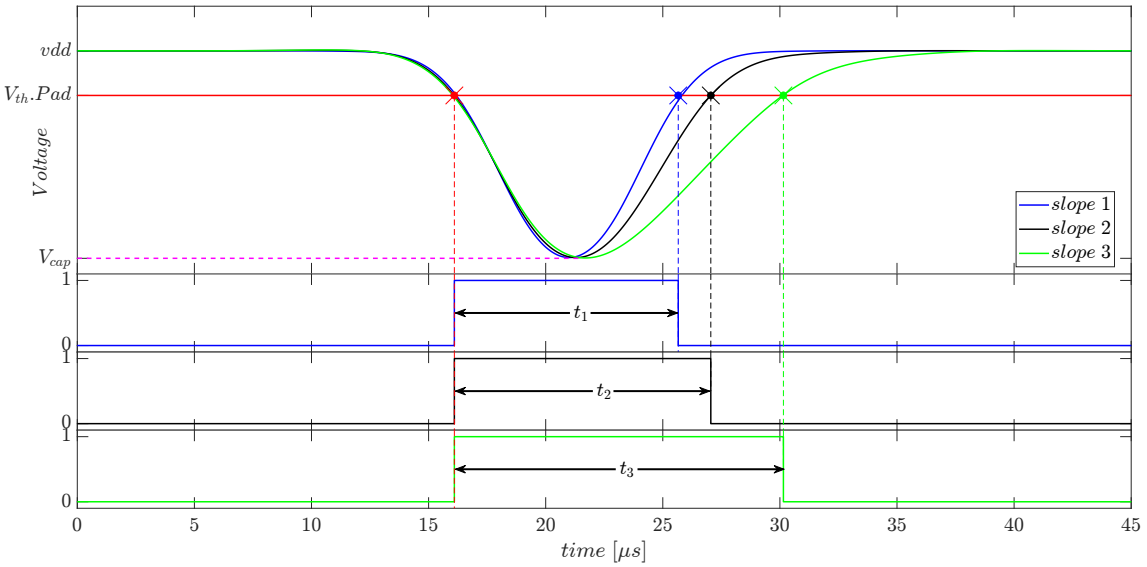


Figure 2.36: Diagram of output comparator pulse duration for three different *VPR* values as a function of time. As the *VPR* increases, the slope increases too, creating a shorter pulse duration at the comparator output.

The relationship between the width of the pulse at the output of comparator and the voltage of the signal can be estimated by subtracting to the threshold voltage (V_{th}) the voltage to which the amplifier output went. By diving that voltage difference with the current to which the capacitor C_1 or C_2 is charged, the pulse width can be obtained.

The width as function of signal voltage can be expressed with the following formula (2.6):

$$\Delta t = \frac{V_{th} - V_{signal}}{slope} \tag{2.6}$$

The slope can be expressed as:

$$slope = \frac{I_{VPR}}{C} \tag{2.7}$$

Where C is the value of the capacitor C_1 or C_2, both are 368 pF. I_{VPR} is the current set by p_2 in figure 2.30 via *VPR* DAC value.

By combining equation 2.6 and 2.7, we arrived to the formula:

$$\Delta t = \frac{C}{I_{VPR}}(V_{th} - V_{signal}) \tag{2.8}$$

The ADC converts the comparator pulse width into 8-bit digital value.

As summary, in figure 2.37 all the relevant signals in single sampling mode for the amp-ADC block are plotted.

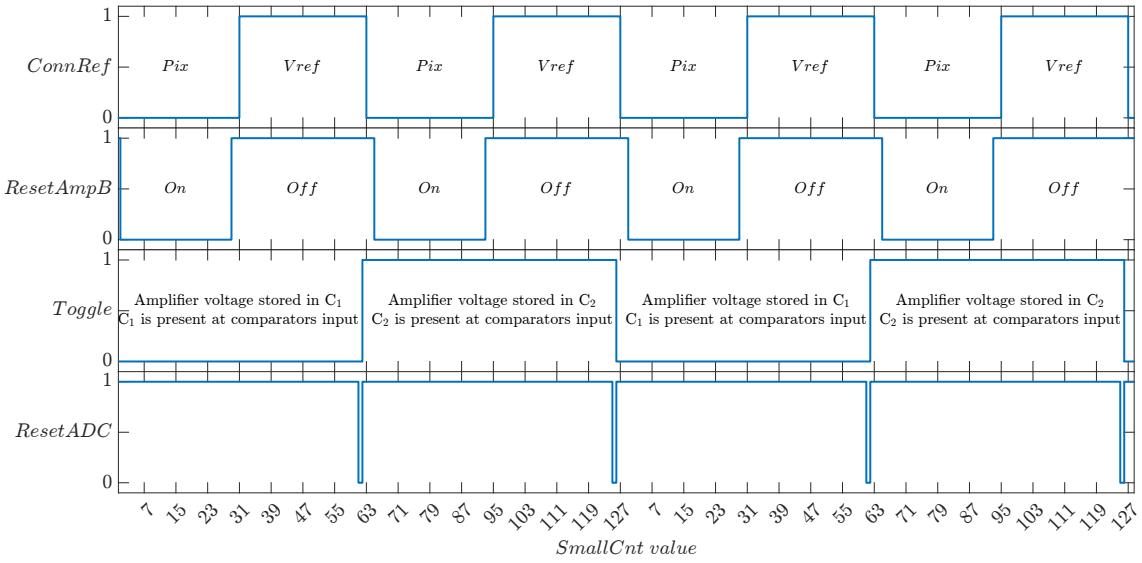


Figure 2.37: Signals used to control the amp-ADC block of HPIXEL in single sampling mode. The x-axis corresponds to the value of the 7-bit counter *Smallcnt*, clocked with a 12.5 MHz clock.

As already mentioned, *ConRef* controls the multiplexer at the input of the amplifier the amplifier. During the time the *Vref* is selected, the amplifier is in a reset state. As soon as *ConRef* becomes "0", the amplifier is enabled (by opening the reset switch) and the amplification of the signal coming from the pixel is performed (equation 2.5). At the same time capacitors C_1 and C_2 are used to sample the output voltage. C_1 or C_2 will be charged while the other will be used to produce the voltage ramp. Finally, the duration of the output pulse will be digitized.

The ADC block contains an 8-bit wide shift register. The data will be serially transmitted out of chip.

2.3.4 Signal shaping block

Most of the signals for controlling the pixels and ADCs are generated by FPGA and the on-chip signal shaping block only buffers and inverts them. This block is mainly a combinational circuit, placed to reduce the amount of IO pads, because its generates the complementary signals of the ones sent by FPGA. A list of the inputs and outputs of the block is given:

- Input signal coming from FPGA
  - *ConRef.Pad* is used to generate the signals used to switch the multiplexer at the input of the amp-ADC block
  - *ResADC.Pad* is used to multiplex the output between the data in the bus and the current pixel readout
  - *ResetAmp.Pad* is used create the signal to reset the amplifier of the amp-ADC block
  - *ResetPix1.Pad* is used to generate the corresponding signal to control the switch *ResNWELLB* in the pixels
  - *ResetPix2.Pad* is used to generate the corresponding signal to control the switch *ResB* in the pixels
  - *SampPix.Pad* is used to generate the *Samp* signal to turn on and off the switch in current pixels

  - *ShiftPix.Pad* is used to generate the *Sel* and *SelB* signals to turn on and off the switch in current and voltage pixels
  - *Toggle.Pad* is used to generate the signals used to switch between capacitors in the amp-ADC block
  - *Ck.Pad* is used to clock the ADC

- Output signals going to the amp-ADC block
  - *ResetADC*
  - *CK*
  - *ConRef* and its complement
  - *Res1B* and its complement
  - *Use2XB* and its complement
  - *Use2YB* and its complement
  - *Conn2YB* and its complement
  - *Conn2XB* and its complement

- Output signals going to the row control block
  - *ResetPix1*
  - *ResetPix2*
  - *SamplePix*
  - *Shift*

2.4 Operation

The data from ADCs are written into parallel in serial out shift register. The register width is 8-bits. The digital data of each chip are sent to the LVDS drivers in series (figure 2.38).

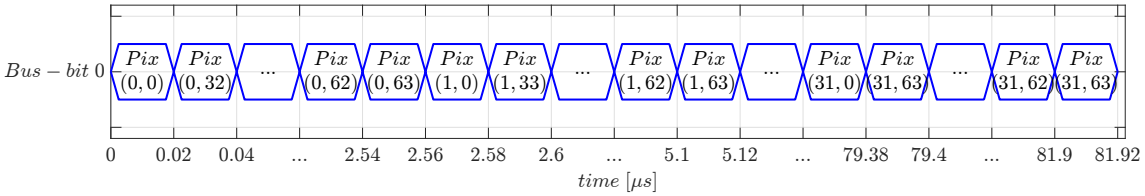


Figure 2.38: Output bus showing only one bit output timing.

The data received by the FPGA are stored in 80-bits wide fifo. Each 80 bit word stores 8 ADC (pixel) values, as well as two extra 8-bit debug words. The data stored in this fifo are then sent to the PC via USB.

The sensor is capable of working in two different modes, CDS and single sampling. Single sampling mode is used for both, current and voltage pixels, while the CDS mode is reserved for the current pixels only.

When using the single sampling voltage mode, the signal *ConRef* generated in the FPGA toggles between “0” and “1”. On the other hand, if CDS mode is used, *ConRef* will be set to digital “0” connect the amplifier input with the pixel signal.

There are two data acquisition modes implemented in software, frame mode and zero suppression mode.

2.4.1 Frame mode

The frame mode is the simplest one. The data sent by the sensor are stored frame by frame. The histogram for each pixels is calculated. The ADC data of all pixels are stored for later offline analysis. This mode is used to acquire data to use as a pedestal in zero suppression mode. This mode of operation creates a large amount of data that needs to be stored, that is why is not convenient for long measurements.

2.4.2 Zero suppressing mode

In this type of data processing, the measurement is subtracted using pedestal values. By gathering numerous frames without a signal source (dark measurement), the pedestals are determined by average the value for each pixel. The FPGA's RAM then stores the value that was determined for each pixel. The FPGA will afterwards deduct each pixel's corresponding pedestal from the measured value of each pixel during measurements.

This approach runs the danger of producing negative numbers, which will be converted into an integer with a high value since the data is made up of 8 bits without a sign. All of the results are shifted by 64 to get around this problem. This the zero to 64 ADU.

2.4.3 Threshold mode

This mode compares each pixel measurement to a threshold value that the user sets in the computer. The entire frame is sent to the PC if the value collected exceeds the threshold, which indicates that a signal has been measured by the pixel.

This approach has the benefit of producing less data overall and avoiding empty frame storage. Signals that are below the threshold will be ignored. This mode and zero suppressing mode can both be used simultaneously.

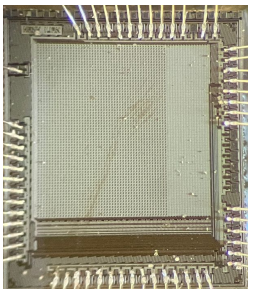
2.5 PCBs

The system needed to work with the HPIXEL consists of two PCBs, the chip carrier, where the sensor is glued and bonded, and the interface PCB, used to connect the chip carrier to the FPGA.

2.5.1 Chip carrier PCB

The chip is glued and bonded to the PCB carrier. The PCB, shown in figure 2.39(a), was designed to fit several chips designed in our group. My motivation was to design a multi-purpose PCB for a cheap, easy, and fast way to wire bond the different sensors of the ADL group without the whole process of design a new PCB each time. This approach reduces the cost and time to have a sensor ready to be measured. To be more versatile, I implemented as part of the PCB a PCI-express (peripheral component interconnect) male type connector. A detailed diagram of the placement and dimensions of the pads is presented in appendix A.1, as well as a list of each pad and their function.

(a) PCB carrier with HPIXEL sensor glued and wire bonded.



(b) Close up of the HPIXEL glued and wire bonded to the PCB carrier.

Figure 2.39: HPIXEL sensor glued and wire bonded to the PCB chip carrier designed with PCI-express connector type.

This universal chip carrier PCB with the HPIXEL sensor bonded on it is then connected via a PCI-express connector to the interface PCB.

2.5.2 Interface PCB

Inside an electron microscope, a vacuum is needed to avoid deflecting the electrons by collisions with air atoms. Since the common material on which PCBs are made (fr4[3]) is porous, it has a high air abortion, which makes more difficult and time-consuming to generate the vacuum level required. Therefore, for this specific application, a ceramic PCB was manufactured as per recommendation from experts at Thermo Fischer, because this material is best suitable to use inside the vacuum chamber.

The interface PCB (figure 2.40) acts as an interface between the sensor and the FPGA, as well as provides test points to connect an oscilloscope for signal probing and several potentiometers to provide the necessary voltages for the sensor to work. This PCB routes the signals shared between FPGA and chip and will supply the power voltages needed by the sensor. The board has a PCI-express type connector to plug the chip carrier while using an FMC (FPGA Mezzanine Card) type connector to connect to the Nexys Video [20].

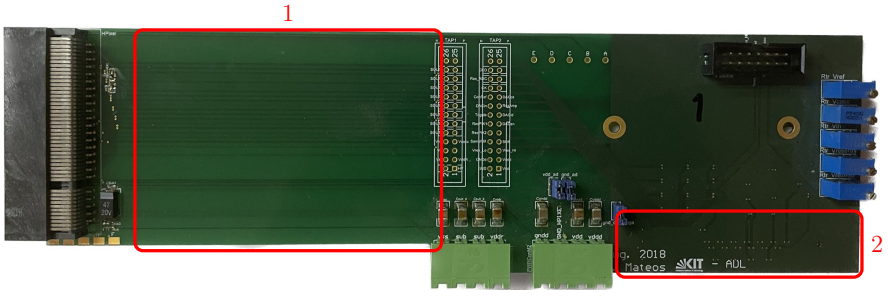


Figure 2.40: PCB interface used to connect the HPIXEL sensor (via PCI-express type connector) to the FPGA (via FMC connector). Boxes in red correspond to the specifications list given by Thermo Fisher Scientific

The main features of this PCB, according to the specifications given by Thermo Fischer Scientific, are:

[3] https://thegundcompany.com/wp-content/uploads/2016/11/NEMA-FR4-EPGC-202-from-The-Gund-Co.pdf

1. Design a long, narrow, and flat part of the PCB to enter the notch of the vacuum lid.
2. Place the FMC connector on the bottom side and bottom right corner to be able to fit the FPGA in the microscope.

After the PCB is placed in the lid, the notch needs to be sealed with special glue to create a tight fit for the vacuum. To make the neck as flat as possible all the tracks are placed on the internal layers, and there is electronic component placed in the neck. In figure 2.41 a picture of the PCB that fits through the vacuum lid is shown.

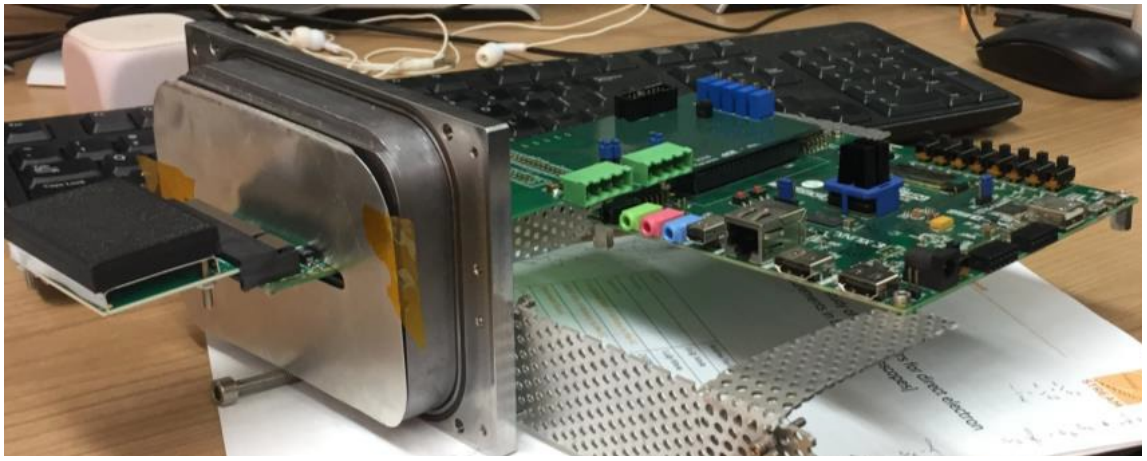


Figure 2.41: PCB interface used for communication between HPIXEL and FPGA after it has been placed in the lid of the vacuum chamber of the TEM.

2.6 FPGA system

The FPGA-board used in this project is the *Nexys Video* by Digilent [20] (figure 2.42). The FPGA firmware is based on the code developed by KIT-ADL. A brief introduction of the relevant blocks will be given in this chapter, as well as an explanation of the main blocks used to control the HPIXEL sensor.

The firmware consists of two blocks: The FTDI communication to establish connection to a PC and the IO multiplexer to manage, configure, and receive data from to HPIXEL.

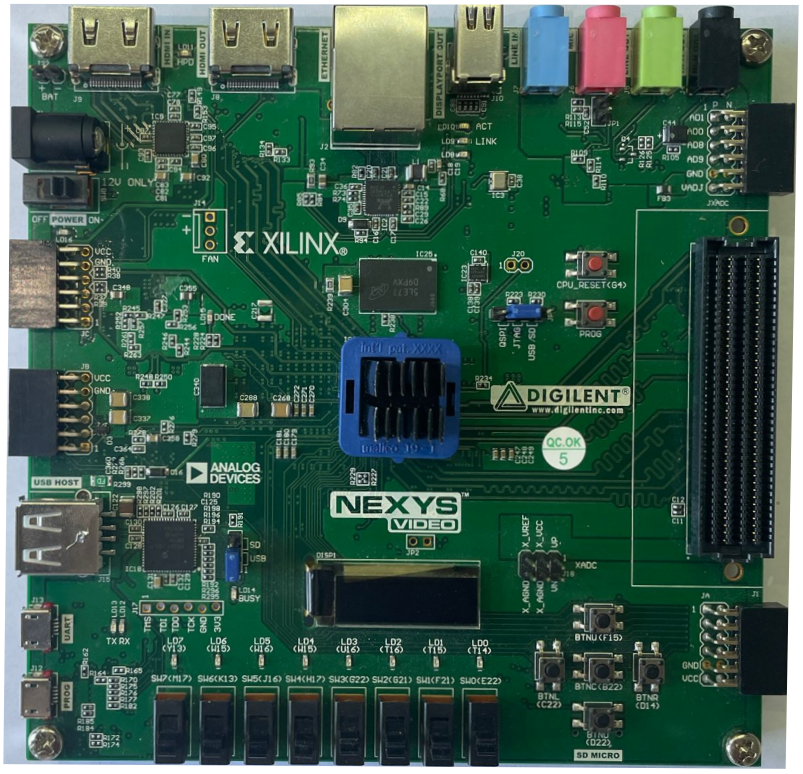


Figure 2.42: Nexys Video board used for data readout from HPIXEL sensor.

2.6.1 IO multiplexer

The IO multiplexer contains different devices that perform the following tasks:

Device 0 iomux2SDS interface, used to produce the signals for writing into HPIXEL DAC shift register when the sensor needs to be configured

Device 1 Not used

Device 2 HPIXEL fast control creates all the control signals and receives the data from the sensor. The chip does not posses memory, so the data generated by HPIXEL must be read continuously. Because of that, the code that generates the control signals for operation of the sensor, will also create extra signals to sort the data into packages of 80 bits to be sent to the FTDI FIFO.

Device 3 Not used

Device 4 Writes into RAM the values of the pedestals in case of zero suppressing measurements

Device 5 Writes into RAM the threshold value sent from the PC

A flow chart of the state machine of the IO multiplexer is shown in appendix A figure A.2.

2.7 Software control

The last part needed to use the HPIXEL is the software. It is based on the Qt software developed by F. Ehrler and R. Schimassek [71, 22] to use in combination with the FPGA firmware. I designed the interface in C++ using the Qt framework.

The interface facilitates the configuration of the DAC values described in section 2.3, as well as allows the user to select between the two different pixel flavors and the measurement modes described in section 2.2. The software is capable of showing in real time the output of the matrix as a frame-by-frame image and a compounding histogram of the data for a user-selected pixel or the whole matrix. This software will save the data sent by the sensor for offline analysis.

Figure 2.43 shows a screen shot of the software interface with all the components described above.

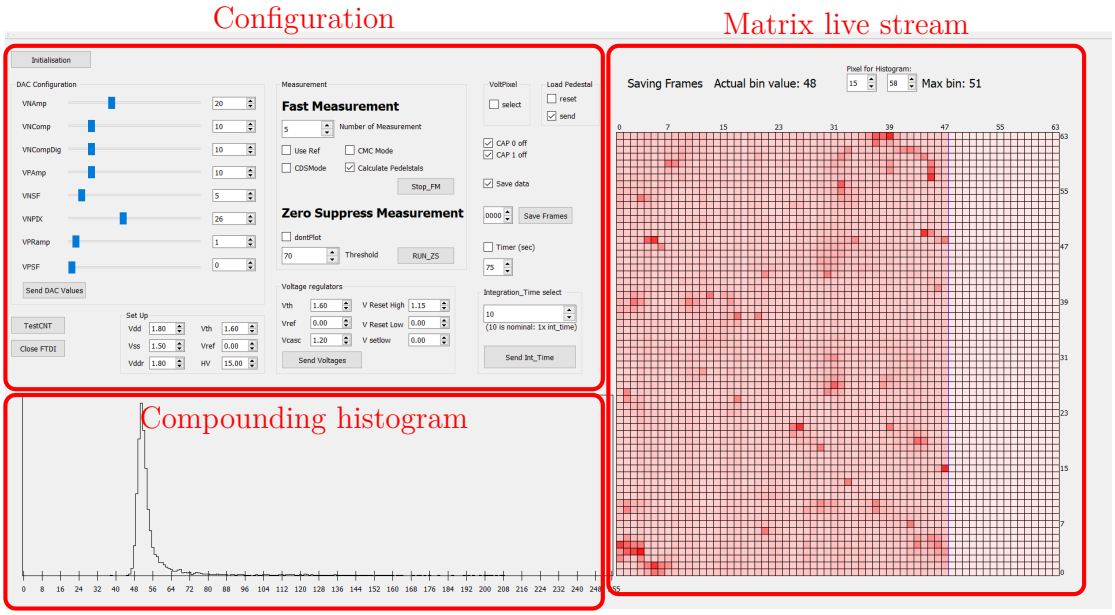


Figure 2.43: Qt software interface of HPIXEL with the three main parts differentiated. Configuration is where all the configurable parameters of the chip are set, the matrix live stream displays the matrix values sent from the FPGA and the compounding histogram section displays the histogram of the whole matrix as it is being calculated.

2.8 HPIXEL measurements

The HPIXEL sensor was tested in the laboratory with x-rays to characterize its behavior and to verify the correct functioning of all components. In section 2.8.1 the results of these measurements will be discussed.

The HPIXEL was also tested under real conditions inside a TEM. All the measurements were carried out in Thermo Fischer Scientific facilities in Eindhoven, the Netherlands, using a TECNAI-F20 TEM. The result of these measurements will be discussed in section 2.8.2.

2.8.1 Laboratory characterization

The output of the sensor is a value between 0 and 255 (digital word of 8-bits) that represents the comparator pulse duration. This time is in turn a representation of the amount of charge that each photodiode sensor acquires during the sensing time. Finally, the amount of charge is directly related to the intensity and energy of the incoming radiation (in the case that the particle is fully absorbed within the depleted region).

To be able to use the sensor as a radiation detector, we need to find a conversion factor between the 8-bit ADC output value (ADU) and the energy of the incident radiation. For that purpose, a series of x-ray measurements were carried out at KIT. Using different materials, a range of x-ray energies can be generated. The x-ray machine utilized was a Seifert ISO-DEBYEFLEX 3003[4] that belongs to the ETP institute (Institut für Experimentelle Teilchenphysik) in KIT[5], with target energies from 6.4 keV up to 25.27 keV.

Each of the target materials and its corresponding energies is listed in table 2.2[6], the x-ray fluorescence (XRF) energy spectrum of each is shown in appendix A figure A.3.

Table 2.2: Target material and its corresponding main energy peaks.

Target material	**Kα [keV]**
Iron (Fe)	6.40
Copper (Cu)	8.05
Zinc (Zn)	8.64
Molybdenum (Mo)	17.48
Silver (Ag)	22.16
Indium (In)	24.21
Tin (Sn)	25.27

The energy of the characteristic x-ray energies of the targets ranges from 6.4 keV to 25.27 keV. The Kα peak corresponds to an electron of the K shell being expelled (by the x-ray photon) and an electron from the L shell takes its place, liberating this way a photon of a characteristic energy [81].

The measurements were carried out using zero suppressing mode and CDS for current pixels and single sampling mode for voltage pixels. A threshold of 72 ADU was set for the current pixels, this allows for the x-ray peak of the different targets to be visible. Since the voltage pixels have a smaller amplification, for them, the maximum gain was used in the amp-ADC block, while the current pixels were set to the minimum gain. An example output histogram measurement for all the materials for current pixels is shown in figure 2.44.

[4] https://usermanual.wiki/Ge-Appliances/GeModulesBrochure648941.922700266/html
[5] https://www.etp.kit.edu/Bestrahlungszentrum.php
[6] http://www.xrfresearch.com/xrf-spectra/

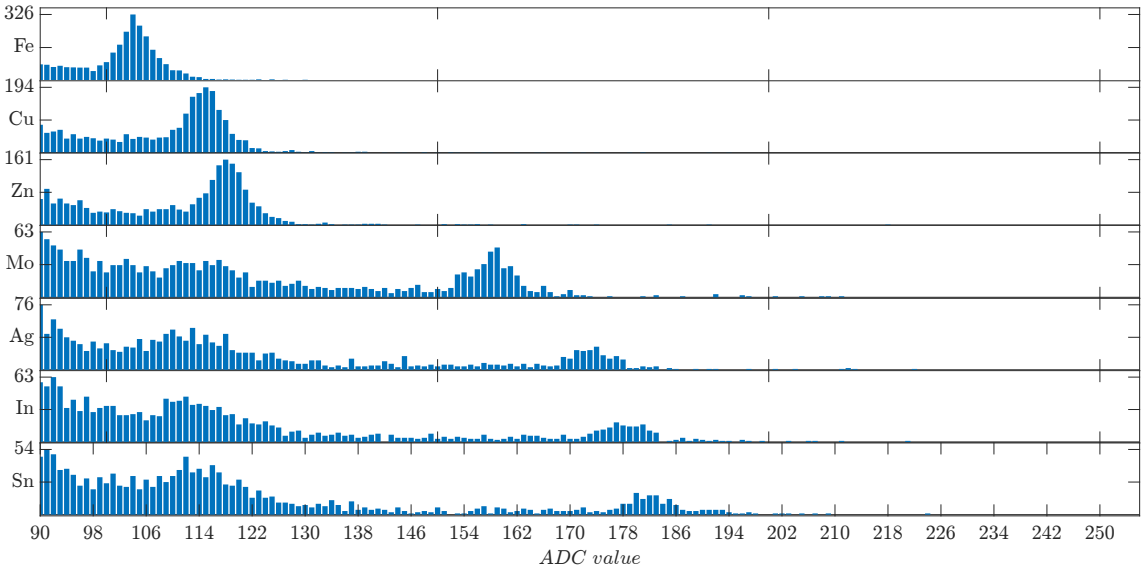


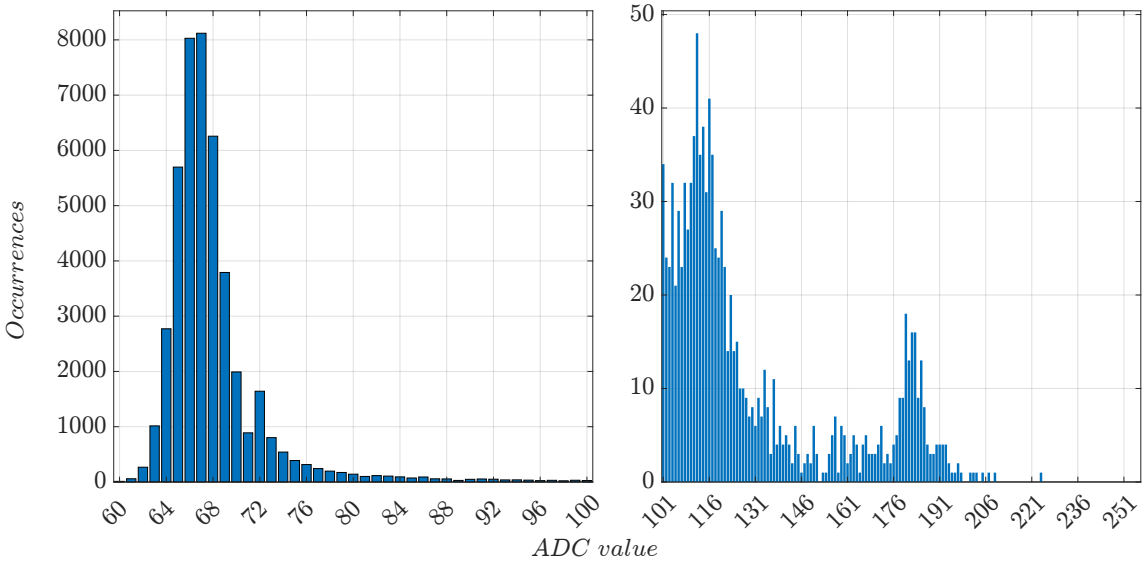
Figure 2.44: Set of histograms (for all the pixels in the matrix) obtained for all the different target materials used to generate x-rays of different energies. The x-axis is the 8-bit ADC value, ADC units (ADU).

Since the histograms presented in figure 2.44 correspond to the whole matrix, the peak caused by pixels without signals at around 66 ADC value has large amplitude compared to the different Gaussian peaks of each energy. Because of that, the histograms were plotted from the value 90 to 256, to be able to distinguish the Gaussian peaks of each energy.

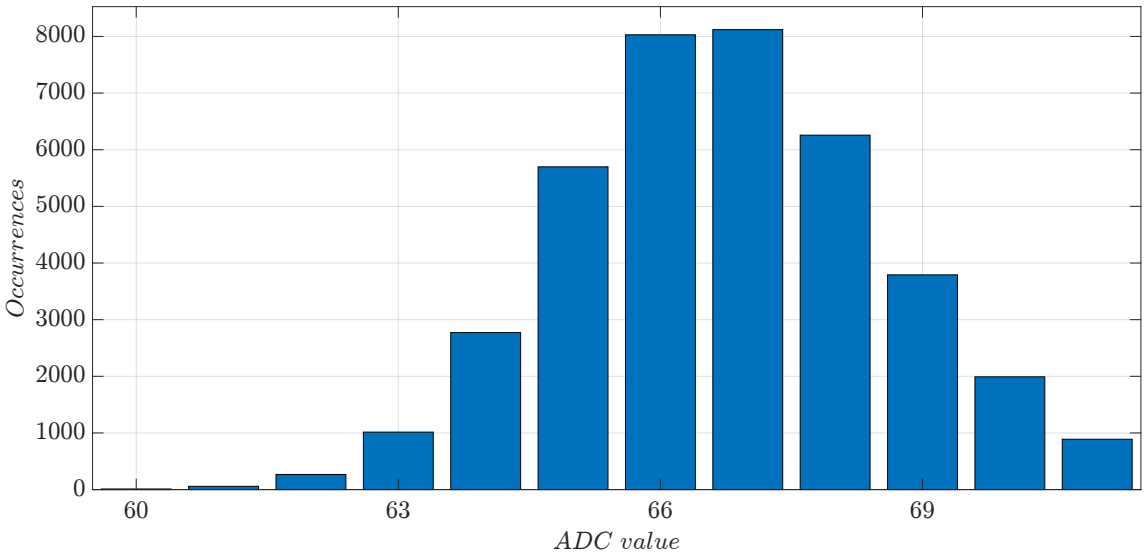
For the measurements with targets of higher energies (molybdenum, silver, indium, and tin) shown in figure 2.44 the histograms show two peaks, one at around ADC value = 133 and another at higher values. The peak at around 113 ADU is caused by the mounting setup of the target inside the x-ray tube, which is made of copper and adds its own x-ray energy to the measurement. This extra peak does not cause a problem, since we are not investigating the amount of counts, but the position of the peaks.

An example, in figure 2.45 the histogram for the tin target is divided into four subplots. The measurement were done by setting a threshold value of 72 ADU. If only a pixel measures a signal larger than 72, the entire frame is readout, including the pixels with values under the threshold.

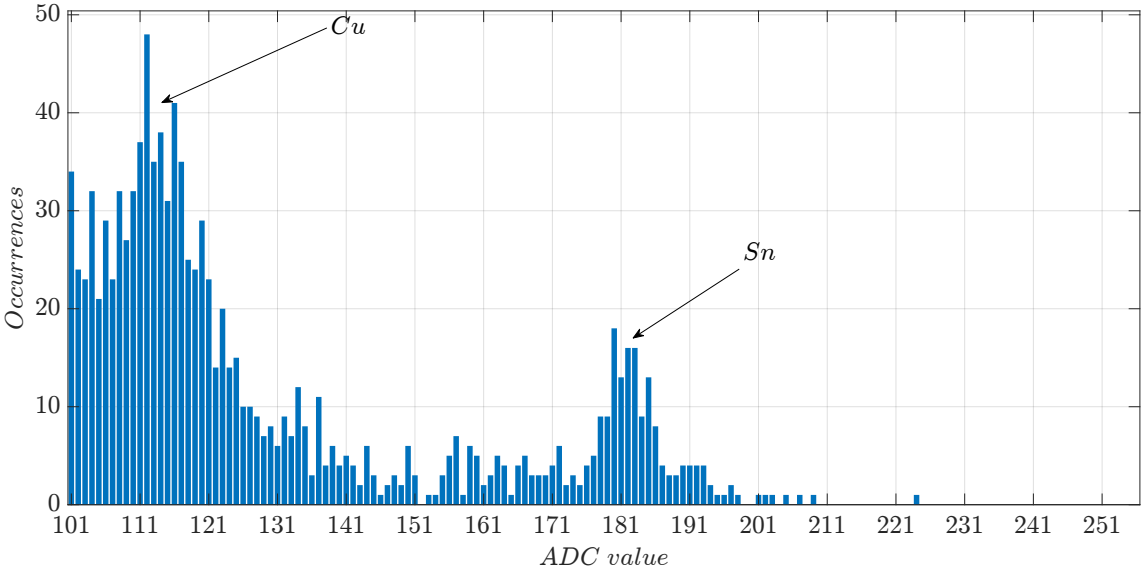
If pedestals are used (zero suppressing mode), it is possible to have negative values due to noise. If that happens, when the data is sorted in Qt and the histogram plotted, those negative values will be placed at the end of the histogram (high ADU values), creating an artifact. To solve this issue, when using pedestals, a value of 64 is subtracted from the data measured in the FPGA, moving the zero to 64 ADU. Because of that all the histograms will start at 64, and it is expected to see a peak at 64 ADU.



(a) Complete histogram divided into two, ADC count distribution of majority of pixels with no signal on the left and Gaussian peaks caused by x-rays on the right. The peak at ADC value 72 corresponds to the tail of noise distribution for pixels that exceeded the threshold (set to 72 ADU).



(b) Distribution caused by ADC count of majority of pixels with no signal.



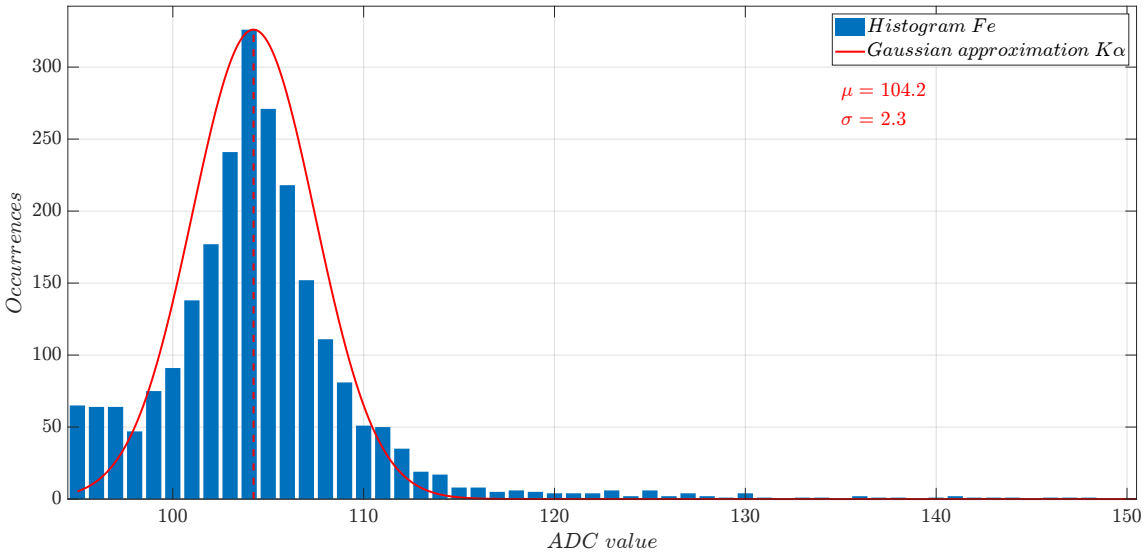
(c) Peaks caused by x-rays.

Figure 2.45: Histogram of the Sn measurement divided into: (a) complete histogram, (b) zoom on the ADC count distribution of majority of pixels with no signal, (c) zoom on the peaks caused by x-rays.

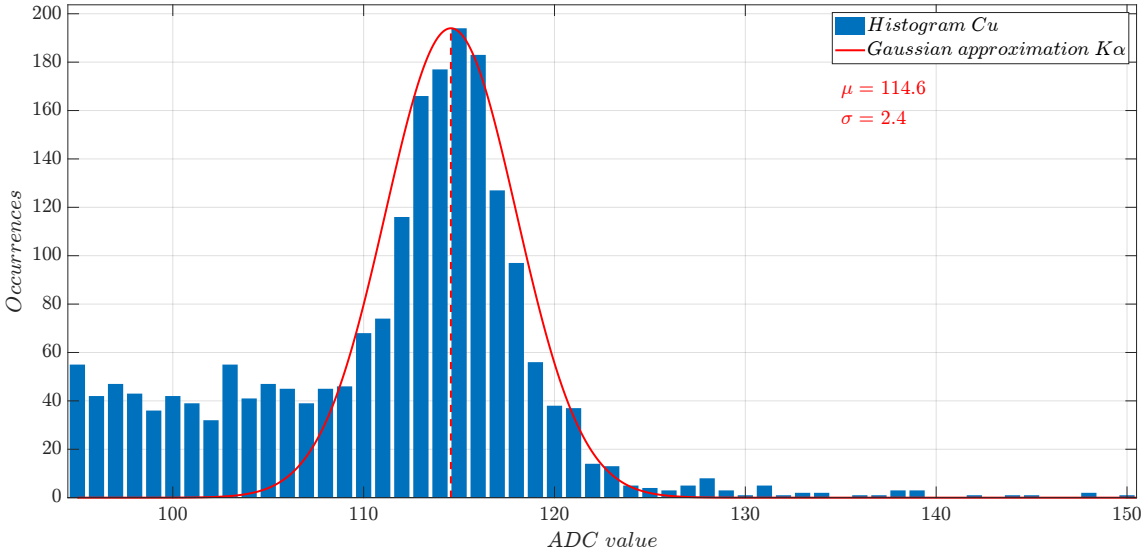
Figure 2.45 (b) shows the peak caused by ADC values below the threshold located around ADC count 66 instead of 64. This can be related to a change in temperature, since the measurement of pedestals were done at the beginning and then all the target measurements were done. As the time passes and the sensor was irradiated, the temperature increased, moving the baseline. On the left plot from figure 2.45 (a) the peak at 72 corresponds to the tail of the noise distribution of the pixels that exceeds the threshold value due to noise. Finally, figure 2.45 (c) shows the Gaussian distribution that correspond to Kα peak of tin as well as the residual peak of copper from the x-ray setup.

To analyze the measurements, the histogram of one pixel for all the frames was computed, and then the Gaussian peak was fitted using equation 2.9. That equation takes into account only the Kα energy peak [81]. The mean value μ will correspond to the ADC count equivalent to the energy peak, while the standard deviation obtained σ represents the noise of the pixel. In table 2.3 the results of the measurements are listed and aligned with the energies. Figure 2.46 shows the histograms obtained for each target, as well as the fit of the energy peaks.

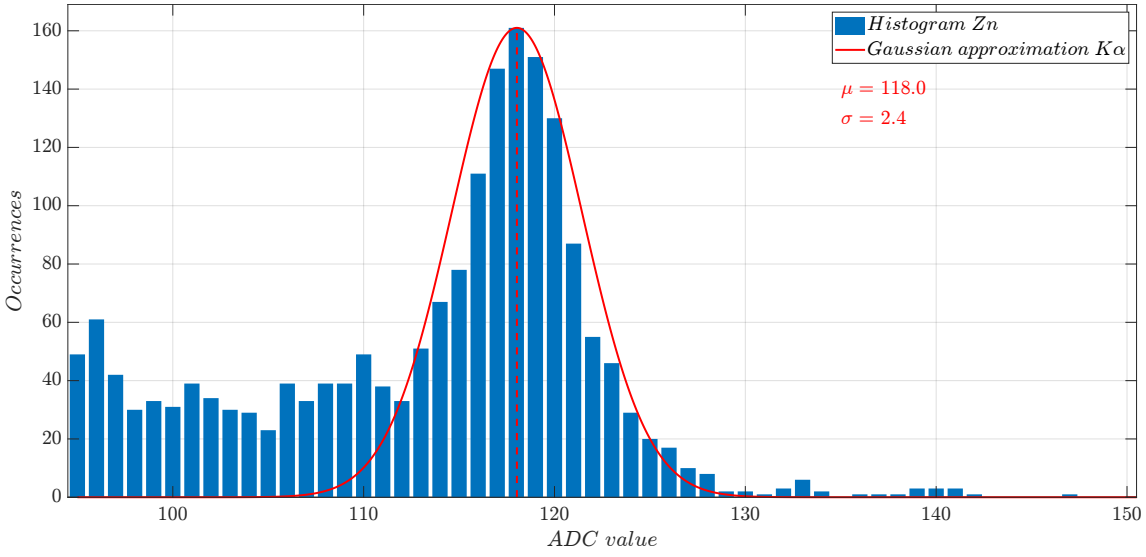
$$y = Ae^{\frac{(x-\mu)^2}{2\sigma^2}} \tag{2.9}$$


Histogram Fe
Gaussian approximation Kα
μ = 104.2
σ = 2.3
Occurrences
ADC value
0
50
100
150
200
250
300
100
110
120
130
140
150

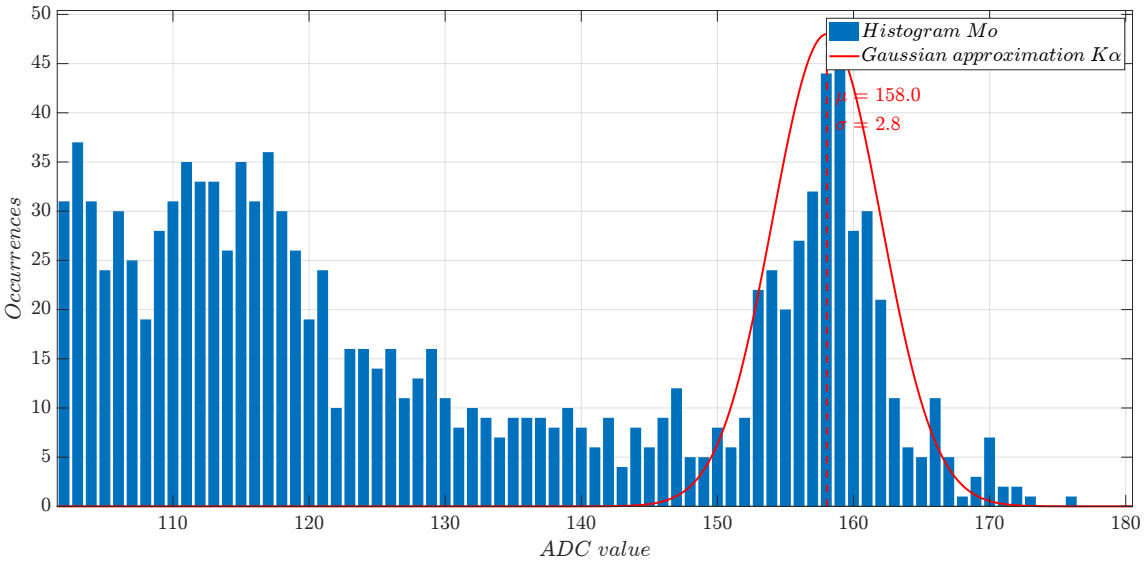
(a)


Histogram Cu
Gaussian approximation Kα
μ = 114.6
σ = 2.4
Occurrences
ADC value
0
20
40
60
80
100
120
140
160
180
200
100
110
120
130
140
150

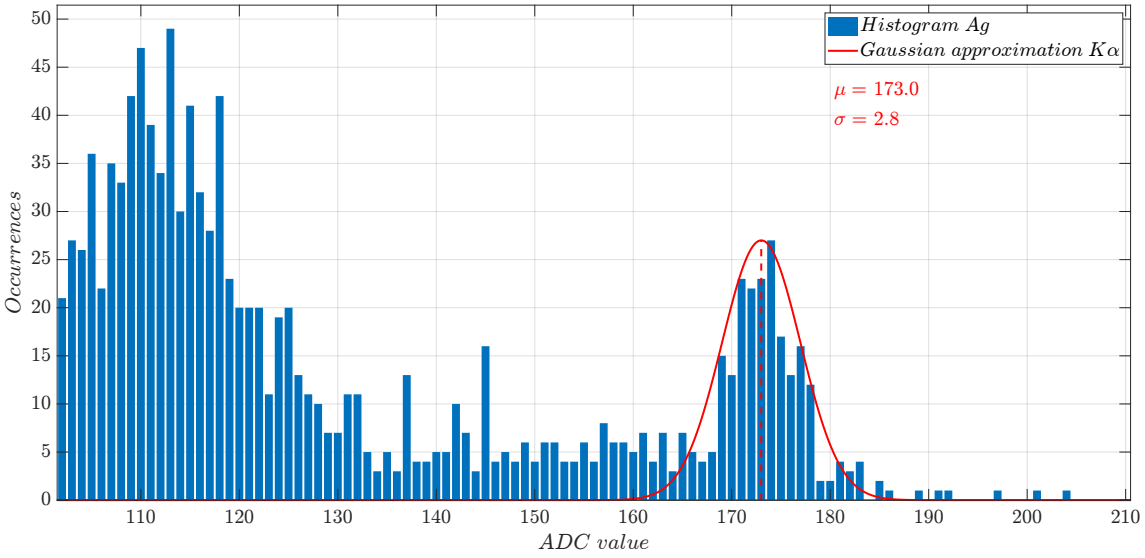
(b)


Histogram Zn
Gaussian approximation Kα
μ = 118.0
σ = 2.4
Occurrences
ADC value
0
20
40
60
80
100
120
140
160
100
110
120
130
140
150

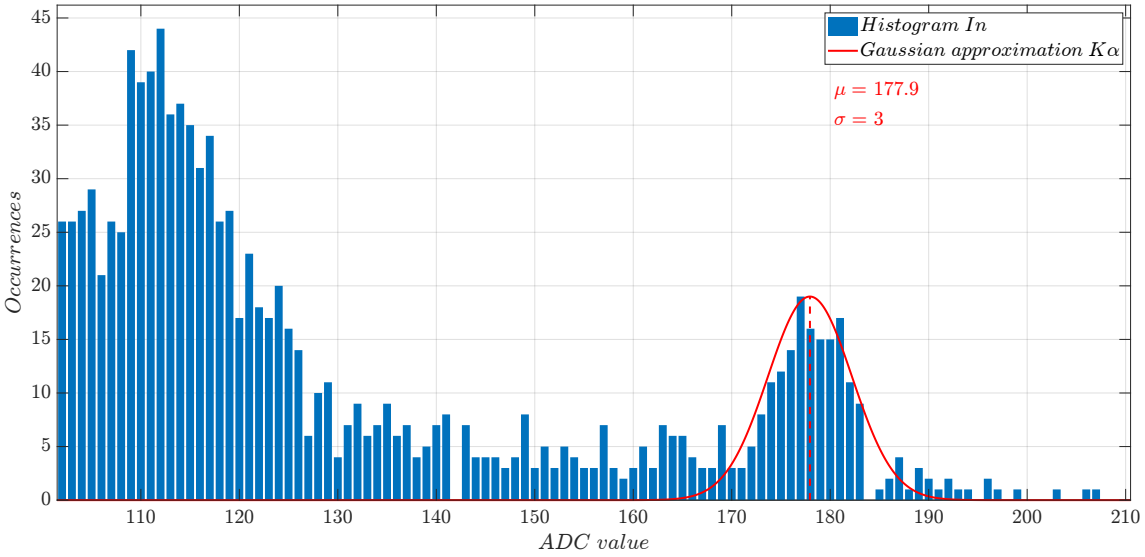
(c)


Histogram Mo
Gaussian approximation Kα
μ = 158.0
σ = 2.8
Occurrences
ADC value

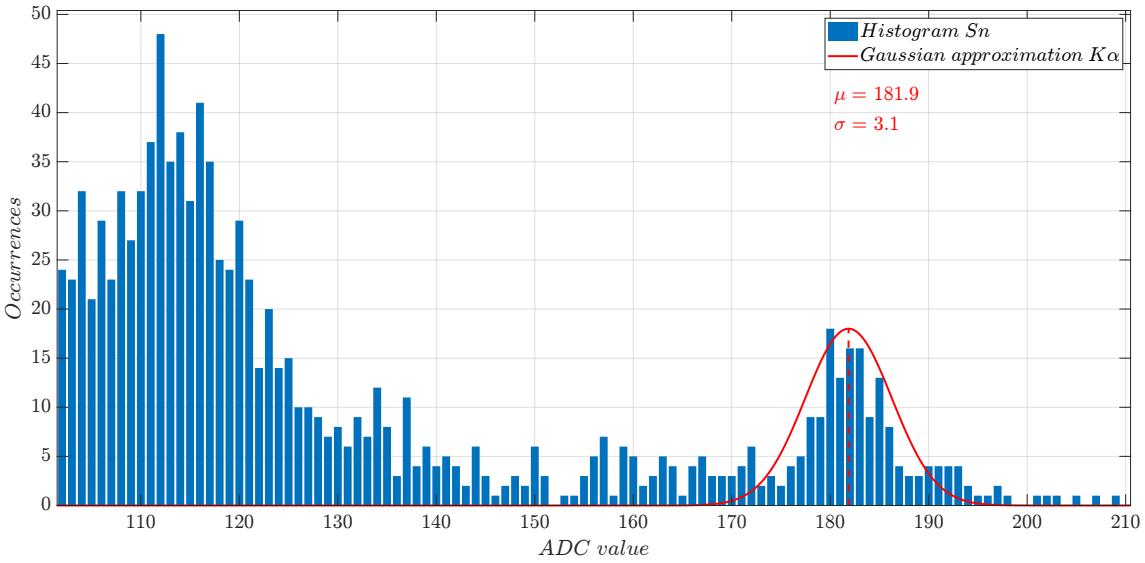
(d)


Histogram Ag
Gaussian approximation Kα
μ = 173.0
σ = 2.8
Occurrences
ADC value

(e)


Histogram In
Gaussian approximation Kα
μ = 177.9
σ = 3
Occurrences
ADC value

(f)



(g)

Figure 2.46: Histogram obtained of Fe (a), Cu (b), Zn (c), Mo (d), Ag (e), In (f), and Sn (g) x-rays. The histograms are fitted with a Gaussian (red) for the Kα peak.

To compute the fittings in figure 2.46 the data are truncated from ADC value 95 to 256, thus ignoring the baseline peak at ∼66 ADC count.

Table 2.3: Energy of the targets(after [81]), the mean values (μ) and sigma (σ) ADU obtained.

Target	**Kα Energy [eV]**	**μ [ADU]**	**σ [ADU]**
Fe	6399.5	104.2	2.3
Cu	8041.0	114.6	2.4
Zn	8631.1	118.0	2.4
Mo	17443.4	158.0	2.8
Ag	22103.1	173.0	2.8
In	24137.8	177.9	3.0
Sn	25192.6	181.9	3.1
Average	-	-	2.7

To obtain the conversion factor between the ADC count output of the chip and the beam energy, a linear fit was performed. The conversion factor is the slope of the linear approximation, which was calculated as being:

$$(244 \pm 6)\frac{eV}{ADU} \ (R^2 = 0.99)$$

The error in the conversion factor comes from the confidence bounds of the linear regression (95%). In figure 2.47 a plot of the measured values as well as the fitted line are shown. The value obtained corresponds to the simulated 254 eV/ADU.

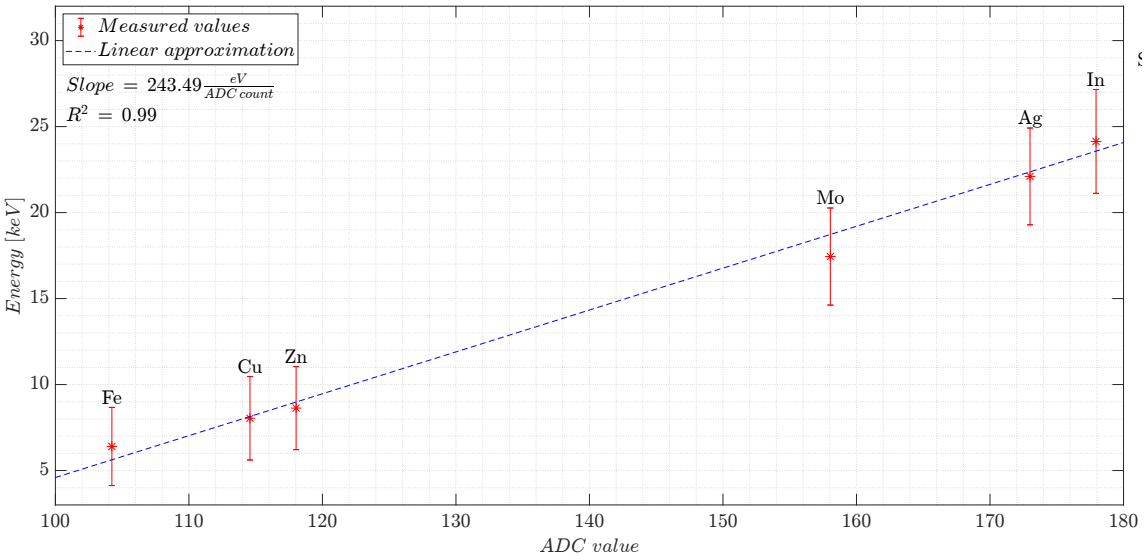


Figure 2.47: Linear regression between ADC value and energy for current pixels. In red the measured data are plotted, while the dashed blue line corresponds to the fit-line.

To compute the average noise of the system, I take the standard deviation (σ) of each Gaussian fit for each target for one pixel (2.3), obtain the average, and I multiply it with the conversion factor previously calculated. I then divide the result with the average energy required to generate one electron-hole pair in silicon to obtain the noise in amount of electrons. Equation 2.10 shows the above described.

$$Noise = \frac{\overline{\sigma} * m}{3.6} \tag{2.10}$$

where

$\overline{\sigma}$: is the average σ calculated in table 2.3
m : is the conversion factor

The noise value obtained is 183 e^-.

The same measurements were performed with the voltage pixels, and the analysis described above was repeated. In table 2.4 the results of the measurements for both, current and voltage pixels, are shown and compared.

Table 2.4: Comparison of the results for the current and voltage pixel noise and conversion factor (slope).

	Noise		**Slope** $\left[\frac{eV}{ADU}\right]$	
	[e^-]	[ADU]	Measured	Simulated
Current pixel	183	2.7	244 ± 6	254
Voltage pixel	226	1.6	509 ± 13	523

2.8.1.1 Radiation hardness

After the energy calibration was performed, to test the radiation hardness of the sensor, a total dose measurement was carried out. The chip was irradiated continuously for ∼6 hours until ∼50 Mrad total ionizing dose (TID) was reached.

It is important to study TID damage, because ionizing radiation induces the build-up of positive charge near the silicon/buried oxide interface. These defects can invert the bottom surface of the silicon channel forming a conducting channel (back channel) between the source and the drain of the transistor, increasing leakage currents, reducing breakdown voltage, and decreasing performance, which can ultimately lead to device failure [73].

After ∼6 hours of irradiation, the chip was working correctly and the calibration factor was 242 ± 6 $\frac{eV}{ADU}$ (as shown in figure 2.48). The noise increased to 242 e^-, which was calculated as before, using formula 2.10.

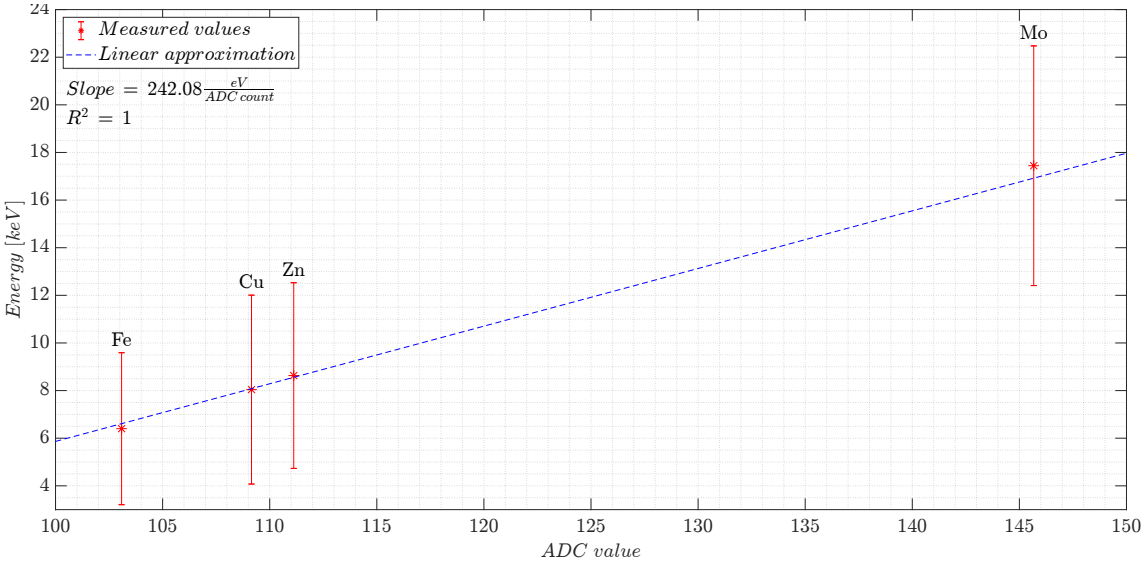


Figure 2.48: Linear regression between ADC value and energy for current pixels after ∼50 Mrad of TID. In red the measured data are plotted, while the dashed blue line shows the linear fit.

For voltage pixels, the lineal regression does not shows a significant variation after ∼50 Mrad. The conversion factor is within the error of the estimation, from 509 ± 13 $\frac{eV}{ADU}$ to 503 ± 13 $\frac{eV}{ADU}$.

The chip was later irradiated for another ∼27 hours to reach ∼250 Mrad of TID. After this, the sensor was tested again with different sources, table 2.5 shows the noise in e^- and ADU, as well as the conversion factor for 0 rad, ∼50 Mrad, and ∼250 Mrad of TID.

Table 2.5: Comparison of the results for the current and voltage pixel noise and conversion factor (slope in [$\frac{eV}{ADU}$]) for different doses.

	Current pixel			**Voltage pixel**		
	Noise		**Slope**	**Noise**		**Slope**
	[e^-]	[ADU]		[e^-]	[ADU]	
0 rad	183	2.7	244 ± 6	226	1.6	509 ± 13
∼50 Mrad	242	3.6	242 ± 6	321	2.3	503 ± 13
∼250 Mrad	376	5.6	242 ± 6	406	2.9	504 ± 13

After ∼250 Mrad, the pixels continue to work, the conversion factor did not change (it was always within the error), and the noise of the system increased as expected.

2.8.2 Measurements in an electron microscope

In May 2019, a set of measurements was performed with two different chips at Thermo Fischer Scientific facilities in Eindhoven, Netherlands. The aim of the test was

to verify the ability of the sensor to detect electrons inside the electron microscope, the possibility to mount the sensor chip inside the TEM, and to perform a set of irradiations to check its radiation tolerance. Figure 2.49 shows how the sensor is placed inside the electron microscope, while figure 2.50 shows close-ups of the setup placed at the bottom of the transmission electron microscope (TEM).

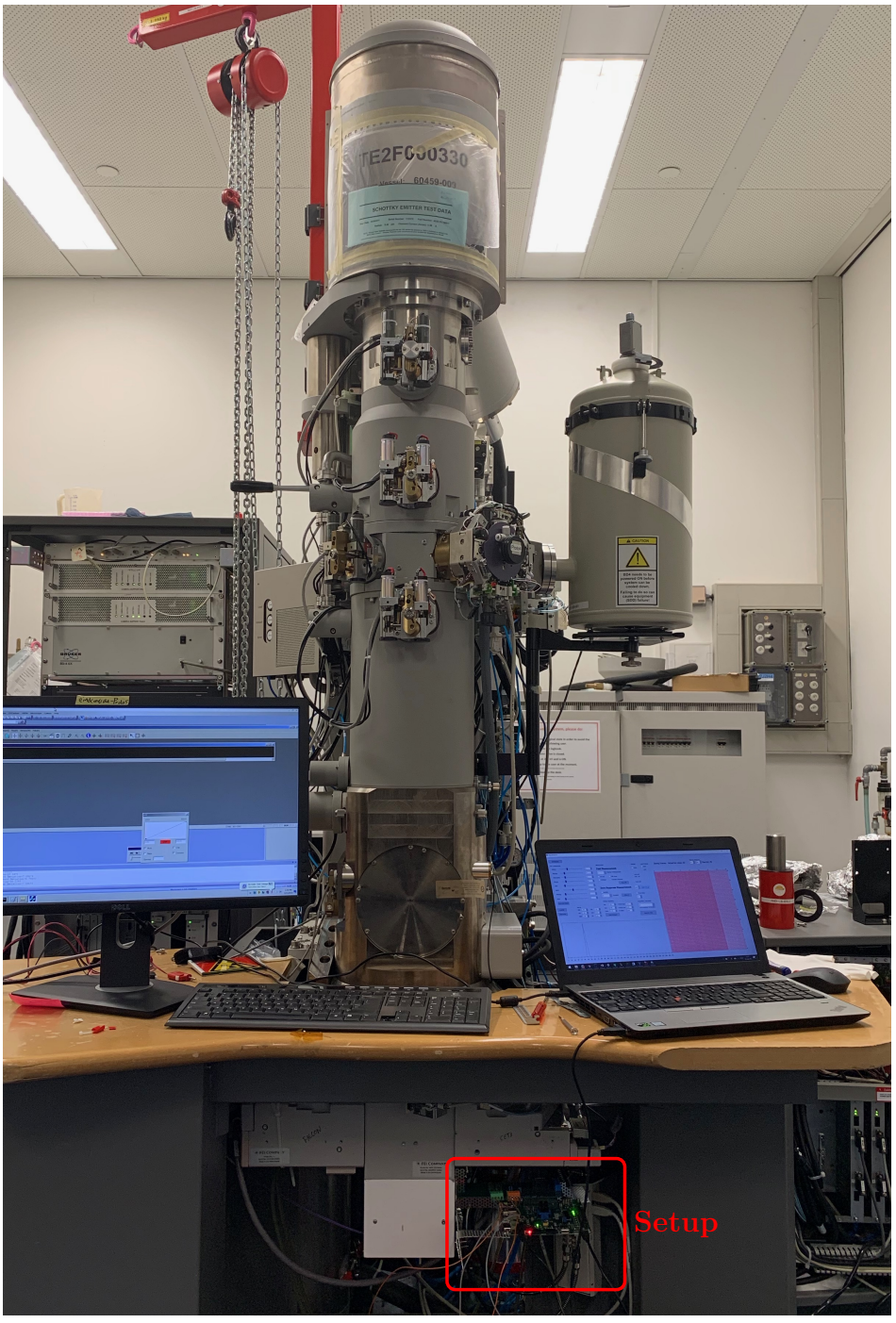


Figure 2.49: TEM used in Thermo Fischer Scientific facilities in Eindhoven to test the HPIXEL sensor. The setup is placed at the bottom of the TEM, right under the table.

(a) Setup placed at the bottom of the TEM, front view.

(b) Setup placed at the bottom of the TEM, angle view.

Figure 2.50: Close-up images of the setup placed in the vacuum chamber of the TEM.

Before the sensor is placed inside the TEM, a Faraday cup connected to an electrometer was used. The computer that controls the TEM allows the user to set the desired current of the beam, however, this parameter is not accurate. Because of that it is necessary to obtain a calibration curve for the current delivered by the beam as function of the current set on the machine (with the aperture of the beam that will be used during measurements). To do that, a Faraday cup in placed inside the microscope connected to an electrometer on the outside to read the real current. Figure 2.51 shows a diagram of the setup described.

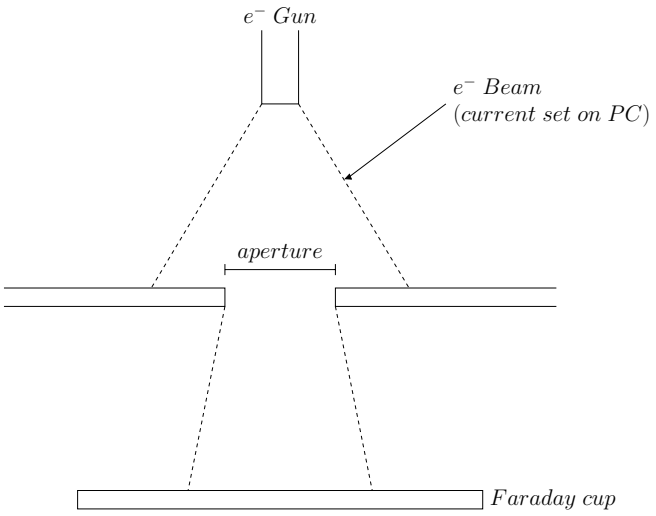


Figure 2.51: Diagram of the setup for measuring the effective current beam after the aperture.

A series of measurements were done, increasing the current on the computer. With the values obtained, I approximate the relationship to the following linear equation:

$$I_{real} = 0.586 * I_{PC} - 19.714pA \tag{2.11}$$

After the calibration of the current was done, the sensor is placed inside the electron microscope, a vacuum is created to avoid that electrons lose energy by interacting with the atoms present in the air. The TEM allows the user to set the desired current, which translates to the number of electrons that are shot, as well as to define the focus and aperture of the beam, to tune the cross section area of the beam.

During the measurements, two chips were irradiated with electrons of 200 keV. With that energy, it is expected around $5.6{\cdot}10^3$ electron-hole pair to be generated for each

electron that hits a pixel. The first chip was homogeneously irradiated, the second sensor was measured with a beam focused only over the matrix.

A measurement of the sensor without the electron gun on was carried out in between different beam currents. With the data of those dark measurements, each frame is corrected to subtract the baseline. There is no need to correct the signals for pedestal since the sensor was used in frame mode.

2.8.2.1 Chip 1

For the first sensor irradiated, we set beam focus to cover the whole sensor. The voltage and current pixels were tested under -1 V and -40 V high voltage bias. The electron beam current was increased between measurements, and between current steps, the noise of the sensor was measured by acquiring frames with the beam turned off and obtaining the histogram. Then a Gaussian was fitted to obtain the mean value (μ) and sigma (σ). The standard deviation will correspond to the pixel noise.

If we compare the histogram of a single pixel measurement for HV = -1 V (figure 2.52) and HV = - 40 V (figure 2.53) when the beam is off, we obtain that the baseline noise decreases from 3.2 ADU to 1.7 ADU (σ) with lower high voltage value.

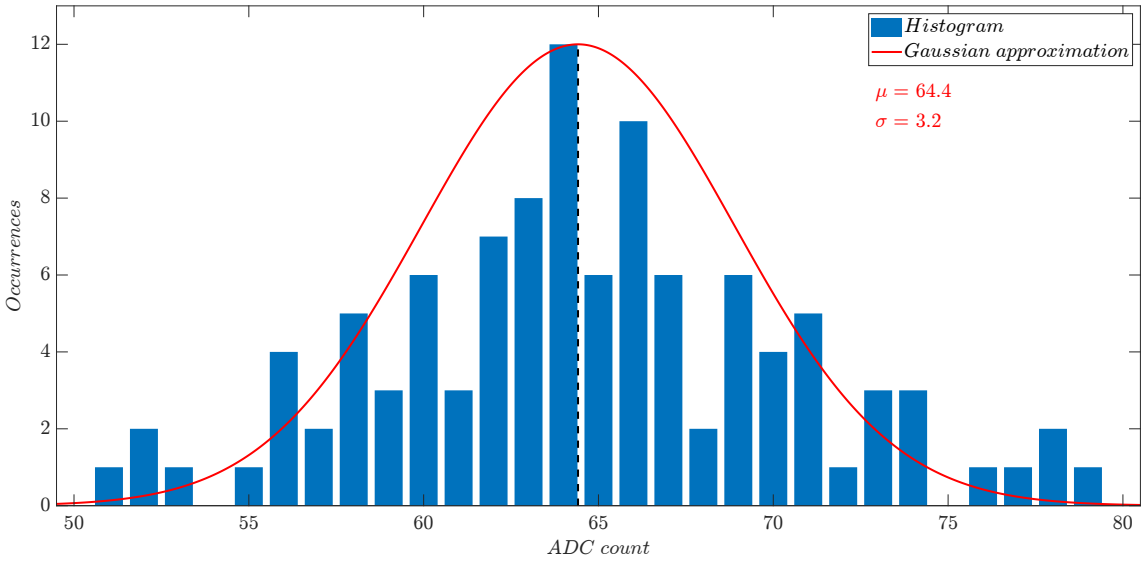


Figure 2.52: Noise of a single current pixel with HV = -1 V before TEM irradiation. Red line is the fitted Gaussian.

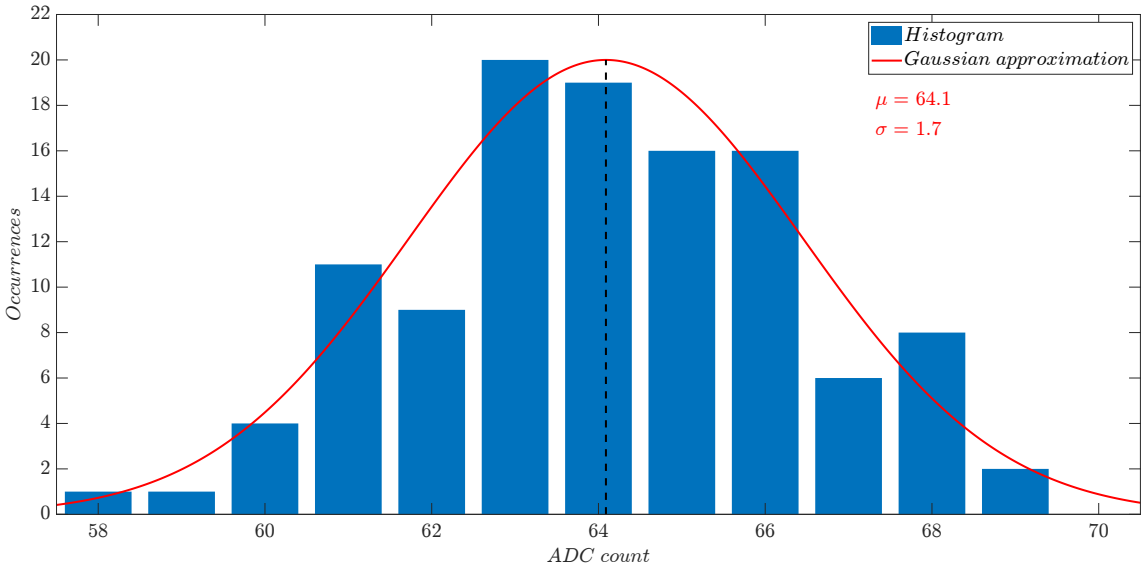
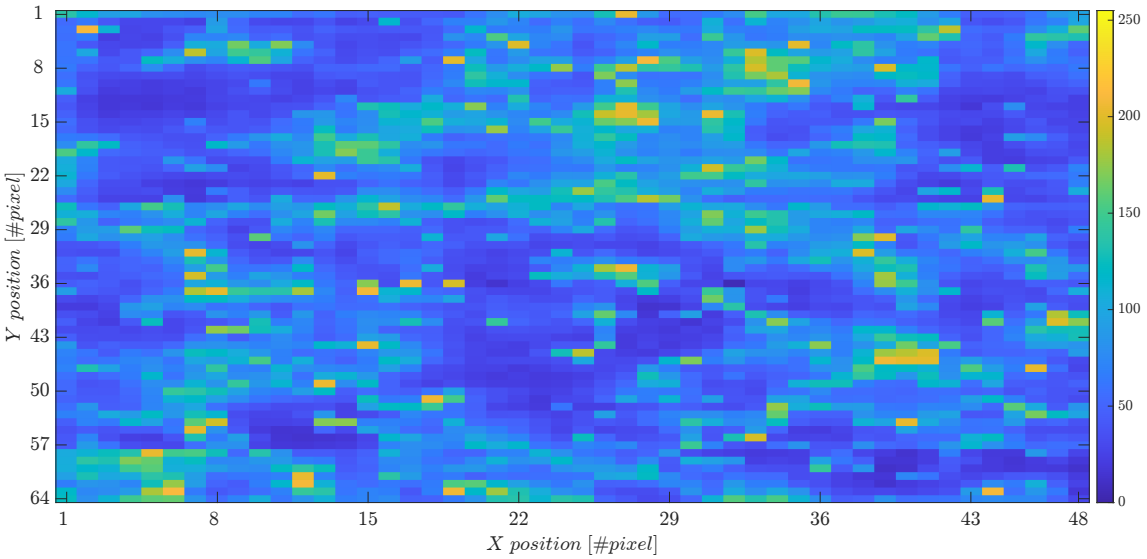


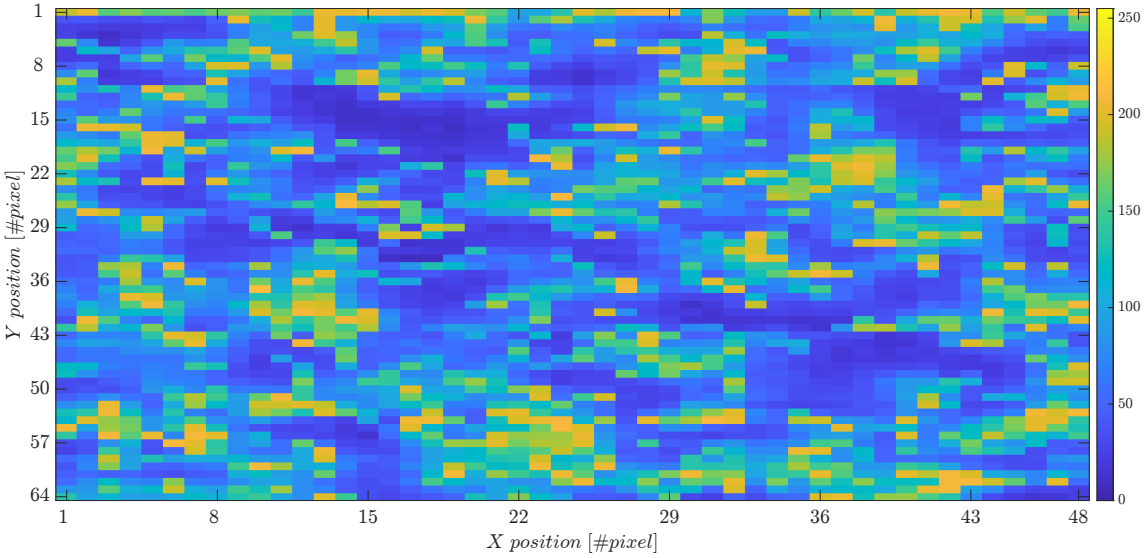
Figure 2.53: Noise of a single current pixel with HV = -40 V before TEM irradiation. Red line is the fitted Gaussian.

After finding the ratio between the number of electrons that hits the sensor and the number of electrons generated by e-gun, HV bias and beam current have been varied. Figure 2.54 shows a qualitative comparison of one frame for current pixels with HV -1 V and -40 V for a TEM current of 800 pA (which translates to $\sim 4.9 \cdot 10^4$ electrons hitting the matrix per frame). We can verify that when an electron hits a pixel it creates a bright spot (a lot of charge is generated in the silicon diode), however, the surrounding pixels also measure a charge larger than the baseline noise probably caused by charge sharing.

The intensity of the yellow color for the measurement with -40 V is higher than for the -1 V. This shows that the amount of charge acquired by the pixels increases as the reverse bias voltage decreases (as expected). If the intensity is translated to amount of electrons that hit the sensor (using the conversion factor in table 2.4), we obtain $\sim 3.5 \cdot 10^4$ electrons per frame for -1 V of bias voltage and $\sim 4.5 \cdot 10^4$ electrons per frame for -40 V of bias voltage.



(a) One frame of the current pixels matrix under the 650 pA electron beam with HV = -1 V.

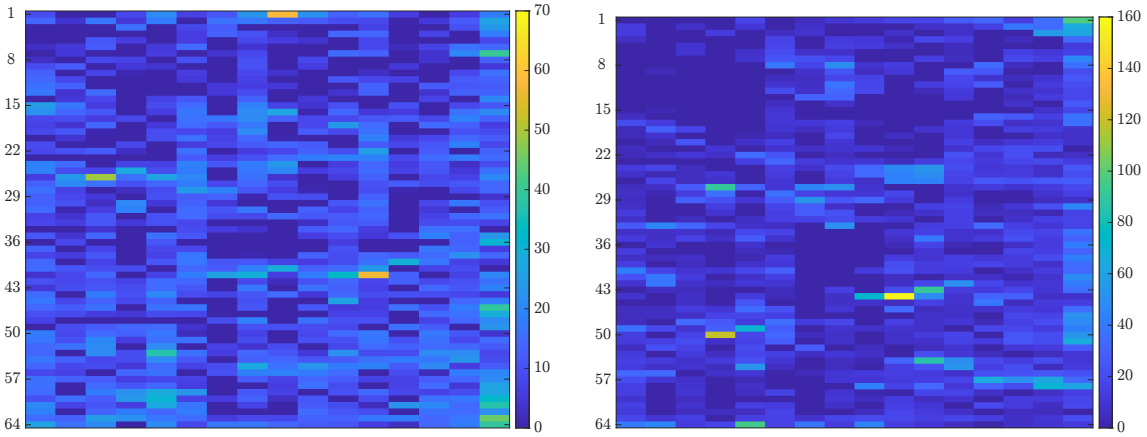


(b) One frame of the current pixels under the 650 pA electron beam with HV = -40 V.

Figure 2.54: Qualitative comparison of one frame of the matrix response for current pixels with HV = -1 V and -40 V.

Figure 2.55 shows the same comparison, for the same settings using voltage pixels. In this case, the intensity is less than it was for the current pixels, since the maximum value acquired does not exceed 70 and 200 ADC count for -1 V and -40 V respectively (was 250 for current pixels at both bias voltages). This verifies what was already discussed, the voltage pixels possess less gain compared to current pixels, however, both are able to detect electrons.

In the case of voltage pixels, it was expected $\sim 1.6 \cdot 10^4$ electrons hitting the matrix per frame. By converting the intensity of the matrix for one frame to number of electrons, we obtain $\sim 4.3 \cdot 10^3$ electrons per frame for -1 V of bias voltage and $\sim 1.2 \cdot 10^4$ electrons per frame for -40 V of bias voltage.



(a) One frame of the voltage pixels under the 230 pA electron beam with HV = -1 V.

(b) One frame of the voltage pixels under the 230 pA electron beam with HV = -40 V.

Figure 2.55: Qualitative comparison of one frame of the matrix response for voltage pixels with HV = -1 V and -40 V.

The leakage current of the sensor increases with the accumulated doses, for this reason, in between a change in beam current, a set of frames with the beam off was acquired to compute the baseline noise (figure 2.56). In the figure, a bight spot can be seen, those pixels were previously irradiated by an unknown dose while the beam was being set. The mean value across all the frames for each pixel is calculated. Later, the noise floor was subtracted from the irradiated frames. By performing this it is possible to make the measurement independent of the increased leakage current generated by radiation damage and makes it possible to compare the frames between different beam currents. However, this method does not compensate for noise.

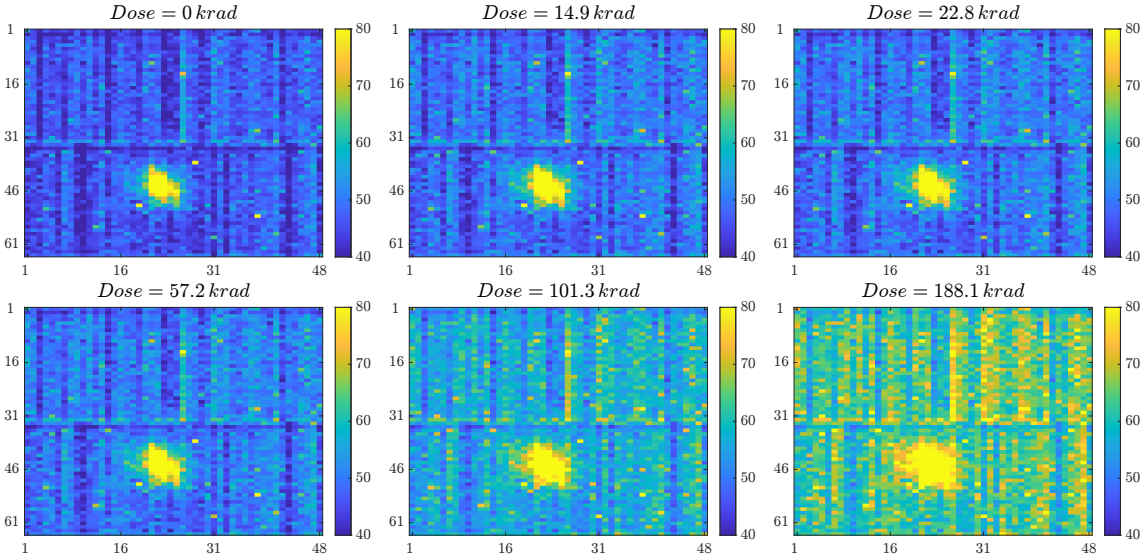
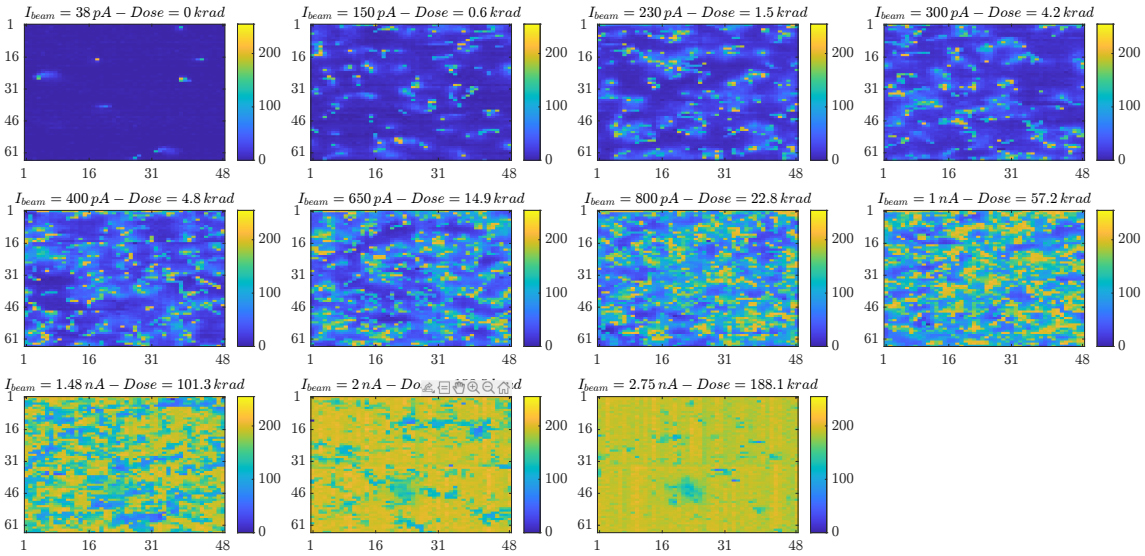
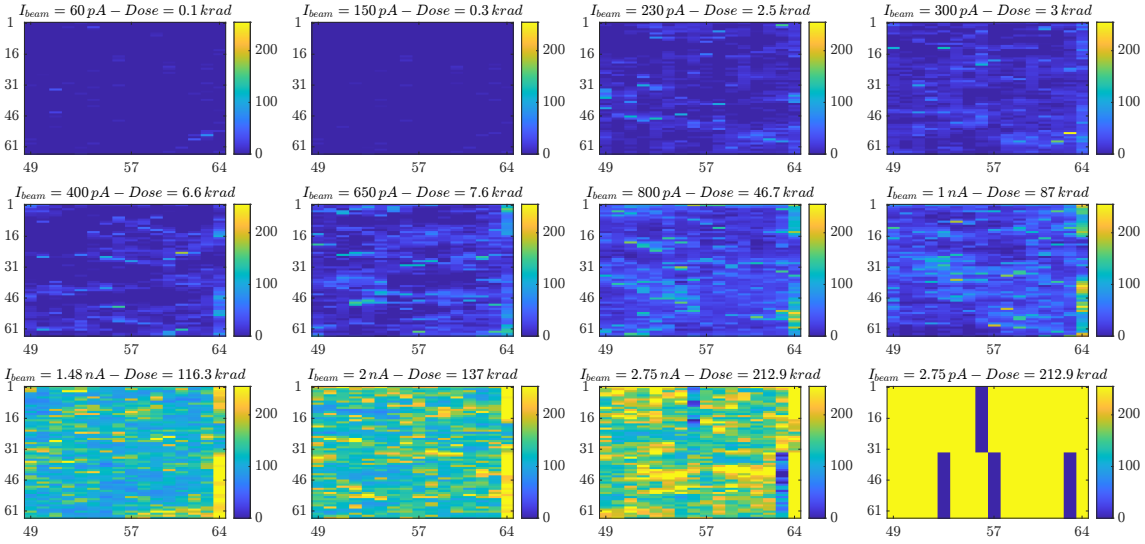


Figure 2.56: Mean value for each pixel across all frames for each dark measurement. X and Y axis correspond to pixel number (position). The bright spot corresponds to an error during set up of the beam, leading to a high intensity illumination of the matrix over the region while the sensor was not acquiring data.

As the beam current increases, it is expected to obtain frames with a higher density of pixels with bigger ADC values. In figure 2.57 a comparison of all the different beam currents used for a random frame at -40 V of current and voltage pixels is shown.



(a) Current pixels



(b) Voltage pixels

Figure 2.57: Random frame for each TEM beam current used with -40 V. The TID, as well as the TEM beam current for each measurement is displayed above each plot. X and Y axis correspond to pixel number (position).

The measurements of current and voltage pixels were done alternated. Almost at the end of the measurement (frame 774 of 812) of the voltage pixels with a beam current of 2.75 nA, the sensor stop working (figure 2.57 (b)). The pixels were either 0 or 255 ADU, suggesting that the digital circuitry failed. Since the last reliable measurement was the voltage pixel with 2.75 nA, the chip withstood at least ∼213 krad of TID.

2.8.2.2 Chip 2

The first chip stopped working after ∼213 krad TID across the whole chip area. I suspect that the periphery of the sensor was damaged and that led to the destruction of the sensor. Because of that, during the test of the second chip, the beam was focused only in the matrix. By doing this, the radiation over the periphery electronics is reduced.

For this sensor, only the current pixels were tested with -40 V of reverse bias. After the setup was placed, and the vacuum generated, with a low beam current, the electron beam

was focused to a spot of ∼550 µm to ∼1 mm (depending on the beam current intensity) and positioned over the matrix, trying to avoid irradiating the periphery electronics as much as possible.

Figure 2.58 shows one frame for each beam current, as well as the accumulated dose of the sensor up to that frame.

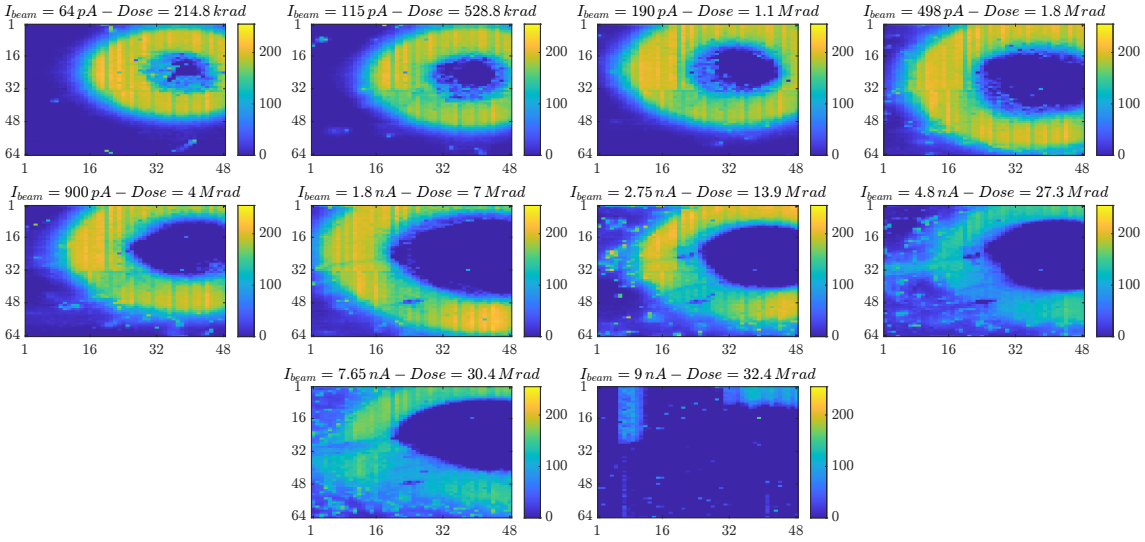


Figure 2.58: One random frame for each TEM beam current used for current pixels at -40 V, TID accumulated, as well as the TEM beam current for each measurement is displayed above each plot. X and Y axis correspond to pixel number (position).

All the plots in figure 2.58 were done by subtracting from the measurement the average pixel value when the beam was off before each increased beam current. Since the beam was focused, the pixels right under the spot acquired a high amount of charge, which leads to a higher damage (increased in leakage current) compared to other pixels on the periphery. In figure 2.59 the matrix when the beam was off after each iteration is shown. There is a bright spot where the beam is focused that shows the damage on the pixels.

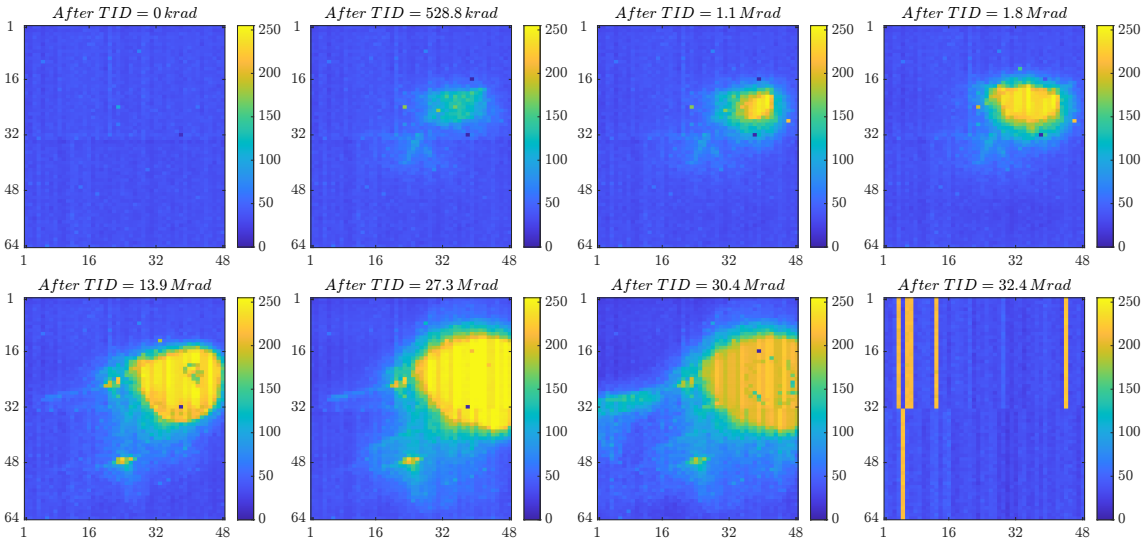


Figure 2.59: Average current pixel value across all frames for each measurement with electron beam off and -40 V bias voltage. Accumulated TID is displayed above each plot. X and Y axis correspond to pixel number (position).

For this chip, the total dose accumulated before the sensor stopped working was ∼30.4 Mrad, ∼140 times more than the first chip (section 2.8.2.1). This result shows that the matrix and its electronics inside can withstand more radiation than the periphery. However, it is not possible to determine exactly how much more radiation can the matrix tolerate, since there was not possible to focus the beam strictly over the matrix all the time, and because the spot is not perfect, there are scattered electrons that hit sensor outside the spot.

3 HINT chip for radiation detection in hadron therapy

Radiotherapy with heavy ionizing particles – such as protons and carbon ions – is an important method in the treatment of tumors. In contrast to x-ray and gamma radiation, ions deposit their energy in a small tissue layer, this effect is called Bragg peak [28, 2]. This is one of the key advantages of this type of cancer treatment [6]. To benefit from this effect, it is necessary to generate a narrow beam with precise direction, intensity, and energy [82]. If all these parameters are precisely adjusted, most of the beam energy will be deposited within the tumor tissue and not in the surrounding healthy cells. A beam monitor should provide dose, position, and spot size information.

During patient irradiation, the beam should be monitored all the time, to ensure the dose delivered and the position of the beam is correct. To perform these measurements ionization chambers and silicon detectors are utilized [74]. There are new technologies being studied, such as flexible organic thin-film [25]. The silicon sensor presented in this chapter is the first version of its kind and was designed with a monolithic HV-CMOS technology.

In this chapter, the whole system will be discussed, starting from the sensor itself (sections 3.1 to 3.4). The relevant parts of the FPGA firmware and software designed to control and to read out the chip are also discussed. Finally, in section 3.5 all the measurements carried out to validate the sensor will be presented, that includes calibration and testing measurements as well as results of test beam measurements.

3.1 Architecture

In modern radiotherapy centers for cancer treatment, like the Heidelberg Ion-Beam Therapy Center, Germany[1], the use of protons or carbons allows for sub-millimeter precision in dose deposition [35]. Because of this, the Heidelberg Ion-Beam Therapy Center Integrating Chip (HINT) has a pixel matrix of 24×24 pixels with a pixel size of 200 µm. The final beam monitor should cover an area of 25×25 cm^2, this can be implemented by a matrix of chips. The insensitive periphery should be as small as possible and part of the electronics can be placed inside the pixels. Since the sensor is done in HV-CMOS process, the fill factor can be 100%.

The HINT has a total area of 4.8 mm × 5.1 mm and was submitted in 2020 in two different versions. The position of each sensor type in the reticle is shown in figure 3.1. The technology used was 180 nm HV-CMOS, which is capable of handling high voltages up to 120 V.

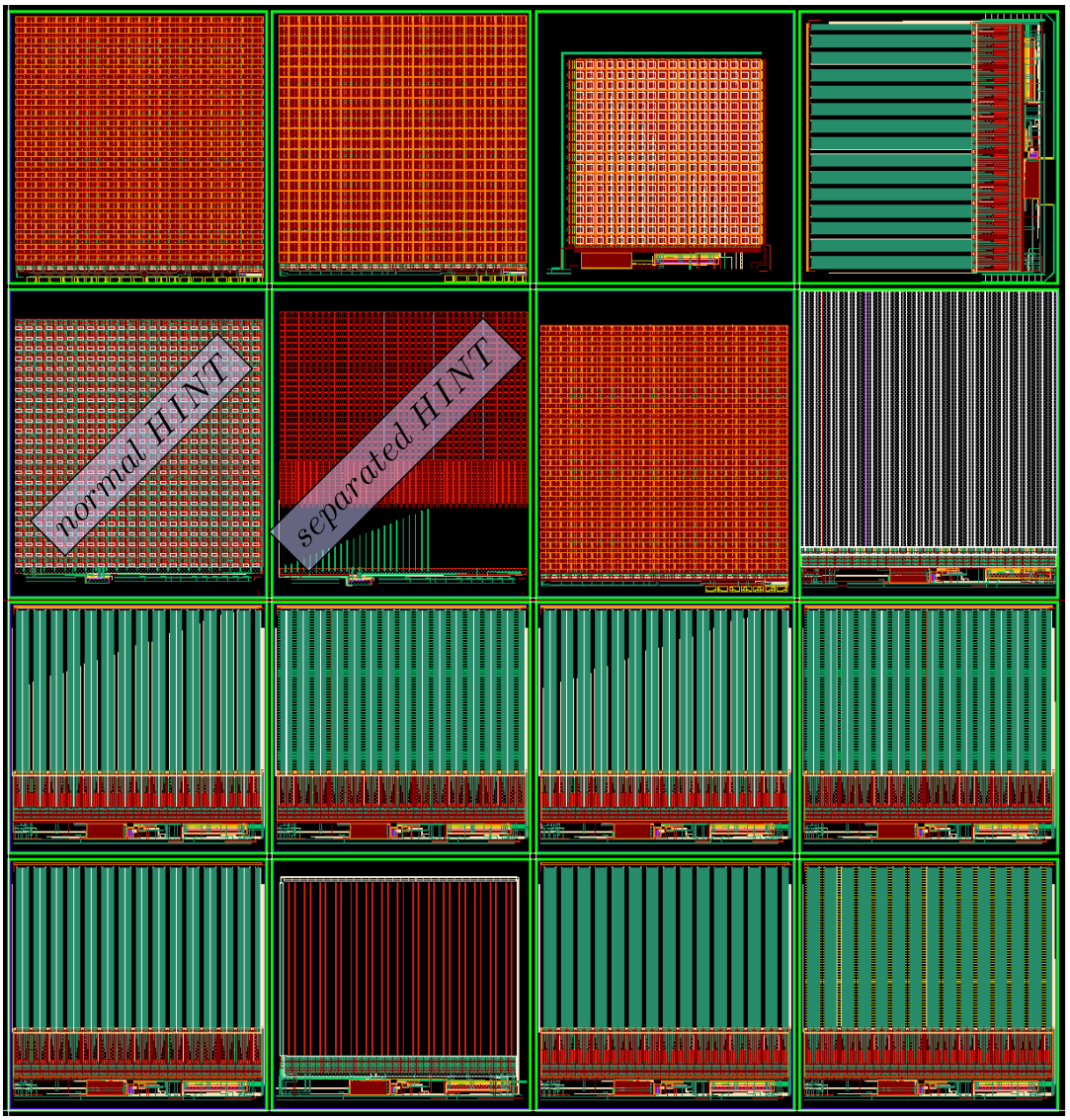


Figure 3.1: Layout of the full reticle for the 2020 year engineering run and the position of the normal and separated HINT.

[1] https://www.klinikum.uni-heidelberg.de/interdisziplinaere-zentren/heidelberger-ionenstrahl-therapiezentrum-hit

The first type of sensor is called “normal”, and it consists of a matrix of 24×24 square pixels with a side length of 200 µm. Part of the electronics is placed inside the sensitive area of the pixel (figure 3.2).

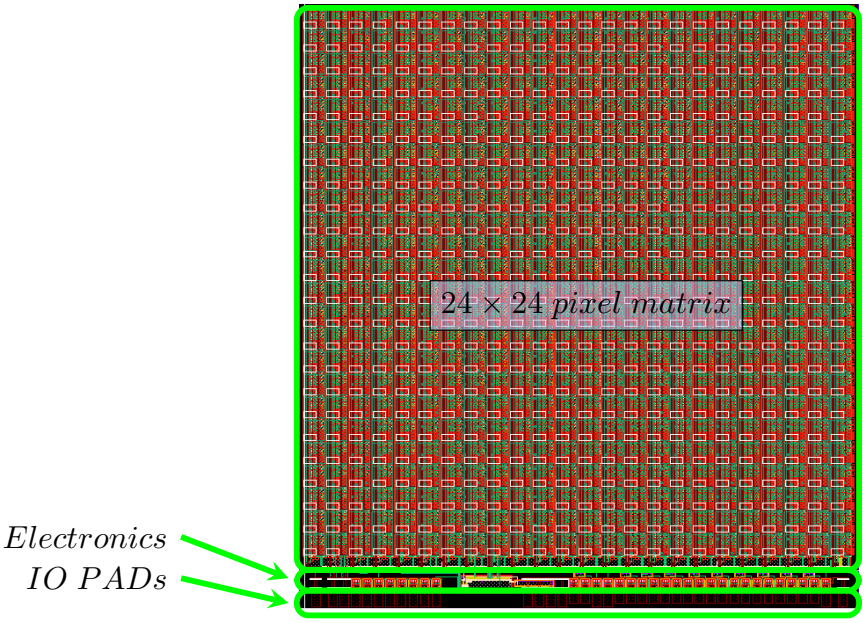


Figure 3.2: Layout of the normal HINT sensor with the main parts (matrix, periphery electronics, and pads) highlighted.

The second topology is called “separated” because the pixels do not contain electronics. The matrix contains 24×40 square pixels with a side length of 120 µm. All the electronics are placed at the bottom of the chip (figure 3.3).

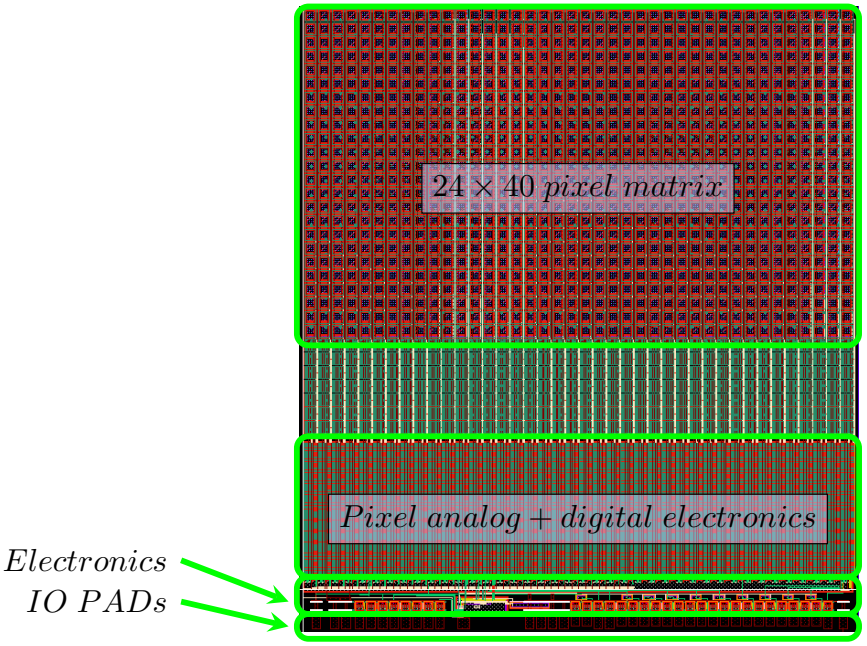


Figure 3.3: Layout of the separated HINT sensor with the main parts (matrix, pixel electronics, periphery electronics, and pads) highlighted, the area between the matrix and the pixel electronics is filled with test diodes.

Some properties of the HINT sensor are listed in table 3.1.

Table 3.1: Properties of both HINT sensors.

HINT normal	**HINT separated**
Pixel size of 200 µm × 200 µm	Pixel size of 120 µm × 120 µm
matrix of 24 rows by 24 columns	Matrix of 24 rows by 40 columns
Analog and digital processing of the sensor current inside pixel area	Analog and digital processing of the sensor current outside pixel area

The chip consists of several blocks, divided into two categories, the sensor with the electronics for signal acquisition and digitizing, and the control electronics. The integrator integrates the charge acquired by the diode and the voltage at its output increases. When this voltage surpasses a threshold, the comparator flips its output, which triggers the digital signal controller that subtracts a defined amount of charge from the integrator input, and thus decreases the integrator output voltage below the threshold. After the integration time ends, the stored number of times that charge was pumped and time-stamp values are read out. At the same time, the row control works as a shift register to output the data of each pixel at each column.

The schematic of each type of sensor (normal and separated HINT) is shown in figure 3.4 and figure 3.5. It can be seen that the normal HINT has the analog and the digitalization part (A+D) inside the diode. In the case of the sensor with the separated diode, electronics are physically separated from the pixel matrix.

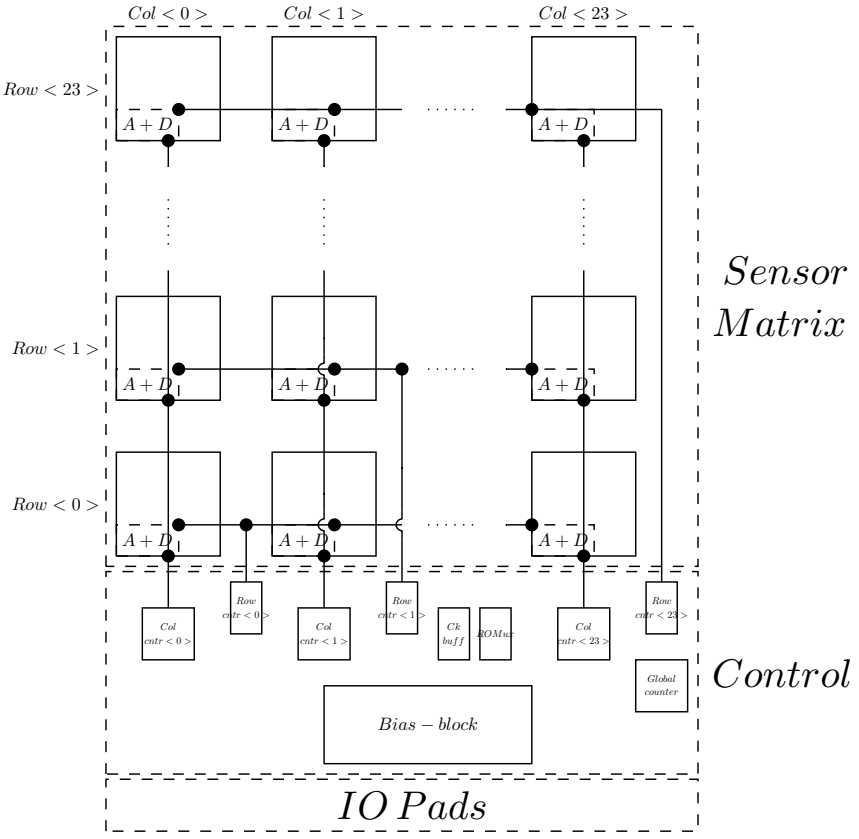


Figure 3.4: Block diagram of normal HINT, the *A+D* block is placed inside each pixel while the rest of the electronics is at the bottom, as well as the input/output pads.

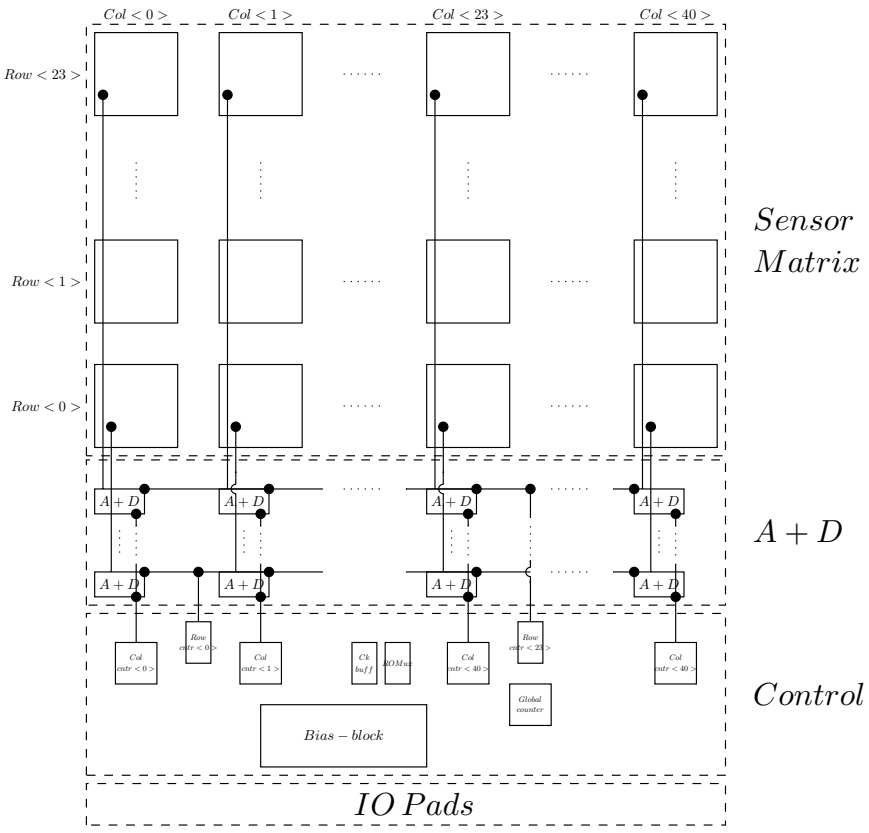


Figure 3.5: Block diagram of separated HINT, the *A+D* of each pixel is placed at the lower edge of the chip, as well as the rest of the electronics, and the input/output pads.

Further in this chapter, the separated HINT will be used as an example. All the descriptions applied for both flavors, if not, the differences will be pointed out.

3.2 The pixel

The sensor is implemented as a deep n-well in a p-substrate diode that can sustain a bias voltage of up to 120 V, which in addition to higher substrate resistivity, creates a thicker depletion region [62, 75], where the particle can generate charge [38]. Thanks to this technology, it is possible to achieve 100% fill factor, since the *pmos* transistors are isolated from the n-well by a *deep p-well* layer. An schematic cross-section of the pixel is shown in figure 3.6

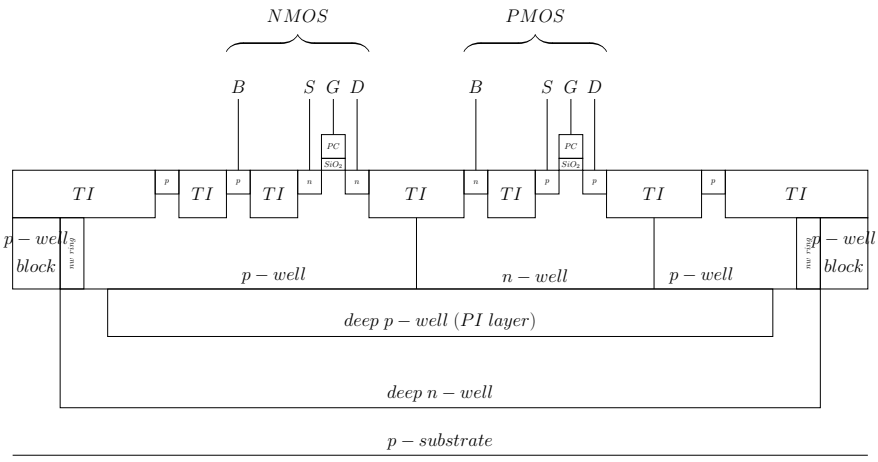


Figure 3.6: Cross-section schematic of the normal HINT pixel.

Figure 3.7 shows the layout of a normal pixel and the analog and digital parts inside. A block diagram of the pixel is shown in figure 3.8

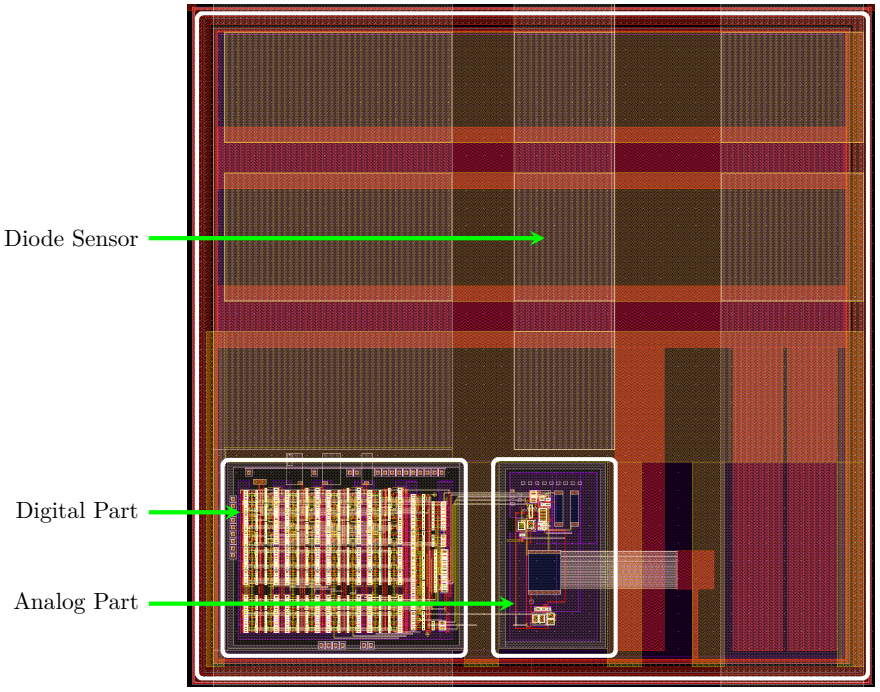


Figure 3.7: Layout of a normal pixel where each part (the diode, analog, and digital part) are highlighted.

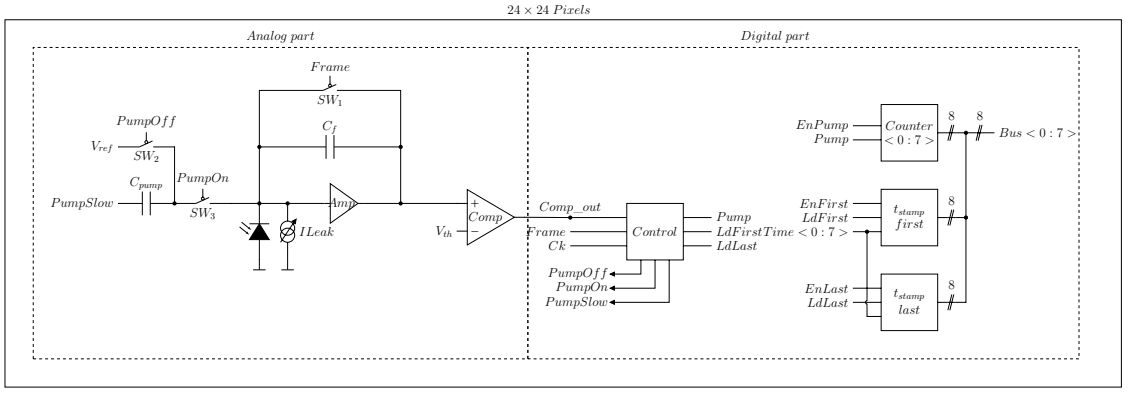


Figure 3.8: Simplified schematic of the pixel sensor with the analog (left) and digital (right) part.

As shown in figure 3.7 the pixel consists of three parts, analog, digital, and sensor diode. The sensor diode (deep n-well in p-type substrate [62]) is connected to the input of the amplifier. The amplifier is implemented as an active load amplifier with cascode [59].

When a particle hits the sensor (diode), it will generate charge [38], that will migrate by drift from the depletion region into the n-well and then into the integrator and will be stored in the capacitor C_f. When several particles arrive, the output of the integrator will appear as a positive ramp. Then, it will be compared to a voltage threshold, set externally. The output of the comparator will change from 0 V to *Vdd* when the integrator voltage exceeds V_{Th}. As long as the comparator output is "0", SW_2 will be close, which will set the capacitor voltage to V_{ref}. Every time the comparator output flips to "1", a short pulse *PumpOff* will be generated, and SW_2 will open while SW_3 closes. With this, the capacitor C_{pump} will be directly connected to the input of the integrator and will subtract a precise amount of charge into the integrator.

The digital part is shown in figure 3.8, it consists of a *Control* block, an 8-bit *Counter*, which counts every pulse generated by the comparator, and two time stamp blocks (t_{stamp} *first* and t_{stamp} *last*). The signal *Time* is generated inside the chip by an 8-bit counter. The *Bus* line is used for transmission and will send the number of *Pump* signals, and the time stamp value of the first and last *Pump*.

The pixel has an 8-bit bus output. Using this bus, the 8-bit time stamps of the first and last pump, as well as the 8-bit number of pumps, are sent to the periphery of the chip. As it will be explained further in this section, using the information about the number of pumps present during integration time, and the time stamps, the precise amount of charge generated by the particles can be calculated. Such time-stamp pump measurement extends the dynamic range of the integrator. The time stamp facilitates an increase in resolution, while the pump gives a wider measurement range. Therefore, the effective resolution of the sensor is 16-bit.

3.2.1 Sensing method

This sensor works by integrating the charge generated by charged particles in the sensitive area. Every time a particle hits the silicon, electron-hole pairs are generated and, by drift [38] the electrons will be collected at the input of the integrator. As more high energy particles pass through the sensor, more charge is integrated, and the voltage at the output of the amplifier increases. Because the output of the amplifier is connected to the non-inverting input of the comparator, while the inverting input is set to a constant voltage value V_{th}, when enough particles hit the chip, the comparator output will become

logic "1". Figure 3.9 presents a schematic of the integrator and comparator, figure 3.10 shows an example diagram of all the relevant waveforms during a frame.

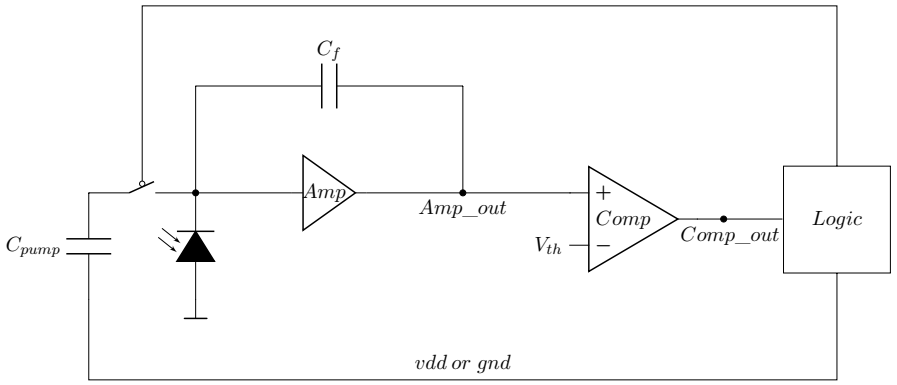


Figure 3.9: Simplified schematic of integrator and comparator, the analog part of the pixel sensor.

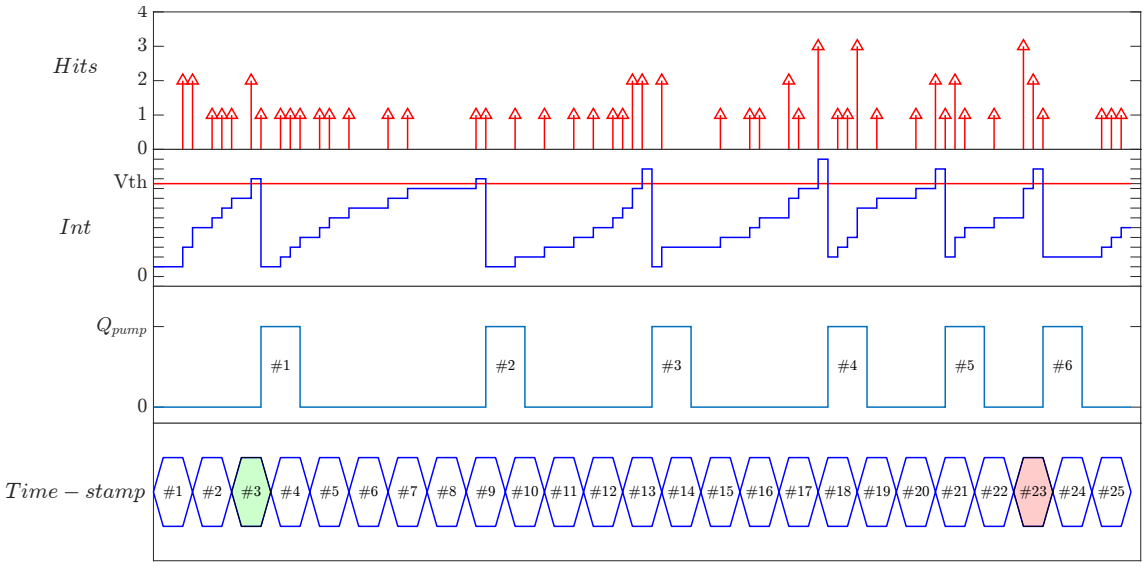


Figure 3.10: Relevant waveforms of the sensing method. Every time there is a hit (red arrow on top plot), the voltage of the integrator increases until it reaches the voltage threshold (V_{th}) of the comparator. At that moment, the *Pump* circuitry will generate a *Pump* pulse, which will be counted. The bottom plot shows the time-stamp counter, when the first *Pump* inside a frame appears, the value of the time-stamp is stored (in green). The same happens when the last *Pump* inside the integration time is present, the value of the counter is stored as the last time-stamp (pink colored).

When the comparator's output flip to "1", the digital logic extracts a precise amount of charge (C_{pump}*Vdd) out of the integrator, which in turn will lower the voltage output of the amplifier, flipping to "0" the output of the comparator.

3.2.2 Analog part of the pixel

The input charge can be measured if we know how many times the integrator output exceeds the voltage threshold as well as the first and last time that this occurs. That is why on each pixel, a digital part contains an 8-bit *Pump* counter, and the logic to store

the 8-bit time-stamp of the first and the last *Pump*. Those three values are sent to the peripheral logic via the 8-bit bus line.

The measurement works only if there are at least two pump signals during the integration time. To ensure this, a leakage current source has been made and can be controlled by on-chip DAC.

Figure 3.11 shows the leakage current source. Normally, a current source is made with one PMOS or NMOS, depending on the current polarity needed [75]. This leakage current source, however, has to generate a very small current, in the range of pA. If a single NMOS is used, the gate voltage would be very low (sub-threshold working point [65]). Then, the current would be very sensitive to local ground level or threshold mismatch [65]. This is why an extra transistor (p_1) was added at the source of the main transistor. This adds extra source resistance and voltage so that the *VNLeak* to ground difference is higher. In this way, the current source is less sensitive to variations (voltage ground level changes) and small currents can be generated.

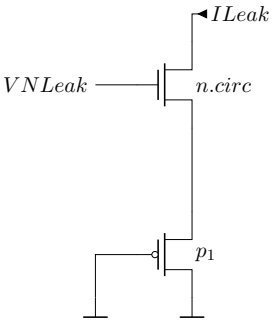


Figure 3.11: Transistor level schematic of leakage current source that produces small currents to inject to pixel analogue electronics.

In figure 3.11, *n.circ* is an NMOS circular (or enclosed) transistor. Because of this, the current source has a high radiation tolerance [76]. The PMOS is a normal one because they are inherently radiation tolerant [11, 12]. The voltage *VNLeak* to set the current is generated on the chip periphery.

In order to conduct a measurement as explained in section 3.2.1, it is necessary to know the amount of the charge that is pumped into the integrator. When a pump pulse is sent to the integrator, the amount of charge that is subtracted from the integrator is equal to:

$$Q_{pump} = Vdd \times C_{pump} \tag{3.1}$$

By design, $C_{pump} = 6.74$ fF, thus $Q_{pump} = 12.132$ fC. The average current that flows into integrator is calculated as:

$$I_{dark} = \frac{Q_{pump}}{\frac{(T_{last} - T_{first})T_0}{N_{pump\_dark} - 1}} \tag{3.2}$$

Where

Q_{pump} :	pumped charge
t_{last} :	time-stamp 8-bit value counter of the last pump
t_{first} :	time-stamp 8-bit value counter of the first pump
T_0 :	period of the LSB (least significant bit) bit of time-stamp counter
N_{pump_dark} :	number of pumps counted without irradiation

If we know the leakage current I_{dark}, it is possible to measure the amount of charge injected by particle hits, using the following formula:

$$Q_{total} = Q_{hit} + Q_{dark}$$
$$Q_{hit} = Q_{total} - Q_{dark}$$
$$Q_{hit} = (N-1)Q_{pump} - \frac{(N_{pump\_dark} - 1)\, Q_{pump}}{\Delta T_{dark} T_0} \Delta T_{hit}\, T_0$$
$$Q_{hit} = Q_{pump} \left[(N-1) - (N_{pump\_dark} - 1) \frac{\Delta T_{hit}}{\Delta T_{dark}} \right] \tag{3.3}$$

Where

Q_{total} :	total charge acquired during the irradiation
Q_{hit} :	charge generated only by the particle hits
Q_{dark} :	charge acquired because of leakage current
N :	number of pumps countered during irradiation
Δt_{dark} :	t_{last} - t_{first} measurement without irradiation
Δt_{hit} :	t_{last} - t_{first} measurement during irradiation

The amplifier from figure 3.12, together with the feedback capacitance C_f, forms an integrator [75] with a reset controlled by the signal *Frame*, which opens and closes the switch SW_1 in parallel to C_f. The signal *Frame* is generated by the FPGA.

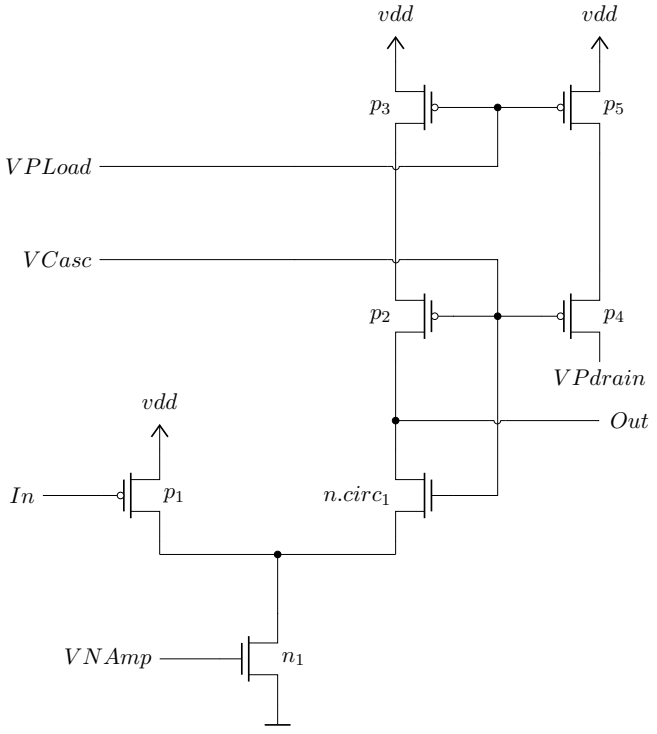


Figure 3.12: Transistor level schematic of the amplifier used as integrator.

The comparator has a Two-Stage Open-Loop topology, where the output of the differential amplifier is connected to the source follower (p_3 and $n.circ_4$) stage. With the logic after the comparator, several control signals will be generated, some of them (*PumpOn*,

PumpOff, and *PumpSlow*) will be used to control the charge subtraction into the integrator through C_{pump}.

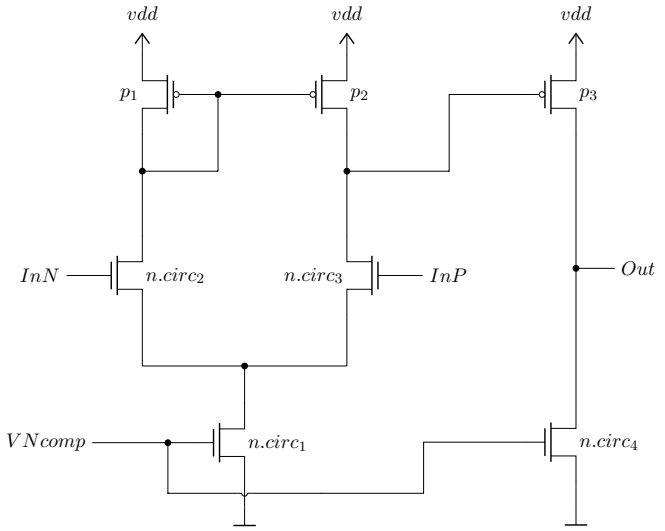


Figure 3.13: Transistor level schematic of the comparator.

The signals *PumpOn*, *PumpOff*, and *PumpSlow* are generated by the *Control* block, which will be discussed further in this chapter.

3.2.3 Digital

The digital part implemented in-pixel starts after the comparator output shown in figure 3.8. The pulse generated by the comparator is stored on a D-latch. The signals *Pump* and *LdFirst* are generated in the digital part (figure 3.14).

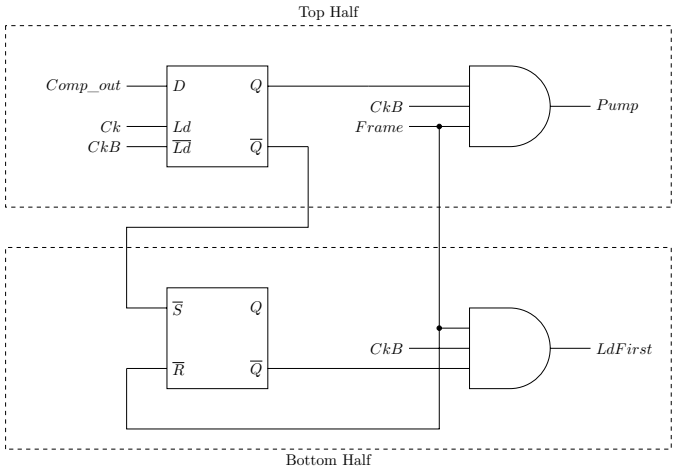


Figure 3.14: Schematic of digital control that produces the *Pump* and *LdFirst* signals.

LdFirst is equal to the signal *CkB* as long as *Frame* is on and there was not a previous comparator pulse during the time frame. As soon as *Comp_out* registers a pulse, the *LdFirst* signal will be "0", until the latch is reset by a new frame.

The circuit at the top half of figure 3.14 generates *Pump* (a pulse that follows the threshold crossing of the integrator output), a pulse in phase with *CkB* will be generated, as long *Comp_out* is on. Figure 3.15 shows waveform signals explained before.

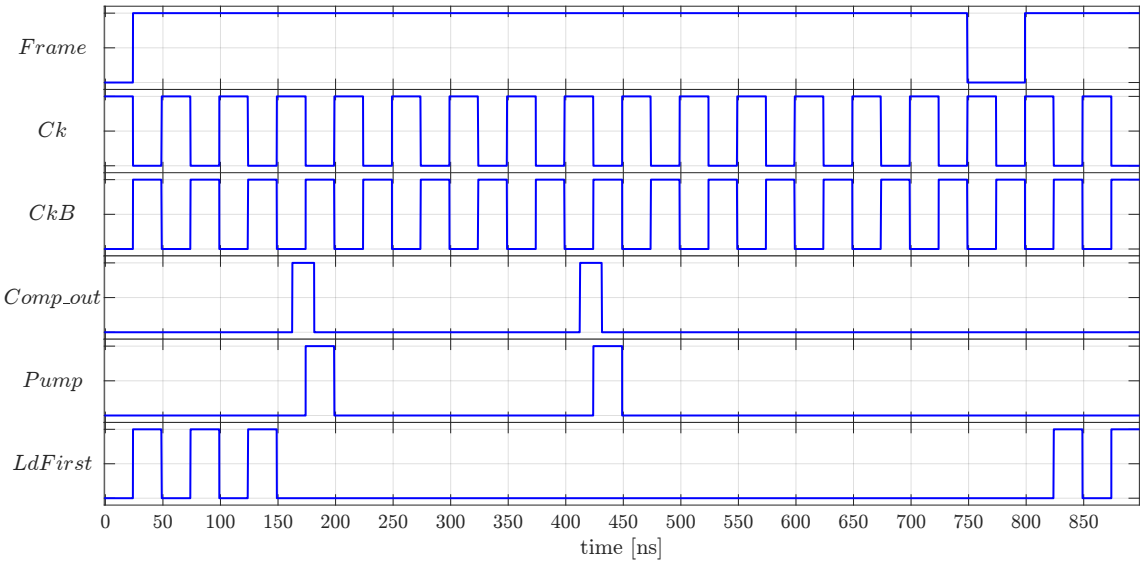


Figure 3.15: Signals that generate *Pump* and *LdFirs* plotted as function of time.

As soon as comparator output exceeds the threshold, it is necessary to discharge the integrator, to be able to continue acquiring charge and not saturate the amplifier. In order to discharge the integrator, beside the already mentioned *Pump*, it is necessary to generate three extra signals, *PumpOff*, *PumpOn*, and *PumpSlow*.

PumpOff is buffered of *Pump* and it drives SW_2 on figure 3.8. This switch will set the voltage of the pump capacitor C_{pump} to V_{ref} (figure 3.8).

PumpOn is inverted *Pump*, this signal will connect C_{pump} and the integrator input.

PumpSlow is delayed *PumpOn* (figure 3.16)

To generate the delay on *PumpSlow*, a current starved inverted [56] is used (figure 3.16). The value of the delay is controlled by transistors *p.2* and *n.2*, both of which are the current source part of a current mirror, where the corresponding diode transistors are placed in the Bias-block, at the periphery of the chip. This delay ranges from 6.4 ns to 377 ps.

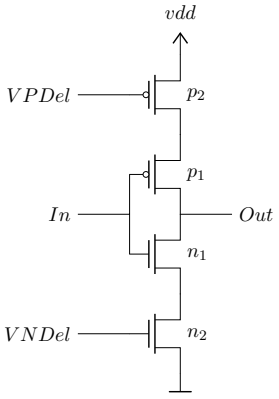


Figure 3.16: Transistor level schematic of the delay block implemented.

The last block of the digital part inside the pixel contains a counter for *Pump* pulses that occurred during the integration time (figure 3.17), a register to store the value of the time-stamp when the first *Pump* appears (figure 3.19), and another register for the time-stamp of the last *Pump* present during frame.

The pump counter is an 8-bit wide, ripple type counter, with a *Reset* signal to reset the value of the bits to "0", and an extra D-latch to store the digital value until the signal *EnBusPump* enables the inverter logic gate.

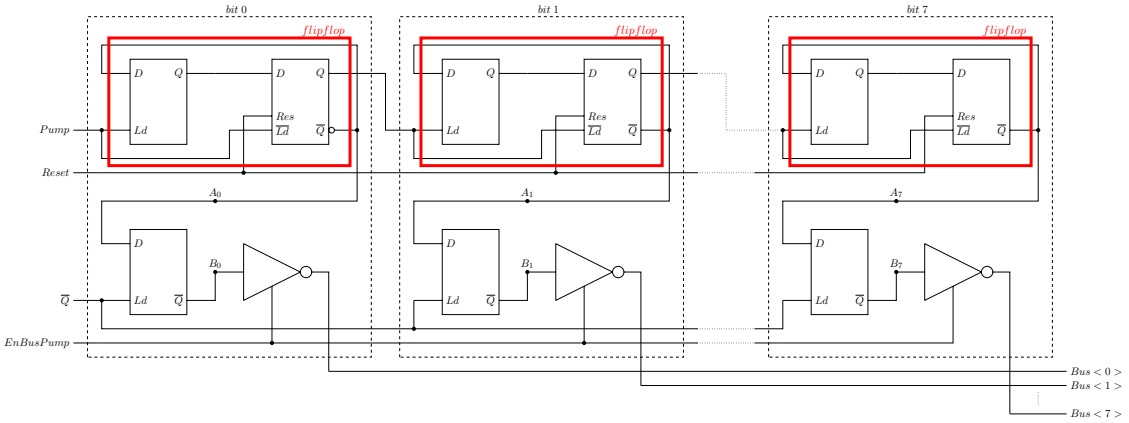


Figure 3.17: Logic schematic of the pump counter designed for HINT.

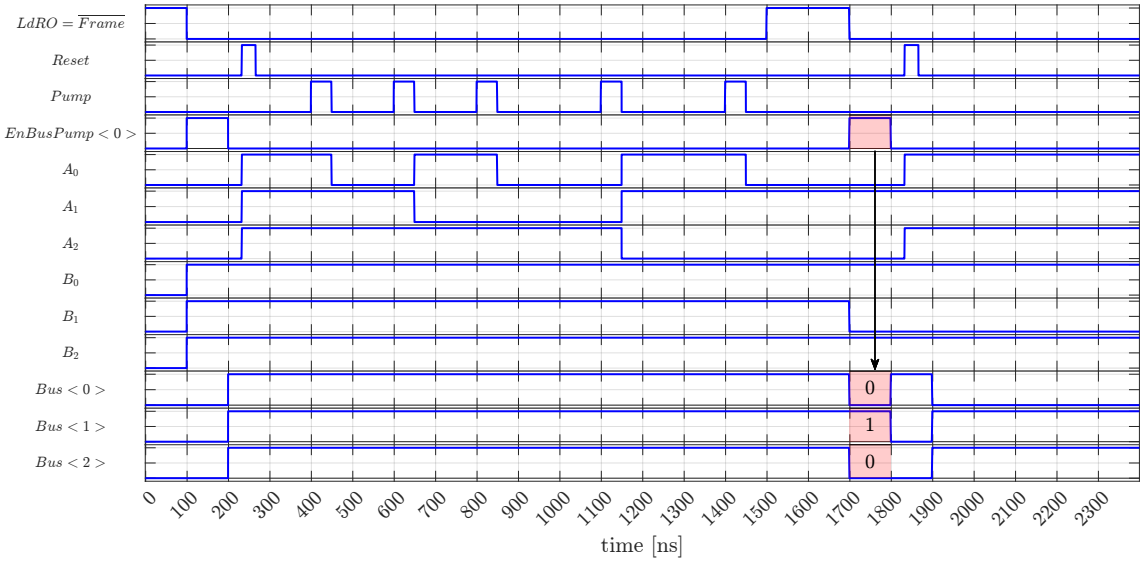


Figure 3.18: Example of pump counter waveform and all the relevant signals as a function of time. When *EnBusPump*<0> is on, the value of *Pump* counter is present in the bus.

Figure 3.18 shows the waveforms for a system with a 3-bit wide bus when five pumps are detected. In this example, the output $Bus<0:2>$ is equal to 010 which translates into the number 2. Because the clock signal of each subsequent bit block on figure 3.17 is connected to Q instead of $\overline{Q}$ this counter counts backwards. In order to obtain the correct output value, it is needed to negate the $Bus<0:2>$ which will result in the number 101, or 5 in decimal base.

The register of the time-stamp when the first pump occurs consists of eight D-latches that store the 8-bit wide *Time* value when the signal *LdFirst* has positive edge. As explained before, *LdFirst* signal will be disabled when the first *Pump* is detected, in this way, the first D-latch will store the value of the *Time* counter at the moment the first *Pump* arrives. When the time frame ends (*LdRO* signal), the value stored in the first D-Latch (figure 3.19) will then be stored in the following D-latch, until readout via *Bus*.

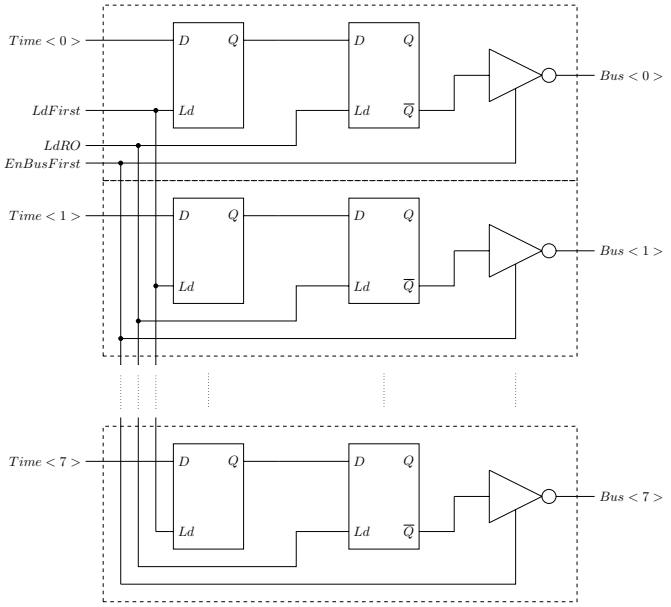


Figure 3.19: Schematic of the register for the time-stamp of the first pump.

An example waveform is shown in figure 3.20. It can be seen that when the last pulse of *LdFirst* appears, the value of *Time*$<0:2>$ is 001. After the frame finish, when the signal *EnBusFirst*$<0>$ is on, the value present at *Bus*$<0:2>$ is the time stamp of the first pump.

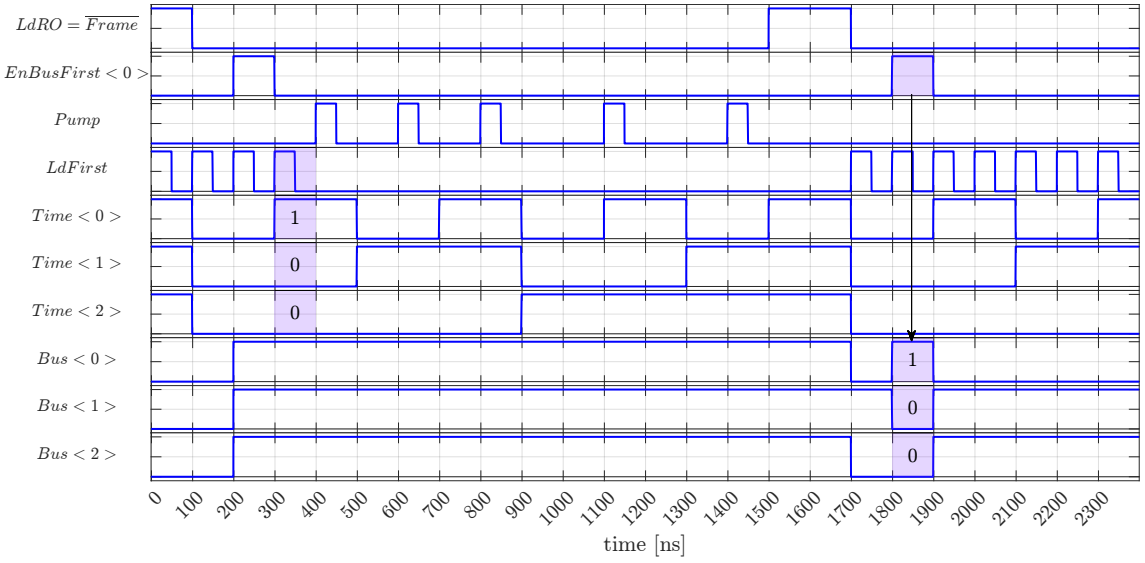


Figure 3.20: Example waveform. During a frame (*LdRO* is "0"), when the last pulse of *LdFirst* happens, the value of the *Time* counter is saved.

The register of the time-stamp for last pump is similar to the first time-stamp, but in this case, the value of the 8-bit signal *Time* will be stored every time a *Pump* occurs, and when the time frame ends, this value will copied in the second D-latch.

An example of the functioning of the time-stamp is shown in figure 3.21, where only the first three bits of the *Time* counter and *Bus* are plotted. When the last pulse of *Pump* appears, the value of *Time*$<0:2>$ is 110, after the frame finish, when the signal *EnBusLast*$<0>$ is on, the value present at *Bus*$<0:2>$ is the time stamp of the first pump.

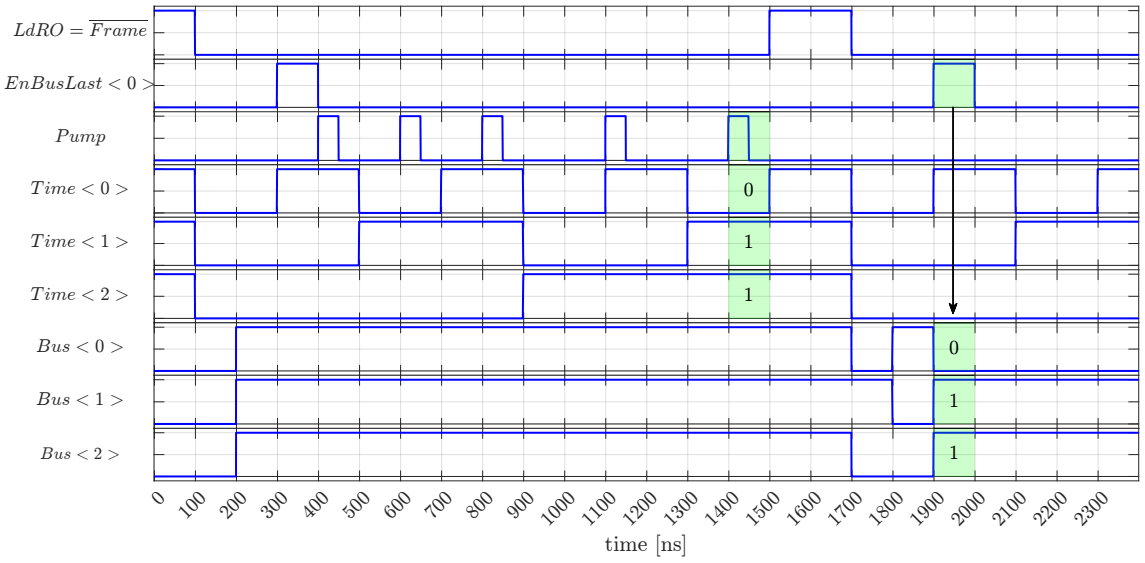
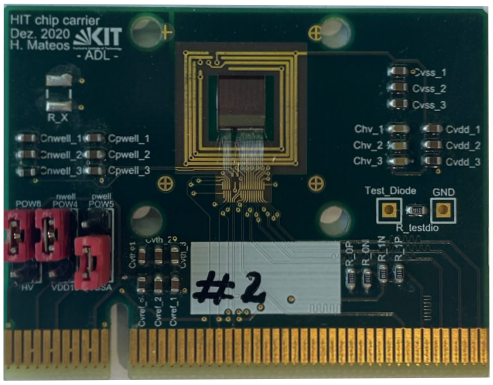


Figure 3.21: Example of time stamp register for the last pump as a function of time. During a frame (*LdRO* is "0"), when the last pulse of *LdLast* happens, the value of the *Time* counter is saved. Later, when *EnBusLast<0>* presents a pulse, the data stored is present at the output bus.

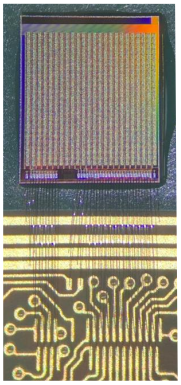
The stored data in the pixels are read out using an 8-bit bus. The signals *EnBusPump*, *EnBusFirst*, and *EnBusLast* control the data transfer via the bus. These three signals are generated in the periphery.

3.3 GECCO interface

The sensor was glued to a PCB (printed circuit board) on which it will be wire bonded. The PCB shown in figure 3.22(a), was designed to fit this chip, and to be connected via PCI (peripheral component interconnect) to the GECCO-board [22]. A detailed diagram of the placement and dimensions of the pads is presented in appendix B, as well as a list of each pad and their function.



(a) PCB carrier with HINT sensor bonded.



(b) Close up of the chip glued and wire bonded to the PCB carrier.

Figure 3.22: HINT sensor chip glued and wire bonded to the PCB carrier. (a) shows the whole PCB and the sensor, while (b) shows only the sensor area and the pads on which the wire bonds are bonded onto the PCB.

The GECCO-board (figure 3.23) acts as an interface between the sensor and the FPGA. This PCB routes the signals between FPGA and chip, and provides the power

voltages. It also has slots for cards that generate voltages *Vth* and *RefIn* (to set V_{Th} and *RefIn*) and injection pulses (used for test and characterization of the sensor, explained in section 3.5). The board has a PCI-express type connector to plug the chip carrier as well as the cards while using an FMC type connector to connect to the Nexys Video FPGA [20].

Figure 3.23: GECCO-board used to communicate the HINT sensor with the FPGA.

3.4 Software control

The last link of the chain to control and use the sensor is the software implemented in the PC. It is based on the Qt software developed by F. Ehrler and R. Schimassek [22, 70] to use in combination with the GECCO-board. This interface was designed in C++ using the Qt framework. It was modified by the author to fit the needs of the HINT sensor.

The interface generates signals for chip configuration (see appendix B.1). The software also allows the user to control the chip, as well as to show in real time the output of the matrix as a frame-by-frame image and a compounding histogram. This software will save the data sent by the sensor. If the USB connection is used, the data will be saved as a text file containing the *pump*, time-stamp *first* and *last*, as well as the configuration DAC values to later analyze the measurements. On the other hand, if the communication is done via ethernet (much faster than USB), the information is stored as a binary file.

Figure 3.24 shows a screenshot of the software interface with all the components above described.

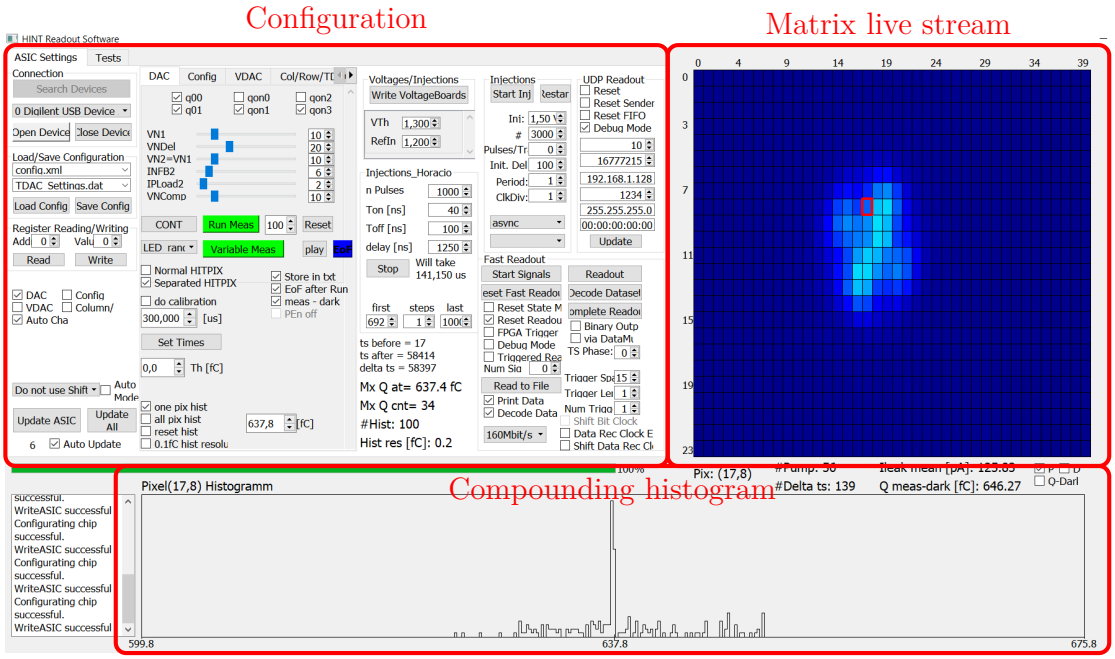


Figure 3.24: Qt software interface, with the three main parts. The part "Configuration" is where all the configurable parameters are set and the start and stop of the measurements can be done. Matrix live stream displays the value of the matrix sensor as the data is received by the computer. The compounding histogram shows the histogram of the data for the whole matrix, or a single pixel, as the data is received by the PC.

3.5 Characterization

In section 3.5.1 the results of tests performed in the laboratory are presented. The aim of these measurements is to characterize the behavior of the chip. Furthermore, it is needed to find the optimal values for some of the parameters, such as the polarization of the substrate with high voltage, leakage current, and integration time.

Section 3.5.2 presents the results of the measurements carried out at the Heidelberg Ion-beam Therapy center (HIT)[2]. There, the sensor, has been tested with both proton and carbon ion beams of different energies and intensities to investigate the behavior under the conditions that the ASIC has been designed for.

3.5.1 Laboratory measurements

Characterization measurements were performed, to verify that the values fabricated in the sensor are accurate compared to the design, and to characterize the behavior of the sensor and find the optimal parameters to use the sensor.

3.5.1.1 Leakage current

The first measurement performed was the verification of the leakage current source designed (section 3.2.2). This current source needs to generate small currents, and for that a divider of 65536 is implemented in several current mirror stages. This can lead to an increased error in the current compared to the design.

[2] https://www.klinikum.uni-heidelberg.de/interdisziplinaere-zentren/heidelberger-ionenstrahl-therapiezentrum-hit

To perform this measurement, we assume that the capacitors C_{inj} and C_{pump} are as designed. A reasonable assumption, since those capacitors were made in metal layers and the 3σ tolerance according to manufacturer is around 12%. The sensor was placed in an obscure environment, and a set of 100 frames were acquired for each different value of the 6-bit DAC register *INFB2* (appendix B.1.6). By plotting the measured current (according to formula 3.2) as a function of the 6-bit DAC value, and performing a linear regression, the linearity of the current source is verified and its resolution (figure 3.25).

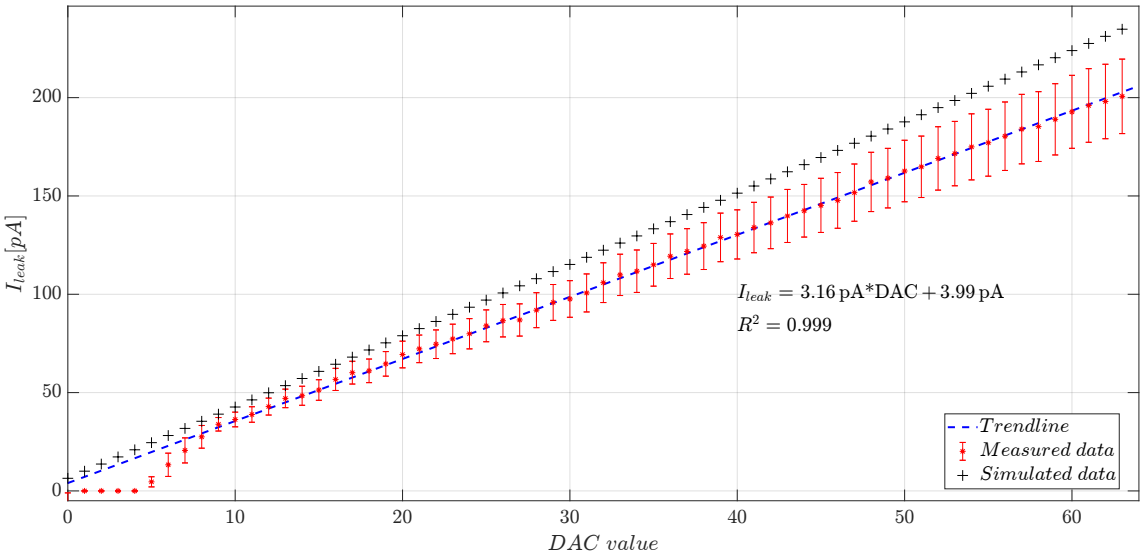


Figure 3.25: Leakage current of the sensor as a function of the 6-bit DAC value *INFB2* in red, blue is the linear regression that fits the data, and in black the simulated data is plotted.

Figure 3.25 presents in red the value of the leakage current measured by the sensor when the *INFB2* DAC varies from 0 to 63. In black the simulated data is presented. The measured data differs from simulation as expected, since there are several sources of error due to the amount of transistors placed in the current chain that can deviate from design.

As expected, the measured behavior of the current source is linear with a slope of 3.16 pA per DAC value (blue line). The maximum value of current that can be achieved is 200.7 pA.

3.5.1.2 Integration time

For a fixed and constant incident signal, the sensor should behave linearly as the integration time increases, if the leakage current *INFB2* does not varies. To verify this, the sensor was placed in an obscure environment, and using a pulsed laser diode (OPV300, VCSEL)[3], that generates 100 pulses of 50 ns duration infra-red (IR) light of 850 nm [84], the charge generated is measured. Figure 3.26 shows the charge measured of one pixel (averaged across 100 frames) as function of integration time.

[3] `https://www.mouser.de/datasheet/2/414/TTRB_S_A0007766311_1-2565389.pdf`

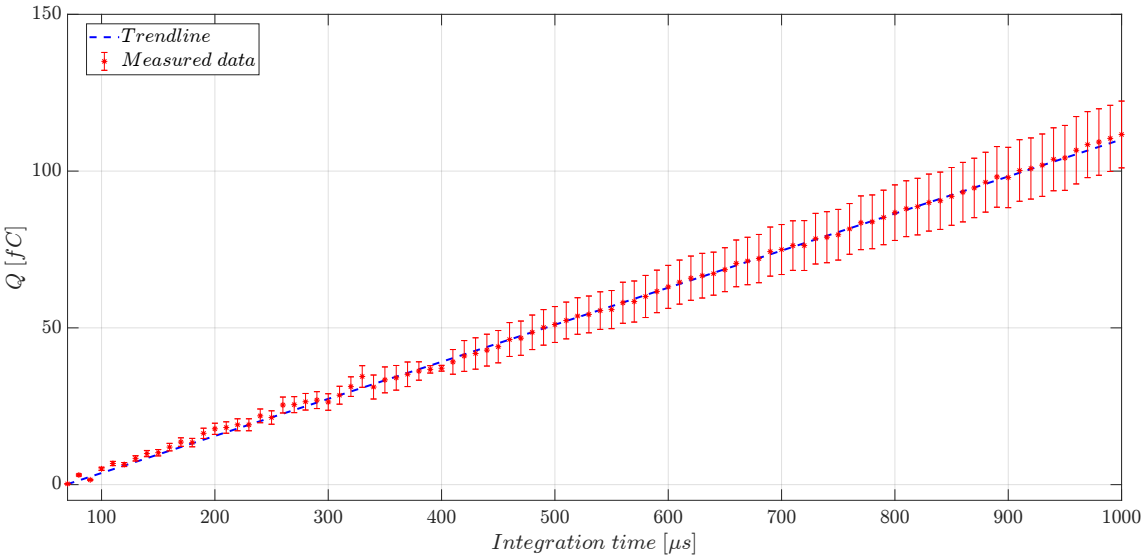


Figure 3.26: Charge measured as function of the integration time in red, the blue line represents the linear regression that fits the data.

Figure 3.26 presents in red the value of charge measured by the sensor when the integration time varies from 70 µs to 1 ms. As expected, the behavior of the sensor is linear as the integration time increases. Further analysis are shown in appendix B.6.

3.5.1.3 Sensor bias voltage

The depleted region increases as the reverse bias voltage applied decreases. This leads to a stronger signal. The nominal breakdown voltage for the deep n-well to p-substrate diode is 12 0V [79][4].

In order to find the optimal value of high voltage, and to verify the maximum value of reverse bias, a set of measurements has been done, maintaining all the parameters constant, and only changing the high voltage applied. Figure 3.27 shows the measurement result.

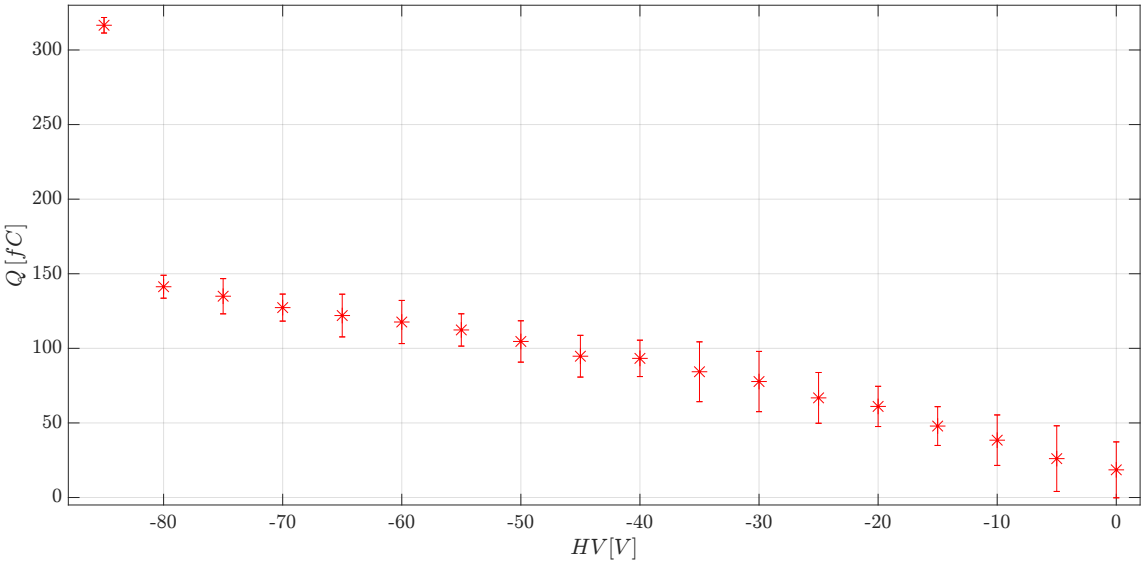


Figure 3.27: Charge measured as a function of the reverse high voltage applied. Increase of current indicates breakdown.

[4] https://www.tsisemi.com/technology/process/

As expected, the amount of charge collected by the integrator increases as the reverse voltage applied decreases. Increase of the current for voltages below -80 V is indication of avalanche multiplication and breakdown. It is possible that the absence of the *BF* layer around the pixel guard ring impedes the attainment of the nominal breakdown voltage.

3.5.1.4 Dynamic range

The sensor has been tested using a pulsed laser diode (OPV300, VCSEL)[5] that generates infra-red (IR) light of 850 nm [84]. By generating several laser pulses (50 ns duration) during the frame time and by calculating the acquired charge, the characteristic curve of the sensor has been obtained (figure 3.28). The mean value (μ) and standard deviation (σ) have been calculated from several measurements.

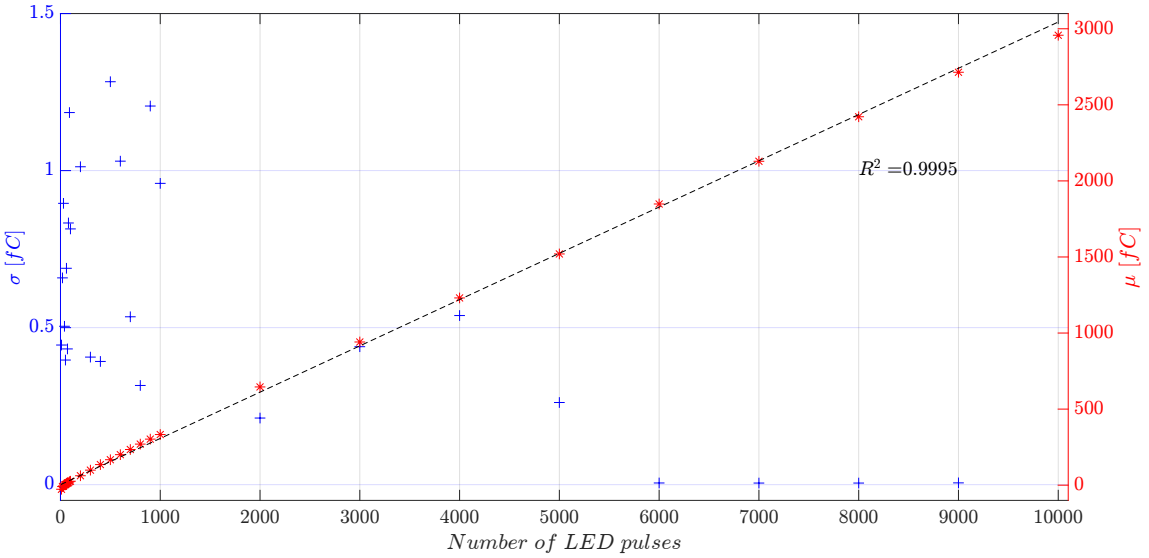


Figure 3.28: Mean value μ (red) and the linear fit (black) with an R^2 of 0.9995, and standard deviation σ (blue) of the measured charge as function of the number of IR-LED pulses for pixel (12|14).

Figure 3.28 shows the charge acquired by one pixel during the integration time when the number of led pulses sent increases. The figure shows that the sensor presents a linear response up to a charge of ∼2700 fC, after that, the last red point doesn't follow the linear trend and the sigma value is outside the limits of the plot. It is worth mentioning that the *Pump* pulse width is generated from the time frame, so no matter the value of the time frame, the maximum charge that this sensor can acquire is equal to:

$$Q_{max} = 256\, Q_{pump} \tag{3.4}$$

Using equation 3.1 to replace in formula 3.4

$$\begin{aligned} Q_{max} &= 256\, Vdd \cdot C_{pump} \\ Q_{max} &= 256 \cdot 1.8\, V \cdot 6.74\, fF \\ Q_{max} &= 3105.8\, fC \end{aligned} \tag{3.5}$$

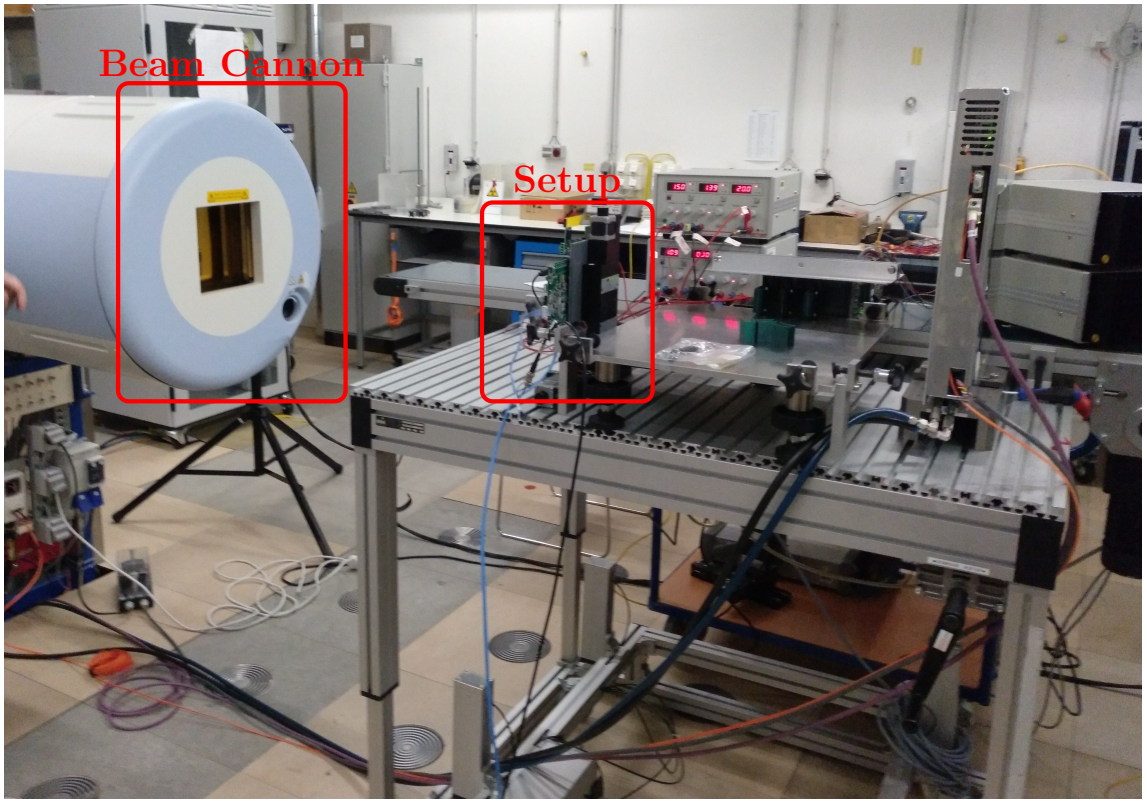
[5] https://www.mouser.de/datasheet/2/414/TTRB_S_A0007766311_1-2565389.pdf

According to equation 3.5 the maximum value of charge that the sensor is capable of acquiring during a frame is 3105.8 fC. In practice, this value will be lower, since the amount of pump pulses set is 250. This is done to avoid having issues of overflow or small changes in signal timing (jitter, noise, etc.). By doing this, the maximum value possible decreases by 2.3%, from 3105.8 fC to 3033 fC.

The noise, obtained by calculating the standard deviation across all the frames for each pixel and each different number of LED pulses, starts at ∼0.8 fC and on average it is constant until the amount of charge acquired is ∼500 fC, after that the noise decreases until it reaches ∼0.1 fC and stays flat until the last point.

3.5.2 Beam-test measurements

To test the sensor under the conditions that the ASIC has been designed for, a set of measurements were performed at the scientific beam site of Heidelberg Ion-beam Therapy center. There the system was placed in front of the particle beam as shown in figure 3.29. The aim of the measurements performed was to verify the functioning of the sensor towards high energetic ions. During the irradiation of patients, the main parameters that need to be monitored are the beam position, full width at half maximum (FWHM) value and intensity (amount of ions per second).



(a) Beam test room with the setup placed in front of the beam cannon.

(b) Setup system in front of the charged particle beam cannon.

(c) Setup system placed in the beam test room.

Figure 3.29: Setup used for beam-test measurements at HIT facilities.

The energy of the beam can be calculated from the charge integrated by the pixels, and by performing a set of measurements with several energies, a calibration curve collected charge vs beam energy can be obtained.

Using charge integration as sensing method, it is possible to obtain the intensity (number of particles per time unit) of the beam, since the sensor is acquiring the charge that the particle generates. By knowing the average charge that a particle generates in the sensor and the total integrated charge, the number of particles can be calculated.

By fitting 2D-Gaussian to the pixel signals it is possible to obtain the beam spot dimensions and position. To simplify the analysis, I calculated projections of the charge acquired in one frame along the rows and the columns. By doing that, two histograms will be obtained, along the x-axis and y-axis, and by fitting a Gauss bell to each of them the mean values can be calculated. Figure 3.30 shows an example of the procedure above described. Calculating of projections, (adding of signals acquired by each column and row) can be online by the FPGA or can be implemented in the sensor electronics (as it was done in the HIT counting sensor [86, 85]) to reduce the amount of data needed to be transmitted.

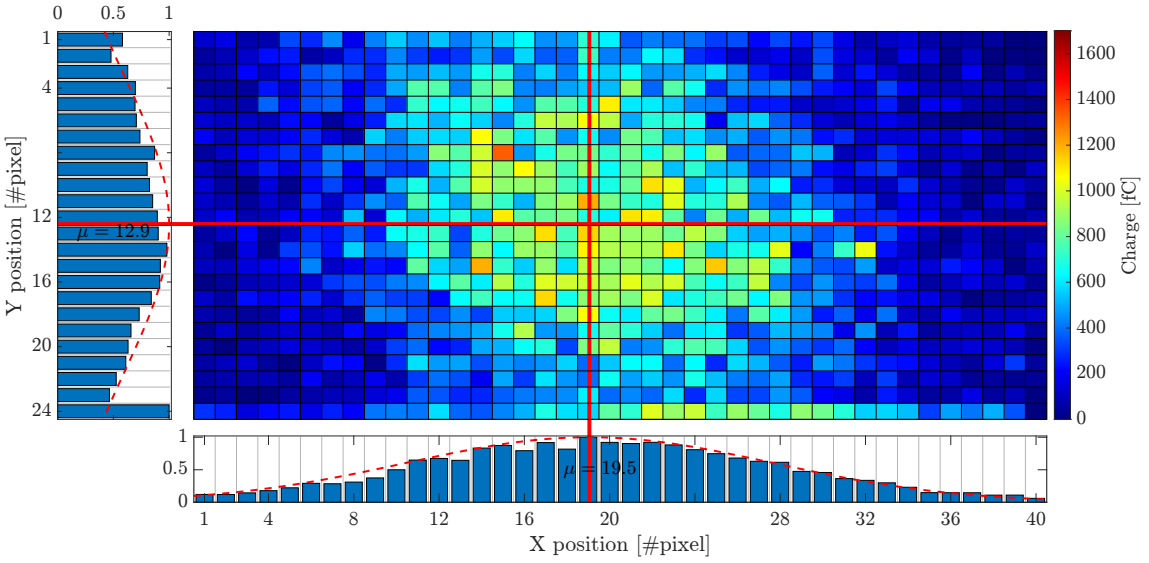


Figure 3.30: Position of the beam calculated by adding all the charge acquired by each column and row and fitting a Gaussian bell to each histogram.

The mean value across the rows corresponds to vertical beam position (Y pixel), while the mean value across columns corresponds to the horizontal position (X pixel). The standard deviation of each Gaussian is related to the focus of the beam. The first and

last row were excluded from the Gaussian approximation, because the charge measured by them is much larger than for other rows. This is because the charge generated in the substrate below will be collected by the nearest row of pixels, creating an excess of charge.

The full width at half maximum value (FWHM) calculated was 21.3 (2.556 mm) pixels in vertical and 20.2 (2.424 mm) pixels in horizontal.

The measurements performed aim to find the behaviour of the sensor when changing the following beam and sensor parameters:

- Energy of the beam (Escan)
- Intensity (ions/s) of the beam (Iscan)
- Integration time
- High voltage

For all the parameters above mentioned, measurements with both, protons (p) and carbon (C) ions, were performed. For all the measurements, before the beam was turned on, a dark measurement needs to be performed in order to measure the leakage current of the sensor for that specific environment under the set-up conditions (voltages, currents, and times).

3.5.2.1 Single energy measurement

Figure 3.31 shows the average values of all the pixels on each frame during the beam test of one energy for protons of 86.72 *MeV/u*. In the course of particle accelerator operations, the beam is intermittently activated and deactivated, yielding a sequence of particle pulses known as a spill.

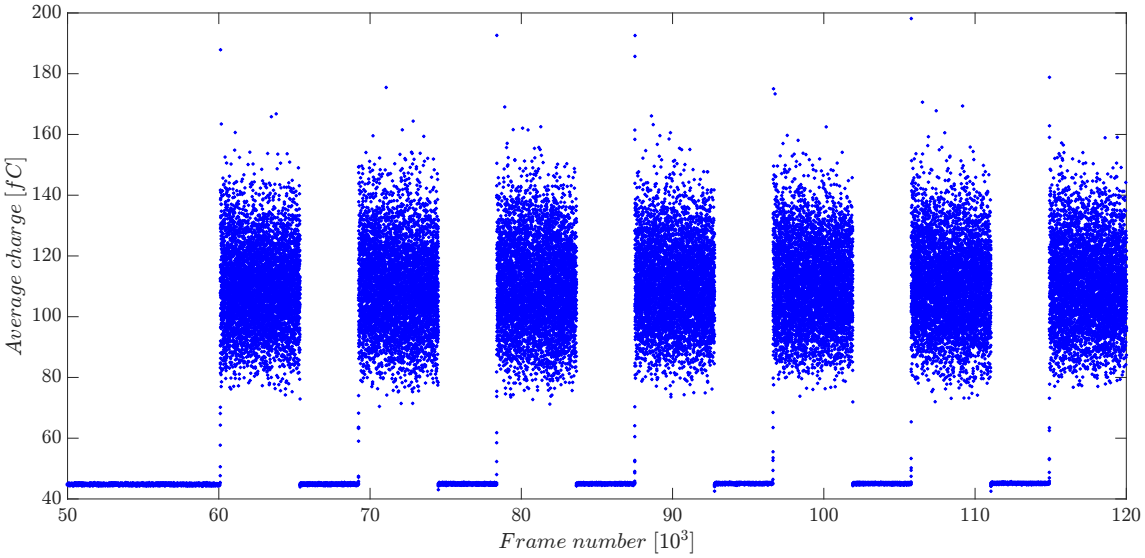
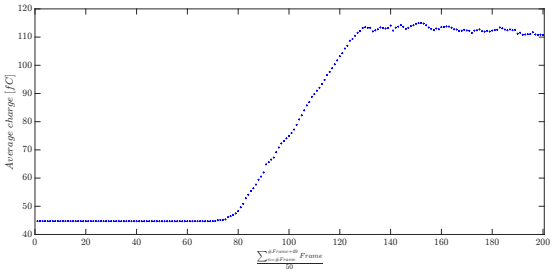


Figure 3.31: Average matrix value (across all pixels) as a function of the frame number. The x-axis, expressed as frame number, can be translated to time by knowing the time frame used(125 µs). The measurement was don using protons of 86.72 $\frac{MeV}{u}$.

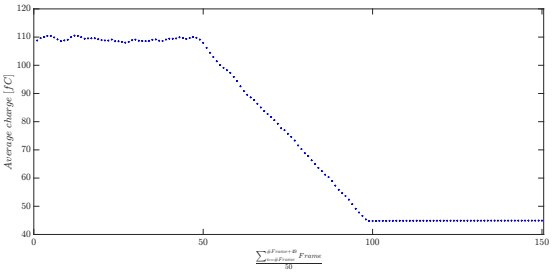
There are seven spills with values significantly larger than the baseline (which is 44 fC). Those pulses represent the frames in which ion beam was on. The average value of the pixels during beam off (baseline) is the base line noise of the sensor. During each spill, the

charge acquired by the pixels fluctuates between 80 fC and 150 fC approximately. This fluctuation of the measured charge is probably the result of the intensity fluctuations of the ion beam [72].

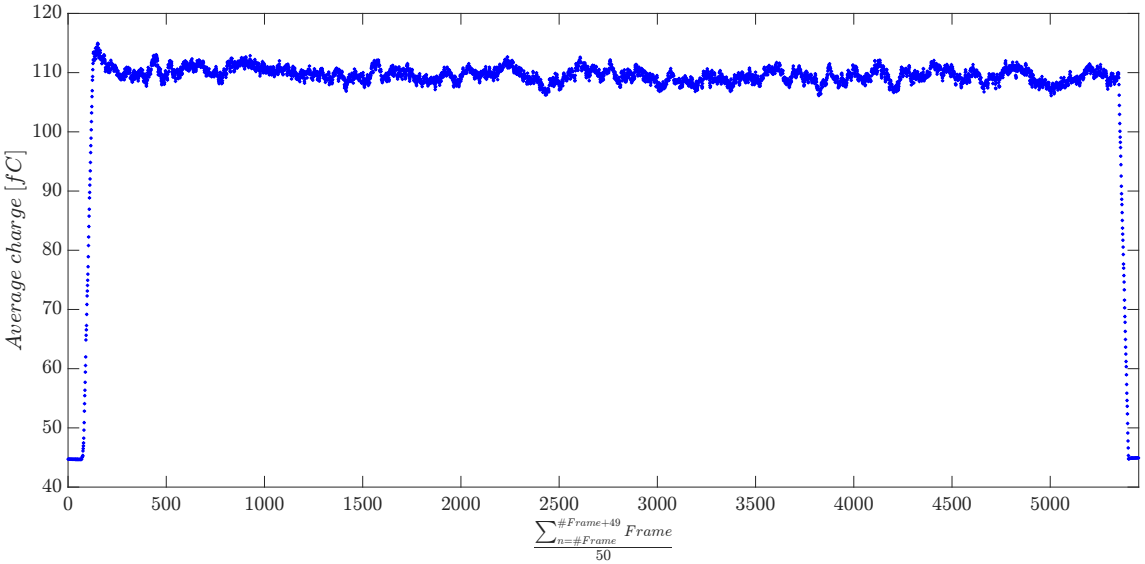
In figure 3.32, a close up of a spill is plotted where a moving average of 50 frames was applied. In the figure the ramp up of the beam is shown, as well as the ramp down and the whole spill.



(a) Average matrix value of the ramp up of the first spill after a moving average with a window of 50 frames was performed.



(b) Average matrix value of the ramp down of the first spill after a moving average with a window of 50 frames was performed.



(c) Average matrix value for the first spill after a moving average with a window of 50 frames was performed.

Figure 3.32: Average matrix value of the first spill with a moving average.

Once the spill frames are discriminated, by performing a histogram of the charge value acquired during those spills the plot on figure 3.33 is obtained.

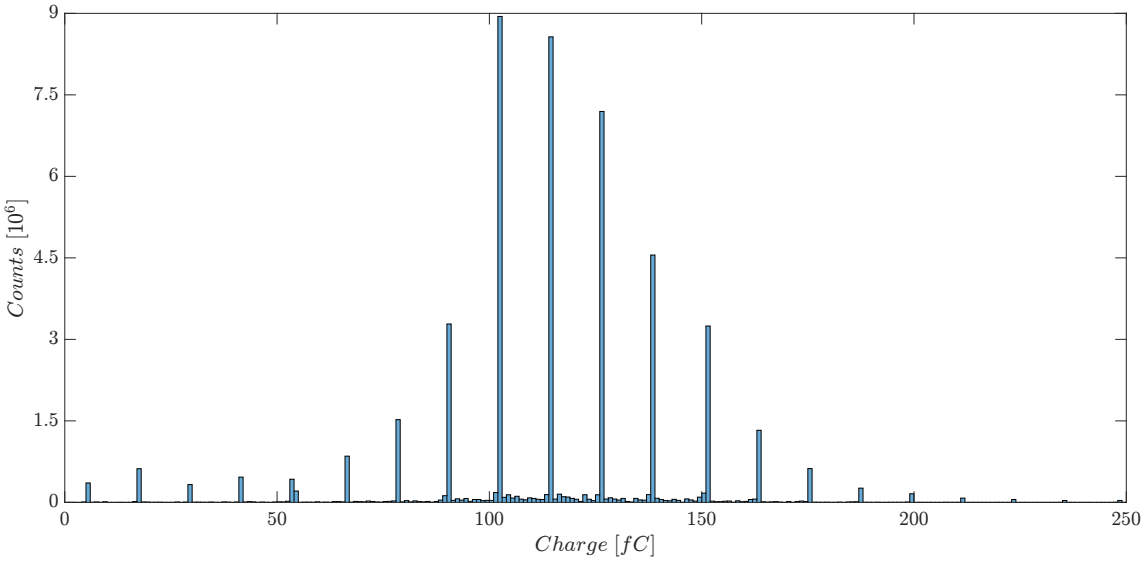


Figure 3.33: Charge histogram of the data after filtering the baseline and using only the frames where the ion beam was on.

The energy of the beam is related to the amount of charge that was measured by the integrator. In figure 3.33 the bins are 1 fC width, and every ∼12 fC (the charge that each pump pulse subtracts from the integrator), the bin count is larger than the surroundings. This effect can be seen in all the beam test measurements and is happening because the time stamp of the pumps are not behaving correctly. Probably due to misbehavior of the time counter under radiation. This issue is planed to be solved in the next version of the sensor.

Despite the issue with the time stamp, if the mean value of the charge from figure 3.33 is calculated, and knowing the relation between generated charge and particle energy (section 3.5.2.2), the average energy of the beam can be calculated. Notice that for a given energy, only the average deposed energy and average charge signal can be calculated. The actual deposed energy is distributed with Landau distribution.

3.5.2.2 Energy scan

An energy scan (Escan) was performed with proton and carbon ions to verify the behavior of the sensor under different parameters (integration time, reverse bias voltage, and threshold voltage) as well as the response for the whole range of energies available. The image obtained with the pixel matrix (one frame) during irradiation can be seen in figure 3.34.

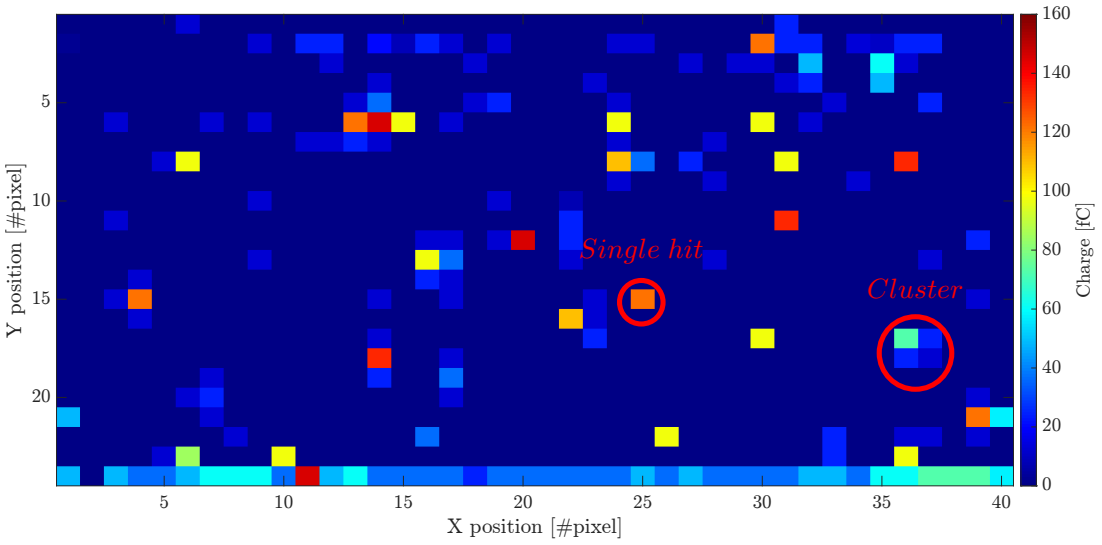
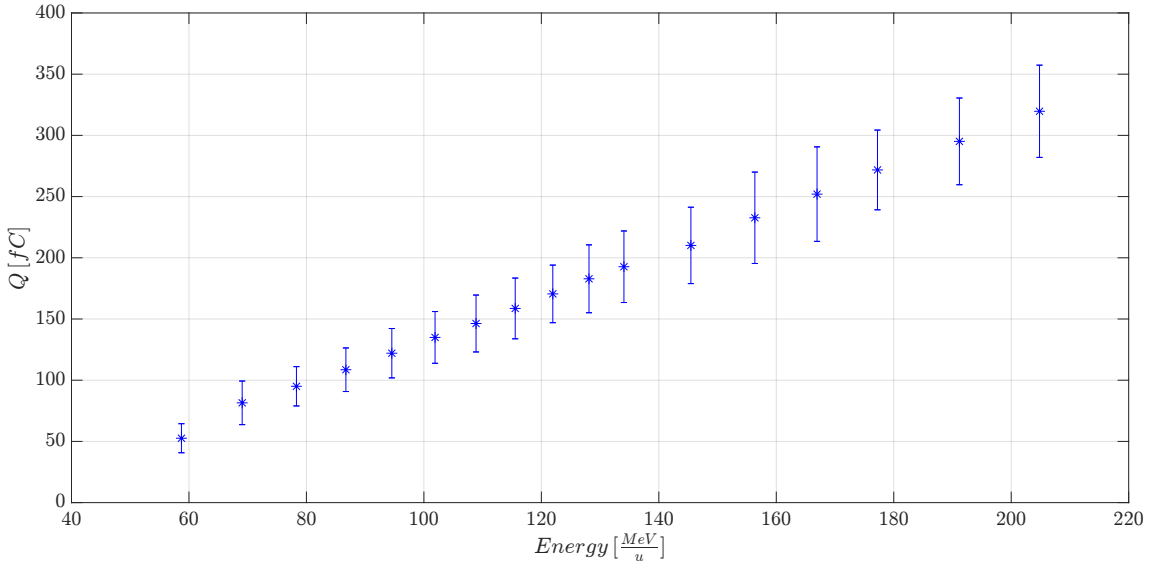


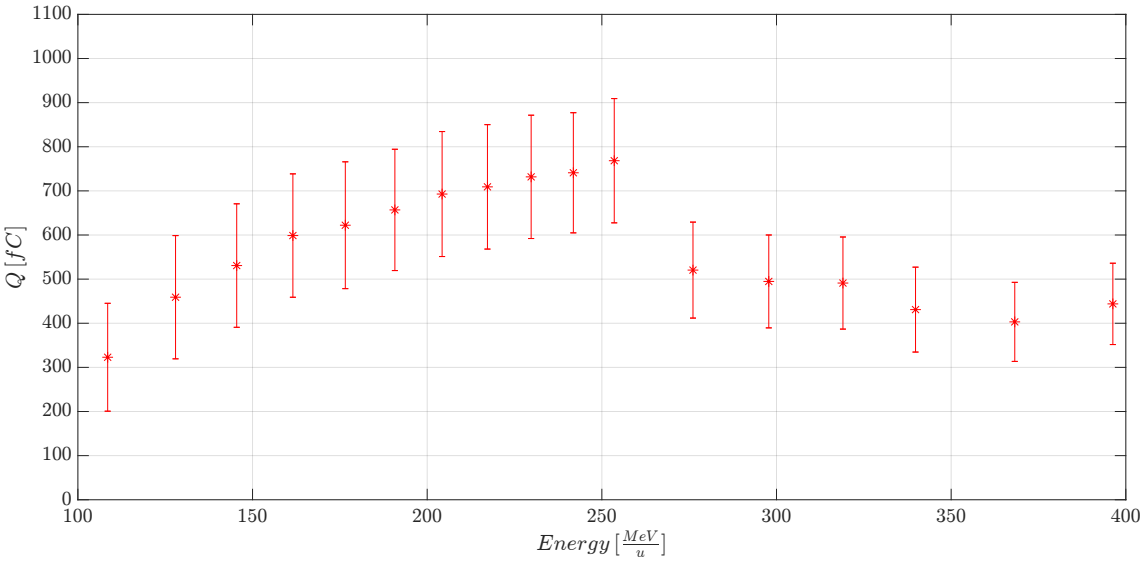
Figure 3.34: Image obtained with the pixel matrix when irradiated with carbon ions with low intensity (3.10^6 ions/s) with an integration time of 125 µs, HV of -15 V.

In figure 3.34, one single pixel hit and one cluster with 4 pixels are marked. Since the intensity of the beam was set low, the number of hits present in the frame is low.

Figure 3.35 shows the average charge acquired by one pixel as a function of the beam energy. This is shown for protons and carbon ions.



(a) Charge measured by one pixel as function of proton beam energy.



(b) Charge measured by one pixel as function of carbon ion beam energy.

Figure 3.35: Charge measured by one pixel as function of beam energy for both, protons (a) and carbon (b) ions with an intensity of $400{\cdot}10^6$ ions/s, an integration time of 1.5 ms, and HV of -45 V.

Measurement from figure 3.35(a) shows that the measured charge increases when the energy of the protons increase. Figure 3.35(b) shows the charge acquired by one pixel as function of energy of carbon ions. Finding a trend is complicated because the accelerator automatically changed the focus of the beam as the energy increases, making the comparison difficult. However, the same energy scan was performed during a prior beam test, where in that case, the focus only changed once after the second energy was done. Figure 3.36 shows the measured signal vs beam energy curve for carbon ions of the previous beam test. The charge acquired decreases with the energy, which is according to the Bethe-Bloch formula [45].

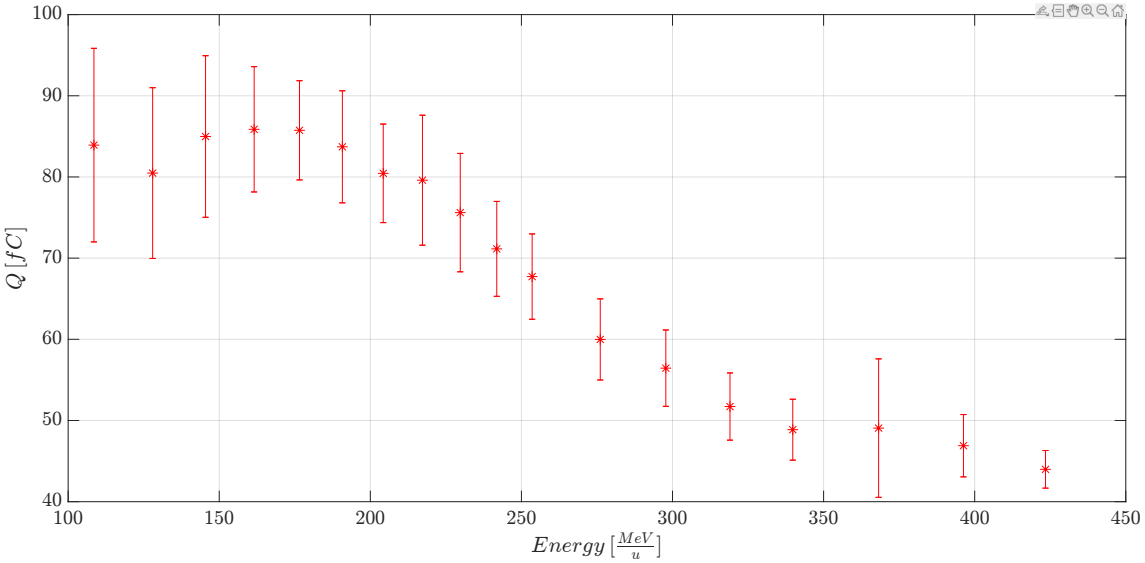


Figure 3.36: Measured charge as a function of energy of carbon ions from the beam test performed on June 2022.

If we compare the measured charge for carbon ions and protons (figure 3.37), we

obtain that the charge generated by protons is lower compared for carbons assuming the same energy [78, 64], this can be seen from Bethe-Bloch formula. The measurement was performed for both, carbon ions and protons, with the same set of parameters (HV, *Tframe*, DACs, intensity of the beam, etc.).

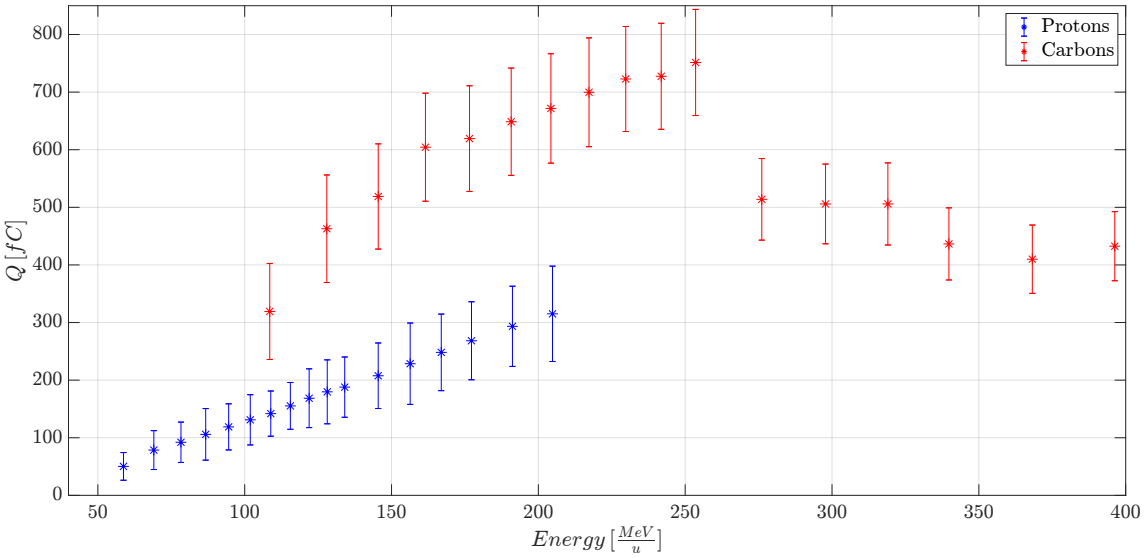


Figure 3.37: Measured charge as function of beam energy for carbon ions and protons.

3.5.2.3 Integration time

Each energy scan was repeated with different integration times (0.5 ms, 1.5 ms, and 2 ms).

Figure 3.38 shows the average charge acquired by a pixel under the beam for each energy used for protons and for the three different integration times. The dashed line represents the linear fit of the data.

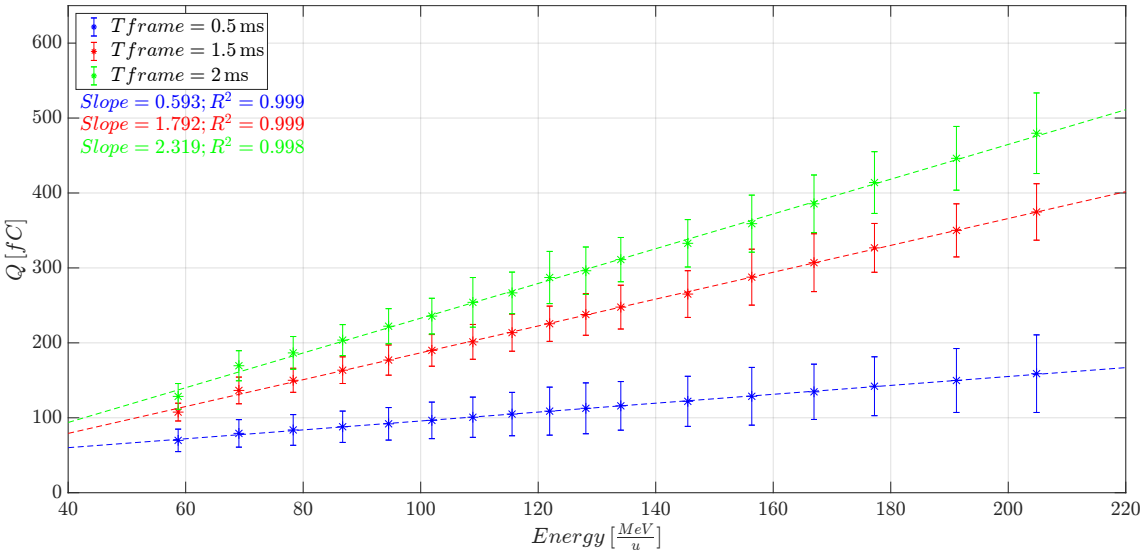


Figure 3.38: Comparison of the charge acquired by the sensor when protons were used for a *Tframe* = 0.5 ms (blue), 1.5 ms (red), and 2 ms (green). As expected, the charge measured for shorter *Tframe* is smaller than the charge acquired with a longer *Tframe*.

It is verified that the sensor response to different integration times is linear. Further analysis can be found in appendix B.6.

3.5.2.4 Reverse bias voltage

Figure 3.39 shows the average charge acquired by the pixel 6|12 (right in the beam spot) for each energy used for protons and for the three different reverse bias voltages. The dashed line represents the linear fit of the data.

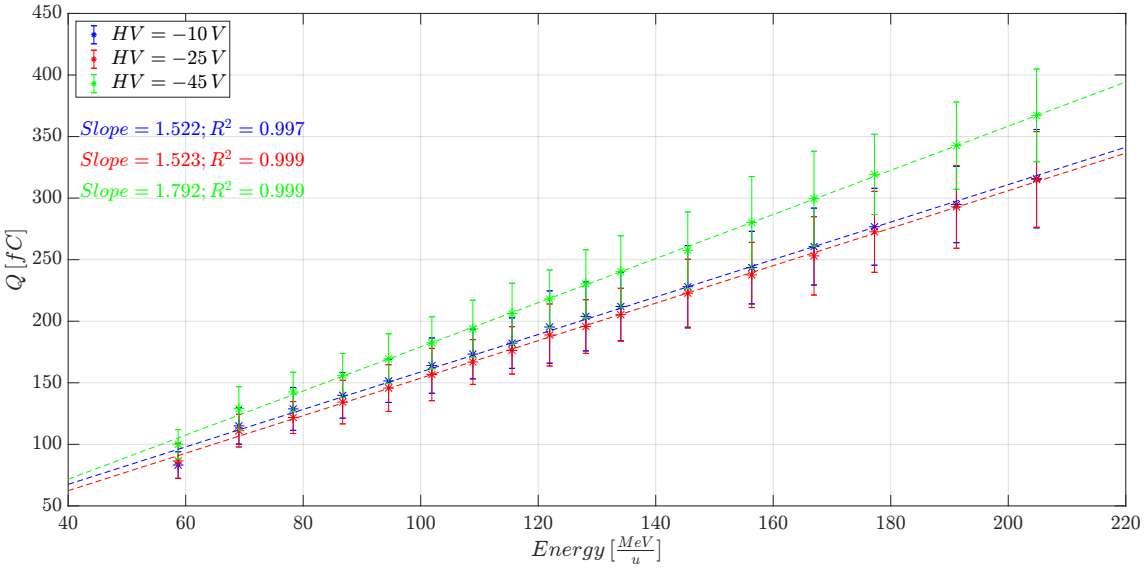


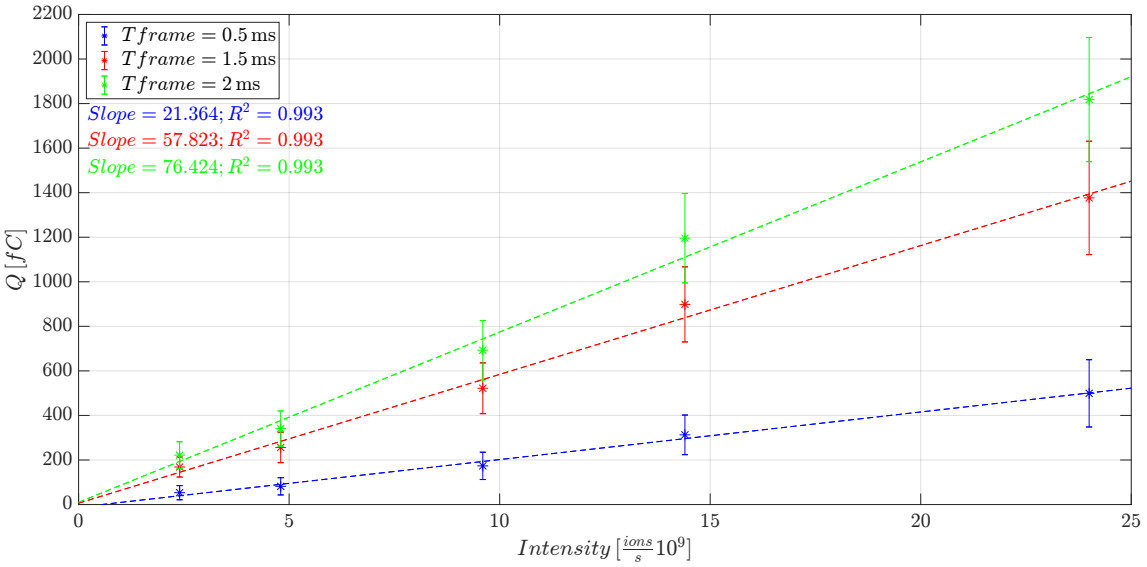
Figure 3.39: Comparison of the charge acquired by the sensor when protons were used for a HV = -10 V (blue), -25 V (red), and -45 V (green). As expected, the charge measured increase as the HV is more negative.

The measurement from figure 3.39, shows that more negative the sensor bias voltage is, the steepest the slope for each measurement is, thus is possible to measure lower beam energies.

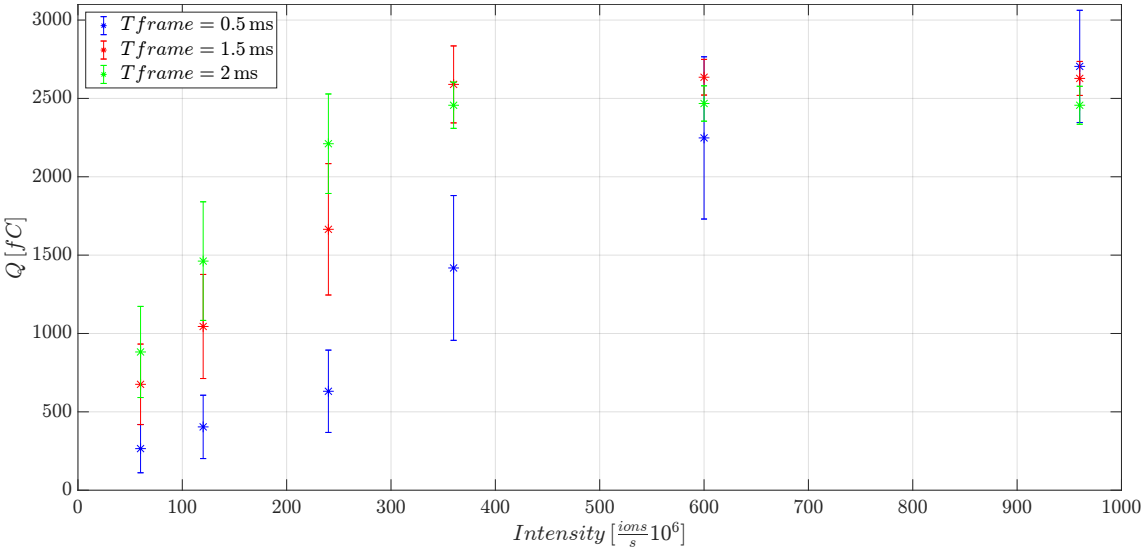
3.5.2.5 Intensity scan

To verify that the sensor behaves linearly with the number of particles that travels through it, an intensity scan (Iscan) was performed. In addition, the Iscan was done for different integration times and reverse bias voltages.

Figure 3.40 shows the intensity scans for protons and carbons ions with different integration times of a pixel in the beam. As expected, the charge measured by the sensor increases linearly with the number of particles that the accelerator delivers.



(a) Charge as a function of the intensity for proton.



(b) Charge as a function of the intensity for carbon ions.

Figure 3.40: Charge as function of the intensity of the beam, protons (a) with energy = 156.35 MeV/u and carbon ions (b) with energy = 297.79 MeV/u. HV of -45 V, *Tframe* = 0.5 ms (blue), 1.5 ms (red), and 2 ms (green). The plots correspond to a pixel in the beam spot.

Figure 3.40(a) shows the charge as function of the intensity of the beam, for three different integration times. The dashed line corresponds to the linear fit and verifies that the sensor behaves linearly as the amount of protons increases. Figure 3.40(b) shows the charge as function of the intensity of carbon ions for three different integration times. The measurement with carbon ions results in a saturation of the sensor for higher intensities. Because of that, the last three measured points are always around the same value (∼2650 fC) which corresponds to the maximum charge that the sensor is capable to register minus the offset baseline of the measurement.

Table 3.3 summarizes the values of the ratios for the different integration times for each measurement. **Proton slope ratio** corresponds to the ratio between the calculated

slopes for each *Tframe*. **Carbon mean charge ratio** corresponds to the average of all the ratios between each point for each *Tframe*.

Table 3.3: Comparison of the charge increment measured as the integration times increase for protons.

***Tframe* ratio**	**Proton slope ratio**	**Carbon mean charge ratio**
1.5 ms/500 µs= 3	2.7 ± 0.4	2.59 ± 0.06
2 ms/500 µs= 4	3.6 ± 0.6	3.48 ± 0.15
2 ms/1.5 ms= 1.3	1.32 ± 0.09	1.34 ± 0.05

4 ASIC verification for Belle II experiment

Particle accelerators are powerful machines that accelerate subatomic particles in order to study their properties. SuperKEKB, located at the KEK laboratory in Tsukuba, Japan, is an accelerator designed to produce high precision, low-energy collisions to produce large numbers of particles containing B mesons, that is why its also called a B-factory. By studying the properties of B mesons, we can learn more about the fundamental laws of nature, specifically about the CP-violation, and the behavior of particles at the subatomic level.

B mesons are hadrons, particles composed of quarks bound together by the strong nuclear force [57]. SuperKEKB produces B mesons composed of a bottom quark (also known as a "b" quark) and another quark (either an up, down, charm, or strange quark). The Belle experiment, started to run in May 1999 [21], to investigate the CP-violation in B mesons.

CP-violation is a phenomenon in particle physics where the laws of physics are not symmetric under the combined transformation of charge conjugation (C) and parity (P). This theory was proposed by Makoto Kobayashi and Toshihide Maskawa in 1973 [39]. The study of CP-violation is an important area of research in particle physics because it may help to understand why the universe is matter instead of antimatter.

Today, the Belle II[1] experiment proceeds the work of Belle, probing even deeper into the mysteries of particle physics. SuperKEKB is designed to produce even more B meson collisions than its predecessor, allowing researchers to study CP-violation and other properties of subatomic particles with high precision. One of the main goals of Belle II is to search for new sources of CP-violation beyond what has already been observed in previous experiments [41].

Belle II detector has onion like arrangement of sub-detectors around the interaction point: vertex detector (VXD), time of propagation detector (TOP), central drift chamber (CDC), electromagnetic calorimeter (ECL), Solenoid, aerogel ring-imaging Cherenkov detector (ARICH), and K_L and muon detectors (KLM). Figure 4.1 shows a schematic picture of the Belle II detector.

[1] `https://www.belle2.org/`

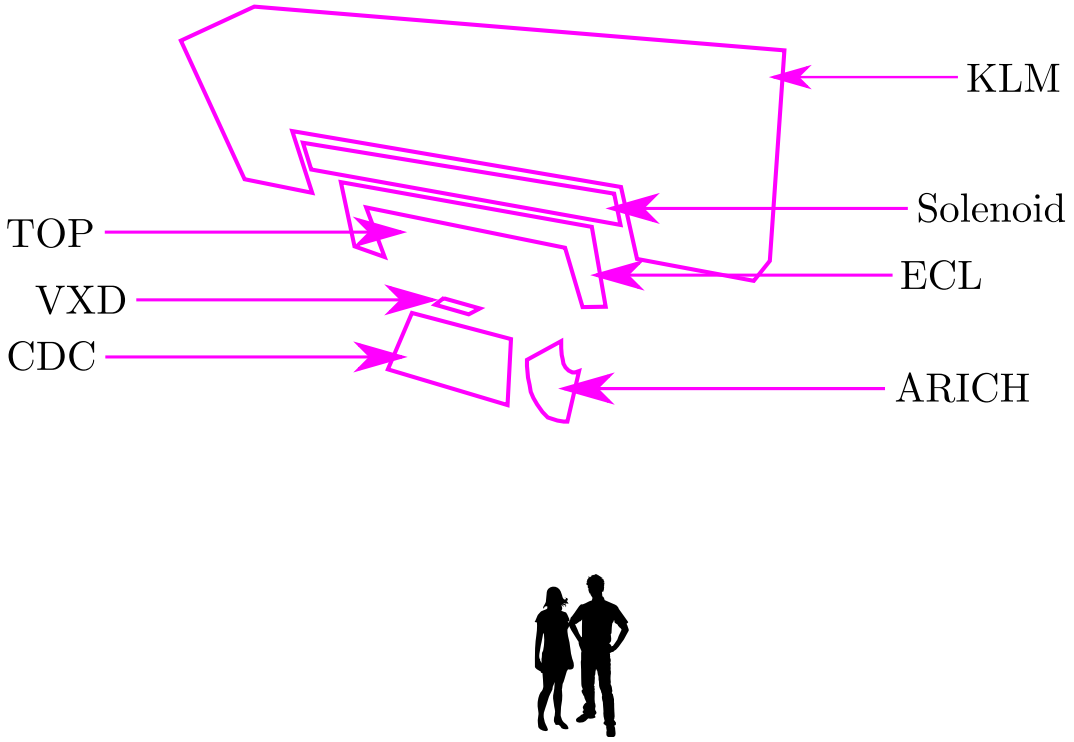


Figure 4.1: Belle II experiment detector comprising sub-detectors (Belle II official website[1], modified).

The ADL group at KIT contributes to this experiment by the development and test of the Drain Current Digitizer (DCD) and SWITCHER [61] ASICs that are bump bonded to the Vertex Detector (VXD) of the Pixel Detector module (PXD) [41]. Both ASICs (DCD and SWITCHER) are designed in 180 nm HVCMOS technology, while the sensor uses a technology called Depleted P-channel Field-Effect Transistor (DEPFET) originally invented by Kemmer and Lutz in 1987 [37]. DCD amplifies and digitizes the current from the DEPFET sensor in the pixels. The SWITCHER ASIC selects the pixel rows for readout and clear the stored signal in the internal gate of the DEPFET pixel.

In order to test DCD and SWITCHER, Dr. R. Blanco and Dr. R. Leys have originally developed and build a probe station to test the chips. During my Ph.D., I upgraded the software to a new version and made it portable. I have also developed a new carrier PCB version, which is smaller and more versatile than the old version. In this way, the probe station is more stable and easy to use, and the institutes of the Belle II collaboration replicated it. The success of these improvements of the probe station setup were validated by characterization of 350 ASICs.

4.1 Belle II detector architecture

The Belle II detector is located around the interaction point, and it consists of several sub-detectors. These sub-detectors are placed in an onion-like shell structure that covers almost 2π solid angle [53]. It is possible to investigate the collision processes by utilizing the data that each sub-detector has collected. The technical design report for Belle II [3] has thorough information on the sub-detectors. This chapter will provide a brief summary of Belle II's components, focusing on the VXD, from the outermost to the innermost detector (as shown in Figure 4.1).

The Belle II detector can be divided into two main parts, external and internal:

External part consists of the K_L^0 and muon detector (KLM), the solenoid, and the electromagnetic calorimeter (ECL).

Internal part contains the aerogel ring-imaging Cherenkov detector (ARICH), time of propagation detector (TOP), central drift chamber (CDC), and vertex detector (VXD).

The KLM detector identifies K_L^0 (a neutral meson particle that is composed of a strange quark and an anti-strange quark) and muons, and is the first layer looking from the outside of the Belle II detector in figure 4.1. It consists of 14 iron plates and in between 14 active detector elements based on glass-electrode resistive plate chambers (RPCs).

Further, inside the Belle II detector, there is the solenoid, a superconducting inductor with the ability to produce a central magnetic field of 1.5 T at 4000 A [48]. By bending the charged particle's paths, this magnetic field enables the reconstruction of the particle momenta using data from the CDC detector [53].

The electromagnetic calorimeter (ECL), which consists of 6624 thallium-doped cesium iodide crystal scintillators, is the final exterior sub-detector. This device can detect photons with energies greater than 20 MeV with high efficiency. The angular coordinates of particle trajectories and photon energy can also be calculated. Additionally, it distinguishes between hadrons and electrons, measures luminosity both online and offline using reconstruction methods, detects the K_L^0 in combination with the KLM, and produces trigger information [24, 53].

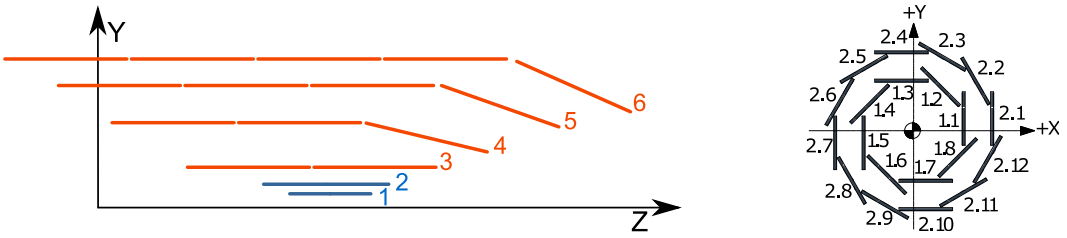
The aerogel ring-imaging Cherenkov detector (ARICH), which is a new particle identification (PID) device located in the end-cap region of the interaction point. The detector was developed to distinguish the signals of π and K up to $2\,\mathrm{GeV}/c$ [32]. The particles passing through the detector create Cherenkov light that reaches the photodetector. Depending on the angle of the photons, the mass of the particle can be calculated [53].

The TOP detector consists of 16 modules, each of them containing two quartz radiator bars with a total length of $\sim$2.5 m [55]. It is located in the direction of the beam pipe. This detector can separate charged kaons ($K^{\pm}$) from charged pions ($\pi^{\pm}$) and is the primary device for particle identification in the barrel region of Belle II [53].

The central drift chamber (CDC) is a cylindrical chamber filled with 50% helium and 50% ethane [16]. It consists of 56 layers (14 336 sense wires and 42 240 field wires) which are biased with opposite voltages and are arranged alternatingly and parallel to the beam pipe. This detector can measure the momenta and reconstructs the tracks of the charged particles and the energy lost in the gas volume is measured to provide information for particle identification [16, 53].

The innermost layer of sensors is the Vertex Detector (VXD), it has the ASICs that will be discussed later. This detector consists of two different sub-detectors, the four layers

of double-sided Silicon Vertex Detector (SVD) and two innermost layers of Pixel Detector (PXD) (figure 4.2). The main task of the SVD is to reconstruct the tracks of the particles generated in the collision and to contribute on determining their momenta. The PXD on the other hand consists of two layers of depleted active pixel detectors (DEPFET). The external layer is comprised of twelve sensor staves, while the inner layers are eight, arranged in a dodecahedral and an octagonal shape respectively. This sensor consists of approximately eight megapixels which are read continuously in rolling shutter mode every 20 µs [10].



(a) Layout of the PXD (layers 1 to 2) and SVD (layers 3 to 6) around the beam pipe.

(b) Arrangement of the PXD layers around the beam pipe.

Figure 4.2: Schematic of the arrangement of the six layers of the VXD detector (after [7]).

4.2 PXD detector

The PXD (Pixel Detector) in Belle II is a key component of the detector system. It is designed to provide precise and detailed information about the trajectory of charged particles produced in collisions within the detector. The most challenging requirements are a short time frame readout (20 µs) and that the total amount of material should be less than 0.3% of the radiation length.

The PXD detector is composed of two layers of eight and twelve sensor modules each in a dodecahedral and an octagonal shape (as shown in the 3D model in figure 4.3). To cope with the short time frame, the sensor matrix is split in two (making a total of 40 PXD sensors). Readout electronics is placed at both ends with an additional parallelization using four DCDs to read out four rows simultaneously.

To reduce the total amount of material requirement, the DEPFET technology has been modified [10, 52]. Each pixel on the inner ring has a pixel size of 50 µm × 55 µm for the 256 pixels closest to the interaction region and 50 µm × 60 µm for the rest. In case of the second layer of PXD, the pixel size is 50 µm × 70 µm for the closest pixels and 50 µm × 85 µm for the rest [52].

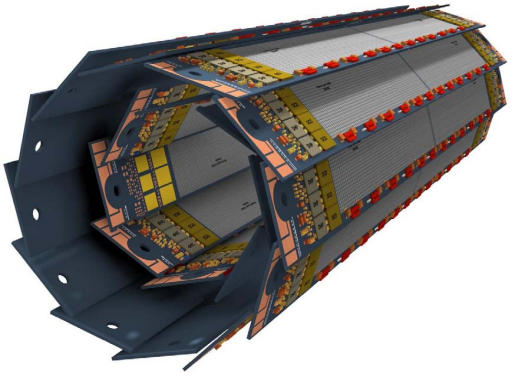


Figure 4.3: 3D model of the two layers of the PXD detector (after [53]).

Each of the 40 sensor modules is an independent hybrid detector, with the sensing device being a matrix of 250×768 pixels implemented in the DEPFET technology. Figure 4.4 shows a 3D schematic of a single PXD module and the position of the SWITCHER and DCD chips. A set of six SWITCHERs are bump bonded along the right longer side of the sensing device (dark square on the right of the figure) in order to select the pixels rows for readout and clear the stored signal charge with fast high voltage pulses of typically 10 ns and 20 V [61]. On the bottom side of the pixel matrix, four DCDs (Drain Current Digitizers) are bump bonded (sand color, bottom side of the figure). They read out the signals of the pixels and digitizes them. Below the DCD, four data handling processors (DHPs) are placed. They filter the data and send it to the data acquisition system off module, and control the timing of the SWITCHER signals.

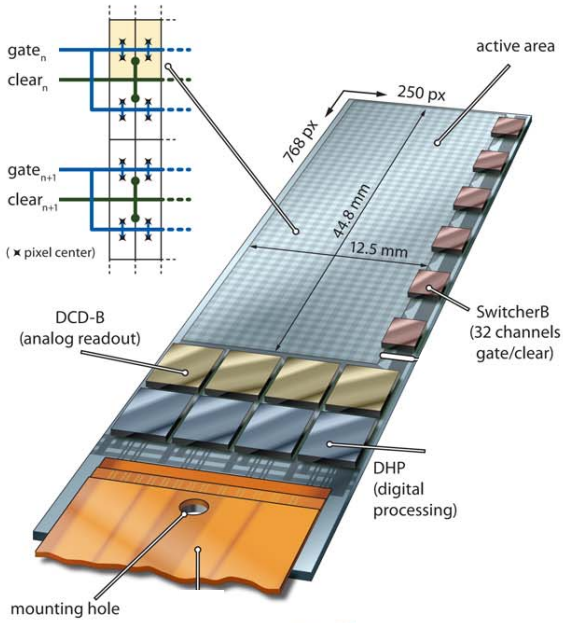


Figure 4.4: 3D model of one PXD module and the position of each bump bonded chip SWITCHERs, DCD, and DHP (after [40] modified).

4.2.1 PXD pixels

DEPFET are formed by implanting impurities to create an n-type silicon region right under the conventional MOSFET channel in order to create a so-called "internal gate" (figure 4.5). When electron-hole pairs are created by a passing particle, the electrons migrate and get trapped in the internal gate, while the holes drift to the p^+ backside. The excess of electrons in the internal gate creates a voltage that modifies the charge in the channel generated in the transistor, thus modulating its current flow. By measuring this alternation of current flow, the amount of trapped charge can be calculated.

Some of the benefits of the DEPFET technology are the low noise measurements with a high energy resolution, as well as low power consumption [68]. Some of the drawbacks are the complex fabrication process, the complex operation, and temperature dependence.

(a) Schematic cross-section of a DEPFET pixel.

(b) 3D schematic view of the DEPFET pixel (after [27]).

Figure 4.5: Schematic of the DEPFET pixel in PXD detector. (a) shows the cross-section of the DEPFET pixel when a particle passes through the n-bulk electron-holes are generated. The electrons migrate and get trapped in the internal gate, while the holes drift to p^+ backside. The accumulation of electrons in the internal gate creates a voltage that modulates the p-channel of the PMOS transistor. By applying a high voltage to the clear contact the internal gate can be emptied and the pixel is ready for a new measurement. (b) shows a 3D schematic of the DEPFET pixel, the clear gate contact is located below of the PMOS transistor.

Since the electrons get trapped in the internal gate, it is necessary to release them by applying a positive voltage to it. For this purpose, an extra contact is implemented in the silicon that connects to the internal gate and forms a discharge path when a high positive voltage is applied. This contact is called clear gate and it consists of a highly doped n-type region. To prevent a loss of signal electrons during accumulation by diffusion, the clear contact is shielded by generating a p-region underneath inside the n-bulk. The equivalent circuit of the DEPFET is shown in figure 4.6.

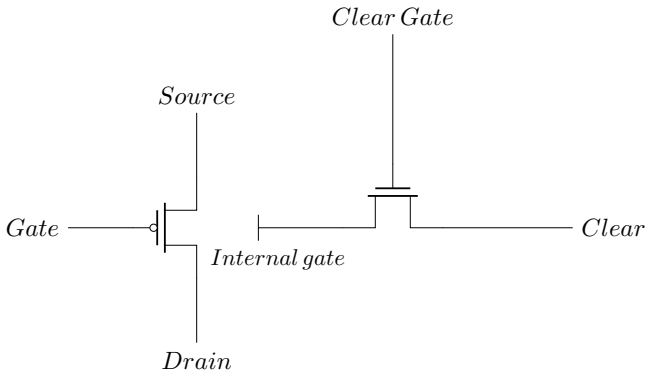


Figure 4.6: Equivalent transistor circuit of the DEPFET pixel.

To control of the readout and clear of the PXD pixel matrix, a high voltage fast signal needs to be generated, thus the necessity for the SWITCHER chips, whose function is to generate these signals in the correct order to readout the matrix in a rolling shutter sequence and clear the internal gate.

4.2.2 SWITCHER ASIC

The SWITCHER ASIC is used to select the pixel rows for readout and clear the stored signal in the internal gate of the DEPFET pixel. This ASIC, developed at KIT and the University of Heidelberg, can generate fast (10 ns into 70 pF) voltage pulses of up to 50 V amplitude [61]. The high voltages generated clears the stored charge in the DEPFET

by discharging the electrons accumulated in the internal gate. The chip was manufactured in AMS 180 nm technology. Figure 4.7 shows a photograph of the SWITCHER.

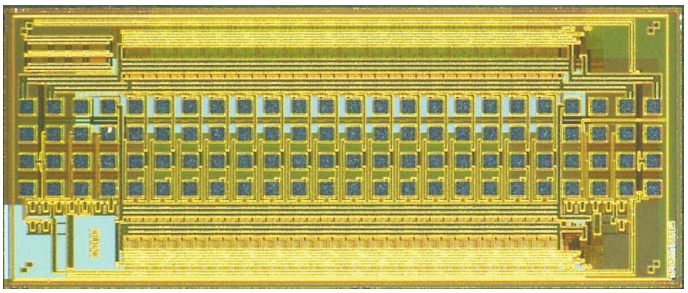


Figure 4.7: Photography of the SWITCHER chip manufactured in 180 nm AMS technology manufactured (after [61]).

The main components of the SWITCHER chip are 32 high voltage channels that generate two high voltages each (thus, 64 high voltages in total per chip). Using a low-voltage control block based on a shift register, each high-voltage channel is selected. Auxiliary high-voltage supplies are generated by two voltage regulators. The block diagram of the chip is shown in figure 4.8.

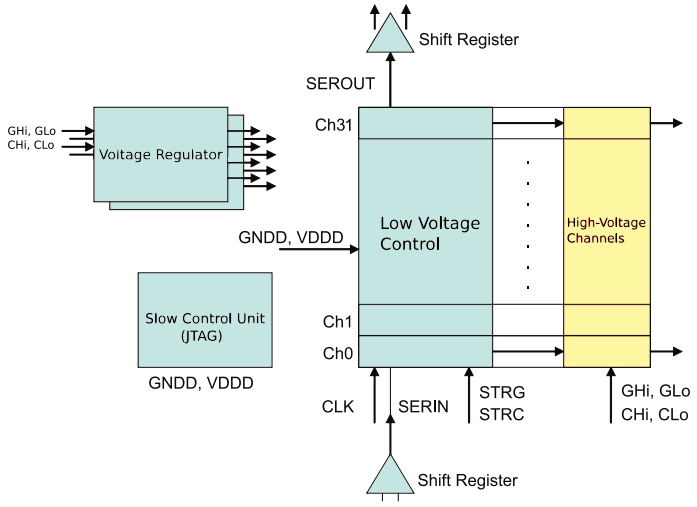


Figure 4.8: Block diagram of the SWITCHER chip structure (after [61]).

The high voltage outputs can switch between the upper voltage Clear-high/Gate-high (CHi/GHi) and the lower voltage Clear-low/Gate-low (CLo/GLo), the voltage difference between high and low can be up to 20 V. The serial output communication line of one ASIC is connected to the serial input of the next one to interconnect the chips in chain. Sequential activation of each high-voltage channel is obtained because the channels are activated by means of a shift register. The low voltage control block and the slow control block are both powered by a 3.3 V voltage supply.

4.2.3 Drain Current Digitizer chip

The DCD chip amplifies and digitizes the currents from the DEPFET sensor in the pixels. The amplifiers are acting as one differential amplifier with 256 inputs. The DCD consists of 256 analog channels, each of them containing a trans-impedance amplifier signal receiver, with a configurable offset current that is added to the input. The output of the

receiver is connected to two current-mode cyclic ADCs based on current-memory cells [61]. Figure 4.9 shows a photograph of the DCD chip. The ASIC is implemented in UMC 180 nm CMOS technology and uses radiation tolerant design, since the ASIC has to be able to withstand up to 10 MRad [61].

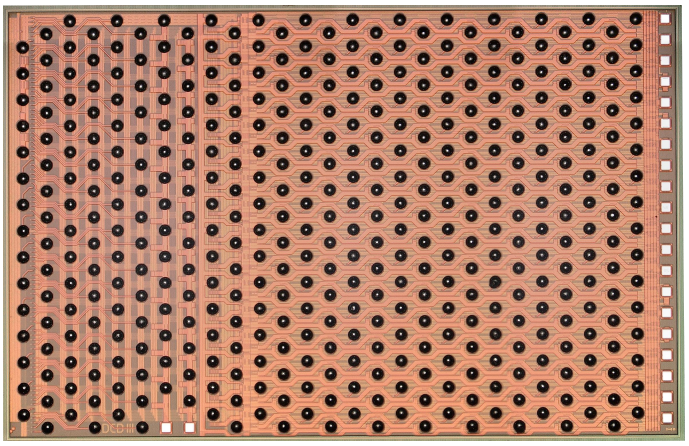


Figure 4.9: Photography of the DCD chip manufactured in 180 nm UMC technology manufactured (after [61]).

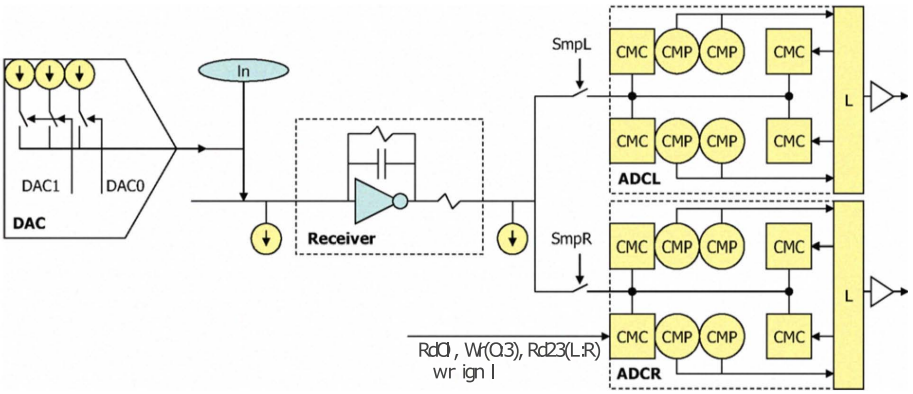


Figure 4.10: Block diagram of one channel of the DCD chip structure (after [61]).

Figure 4.10 shows a block diagram of one channel. The input current from the DEPFET and the two-bit DAC, added for pedestal correction, is amplified when passing trough a current-receiver based on a trans-impedance amplifier with a "bleeding resistor" on its output to discharge the voltage of the capacitor when power is removed. Two current-mode cyclic ADCs (ADCR and ADCL) based on current-memory cells (CMC) convert the analog signal to digital [61]. This data in sent to Data Handling Processors (DHPs) where the digital processing is carried out.

4.3 Probe station for Belle II ASICs

For the construction of the whole PXD detector of Belle II, around 400 SWITCHERs and DCDs chips are required. Since they will be bump bonded to the PXD pixel matrix, it is mandatory to test each of the ASICs before assembly, since a single malfunctioning ASIC will result in the failure of that module. For testing each chip prior to assembly, a probe station was developed at KIT. It provides the structural and mechanical needs to mount special probe cards for ASIC testing.

The probe station, shown in figure 4.11, consists of the x, y, z, and ϕ table, which moves the chips under the fixed needle card. Each axis is controlled by a stepper motor to achieve high precision and repeatability of the movements. The position of the chips under the needle card is monitored by high-resolution camera microscope. The chips are protected against unwanted movement by usage of vacuum attachment.

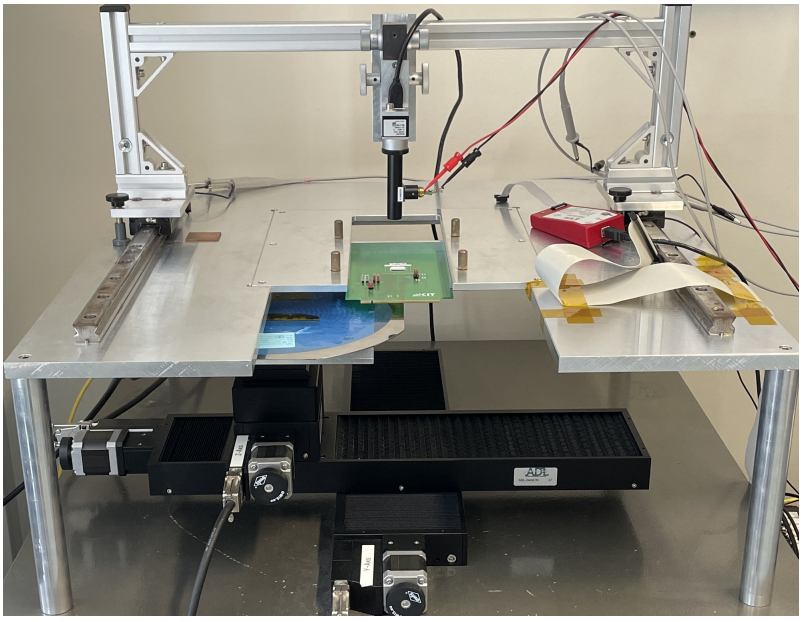
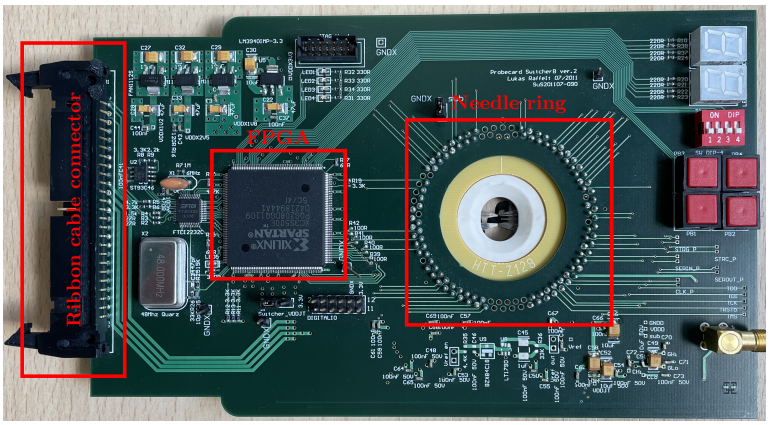


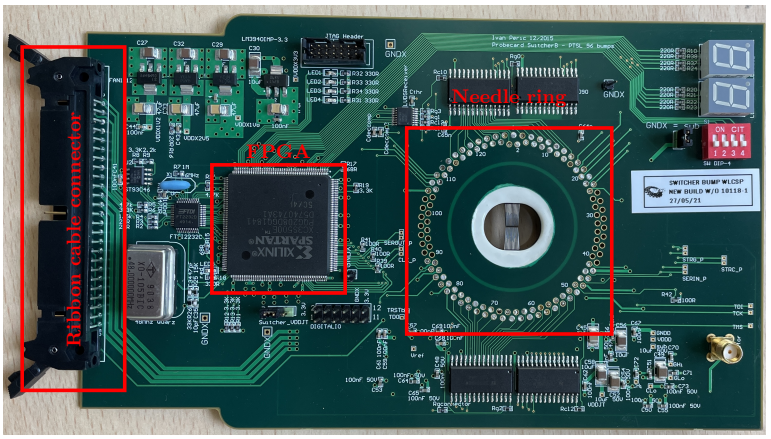
Figure 4.11: Photograph of the probe station used to test SWITCHER and DCD chips.

The process of probing a chip consists of placing it onto a surface on which a vacuum pump fixes the ASIC making it not possible to move in the any direction. Then an arrangement of needles mounted on a PCB probe-card, is moved towards the fixed chip, with the help of a microscope camera to align the needles over the pads. When those needles make contact with the chip pads, an ohmic contact between the input/output is created. By doing this it is possible to access and operate the ASIC without the necessity of bump bonding it.

Since each chip has a different pad layout and performs different operations, custom PCBs were developed (figure 4.12), each of them with a dedicated needle ring, that can contact each pad individually and connect it to the readout electronics of the PCB. The PCB is connected via a JTAG to a PC, to configure the FPGA. The voltages needed to power the chips and the high voltages for SWITCHER drivers are connected to a delivery card (figure 4.14), as well as all the input/output digital signals (connected via USB from a PC). All these voltages and signals are then routed to the probe card (figure 4.12) via a ribbon cable. A block diagram of the probe station setup is shown in figure 4.13.



(a) Probe card with FPGA and needle ring at the center for testing DCD chips.



(b) Probe card with FPGA and needle ring at the center for testing SWITCHER chips.

Figure 4.12: Probe cards developed for the test of DCD (a) and SWITCHER (b) chips.

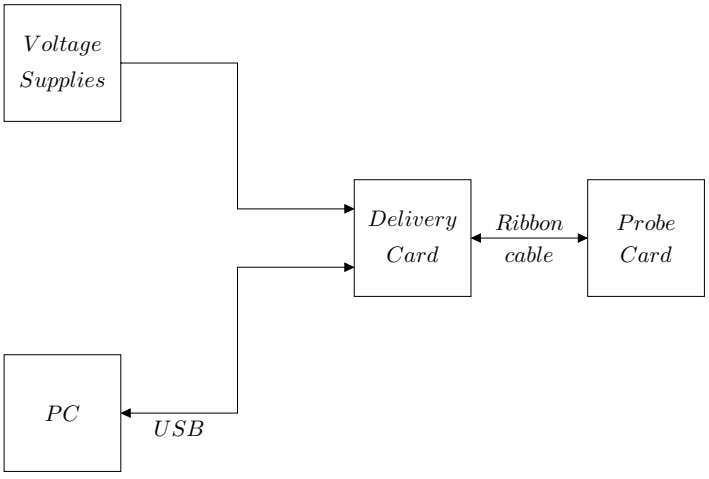
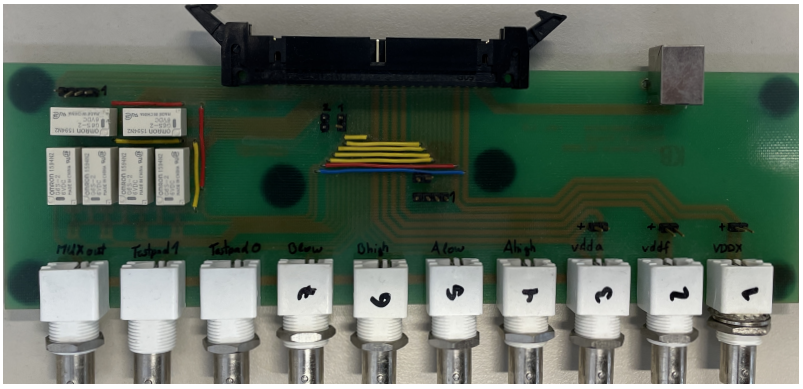


Figure 4.13: Block diagram of the probe station setup.

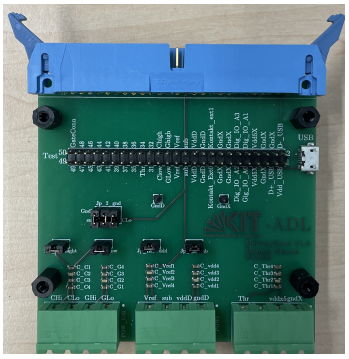
We are working in cooperation with Halbleiterlabor in Max-Planck Institute in München (HMPI[2]). I have tested 150 DCD chips and approximately 200 SWITCHERs. Based on our hardware and software design (probe cards, delivery card, as well as software

[2] https://www.hll.mpg.de/2820618/ueber-uns

and firmware) and test routine, HMPI will implement another test site to increase throughput of chips. For that purpose, I designed a new improved delivery card since an upgrade was necessary to share the design and extend the capabilities of the delivery card. The new delivery card is two times smaller, features a probe point to connect an oscilloscope probe to monitor every signal, and includes a micro-USB interface, filtering capacitors for each supply voltage, and a set of jumpers to simplify the voltage supply if needed.



(a) Old delivery card used for communication of PC and probe card via USB, and to deliver supply voltages the probe card.



(b) New design of the delivery card.

Figure 4.14: Old delivery card (a) and new design (b).

The deployed software to test the correct functioning of the ASICs was developed for an old distribution of Linux and Qt. Because of that, a migration of the software to newer versions is not possible and restricts the use of the software to only the PC on which it was running. To share this software with the group at Max-Planck, I migrate the software to the latest version of the used development framework (Qt6[3], Ubuntu 22.04.1 LTS[4], and ROOT v6.26[5]). Since our software is the only one available to test the SWITCHERs and DCDs ASICs, the group at MPI requested our probe station (software and firmware design) to set up their own testing facility. To do that I have set up a virtual machine by cloning the new software setup and sharing the files with the Belle II collaboration. My work is connected to the developments started by Dr. R. Leys. His contribution is invaluable for the success of this project.

[3] `https://www.qt.io/product/qt6`
[4] `https://ubuntu.com/download/desktop`
[5] `https://root.cern/`

5 Wire bonding

To use the ASICs developed in ADL group, it is needed to electrically connect the pads to the signals from the FPGA, as well as power and bias voltages. The size of the pads is in the scale of a hundred micrometers. That makes impossible to directly solder a wire by hand, instead a technique called wire bonding is used. Our lab has the Bondjet Bj653 form Hesse Mechatronics[1], figure 5.1 shows the wire bonder.

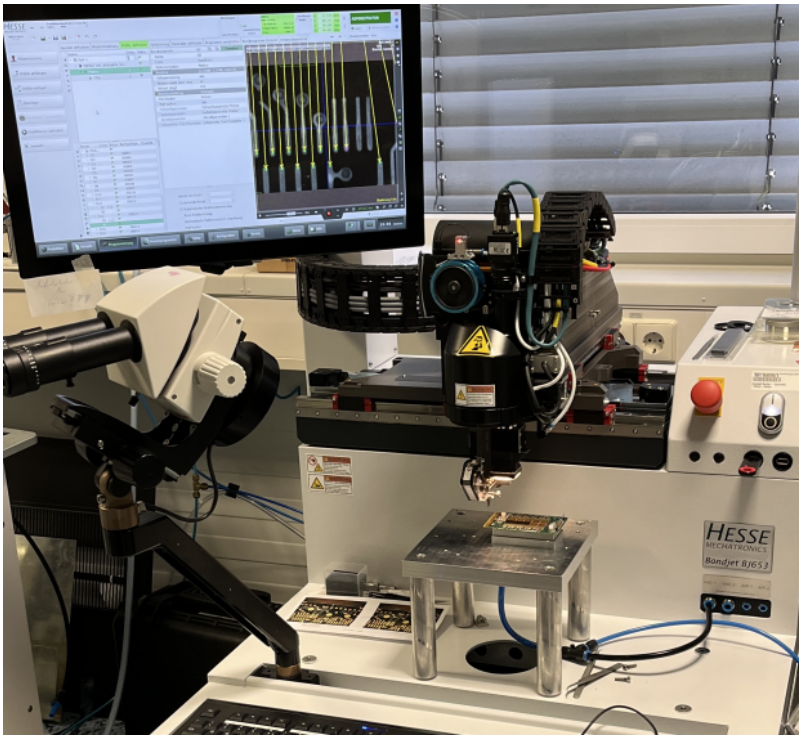


Figure 5.1: Bonder machine available at KIT.

My task was to operate the machine. The needle of the bonder feeds a thin wire (in the order of 100 µm) and it is placed over the sensor pad. Through pressure and an ultrasonic movement of the needle, the wire is fixed to the pad, as shown in figure 5.2.

[1] https://www.hesse-mechatronics.com/en/

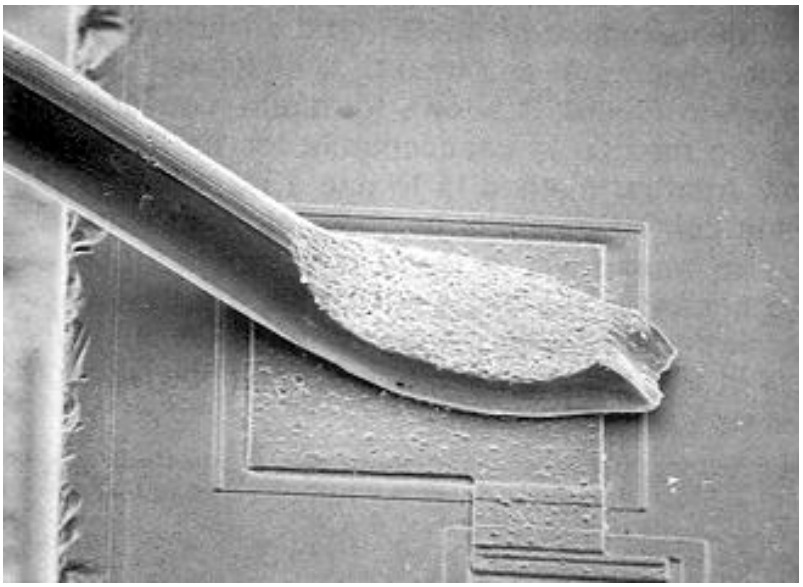


Figure 5.2: Micrography of a wire bond wedge to a chip pad (after [49])

The machine then moves the needle trough a determined path to reach the PCB pad, were the final wedge is performed and the electric connection is completed. By modifying the path that the needle travels it is possible to create a more strong and durable connection between wire and pad.

The acquisition of this ability allowed me to bond not only my sensors, but also the ones from my colleges at ADL, those are:

- PicoPix (figure C.1)
- BabyPix (figure C.2) [2]
- HitPix v1 (figure C.3) [85]
- HitPix v2 (figure C.4) [2]
- HitPix matrix (figure C.5) [85]
- AstroPix (figure C.6) [77]
- CLIC Fast [42]
- HVMAPS (figure C.7)
- MPROC (figure C.8)
- TelePix Fast (figure C.9) [8]
- Panda Fast (figure C.10)
- MightyPix (figure C.11)

Pictures of each wire-bonded sensor can be seen in appendix C

[2] Publication in review

6 Outlook

In this thesis two detector ASICs have been developed and characterized. The HPIXEL sensor, designed to work as an electron detector for electron microscopy. The second sensor, HINT, was developed for carbon ion and proton beams monitoring in radiotherapy centers with a charge integrating approach that can achieve high dynamic range with the possibility of particle counting.

- The first sensor, HPIXEL, is prototype for an imaging sensor for electron microscopy. This application is challenging because of the radiation hardness requirements. The prototype developed was fabricated in AMS 180 nm HVCMOS technology, with a matrix of 64×64 pixels, a total sensing area of 1.6 mm × 1.6 mm, and two different sensor topologies. I developed a special ceramic PCB to be placed in the vacuum chamber of the TEM, as well as an interface PCB with specific geometrical, material, and design characteristics to meet the specifications given by Thermo Fischer Scientific[1] specialists. I have also developed the software and firmware of the test system. In summary two types of measurements were performed:

  X-ray measurements: In order to characterize the sensor's ability to detect charge generated by radiation, the chip was irradiated at ETP Institute at KIT with X-rays of different energies. The aim of these measurements was to verify the sensor functionality, the linearity of the response, and radiation hardness.

  TEM measurements: The sensor was characterized at the facilities of the industrial project partner Thermo Fischer Scientific in Eindhoven. The PCB designed by me worked in a vacuum environment and fitted in the small place that was available. The sensor was able to successfully detect electron beams even for low-intensities. The spatial resolution improves with a larger magnitude of negative sensor bias voltage since the electrons are stronger attracted to the electrode collection and a cross charge collection between pixels is reduced. The radiation tolerance in electron beam was ∼213 krad, while for X-ray was at least ∼250 Mrad. I suspected that the radiation tolerance of the matrix could be higher, I have investigated this by using a second fresh chip, where the beam was focused only on the pixel matrix, to verify if the periphery electronics were not as radiation-hard as the matrix. These measurements show that the sensor matrix could withstand up to ∼30.4 Mrad before it stops working. I believe that this limit can be even higher, for the following reason:

[1] `https://www.thermofisher.com/de/de/home.html`

the matrix is small and the beam spot is large in comparison. Also the position of the beam spot was not precise, it was not possible to completely avoid hitting the periphery electronics, resulting in radiation damage to the periphery electronics.

To improve the radiation hardness of the periphery electronics, I re-designed the sensor layout. By placing a gap between the sensor matrix and the periphery electronics it is possible to shield the weak part of the design. I have also implemented, beside radiation hardening, a re-design of the digital part of the sensor to use serial communication, instead of parallel, to reduce the noise generated by the cross-talk of digital signals.

I compared both sensor topologies, the current pixels that can perform correlated double sampling (CDS) measurements and the voltage pixels which are simpler but can not perform CDS. The x-ray measurements results show that the voltage pixels didn't perform as well as the current pixels (more complex design). The voltage pixels showed a lower amplification (as expected) with a higher noise (about 1.3 times higher). Due to this findings I recommend the usage of the current flavor for further development, since they have larger gain, the possibility to use CDS mode, and lower the output noise.

- The second sensor discussed in this thesis is the HINT, which is designed to monitor a medical ion beam, more precisely therapy with carbon ions and protons, used in the Heidelberg Ionenstrahl-Therapiezentrum (HIT)[2]. The sensor electronics performs integration of the current generated in the silicon substrate by the incident particles. The integrator employs a charge pump and a counter that counts how many times the integrator was discharged in a period of time which leads to a linear, wide dynamic range, without amplifier saturation. The sensor is fabricated by TSI in 180 nm HV technology, which allows reverse bias voltages up to -120 V, to increase the charge signal of the sensor, and with a radiation hard approach using enclosed transistors.

  The HINT chip designed was characterized in the laboratory with an infra-red fast pulsed emitting laser, to verify its functionality and characterize it. The chip has a linear response up to the maximum charge possible (∼2700 fC), with a noise floor of about 0.8 fC.

  After the laboratory measurements, the chip was measured under carbon ion and proton beams at Heidelberg Ionenstrahl Therapiezentrum, with different energies and intensities, as well as with different reverse bias voltages and integration times. The results of these measurements show that the sensor behaves linearly in the entire dynamic range as the intensity of the beams increase. The sensor can accurately determine the beam profile, and it is possible to see how the increment of the beam energy of carbon ions leads to a decreased input signal.

  The application of a bias voltage of -45 V (half of the breakdown voltage measured) results in an increase of 1.3 times of the sensor charge collection to respect of bias voltage of -10 V.

  It was also demonstrated that it is possible to use the sensor as a beam positioning device by off-line processing the data, and accurately obtaining the *xy* beam position as well as its spread or focus.

  By increasing the clock speed, it is possible to obtain measurements of an intense beam across multiple frames, thus virtually increasing the dynamic range. The fastest reliable clock speed tested was 2.5 MHz, with theoretically no lower limit. However,

[2] `https://www.klinikum.uni-heidelberg.de/interdisziplinaere-zentren/heidelberger-ionenstrahl-therapiezentrum-hit`

higher clock speeds come at the cost of high variability in the measurements due to the beam presenting high fluctuations under 1 ms of integration time. Slower clock speeds offer more reliable measurements but may lead to sensor saturation when dealing with intense beams.

Further measurements are needed to verify the radiation tolerance of the sensor.

Because of the absence of a latch circuit, it is currently not possible to do a readout during measurement. I suggest to modify the current design to allow continuous readout during measurements, to increase the speed of the effective frame rate.

The ADL group at KIT takes part on the Belle II experiment. We developed the SWITCHER and DCD chips and contributed to module assembly by testing the SWITCHER and DCD ASICs before are bump bonded to the VXD detector. During this thesis 150 DCDs and 200 SWITCHERs were tested, with a yield of 99.3% for DCD and 92.5% for SWITCHERs, which is an important contribution to one very interesting detector assembly: Belle II pixel detector.

In addition to the support given by testing the DCD and SWITCHER chips, the sensor probe station was improved by designing and assembling a new delivery card PCB to act as an interface between the probe card and the PC, as well as by updating the outdated software and firmware of the setup and by making them portable to share with the group at Max-Planck Institute.

During the time of my Ph.D., it was required to wire bond and test a large number of sensors. For this purpose, I developed an universal PCB, on which any sensor of up to 6 mm $\times$ 6 mm of area and up to 32 pads per side can be wire bonded. This design was done with minimum-length tracks and differential pair tracks. The design gives flexibility since it is possible to glue any sensor with the given pin count designed by the ADL group and wire bond them easily. With the addition of the 96-line PCI-express type connector, the PCB can be connected to the versatile GECCO system.

Finally, I learned wire bonding of chips, a valuable skill, not only for my research but also for the whole ADL group. This allowed me to increase the speed at which any college of the group could have the sensors wire bonded, shortening the waiting time from weeks to a couple of hours.

Appendix

A HPIXEL

A.1 Pads

Figure A.1 shows the dimensions and position of the pads of the HPIXEL. The numbering of the pads starts on the top left pad and increases clockwise. This information is crucial to generate the bonding plan as well as for designing the carrier PCB where the chip will be bonded.

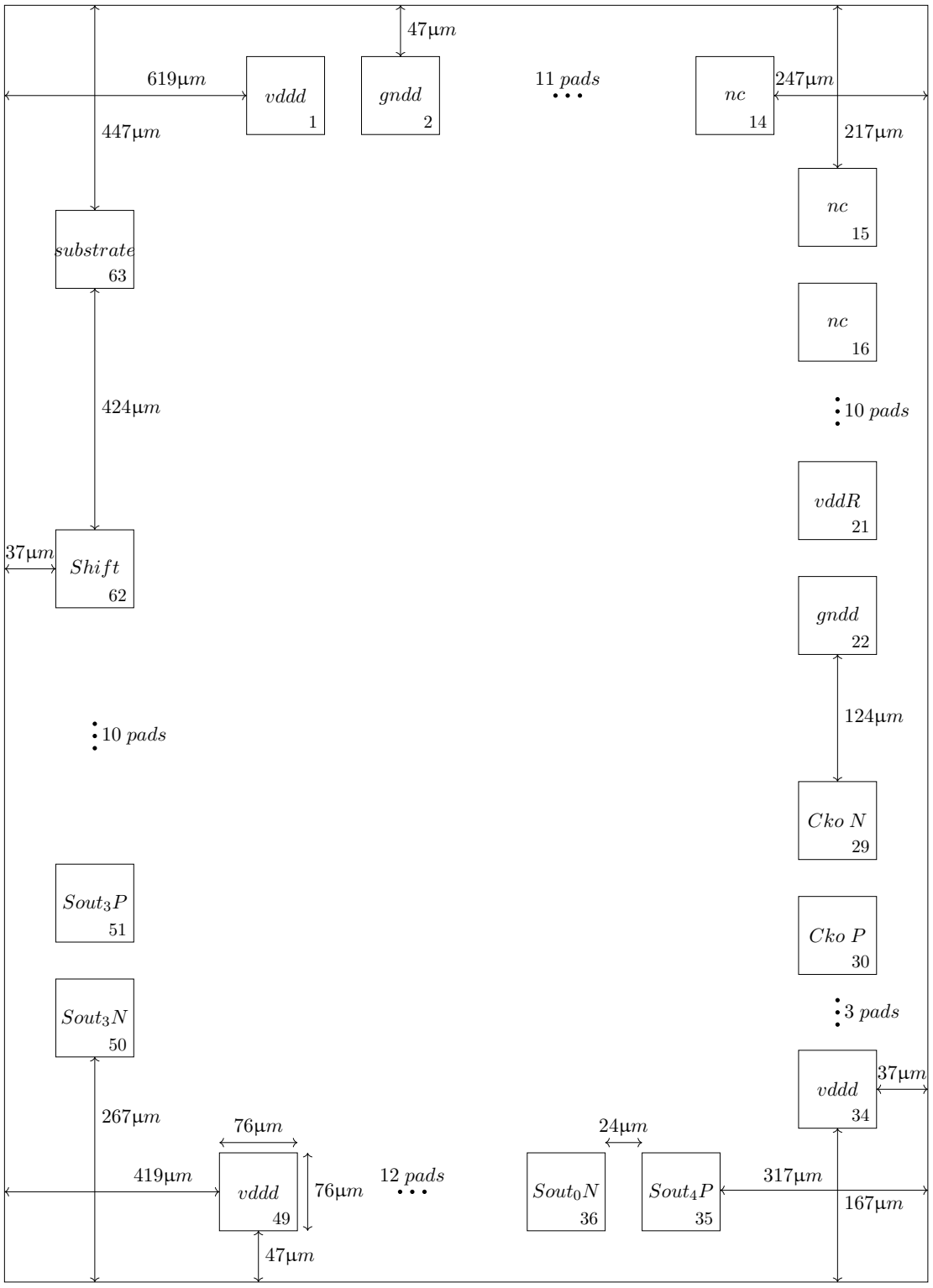


Figure A.1: Dimensions and positioning of the pads of HPIXEL.

In figure A.1, all the pads are the same size (76 µm × 76 µm), and the clearance between adjacent pads is the same (24 µm) unless stated otherwise.

Table A.1: List of pads and its function of the HPIXEL.

Number	**Name**	**Function**
1	*vddd*	Digital voltage supply
2	*gndd*	Digital ground
3	*DACCk*	Clock signal of the DAC used in the bias-block
4	*DACSin*	Serial in data of the DAC used in the bias-block
5	*DACLd*	Load signal of the DAC used in the bias-block
6	*DACEn*	Enable signal of the DAC used in the bias-block
7	V_{ref}	Voltage reference for the reference mode measurement
8	V_{casc}	Cascode voltage of the amplifier in amp-ADC block
9	V_{th}	Voltage threshold for the comparator in amp-ADC block
10	*VResetHi*	Reset diode high voltage
11	*VResetLo*	Reset diode low voltage
12	*nc*	Not connected
13	*vss*	Voltage supply of the charge amplifiers
14	*nc*	Not connected
15	*nc*	Not connected
16	*nc*	Not connected
17	*substrate*	Substrate contact for sensor bias
18	*gnda*	Analog ground
19	*vdda*	Analog voltage supply
20	*vddd*	Digital voltage supply
21	*vddR*	Voltage supply of the mirror transistor of VPR
22	*gndd*	Digital ground
23	*nc*	Not connected
24	*nc*	Not connected
25	*nc*	Not connected
26	*nc*	Not connected
27	*nc*	Not connected
28	*nc*	Not connected
29	Ck_oN	Output clock LVDS negative signal
30	Ck_oP	Output clock LVDS positive signal
31	$Sout_4N$	Negative LVDS serial output 4
32	*vddd*	Digital voltage supply
33	*gndd*	Digital ground
34	*vddd*	Digital voltage supply
35	$Sout_4P$	Positive LVDS serial output 4
36	$Sout_0N$	Negative LVDS serial output 0
37	$Sout_0P$	Positive LVDS serial output 0
38	$Sout_5N$	Negative LVDS serial output 5
39	$Sout_5P$	Positive LVDS serial output 5
40	$Sout_1N$	Negative LVDS serial output 1
41	$Sout_1P$	Positive LVDS serial output 1
42	$Sout_6N$	Negative LVDS serial output 6
43	$Sout_6P$	Positive LVDS serial output 6
44	$Sout_2N$	Negative LVDS serial output 2
45	$Sout_2P$	Positive LVDS serial output 2
46	$Sout_7N$	Negative LVDS serial output 7
47	$Sout_7P$	Positive LVDS serial output 7

48	*gndd*	Digital ground
49	*vddd*	Digital voltage supply
50	$Sout_3N$	Negative LVDS serial output 3
51	$Sout_3P$	Positive LVDS serial output 3
52	*ConRef*	Multiplexer select signal at the input of amp-ADC block
53	*ResADC N*	Negative LVDS shift signal for ADC output
54	*ResADC P*	Positive LVDS shift signal for ADC output
55	*Ck N*	Negative LVDS clock of the ADC
56	*Ck P*	Positive LVDS clock of the ADC
57	*ResetAmp*	Reset amplifier in amp-ADC block
58	*Toggle*	Controls the double capacitor circuitry in amp-ADC block
59	*ResetPix1*	Signal used to reset the diode sensor in the pixels
60	*ResetPix2*	Signal used to reset the charge amplifier in the pixels
61	*Samp*	Signal used to store the charge in the pixels
62	*Shift*	Signal used synchronize the row control blocks
63	*substrate*	Substrate contact for sensor bias

A.2 State machine of the input-output manager

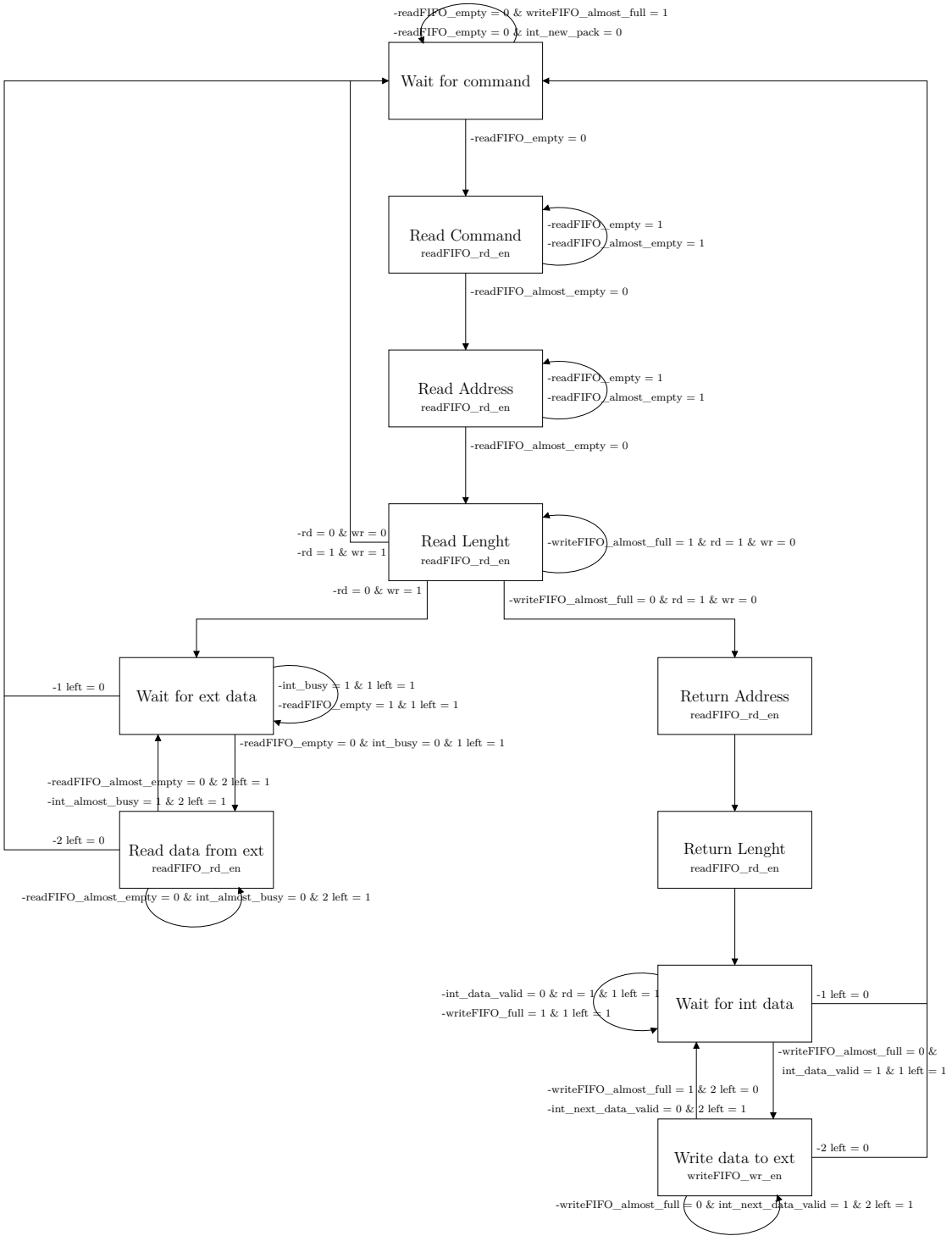
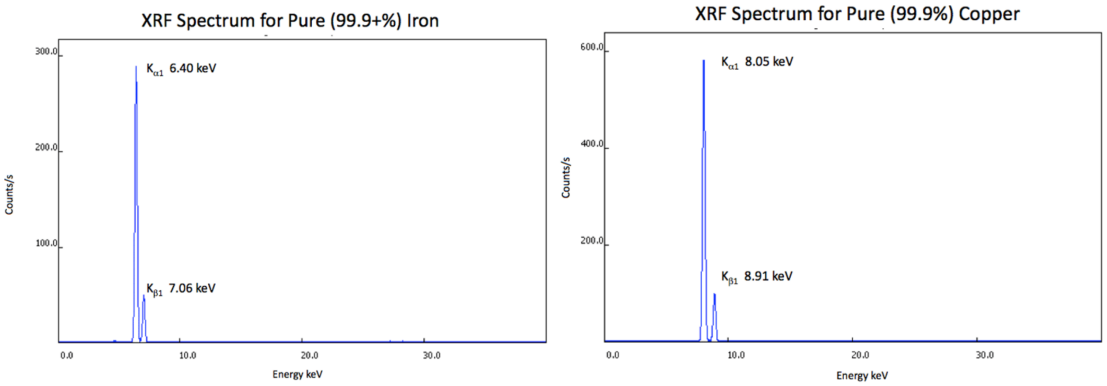


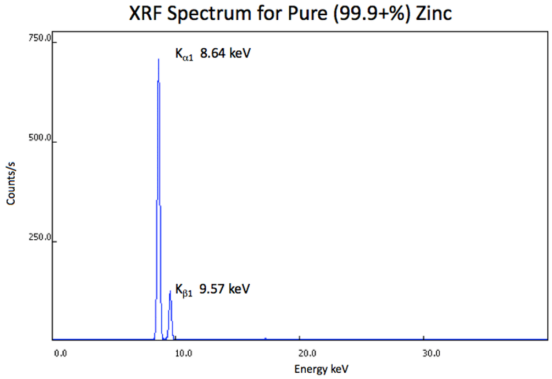
Figure A.2: State-machine flow chart of the IO manager for the firmware of HPIXEL.

A.3 X-ray fluorescence spectrum of targets used

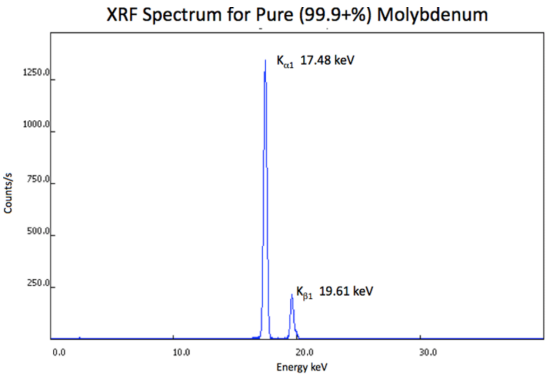


(a)

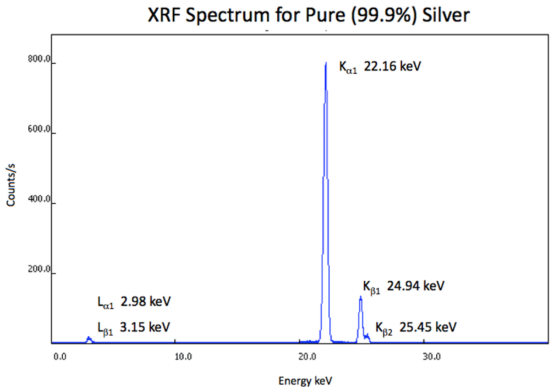
(b)



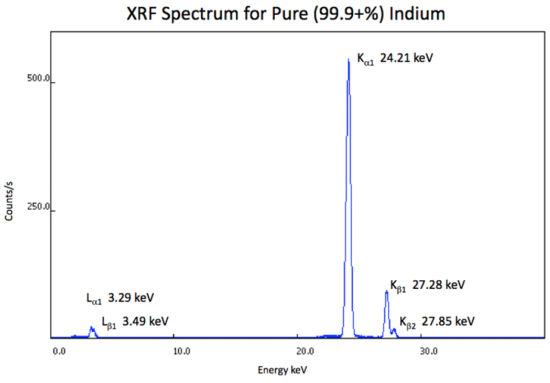
(c)



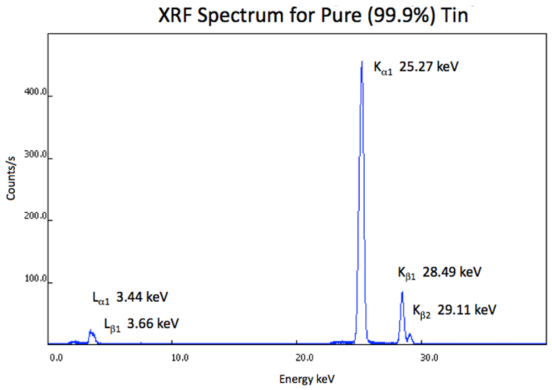
(d)



(e)



(f)



(g)

Figure A.3: X-ray fluorescence energy spectrum of the targets used: (a) Iron, (b) Copper, (c) Zinc, (d) Molybdenum, (e) Silver, (f) Indium, and (g) Tin (extracted from`http://www.xrfresearch.com/xrf-spectra/`).

B HINT

B.1 Periphery electronics

B.1.1 Column control

In this section, the column control block will be discussed. It is placed at the bottom of each 24-pixel column, where the periphery of the chip starts. Figure B.1 shows the layout of the column control block implemented on the sensor. Figure B.2 shows the schematic of this block, which buffers the signals *TimeIn*, *CkIn*, *FrameIn*, *LdROIn*, and *Bus*.

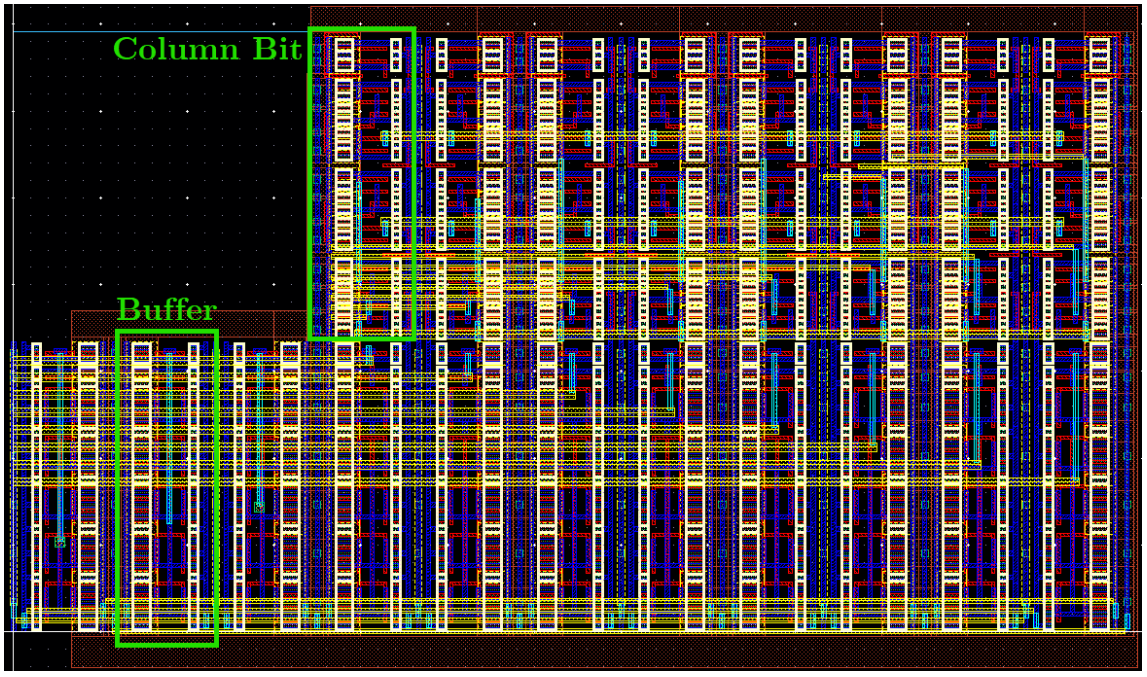


Figure B.1: Layout of the column control block designed. The top half corresponds to each of the 8 column bits. In the bottom half, the 11 buffers are placed.

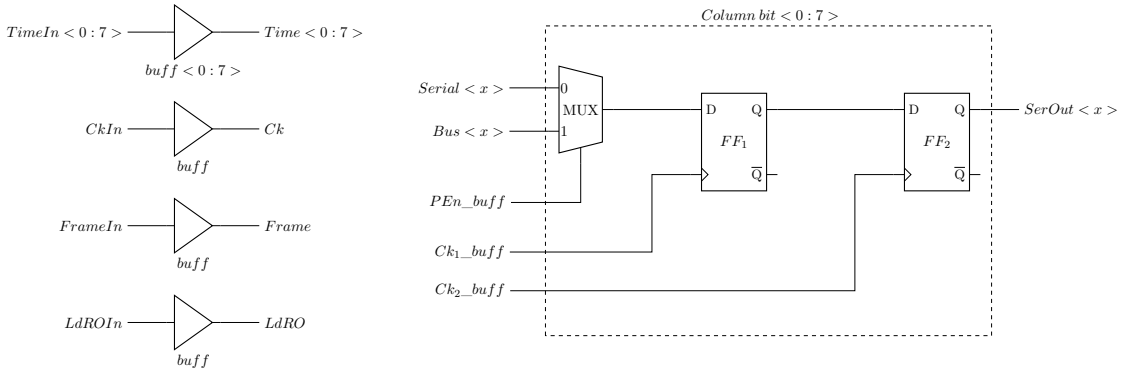


Figure B.2: Logic schematic of the column control block.

This block drives some of the signals that are used by 24 sensors in each column. In addition, there is a multiplexer that selects serial or parallel input, and two latches with two non overlapping clocks (Ck_1_buff and Ck_2_buff).

By controlling *PEn*, either the data from bus can be stored or the bits stored in the latches can be shifted.

B.1.2 Row control

The second block placed at the bottom of each column, in the periphery of the chip, generates the signals to control when each data set (number of pumps, and the two time-stamps) acquired by the sensors will be multiplexed to the column *Bus*. This is done by using a series of consecutive signals (*EnBusPump*, *EnBusFirst*, and *EnBusLast*). Figure B.3 shows the layout of the row control block designed.

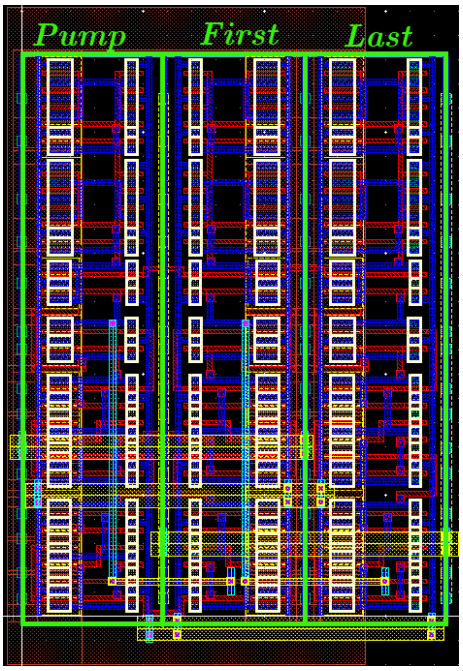


Figure B.3: Layout of the row control block. Each column corresponds to *EnBusPump*, *EnBusFirst*, and *EnBusLast*.

The block is a 3-bit shift register (figure B.4). The layout of the design is shown in figure B.3 while the block diagram is presented in figure B.5. In this way, it is possible to obtain a waveform as shown in figure B.6; two signals will never be "1" at the same time. *Ck₁Row_buff* and *Ck₁Row_buff* are generated by the *Clock Buffer* based on signals from *ROMUX* block (discussed in section B.1.5).

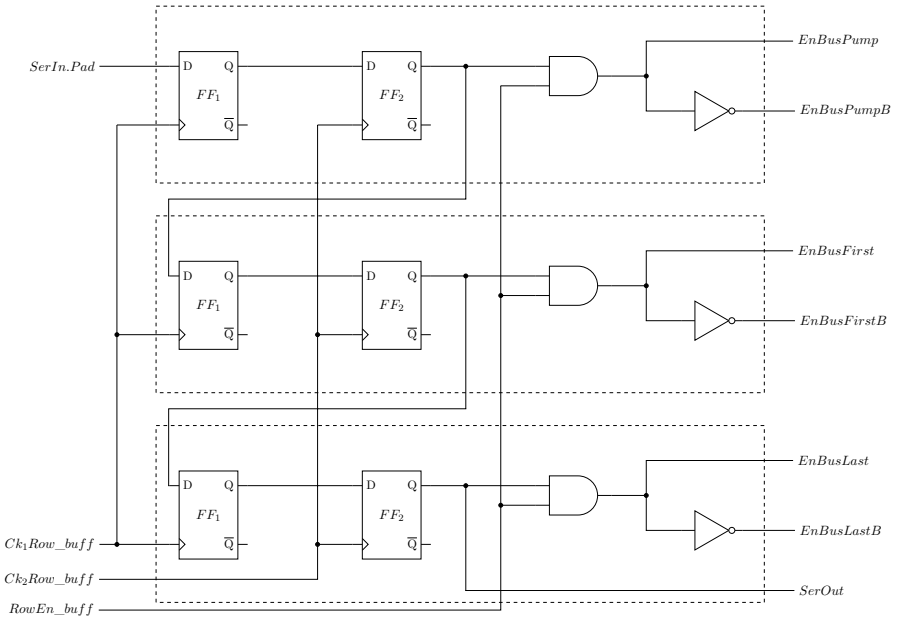


Figure B.4: Logic schematic of the row control block.

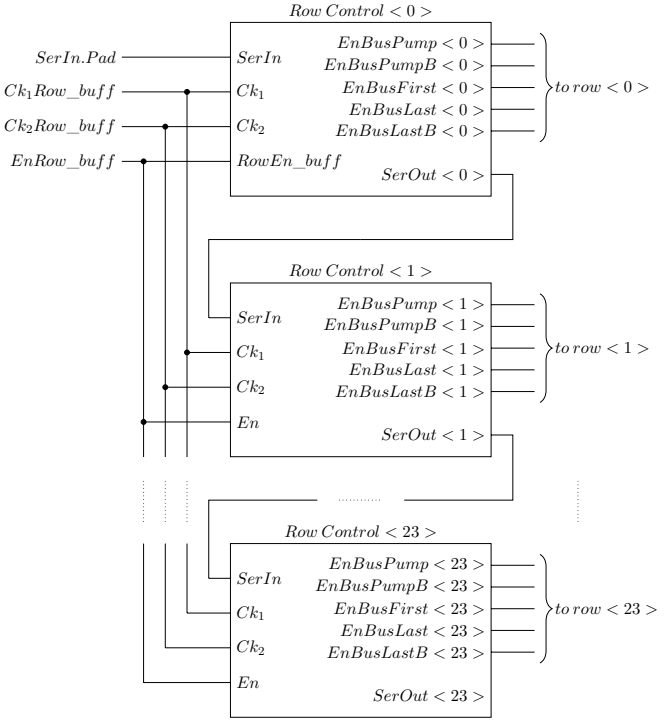


Figure B.5: Schematic of the row control blocks interconnected to each other to properly sequence the signals.

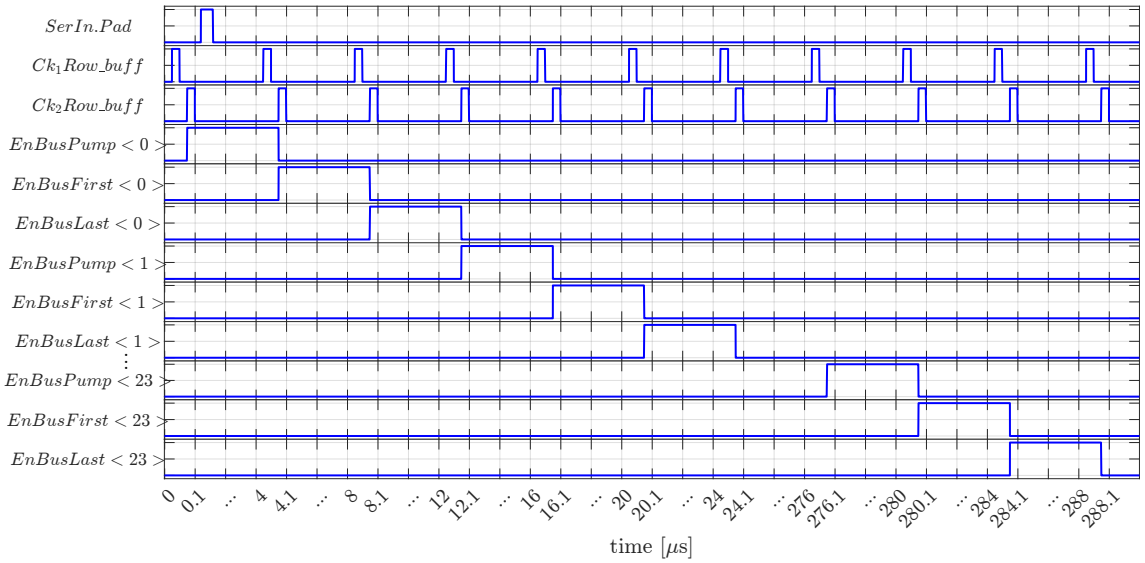


Figure B.6: Enable Bus signals waveform as function of time, showing how the system designed creates a sequential pulse on each *EnBusPump*, *EnBusFirst*, and *EnBusLast* line of each row control block.

SerIn.Pad is generated by the FPGA, and is to be the seed of the pulse train. After all the *EnBus* signals are generated, it will be needed a new *SerIn.pad* pulse to start the new sequence.

B.1.3 Global counter and buffers block

Another necessary blocks, placed at the periphery, generates the time-stamp counter and the buffers for some of the distributed signals. The layout of this block can be seen in figure B.7. The signal *LdRO* (load row output) and *FrameIn* are also generated in this block. Figure B.8 shows the schematic of this block.

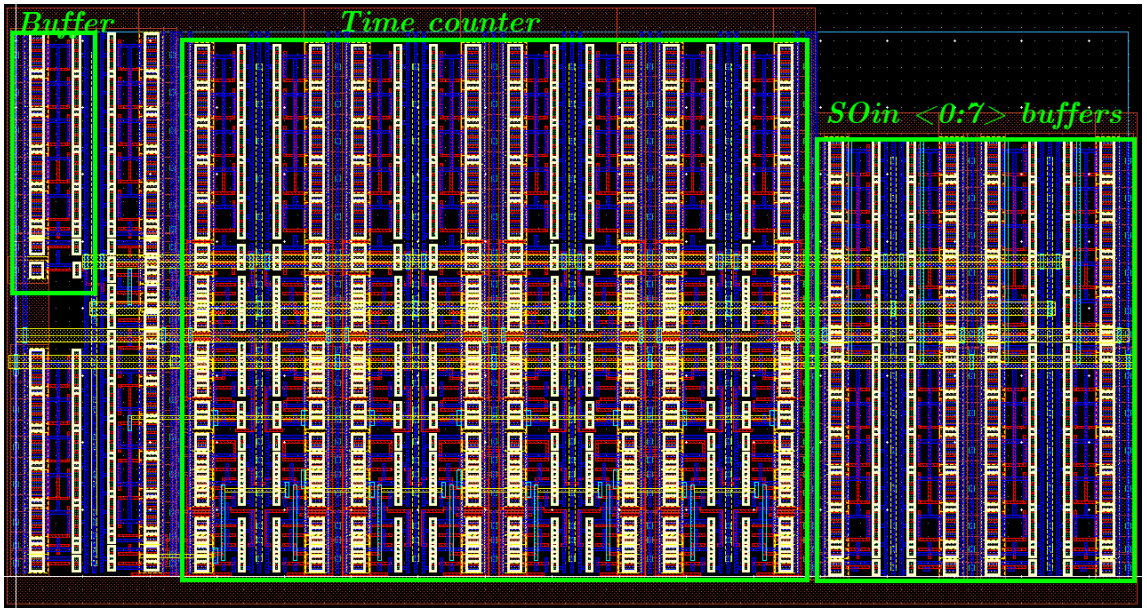


Figure B.7: Layout of the global counter block. In the center the 8 bits of the time counter are placed. At the right the 8 buffers for the signal input are located. On the left side, the other buffers and circuitry are present.

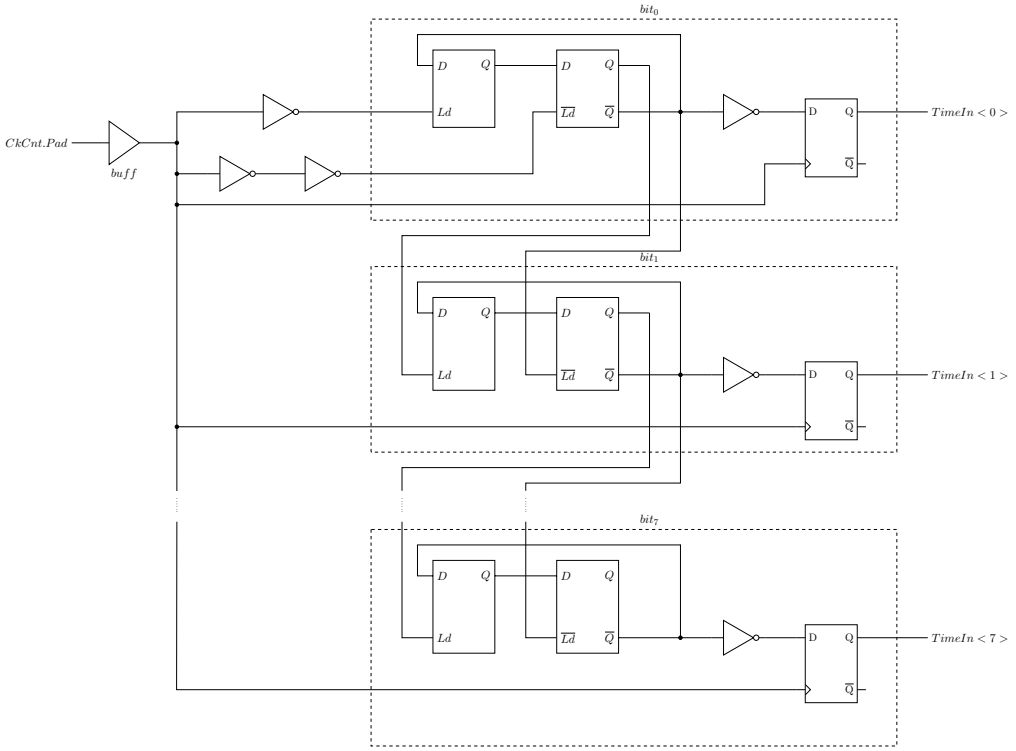


Figure B.8: Schematic of the *Time* counter.

Figure B.8 is the schematic of the counter [9] with a time base defined by *CkCnt.Pad*. This counter generates the 8-bit signal *TimeIn*, used for the time stamps. Since it is an 8-bit counter its maximum value is 255. To avoid overflow, *CkCnt.Pad* should be a square wave with a 50% duty cycle and a period equal to $T_{Frame}/256$.

B.1.4 Clock buffer

This block drives the *Ck1*, *Ck2*, *PEn* (parallel enable), and *RowEn* signals and generates Ck_1Row_buff and Ck_1Row_buff signals. These last two are fundamental for the correct timing of *EnBus* signals. Figure B.9 shows the layout created for this block, and figure B.10 shows the schematic of the block

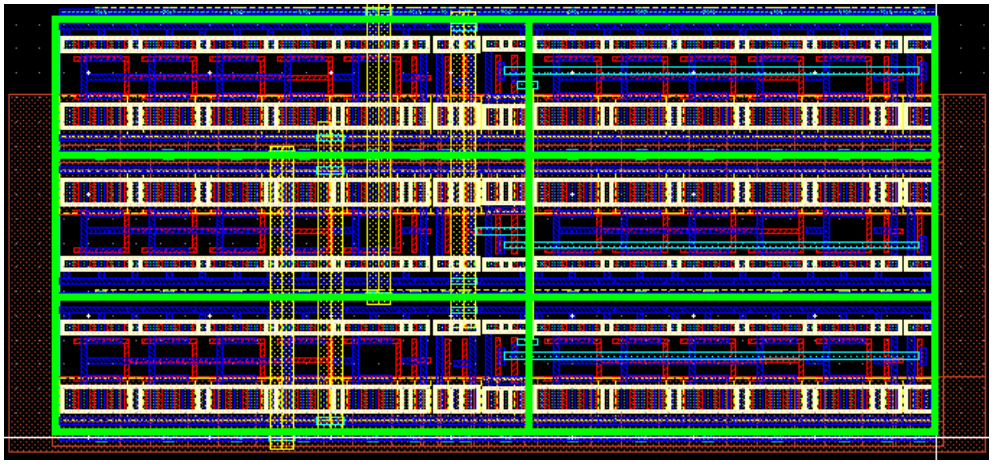


Figure B.9: Layout of the clock buffer block containing each one of the six buffers.

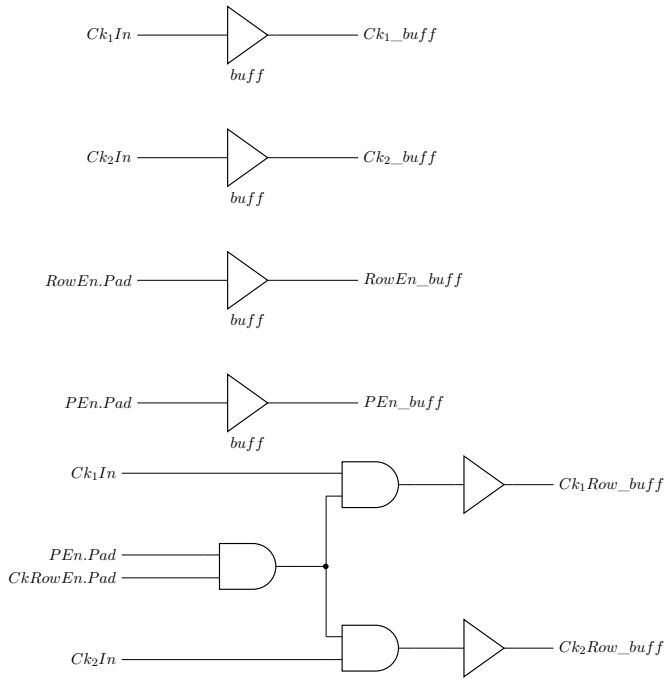


Figure B.10: Logic schematic of the clock buffer counter.

This block will drive the signals *Ck1In* and *Ck2In* to be used inside each sensor of the matrix. It will also drive *RowEn.Pad*, a signal generated by the FPGA that will enable the generation of *EnBusPump*, *EnBusFirst*, and *EnBusLast* signals.

Another important signal, buffered in this block, is *PEn_buff* (parallel enable). This signal, generated by the FPGA, will select the output of the multiplexer of figure B.2.

The logics generates *Ck1Row_buff* and *Ck2Row_buff*. This two clocks are equal as *Ck1In* and *Ck2In* when *CkRowEn.Pad* is "1". The row control block (figure B.4) generates the sequential signals *EnBus* only when *PEn.Pad* is "1".

B.1.5 Read-out multiplexer

This block has two functions, to generate the *Ck1* and *Ck2* signals, and to convert the 8-bit pixel output into 2-bit. Figure B.11 shows the layout implemented for this block.

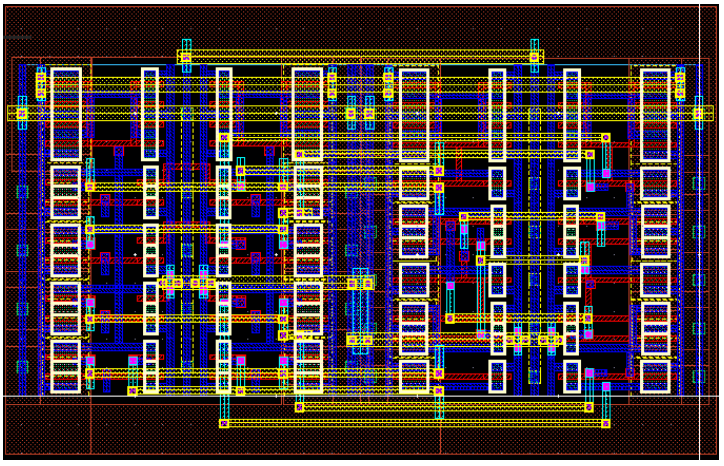


Figure B.11: Layout of the ROMux block.

Clock generation

This block generates the two clock signals necessary to shift the data out. Figure B.12 shows the schematics of the block.

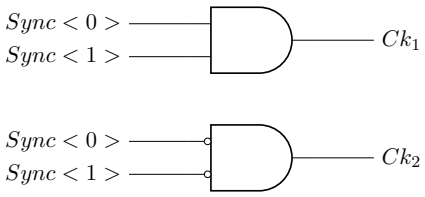


Figure B.12: Schematic of the logic for Ck_1 and Ck_2 generation.

The signal pattern of $Sync<0>$ and $Sync<1>$ can be seen in figure B.13, as well as the outputs Ck_1 and Ck_2, two non overlapping clocks.

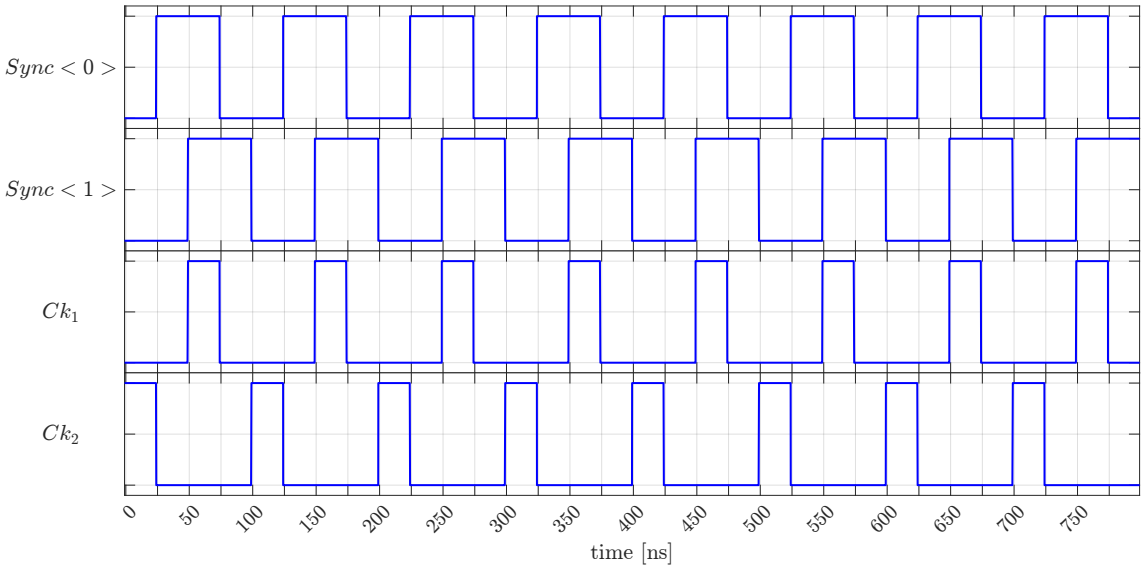


Figure B.13: $Sync<0:1>$, Ck_1, and Ck_2 waveform as function of time.

8-bit to 2-bit output conversion

To minimize the noise created by cross-talk [15] between the output lines without increasing the amount of output lines or to reduce too much the read-out speed, it was decided to serialize the 8-bit output into 2-bit, then transform those two lines into LVDS. The total amount of pins will be four.

In order to be able to decode the 2-bit output on the FPGA side, it is necessary to have an 8-bit pixel output with the same frequency as signals $Sync<0>$ and $Sync<1>$. The schematic of the system that performs that conversion is shown in figure B.14.

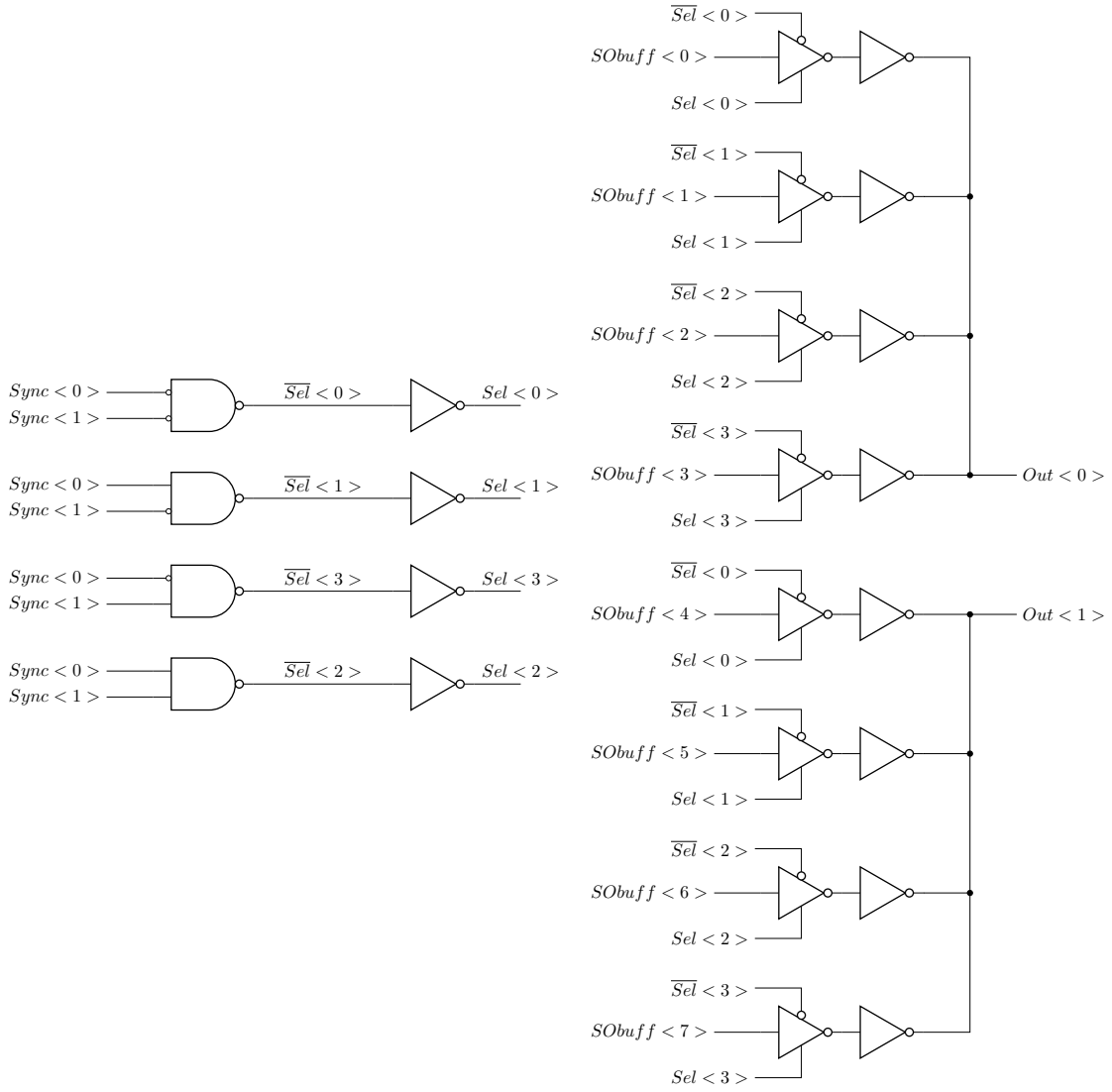


Figure B.14: Schematic of the logic for 8-bit to 2-bit converter.

In order to do the conversion, it is necessary to generate four sequential pulses, to enable each of the *Not* gates without overlapping the signal present at each *Out*. For this purpose, $Sel<0:3>$ signals are created, each of them will let the correct *SObuff* be present at the output lines *Out*. Figure B.15 shows the waveform of $Sel<0:3>$ and how they are compared to $Sync<0:1>$.

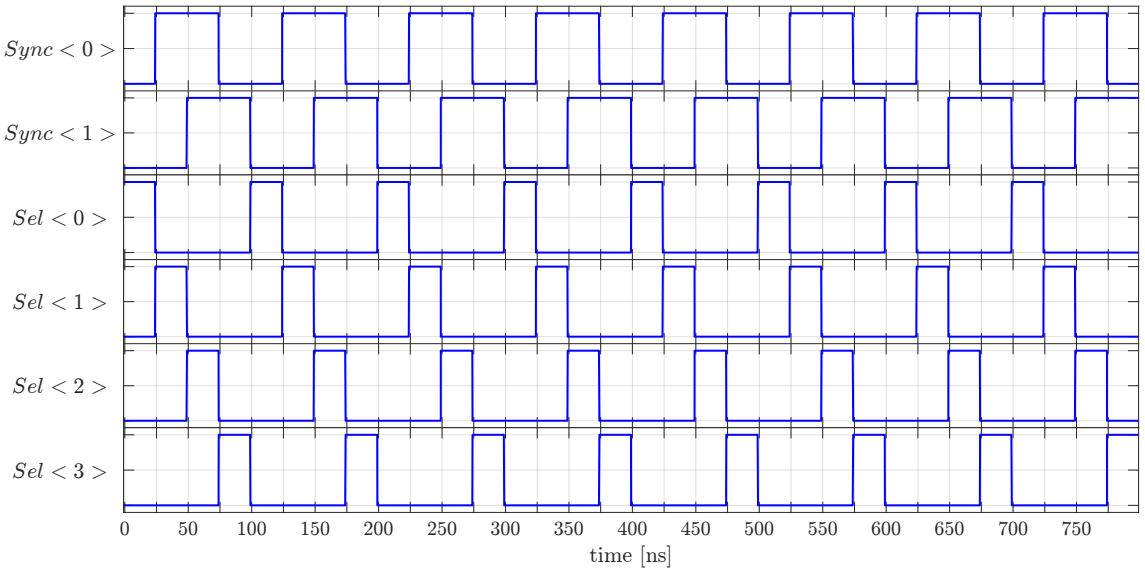


Figure B.15: *Sync*< 0 : 1 > and *Sel*< 0 : 3 > waveform as function of time. *Sel*< 0 : 3 > presents a pulse sequentially every 100 ns.

An example for a certain *SObuff*< 0 : 7 > values, and how they are present at *Out* when the *Not* gates are enabled is shown in figure B.16. Depending on which *Sel* signal is on, the output will have only one *SObuff*, in this way, four parallel signals are transformed into one serial signal four times faster.

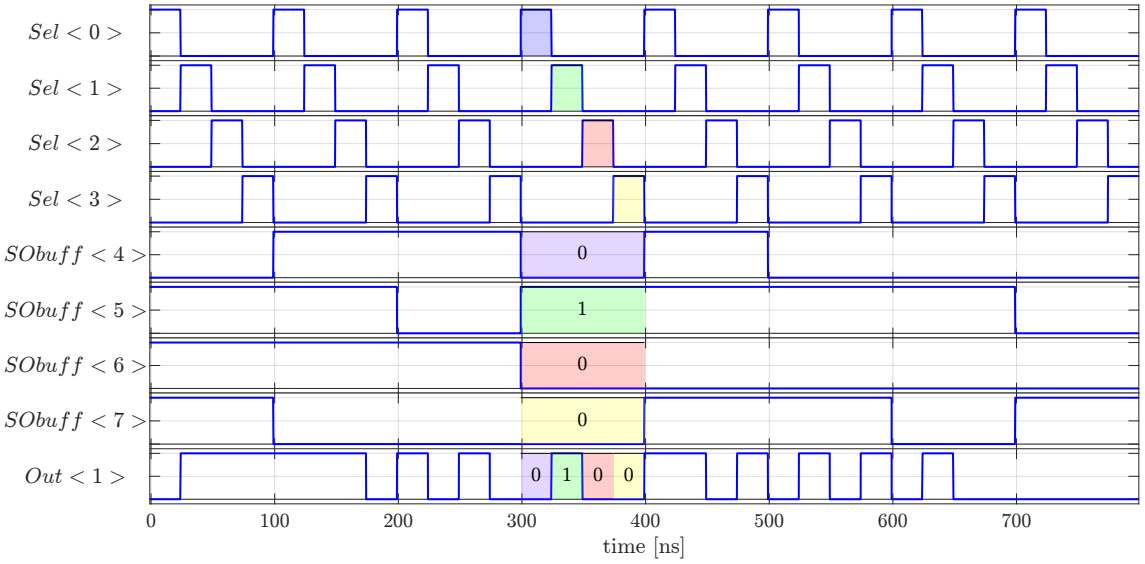


Figure B.16: Value of *Out*< 1 > for a certain *SObuff*< 4 : 7 > data. Each color represents the value of one of the four *SObuff* lines that are compressed to fit the last four bits in 100 ns time of *Out<1>*.

B.1.6 Bias-block

The Bias-block receives the DAC setting from the FPGA and generates bias voltages for the pixels. Figure B.17 shows the schematic of this block.

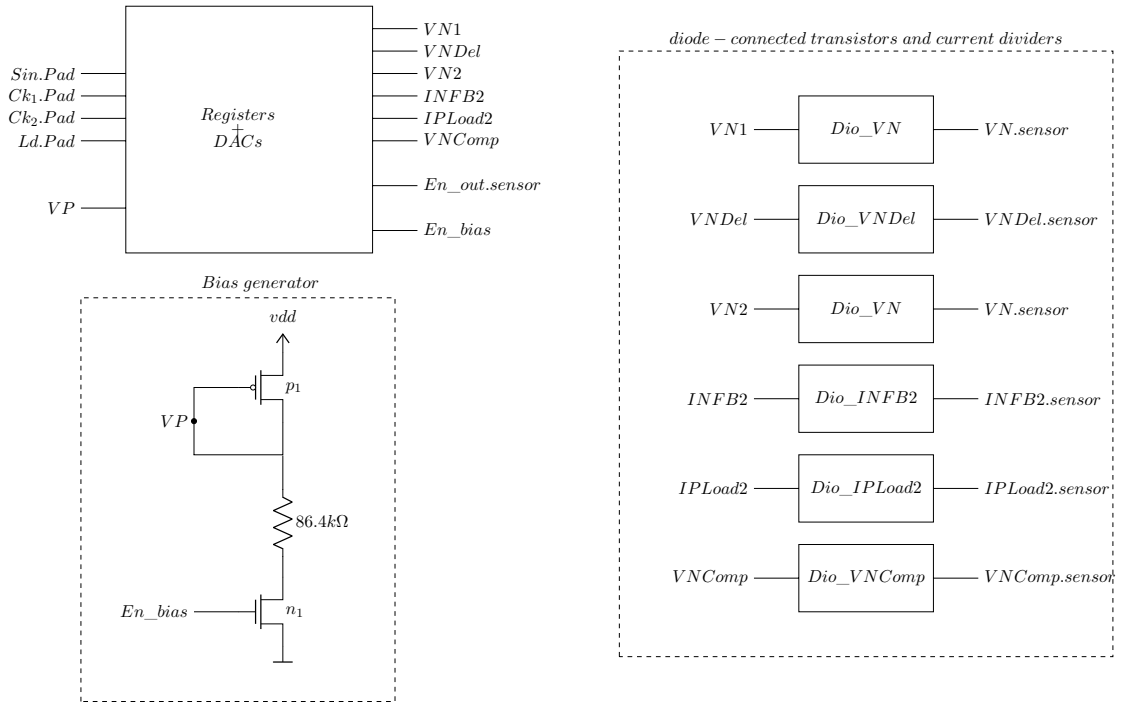


Figure B.17: Schematic of the main blocks (Register and DACs, bias generator and current dividers with diodes).

The Bias-block consists of three main parts:

- Registers and DACs.
- Bias voltage generator.
- Current dividers with diode-connected transistors.

Figure B.18 shows a detailed schematic of the 6-bit current source DAC. By performing a simulation on *Cadence* with the *ADL L* tool, it is possible to check that the current I_{ref} is 15 µA. Equation 6.1 shows the formula to calculate the output current *IOut*.

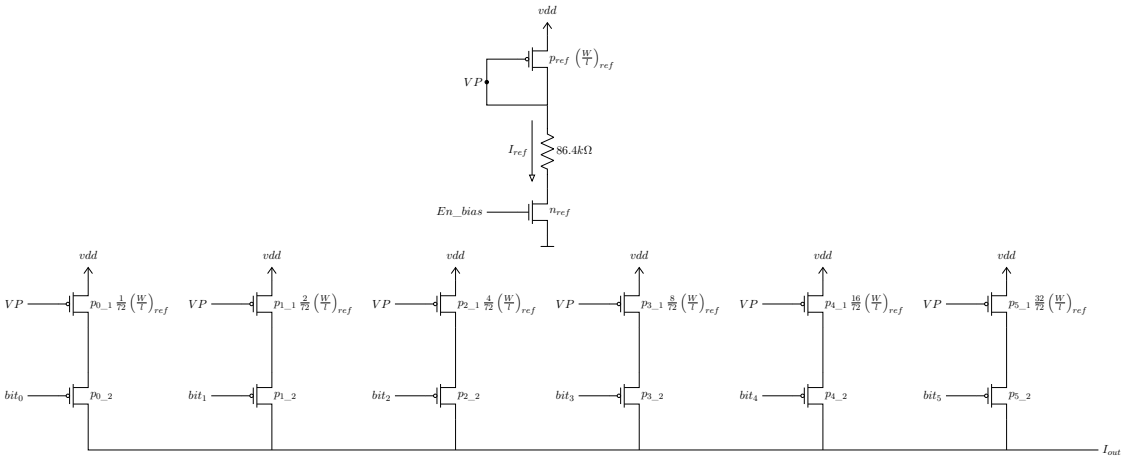


Figure B.18: Transistor level schematic of the 6-bit coded current-source DAC.

$$I_{out} = \frac{I_{ref}}{72} * \sum_{n=0}^{5} bit_n * 2^n \tag{6.1}$$

The DAC values configure how much current the following parts of the sensor will consume:

- Amplifier of the integrator (VN1 and VN2).
- Comparator (VNComp).
- Load element of the comparator (IPLoad2).
- Delay block for *PumpSlow* signal (VNDdel).
- Leakage current for the pixel (INFB2).

Those currents should be as small as possible, since that will lead to less power consumption, and lower voltage drops across the sensor. However, small currents will lead to slower transistors, and thus, slower comparators, amplifiers, etc. Some nominal currents need to be smaller than the resolution of the 6-bit current source shown in figure B.18, each *Dio current source* was designed to divide the I_{out} current by a fixed value.

By design, the nominal currents should be approximately as shown in table B.2.

Table B.2: Nominal current values.

Nominal current in the current source in pixel	Value
Amplifier	4 µA
Comparator	2 µA
Amplifier's cascode	500 nA

Since some nominal currents are smaller than the resolution of the 6-bit current source shown in figure B.18, I_{out} currents are divided as shown in table B.3.

Table B.3: Current divider value of each *Dio current source*.

Current	Divider value
Dio_VN	2
Dio_INFB2	65536
Dio_VNComp	1

In table B.3, the current divider value for the *Dio_VN* is equal to 2, because there are two separate diodes sourcing current to the same point.

All the current sources here implemented are PMOS type, to ensure that the currents will flow from *vdd* to *gnd*.

From nominal currents and divider values, it is possible to calculate the DAC value that needs to be set to obtain the desired currents. Table B.4 presents those values.

Table B.4: Recommended DAC values to operate the sensor.

Bias Block Name	Sensor	Recommended value
VN1	Amp Current	10
VNDel	Delay	30
VN2	Amp Current	10
IPLoad2	Cascode Amp Current	2
VNComp	Comparator Current	10
q00	Connect resistor for termination	1
q01	Output enable	1
qon	4-bit Turn on DAC	10

B.2 Pads

Figure B.19 and figure B.20 shows the dimensions and position of the pads of normal and separated HINT. Both chips follow the same pattern, with the exemption of one extra pad in separated HINT sensor. The numbers of the pads increases from left to right. This information is needed to generate the bonding plan as well as to designing the carrier PCB where the chips will be bonded.

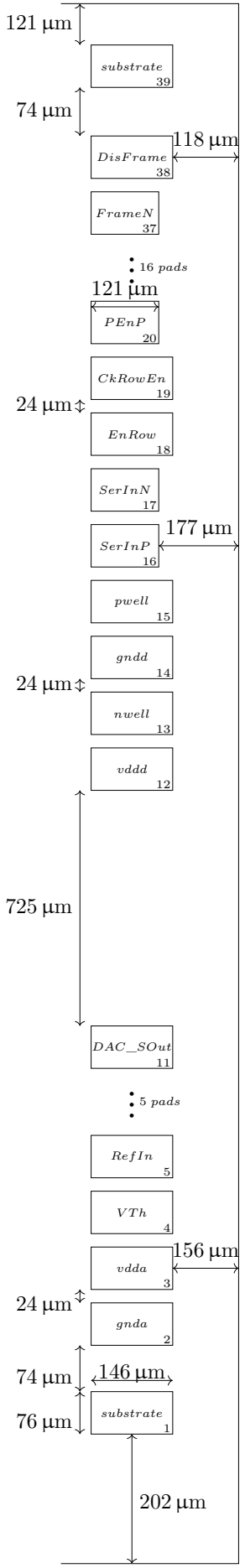


Figure B.19: Schematic of pads for normal HINT.

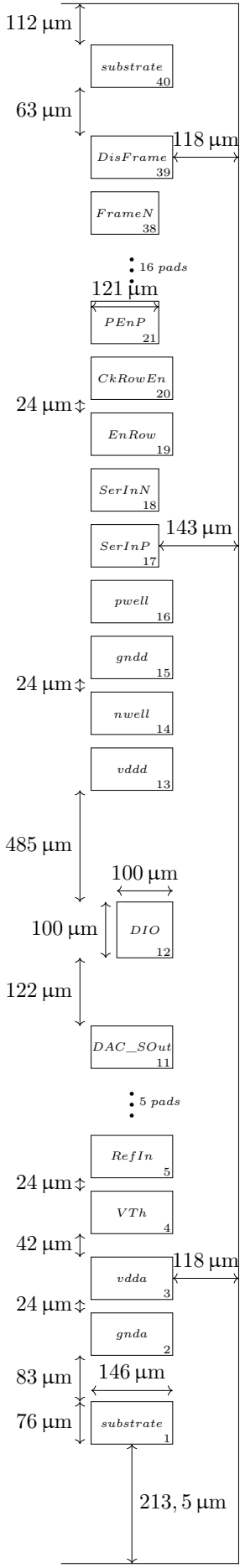


Figure B.20: Schematic of pads for separated HINT.

Table B.5: List of pads and their function of the normal HINT.

Number	Name	Function
1	*substrate*	Substrate contact
2	*gnda*	Analog ground contact
3	*vdda*	Analog supply voltage
4	V_{Th}	Threshold voltage for the comparator
5	*RefIn*	DC reference voltage for the integrator
6	*DAC_Ld*	Load the DAC configuration (active high)
7	DAC_Ck_2	Second clock of the DAC
8	DAC_Ck_1	First clock of the DAC
9	*DAC_SIn*	Serial input to write the DAC shift registers
10	*CapInj*	Injection signal input to the integrator through capacitor C_{inj}
11	*DAC_SOut*	Serial output to read out the DAC shift registers
12	*vddd*	Digital supply voltage
13	*nwell*	N-well contact
14	*gndd*	Digital ground contact
15	*pwell*	P-well contact
16	*SerInP*	Positive LVDS signal that starts the generation of the sequential enable pump, time-stamp first, and time-stamp last
17	*SerInN*	Negative LVDS signal that starts the generation of the sequential enable pump, time-stamp first, and time-stamp last
18	*EnRow*	Control bit to enable the creation of the sequential enable pump, time-stamp first and time-stamp last for each row
19	*CkRowEn*	Control bit to enable the generation of the two clocks that drives the shift register of the columns
20	*PEnP*	Positive LVDS to enable the shift of the column shift registers
21	*PEnN*	Negative LVDS to enable the shift of the column shift registers
22	Out_0N	Negative LVDS output 0 of the chip
23	Out_0P	Positive LVDS output 0 of the chip
24	Out_1N	Negative LVDS output 1 of the chip
25	Out_1P	Positive LVDS output 1 of the chip
26	$Sync_0P$	Positive LVDS synch 0 for 8-bit to 2-bit output converter and shift register column clocks generator
27	$Sync_0N$	Negative LVDS synch 0 for 8-bit to 2-bit output converter and shift register column clocks generator
28	$Sync_1P$	Positive LVDS synch 1 for 8-bit to 2-bit output converter and shift register column clocks generator
29	$Sync_1N$	Negative LVDS synch 1 for 8-bit to 2-bit output converter and shift register column clocks generator
30	*ResP*	Positive LVDS reset of the pump counter
31	*ResN*	Negative LVDS reset of the pump counter
32	*CkP*	Positive LVDS clock for the pump pulse
33	*CkN*	Negative LVDS clock for the pump pulse
34	*CkCntP*	Positive LVDS clock for the time counter
35	*CkCntN*	Negative LVDS clock for the time counter
36	*FrameP*	Positive LVDS frame signal
37	*FrameN*	Negative LVDS frame signal
38	*DisFrame*	Control bit to disable frame signal (active high)
39	*substrate*	Substrate contact

Table B.6: List of pads and its function of the separated HINT.

Number	Name	Function
1	*substrate*	Substrate contact
2	*gnda*	Analog ground contact
3	*vdda*	Analog supply voltage
4	V_{Th}	Threshold voltage for the comparator
5	*RefIn*	DC reference voltage for the integrator
6	*DAC_Ld*	Load the DAC configuration (active high)
7	DAC_Ck_2	Second clock of the DAC
8	DAC_Ck_1	First clock of the DAC
9	*DAC_SIn*	Serial input to write the DAC shift registers
10	*CapInj*	Injection signal input to the integrator through capacitor C_{inj}
11	*DAC_SOut*	Serial output to read out the DAC shift registers
12	*DIO*	Diode contact
13	*vddd*	Digital supply voltage
14	*nwell*	N-well contact
15	*gndd*	Digital ground contact
16	*pwell*	P-well contact
17	*SerInP*	Positive LVDS signal that starts the generation of the sequential enable pump, time-stamp first, and time-stamp last
18	*SerInN*	Negative LVDS signal that starts the generation of the sequential enable pump, time-stamp first, and time-stamp last
19	*EnRow*	Control bit to enable the creation of the sequential enable pump, time-stamp first and time-stamp last for each row
20	*CkRowEn*	Control bit to enable the generation of the two clocks that drives the shift register of the columns
21	*PEnP*	Positive LVDS to enable the shift of the column shift registers
22	*PEnN*	Negative LVDS to enable the shift of the column shift registers
23	Out_0N	Negative LVDS output 0 of the chip
24	Out_0P	Positive LVDS output 0 of the chip
25	Out_1N	Negative LVDS output 1 of the chip
26	Out_1P	Positive LVDS output 1 of the chip
27	$Sync_0P$	Positive LVDS synch 0 for 8-bit to 2-bit output converter and shift register column clocks generator
28	$Sync_0N$	Negative LVDS synch 0 for 8-bit to 2-bit output converter and shift register column clocks generator
29	$Sync_1P$	Positive LVDS synch 1 for 8-bit to 2-bit output converter and shift register column clocks generator
30	$Sync_1N$	Negative LVDS synch 1 for 8-bit to 2-bit output converter and shift register column clocks generator
31	*ResP*	Positive LVDS reset of the pump counter
32	*ResN*	Negative LVDS reset of the pump counter
33	*CkP*	Positive LVDS clock for the pump pulse
34	*CkN*	Negative LVDS clock for the pump pulse
35	*CkCntP*	Positive LVDS clock for the time counter
36	*CkCntN*	Negative LVDS clock for the time counter
37	*FrameP*	Positive LVDS frame signal
38	*FrameN*	Negative LVDS frame signal
39	*DisFrame*	Control bit to disable frame signal (active high)
40	*substrate*	Substrate contact

B.3 Data Readout

In order to explain the functioning of the matrix, and how the data will be sent via $Bus<0:7>$, an example of a small matrix (2×2) will be used. Figure B.21 shows a schematic of the small matrix, as well as the relevant signals for this analysis and part of the logic at the periphery, responsible for the *Bus* data control.

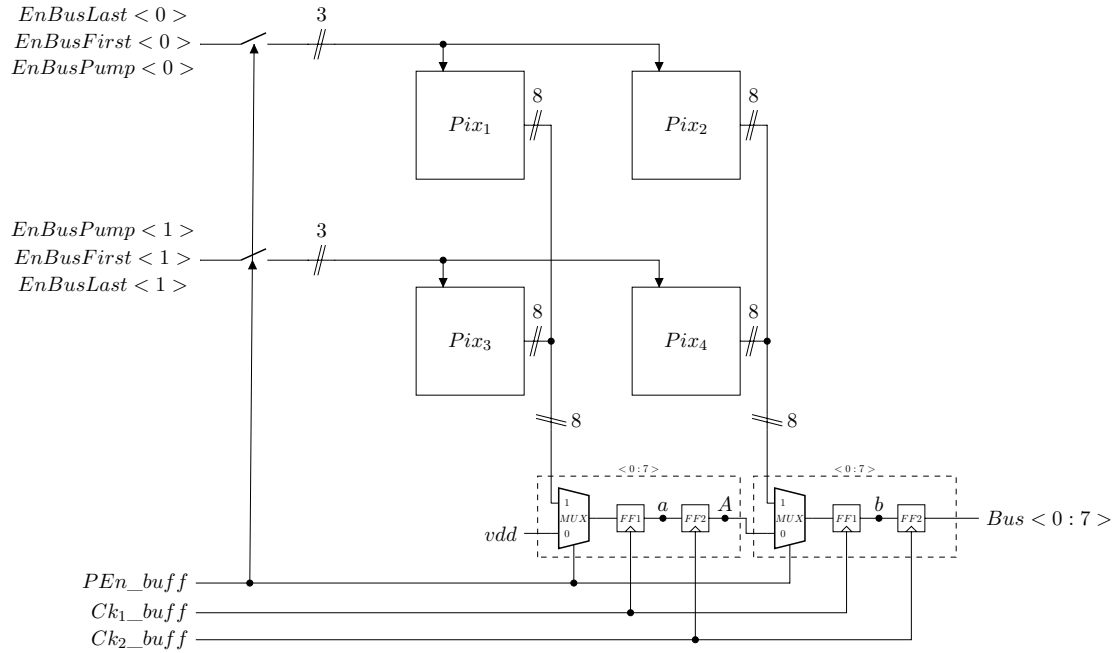


Figure B.21: Schematic of a 2×2 matrix example with the *Bus* control periphery.

The signal at the middle nodes (a, A, and b) as well as the $Bus<0:7>$ are shown in figure B.22. It can be seen that because of the correct timing of *PEn_buff* the *Bus* have the correct sequence of data from the pixels.

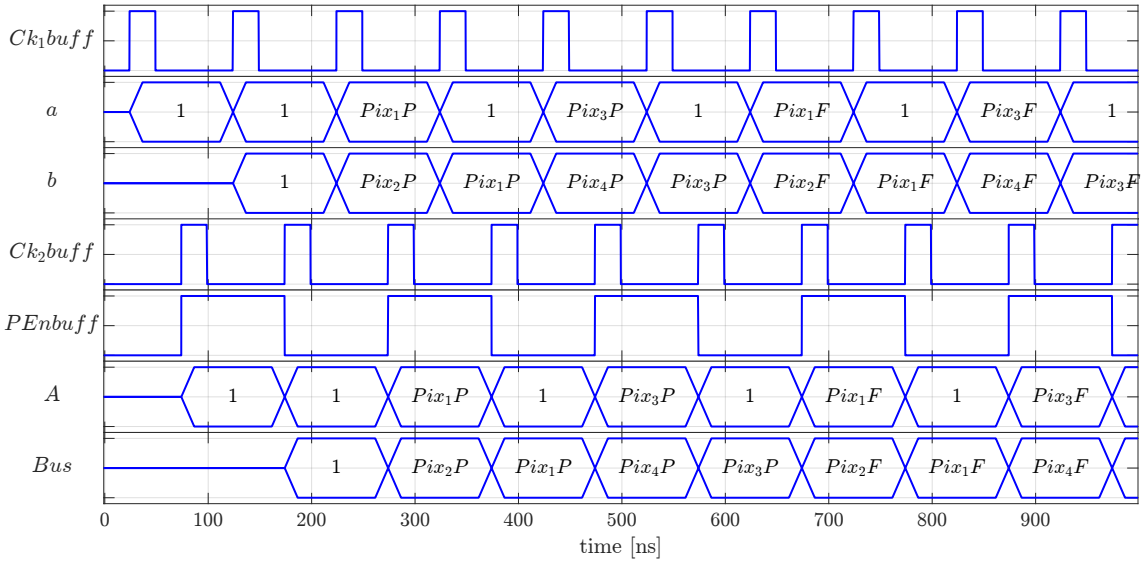


Figure B.22: Waveform of important signals for the example 2×2 matrix as a function of time. The data of each pixel is shown inside each time slot to exemplify the flow of the data.

Data are readout row by row, from the most right pixel to the left, starting from the top row. At the beginning all the values for the *Pump* will be sent via bus, followed by the time-stamp *First* for all the pixels, and ending with *Last* time-stamp. This is important to later acquire and sort correctly (in the software) the data from each pixel.

Another remark regarding the *EnBus* signals in this example is that they are indirectly controlled by *PEn_buff*, because *EnBus* is clocked by Ck_1Row_buff and Ck_2Row_buff (section B.1.2), and those clocks are enabled when *PEn.Pad* is "1" (section B.1.4). This means, only when *PEn.Pad* is on, the *EnBus* signals will be generated, and when this happens they will keep the correct timing between each other (figure B.6).

B.4 Signals summary

In order to clarify the signals needed to control and use the sensor, this section will sum up all the values and relationships of each waveform generated by the FPGA.

The LVDS signals should be generated as in table B.7. Here there are four levels of freedom to fix the timing, and they are:

- The resolution of the FPGA clock (T_{FPGA}).
- The period of $Sync_0.Pad$.
- The *Reset.Pad* signal should be "1" before *Frame.Pad* starts and flips to "0" when the Frame goes high.
- The amount of time that *Frame.Pad* is on (integration time) can be freely set, however, during readout, there is a minimum time, where *Frame.Pad* should be off. On table B.7 this time is calculated under T of *Frame.Pad*.

Table B.7: Timing relationships to control the sensor.

Signal	T [ns]	T_{on} [ns]	delay [ns]
$Sync_0.Pad$	$T_{Sync_0.Pad}$	50% duty cycle	0
$Sync_1.Pad$	$T_{Sync_0.Pad}$	50% duty cycle	$T_{Sync_0.Pad}/4$
Frame.Pad	$3T_{Sync_0.Pad}/4$+n°col×(3n°rows+1)× $T_{Sync_0.Pad}$	Accordingly to have 256 cycles of *Ck.Pad*	0
Ck.Pad	$T_{on_{Frame.Pad}}/256$	50% duty cycle	0
CkCnt.Pad	$T_{on_{Frame.Pad}}/256$	50% duty cycle	$T_{Ck.pad}/2$
SerIn.Pad	$T_{Frame.Pad}$	$3T_{Sync_0.Pad}/4$	$T_{Frame.Pad}$
PEn.Pad	$T_{Sync_0.Pad} \times n°col$	$T_{Sync_0.Pad}$	$T_{Frame.Pad}$

Example values for the timing settings are:

- $Sync_0.Pad$: periodic square wave with 50% duty cycle and T = 100 ns. The signal should start when *Frame.Pad* goes to digital "1".
- $Sync_1.Pad$: periodic square wave with 50% duty cycle, T = 100 ns, and a delay of 25 ns respect to $Sync_0.Pad$. The signal should start when *Frame.Pad* goes to digital "1".
- *Frame.Pad*: periodic signal with T_{on} = 174.08 µs and T = 175.275 µs.
- *SerIn.Pad*: periodic signal with T_{on} = 85 ns, T = $T_{Frame.Pad}$.
- *Reset.Pad*: equal to logic "1" until *Frame.Pad* is on.
- *Ck.Pad*: periodic square wave with 50% duty cycle and T = 680 ns. The signal should start when *Frame.Pad* goes to digital "1".
- *CkCnt.Pad*: same as *Ck.Pad* but with an opposite phase.

- *PEn.Pad*: periodic square wave with T_{on} = 100 ns and T = 2.4 µs. The signal should start when *Frame.Pad* goes to digital "1".

If all the above relationships are maintained, the sensor should work as expected and the output *Bus* will present the digital values of *Pump*, time-stamp *First*, and time-stamp *Last*. Figure B.23 shows an schematic of the signals timing for a 24×24 sensor matrix and in figure B.24 the output *Bus* order of the data can be seen.

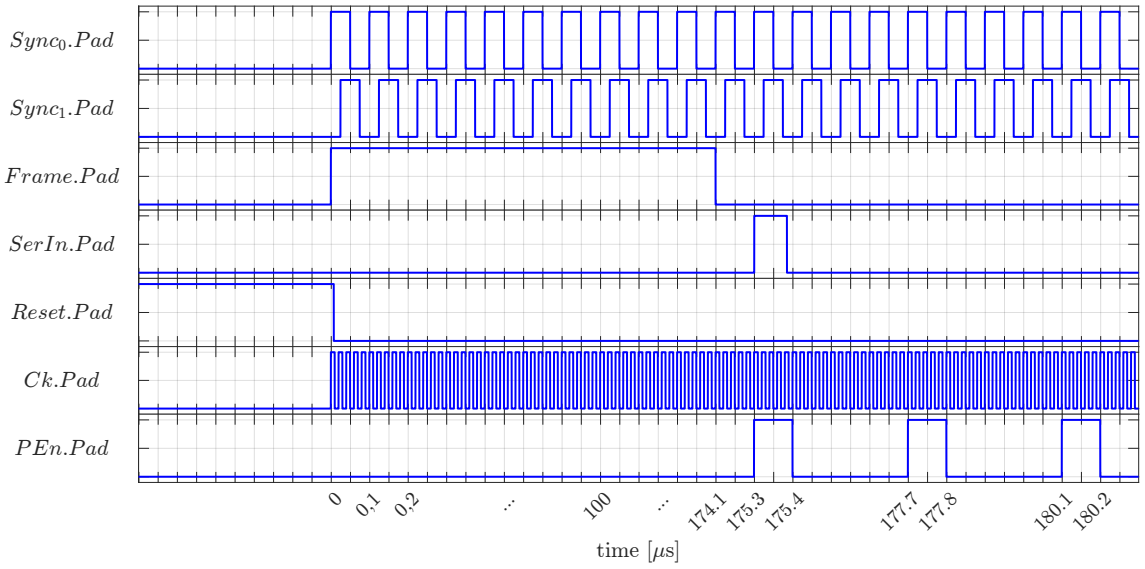


Figure B.23: Signals used to control the chip as a function of time.

In the schematic figure B.23, the signal *Ck.Pad* is not following the relationships before detailed, because otherwise, it wouldn't be possible to see the waveform within the time resolution used. However, the outline of the signal is the correct one.

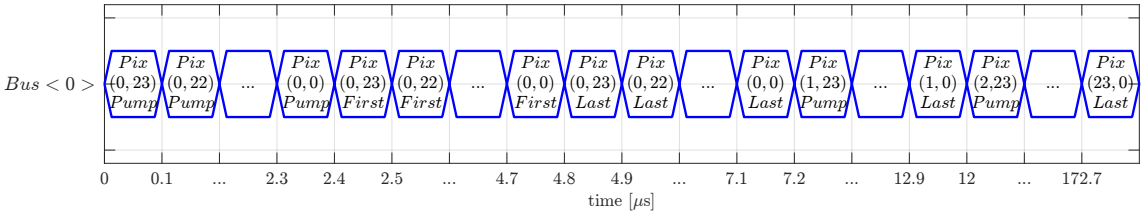


Figure B.24: Output *Bus* showing only one bit of the 8-bit bus and how the data is positioned in time.

As it can be seen in figure B.24, the *Bus* transfers *Pump* values for each pixel on the first row (identified as 0) from the far right to the left, after that, the time-stamp *First* will be sent, followed by the time-stamp *Last*. Once all the data (*Pump*, *First*, and *Last*) for the first row are sent, everything repeats for second row. A schematic of the Bus's filling in relation to the sensor matrix is shown infigure B.25.

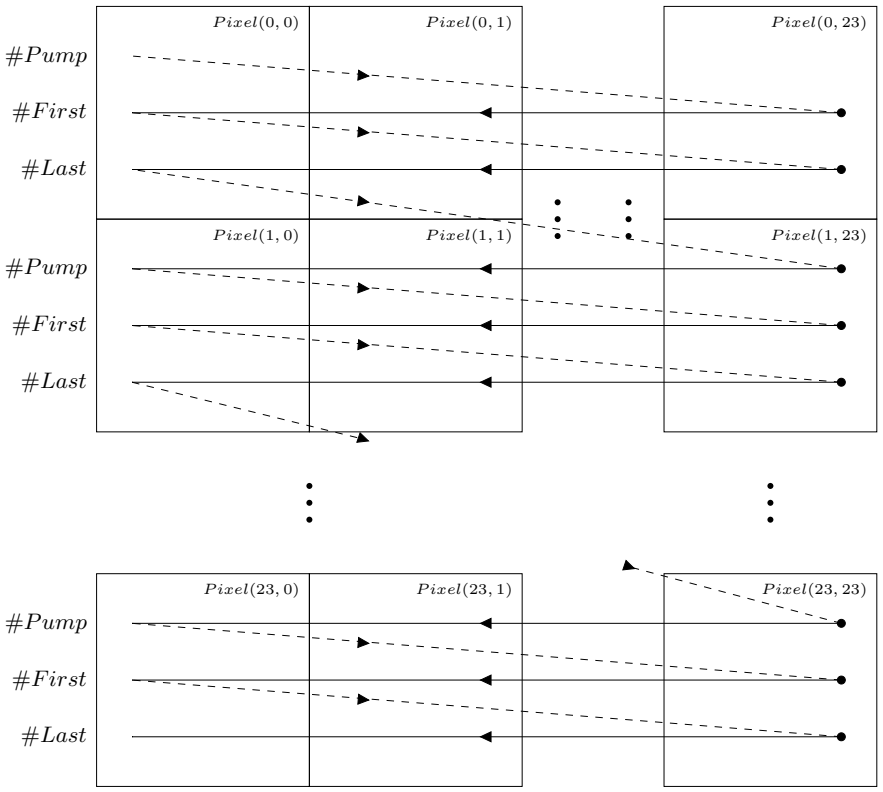


Figure B.25: Schematic of the order in which the *Bus* is filled with pixel data.

B.5 FPGA system

The FPGA-board used in this project is the *Nexys Video* by Digilent [20] (figure B.26). The FPGA firmware implemented is based on the code developed by R. Schimassek and F. Ehrler for the GECCO project [22]. A brief introduction of the relevant blocks will be given in this chapter, as well as a detailed explanation of the code developed to suit the needs of the HINT sensor.

The firmware has the following blocks:

1. FTDI communication.
2. UDP communication.
3. Run-read state-machine.
4. Signal generator: creates the signals necessary to operate the sensor.
5. Output converter: read the data sent by the chip and convert and sort it to words of 8-bits each.
6. Injection pulse generator: module to generate pulses of a specific time, used for LED measurements (section 3.5).

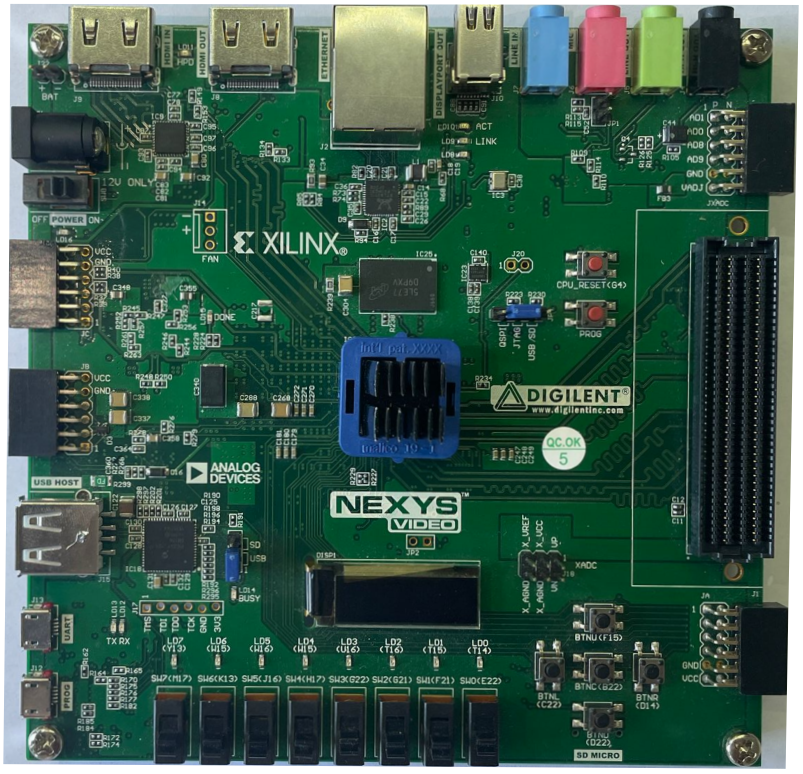


Figure B.26: Nexys Video board used to generate and control the signals coming from and to PC and sensor.

B.5.1 Run-read state-machine

As was before explained, the run-read state machine is the main control of the chip.

This state machine consists of five states, *IDLE*, *ONCE SIGNAL GENERATION*, *CONTINUOUS SIGNAL GENERATION*, *ONCE READ*, and *CONTINUOUS READ*. The *IDLE* state is the default one, on which the FPGA does nothing and waits for the PC command to start. As it is shown in figure B.27, the state machine is divided into two branches, the "continuous frame" generation and the "one frame" generation. As the name implied, when the continuous part is selected, the state machine will generate the signals and the read-out system will send the data via the ethernet module until the command to stop is sent by the software. There will be no dead time between readout time and next frame.

On the other branch, only one frame will be generated, and the data obtained will be sent upon PC request via the USB connection.

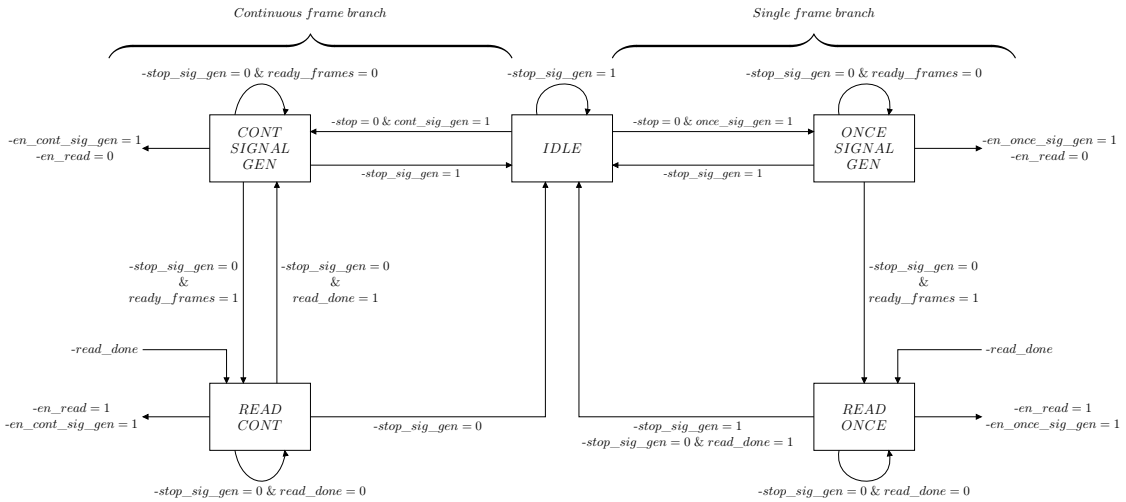


Figure B.27: State-machine flow chart.

B.5.2 Signal generation

This block generates the necessary signals to control the sensor and read the data (described in section B.4).

Table B.8 enumerates the flags and registers that enter the block, the signals used to communicate with other blocks (like state-machine or readout decoding), as well as their meaning.

Table B.8: Input-Output flags and registers used to generate the sensor control signals.

Input name	Description
clk_HINT	Time base used to generates the signals (200 MHz)
reset	Reset signal
en_once_sig_gen	Flag to signalling when the signals should be generated once
en_cont_sig_gen	Flag to signalling when the signals should be continuously generated
normal_HINT	Flag that signals if the timing should be generated for the normal HINT or the separated HINT
ResetPump_on_time	8-bit value of to set the reset Pump time, this number comes from the Qt interface
Sync_on_time	8-bit value of to set the Sync timing signals, this number comes from the Qt interface
SerIn_off_time	8-bit value of to set the time while *SerIn* is on, this number comes from the Qt interface
PEn_on_time	1-bit value of to set the *PEn* on time, this number comes from the Qt interface
PEn_off_time	16-bit value of to set the *PEn* off time, this number comes from the Qt interface
Ck_time	16-bit value of *Ck* and *CkCnt* period, this number comes from the Qt interface
Frame_on_time	24-bit value of the integration time, this number comes from the Qt interface
read-out_time	24-bit value of to set the read-out time, this number comes from the Qt interface

Output name	
ready_frames	Flag to signal the state machine that the integration time was finished and can enter the *READ DATA* state
read_done	Flag that signals the state machine that the data was read, and can enter the *IDLE* state

This module creates all the necessary signals to control the sensor (a list of them can be found in section B.4). Table B.9 summarizes the signals that this module produces.

Table B.9: Output signals from module.

Signal	Description
$Sync_0$	Clocks the shift-register column and the converts the 8-bit to 4-bit 2 lines output
$Sync_1$	Clocks the shift-register column and the converts the 8-bit to 4-bit 2 lines output
Frame	Integration time
Ck	Base time for pump pulse
CkCnt	Base time for time-stamp clock
SerIn	Starts the serial input pulse train
PEn	Enables the outputs of the column registers
Res_pump_cnt	Resets the pump counter

B.5.3 Injection pulse generator

One of the tests carried out was the response of the sensor under infrared light with a fast LED. In order to create short-duration pulses of ∼50 ns, I developed this module. It receives data from the Qt software, which configures the different parameters of the injected pulse (figure B.28).

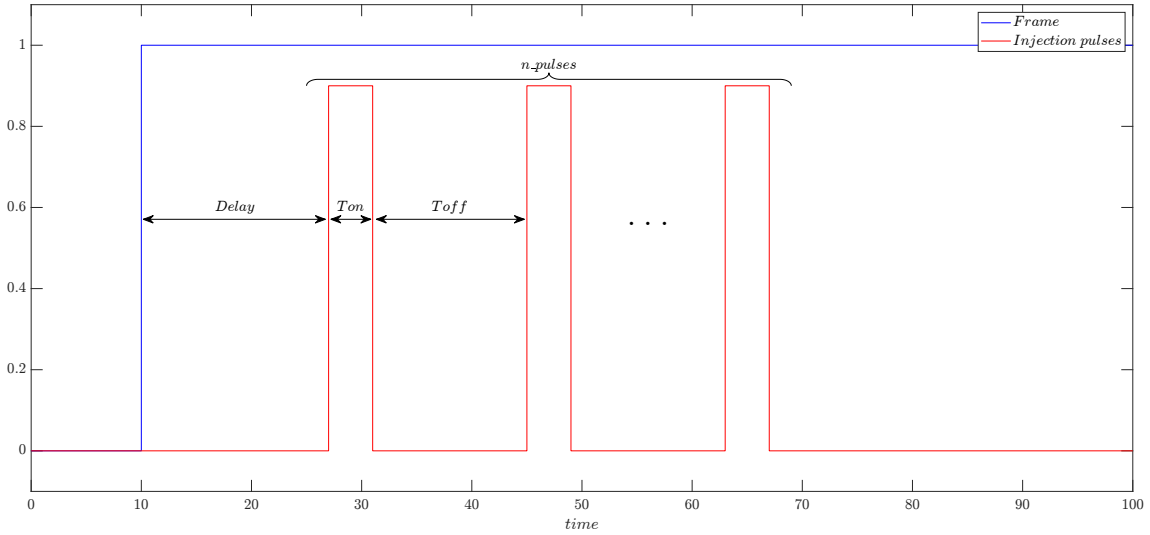


Figure B.28: Injection pulse (red) and its configurable parameters. In blue the *Frame* signal is drawn to which the delay is set.

delay, *Ton*, *Toff*, and *n_pulses* are all a 16-bit register value, which gives a wide range to configure the injections.

This module will produce the pulses in synchronization with the *Frame* signal to ensure that exactly the desired amount of pulses will be present during the integration time.

B.6 Beam-test integration time

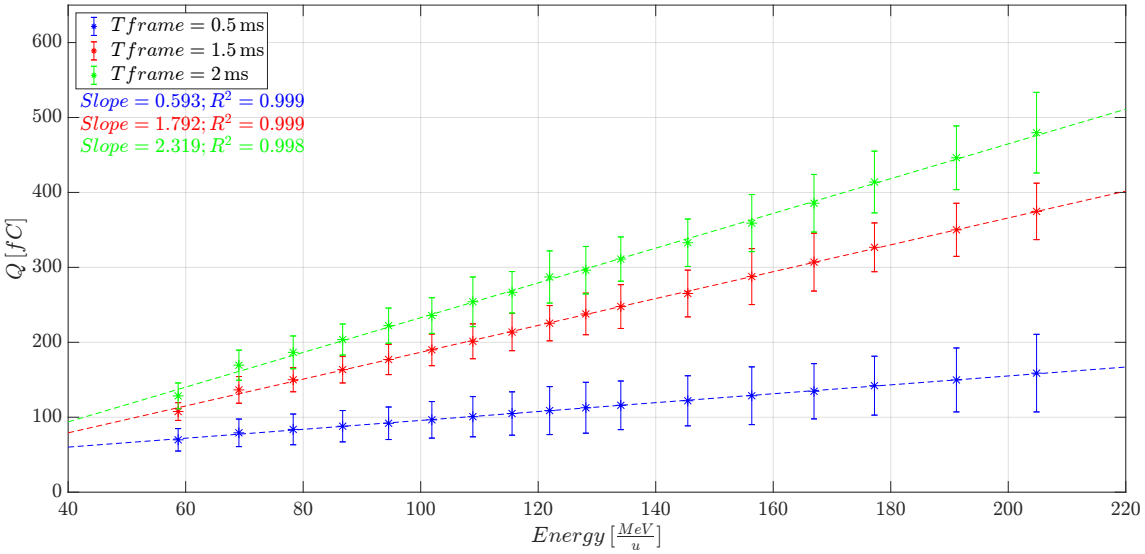


Figure B.29: Comparison of the charge acquired by the sensor when protons were used for a *Tframe* = 0.5 ms (blue), 1.5 ms (red), and 2 ms (green). As expected, the charge measured for shorter *Tframe* is smaller than the charge acquired with a longer *Tframe*.

Figure B.29 shows the slope for each integration time. If we compare the ratio between integration times, they match the ratios of the slopes, we can verify the sensor behavior as shown in table B.11. The error presented corresponds to the 95% confidence value reported by the linear fit with the least squares method.

Table B.11: Comparison of the charge increment measured as the integration times increase for protons.

***Tframe* ratio**	**Slope ratio**
$1.5\,ms/500\,\mu s = 3$	3.02 ± 0.04
$2\,ms/500\,\mu s = 4$	3.91 ± 0.06
$2\,ms/1.5\,ms = 1.3$	1.29 ± 0.08

Since it is not possible to fit a curve for the carbon energy scan as explained before, the charge ratio for each point was done, and the average over all the energies was calculated. The results are shown in table B.12, where the error corresponds to the standard deviation.

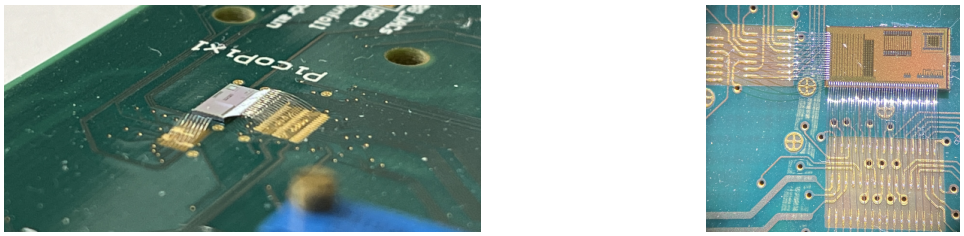
Table B.12: Comparison of the charge increment measured as the integration times increase for carbon ions.

***Tframe* ratio**	**Mean charge ratio**
$1.5\,ms/500\,\mu s = 3$	2.8 ± 0.2
$2\,ms/500\,\mu s = 4$	3.59 ± 0.13
$2\,ms/1.5\,ms = 1.3$	1.29 ± 0.07

The values obtained in table B.11 and B.12 verify the assumption that the charge acquired should follow a 1:1 relationship between integration time and charge acquired.

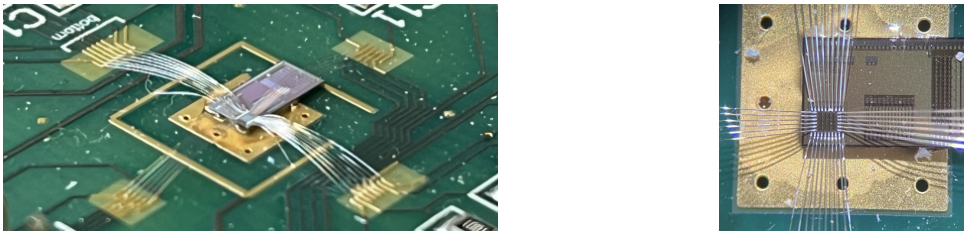
C Wire bonding

Following figures (C.1 to C.11) present the wire-bonded sensors of ADL group.



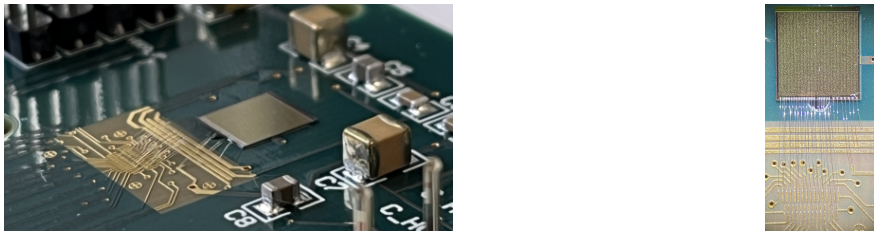
(a) (b)

Figure C.1: PicoPix wire bonded to the PCB carrier.



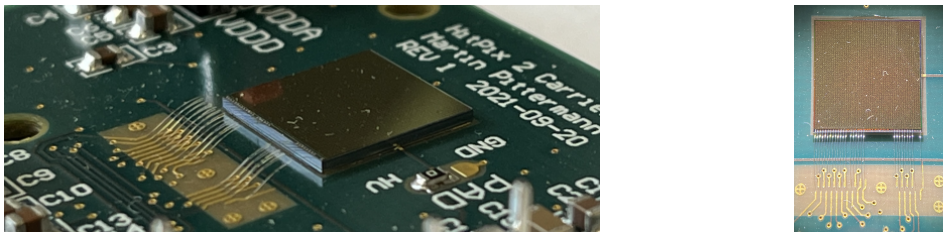
(a) (b)

Figure C.2: BabyPix wire bonded to the PCB carrier.



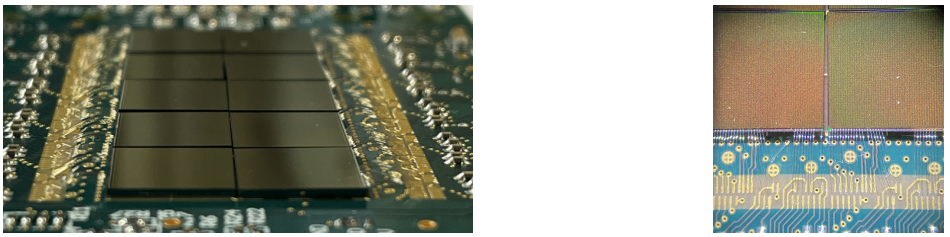
(a) (b)

Figure C.3: HitPix v1 wire bonded to the PCB carrier.



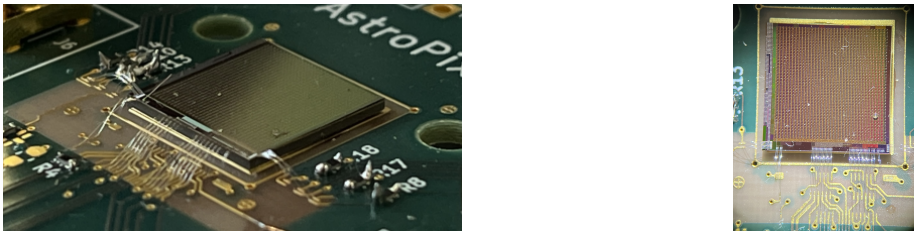
(a) (b)

Figure C.4: HitPix v2 wire bonded to the PCB carrier.



(a) (b)

Figure C.5: HitPix matrix wire bonded to the PCB carrier.

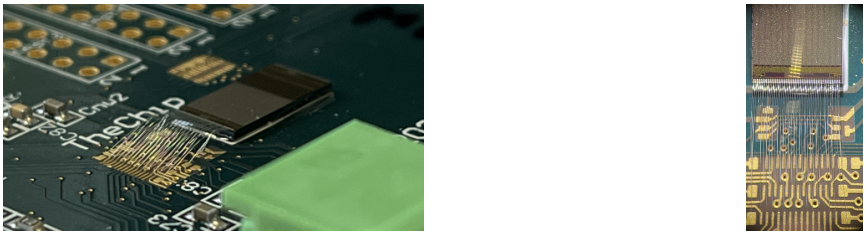


(a) (b)

Figure C.6: AstroPix wire bonded to the PCB carrier.

(a) (b)

Figure C.7: HVMAPS wire bonded to the PCB carrier.

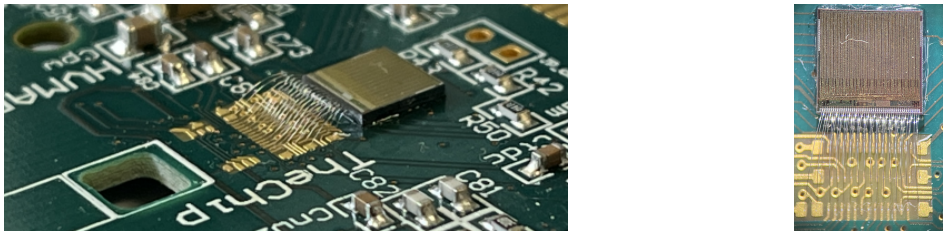


(a) (b)

Figure C.8: MPROC wire bonded to the PCB carrier.

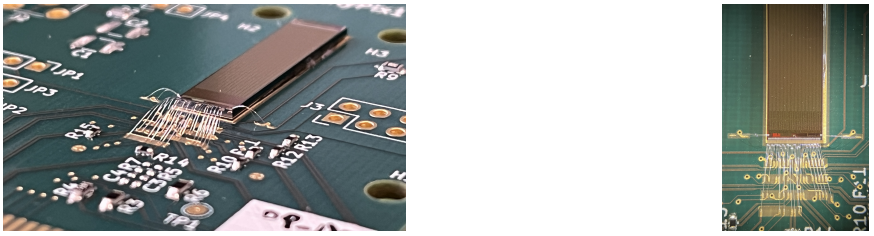
(a) (b)

Figure C.9: TelePix Fast wire bonded to the PCB carrier.



(a) (b)

Figure C.10: Panda Fast wire bonded to the PCB carrier.



(a) (b)

Figure C.11: MightyPix wire bonded to the PCB carrier.

Publications

List of Publications

[1] H. Mateos, F. Ehrler, R. Schimassek, S. Scherl, N. Striebig, and I. Perić. Development and characterization of high voltage cmos particle pixel sensor with integrating electronics. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*:167690, 2022. DOI: 10.1016/j.nima.2022.167690.

[2] H. Mateos, A. Ferretti, L. Mele, and I. Perić. Development of cmos sensors for electron microscopy. *Journal of Instrumentation*, 14(12):Art.–Nr. C12002, 2019. ISSN: 1748-0221. DOI: 10.1088/1748-0221/14/12/C12002. 54.02.03; LK 01.

List of Conference Posters

1. *Development and Characterization of High Voltage CMOS Particle Pixel Sensor with Integrating Electronics.* 15th Pisa Meeting on Advanced Detectors. La Biodola, Isola d'Elba, May 22-28, 2022
2. *Development of CMOS Sensors for Electron Microscopy.* 21st International Workshop on Radiation Imaging Detectors. Creete, Greece, Jul 7 – 12, 2019
3. *Development and Characterization of CMOS Sensors for Electron Microscopy.* 1st Argentine Conference on Electronics (CAE). Mar del Plata, Argentine, March 14-15, 2019

Bibliography

[1] 12.6 limits of resolution: the rayleigh criterion. DOUGLAS COLLEGE PHYSICS 1207. URL: https://pressbooks.bccampus.ca/introductorygeneralphysics2phys1207/chapter/27-6-limits-of-resolution-the-rayleigh-criterion/.

[2] A critical review of radiation therapy: from particle beam therapy (proton, carbon, and bnct) to beyond. *Journal of Personalized Medicine*, 11(8), 2021. DOI: 10.3390/jpm11080825.

[3] T. Abe, I. Adachi, K. Adamczyk, S. Ahn, H. Aihara, K. Akai, M. Aloi, L. Andricek, K. Aoki, Y. Arai, A. Arefiev, K. Arinstein, Y. Arita, D. M. Asner, V. Aulchenko, T. Aushev, T. Aziz, A. M. Bakich, V. Balagura, Y. Ban, E. Barberio, T. Barvich, K. Belous, T. Bergauer, V. Bhardwaj, B. Bhuyan, S. Blyth, A. Bondar, G. Bonvicini, A. Bozek, M. Bracko, J. Brodzicka, O. Brovchenko, T. E. Browder, G. Cao, M. .-. Chang, P. Chang, Y. Chao, V. Chekelian, A. Chen, K. .-. Chen, P. Chen, B. G. Cheon, C. .-. Chiang, R. Chistov, K. Cho, S. .-. Choi, K. Chung, A. Comerma, M. Cooney, D. E. Cowley, T. Critchlow, J. Dalseno, M. Danilov, A. Dieguez, A. Dierlamm, M. Dillon, J. Dingfelder, R. Dolenec, Z. Dolezal, Z. Drasal, A. Drutskoy, W. Dungel, D. Dutta, S. Eidelman, A. Enomoto, D. Epifanov, S. Esen, J. E. Fast, M. Feindt, M. F. Garcia, T. Fifield, P. Fischer, J. Flanagan, S. Fourletov, J. Fourletova, L. Freixas, A. Frey, M. Friedl, R. Fruehwirth, H. Fujii, M. Fujikawa, Y. Fukuma, Y. Funakoshi, K. Furukawa, J. Fuster, N. Gabyshev, A. G. d. V. Cueto, A. Garmash, L. Garrido, C. Geisler, I. Gfall, Y. M. Goh, B. Golob, I. Gorton, R. Grzymkowski, H. Guo, H. Ha, J. Haba, K. Hara, T. Hara, T. Haruyama, K. Hayasaka, K. Hayashi, H. Hayashii, M. Heck, S. Heindl, C. Heller, T. Hemperek, T. Higuchi, Y. Horii, W. .-. Hou, Y. B. Hsiung, C. .-. Huang, S. Hwang, H. J. Hyun, Y. Igarashi, C. Iglesias, Y. Iida, T. Iijima, M. Imamura, K. Inami, C. Irmler, M. Ishizuka, K. Itagaki, R. Itoh, M. Iwabuchi, G. Iwai, M. Iwai, M. Iwasaki, M. Iwasaki, Y. Iwasaki, T. Iwashita, S. Iwata, H. Jang, X. Ji, T. Jinno, M. Jones, T. Julius, T. Kageyama, D. H. Kah, H. Kakuno, T. Kamitani, K. Kanazawa, P. Kapusta, S. U. Kataoka, N. Katayama, M. Kawai, Y. Kawai, T. Kawasaki, J. Kennedy, H. Kichimi, M. Kikuchi, C. Kiesling, B. K. Kim, G. N. Kim, H. J. Kim, H. O. Kim, J. .-. Kim, J. H. Kim, M. J. Kim, S. K. Kim, K. T. Kim, T. Y. Kim, K. Kinoshita, K. Kishi, B. Kisielewski, K. K. van Dam, J. Knopf, B. R. Ko, M. Koch, P. Kodys, C. Koffmane, Y. Koga, T. Kohriki, S. Koike, H. Koiso, Y. Kondo, S. Korpar, R. T. Kouzes, C. Kreidl, M. Kreps, P. Krizan, P. Krokovny, H. Krueger, A. Kruth, W. Kuhn, T. Kuhr, R. Kumar, T. Kumita, S. Kupper, A. Kuzmin, P. Kvasnicka, Y. .-. Kwon, C. Lacasta, J. S. Lange, I. .-. Lee, M. J. Lee, M. W. Lee, S. .-. Lee, M. Lemarenko, J. Li, W. D. Li, Y. Li, J. Libby, A. Limosani, C. Liu, H. Liu, Y. Liu, Z. Liu, D. Liventsev, A. L. Virto, Y. Makida, Z. P. Mao, C. Marinas, M. Masuzawa, D. Matvienko, W. Mitaroff, K. Miyabayashi, H. Miyata, Y. Miyazaki, T. Miyoshi, R. Mizuk, G. B. Mohanty, D. Mohapatra, A. Moll, T. Mori, A. Morita, Y. Morita, H. .-. Moser, D. M. Martin, T. Mueller, D. Muenchow, J. Murakami, S. S. Myung, T. Nagamine, I. Nakamura, T. T. Nakamura, E. Nakano, H. Nakano, M. Nakao,

H. Nakazawa, S. .-. Nam, Z. Natkaniec, E. Nedelkovska, K. Negishi, S. Neubauer, C. Ng, J. Ninkovic, S. Nishida, K. Nishimura, E. Novikov, T. Nozaki, S. Ogawa, K. Ohmi, Y. Ohnishi, T. Ohshima, N. Ohuchi, K. Oide, S. L. Olsen, M. Ono, Y. Ono, Y. Onuki, W. Ostrowicz, H. Ozaki, P. Pakhlov, G. Pakhlova, H. Palka, H. Park, H. K. Park, L. S. Peak, T. Peng, I. Peric, M. Pernicka, R. Pestotnik, M. Petric, L. E. Piilonen, A. Poluektov, M. Prim, K. Prothmann, K. Regimbal, B. Reisert, R. H. Richter, J. Riera-Babures, A. Ritter, A. Ritter, M. Ritter, M. Roehrken, J. Rorie, M. Rosen, M. Rozanska, L. Ruckman, S. Rummel, V. Rusinov, R. M. Russell, S. Ryu, H. Sahoo, K. Sakai, Y. Sakai, L. Santelj, T. Sasaki, N. Sato, Y. Sato, J. Scheirich, J. Schieck, C. Schwanda, A. J. Schwartz, B. Schwenker, A. Seljak, K. Senyo, O. .-. Seon, M. E. Sevior, M. Shapkin, V. Shebalin, C. P. Shen, H. Shibuya, S. Shiizuka, J. .-. Shiu, B. Shwartz, F. Simon, H. J. Simonis, J. B. Singh, R. Sinha, M. Sitarz, P. Smerkol, A. Sokolov, E. Solovieva, S. Stanic, M. Staric, J. Stypula, Y. Suetsugu, S. Sugihara, T. Sugimura, K. Sumisawa, T. Sumiyoshi, K. Suzuki, S. Y. Suzuki, H. Takagaki, F. Takasaki, H. Takeichi, Y. Takubo, M. Tanaka, S. Tanaka, N. Taniguchi, E. Tarkovsky, G. Tatishvili, M. Tawada, G. N. Taylor, Y. Teramoto, I. Tikhomirov, K. Trabelsi, T. Tsuboyama, K. Tsunada, Y. .-. Tu, T. Uchida, S. Uehara, K. Ueno, T. Uglov, Y. Unno, S. Uno, P. Urquijo, Y. Ushiroda, Y. Usov, S. Vahsen, M. Valentan, P. Vanhoefer, G. Varner, K. E. Varvell, P. Vazquez, I. Vila, E. Vilella, A. Vinokurova, J. Visniakov, M. Vos, C. H. Wang, J. Wang, M. .-. Wang, P. Wang, A. Wassatch, M. Watanabe, Y. Watase, T. Weiler, N. Wermes, R. E. Wescott, E. White, J. Wicht, L. Widhalm, K. M. Williams, E. Won, H. Xu, B. D. Yabsley, H. Yamamoto, H. Yamaoka, Y. Yamaoka, M. Yamauchi, Y. Yin, H. Yoon, J. Yu, C. Z. Yuan, Y. Yusa, D. Zander, M. Zdybal, Z. P. Zhang, J. Zhao, L. Zhao, Z. Zhao, V. Zhilich, P. Zhou, V. Zhulanov, T. Zivko, A. Zupanc, and O. Zyukova. Belle ii technical design report, 2010. DOI: 10.48550/ARXIV.1011.0352.

[4] Adel S. Sedra and Kenneth C. Smith. *Microelectronic Circuits*. Oxford University Press, fifth edition, 2004.

[5] P. Allen, B. Dobkin, D. Holberg, J. Williams, and E. S. bibinitperiod T. (Firm). *CMOS Analog Circuit Design*. Analog Circuit Design: A Tutorial Guide to Applications and Solutions. Oxford University Press, USA, 2011. ISBN: 9780123851857.

[6] U. Amaldi and G. Kraft. Radiotherapy with beams of carbon ions. *Reports on Progress in Physics*, 68(8):1861–1882, July 2005. DOI: 10.1088/0034-4885/68/8/r04.

[7] M. Andreas, A. Karlheinz, R. Martin, G. Immanuel, and K. Christian. *The vertex detector numbering scheme. Belle II Note*. (0010). 2012.

[8] H. Augustin, S. Dittmeier, J. Hammerich, A. Herkert, L. Huth, D. Immig, I. Perić, A. Schöning, A. Simancas, M. Stanitzki, and B. Weinläder. Telepix – a fast region of interest trigger and timing layer for the eudet telescopes. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 1048:167947, 2023. ISSN: 0168-9002. DOI: https://doi.org/10.1016/j.nima.2022.167947.

[9] M. Balch. *Complete Digital Design*, volume 53. 2015. ISBN: 9788578110796. DOI: doi.org/10.1017/CBO9781107415324.004.

[10] R. Blanco. *Customized Integrated Circuits for Scientific and Medical Applications*. PhD thesis, Karlsruher Institut für Technologie (KIT), 2019. 195 pages. DOI: 10.5445/IR/1000091922. 54.02.03; LK 01.

[11] T. Borel, S. Furic, E. Leduc, A. Michez, J. Boch, A. Touboul, B. Azais, S. Danzeca, and L. Dusseau. Total Ionizing Dose Effect in LDMOS Oxides and Devices. *IEEE Trans. Nucl. Sci.*, 66(7):1606–1611, 2019. DOI: doi.org/10.1109/TNS.2019.2914091.

[12] G. Borghello. *Ionizing radiation effects in nanoscale CMOS technologies exposed to ultra-high doses*, 2018. URL: https://cds.cern.ch/record/2680840. Presented 08 Mar 2019.

[13] A. Brahme. *Comprehensive Biomedical Physics*. Elsevier Science, 2014. ISBN: 9780444536334. DOI: 10.1016/c2009-0-61095-3.

[14] T. Carusone, D. Johns, and K. Martin. *Analog Integrated Circuit Design*. Analog Integrated Circuit Design. Wiley, 2011. ISBN: 9780470770108.

[15] I. Catt. Crosstalk (noise) in digital systems. *IEEE Transactions on Electronic Computers*, EC-16(6):743–763, 1967. DOI: doi.org/10.1109/PGEC.1967.264721.

[16] K. Chaiwongkhot, T. Kohriki, N. Taniguchi, S. Uno, E. Nakano, U. Tippawan, S. Minemura, M. H. A. Nouxman, and K. A. B. Azmi. Inner chamber of the belle ii central drift chamber. In *2013 IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC)*, pages 1–3, 2013. DOI: 10.1109/NSSMIC.2013.6829461.

[17] D. Contarato, P. Denes, D. Doering, J. Joseph, and A. Krieger. High speed, radiation hard cmos pixel sensors for transmission electron microscopy. *Physics Procedia*, 37:1504–1510, Dec. 2012. DOI: 10.1016/j.phpro.2012.04.103.

[18] D. Contarato, P. Denes, D. Doering, J. Joseph, and B. Krieger. High speed, radiation hard cmos pixel sensors for transmission electron microscopy. *Physics Procedia*, 37:1504–1510, 2012. ISSN: 1875-3892. DOI: https://doi.org/10.1016/j.phpro.2012.04.103. Proceedings of the 2nd International Conference on Technology and Instrumentation in Particle Physics (TIPP 2011).

[19] N. Costantino, R. Serventi, F. Tinfena, P. D'Abramo, P. Chassard, P. Tisserand, and L. Fanucci. Design and test of an hv-cmos intelligent power switch with integrated protections and self-diagnostic for harsh automotive applications. *Industrial Electronics, IEEE Transactions on*, 58:2715–2727, Aug. 2011. DOI: 10.1109/TIE.2010.2084979.

[20] Digilent. 999. URL: https://digilent.com/reference/programmable-logic/nexys-video/start.

[21] Ed. A.J. Bevan, B. Golob, Th. Mannel, S. Prell, B.D. Yabsley. The physics of the b factories. *The European Physical Journal C*, 74(11), Nov. 2014. DOI: 10.1140/epjc/s10052-014-3026-9.

[22] F. M. Ehrler. *Characterization of monolithic HV-CMOS pixel sensors for particle physics experiments*. PhD thesis, Karlsruher Institut fur Technologie (KIT), 2021. DOI: doi.org/10.5445/IR/1000133748. 54.12.01; LK 01.

[23] L. Fanucci, G. Pasetti, P. D'Abramo, R. Serventi, F. Tinfena, P. Chassard, L. Labiste, and P. Tisserand. An high voltage cmos voltage regulator for automotive alternators with programmable functionalities and full reverse polarity capability. In *2010 Design, Automation and Test in Europe Conference and Exhibition (DATE 2010)*, pages 526–531, 2010. DOI: 10.1109/DATE.2010.5457150.

[24] T. Ferber. Electromagnetic calorimeter reconstruction in belle ii, Mar. 2019. 20.

[25] I. Fratelli, A. Ciavatti, E. Zanazzi, L. Basiricò, M. Chiari, L. Fabbri, J. E. Anthony, A. Quaranta, and B. Fraboni. Direct detection of 5-mev protons by flexible organic thin-film devices. *Science Advances*, 7(16):eabf4462, 2021. DOI: 10.1126/sciadv.abf4462.

[26] N. Guerrini, R. Turchetta, G. V. Hoften, R. Henderson, G. McMullan, and A. R. Faruqi. A high frame rate, 16 million pixels, radiation hard CMOS sensor. *Journal of Instrumentation*, 6(03):C03003–C03003, Mar. 2011. DOI: 10.1088/1748-0221/6/03/c03003.

[27] J. Haidl and C. Kiesling. *Readout Optimization for the Belle II Pixel Detector: Characterization by ADC Transfer Curves*. PhD thesis, Munich, LMU, Munich, 2016. Presented on 07 04 2016.

[28] W. R. Hendee. *Proton and Carbon Ion Therapy*. CRC Press, 2012. DOI: doi.org/10.1201/b13070.

[29] C. Hu. *Modern Semiconductor Devices for Integrated Circuits*. Prentice Hall, 2010. ISBN: 9780136085256. URL: https://books.google.de/books?id=PosRbWdafnsC.

[30] B. Hyams, U. Koetz, E. Belau, R. Klanner, G. Lutz, E. Neugebauer, A. Wylie, and J. Kemmer. A silicon counter telescope to study short-lived particles in high-energy hadronic interactions. *Nuclear Instruments and Methods in Physics Research*, 205(1):99–105, 1983. DOI: doi.org/10.1016/0167-5087(83)90177-1.

[31] International Commission on Radiation Units and Measurements. ICRU Report No. 87: Radiation dose and image-quality assessment in computed tomography. *Journal of the ICRU*, 16(1-2):3–3, 2016. DOI: 10.1093/jicru_ndy025.

[32] S. Iwata, I. Adachi, K. Hara, T. Iijima, H. Ikeda, H. Kakuno, H. Kawai, T. Kawasaki, S. Korpar, P. Križan, T. Kumita, S. Nishida, S. Ogawa, R. Pestotnik, L. Šantelj, A. Seljak, T. Sumiyoshi, M. Tabata, E. Tahirovic, and Y. Yusa. Particle identification performance of the prototype aerogel rich counter for the belle ii experiment. *Progress of Theoretical and Experimental Physics*, 2016(3), Mar. 2016. DOI: 10.1093/ptep/ptw005.

[33] S. Joel, S. Stanley, and D. Michael. The diffraction barrier in optical microscopy. 2022. URL: https://www.microscopyu.com/techniques/super-resolution/the-diffraction-barrier-in-optical-microscopy.

[34] A. Kaech. An introduction to electron microscopy instrumentation, imaging and preparation. In 2013.

[35] F. J. Kaiser, N. Bassler, and O. Jäkel. COTS Silicon diodes as radiation detectors in proton and heavy charged particle radiotherapy 1. *Radiat Environ Biophys*, 49(3):365–371, Aug. 2010.

[36] T. Kato, F. Makino, T. Nakane, N. Terahara, T. Kaneko, Y. Shimizu, S. Motoki, I. Ishikawa, K. Yonekura, K. Namba, and et al. Cryotem with a cold field emission gun that moves structural biology into a new stage. *Microscopy and Microanalysis*, 25(S2):998–999, 2019. DOI: 10.1017/S1431927619005725.

[37] J. Kemmer and G. Lutz. New detector concepts. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 253(3):365–377, 1987. ISSN: 0168-9002. DOI: https://doi.org/10.1016/0168-9002(87)90518-3.

[38] G. F. Knoll and H. W. Kraner. *Radiation Detection and Measurement*, volume 69 of number 4. 2010, page 495. ISBN: 9780470131480. DOI: doi.org/10.1109/PROC.1981.12016.

[39] M. Kobayashi and T. Maskawa. CP-Violation in the Renormalizable Theory of Weak Interaction. *Progress of Theoretical Physics*, 49(2):652–657, Feb. 1973. DOI: 10.1143/PTP.49.652.

[40] M. Koch. *Development of a Test Environment for the Characterization of the Current Digitizer Chip DCD2 and the DEPFET Pixel System for the Belle II Experiment at SuperKEKB*, 2011. URL: https://cds.cern.ch/record/1380639. Presented 05 Sep 2011.

[41] P. Kodyš, F. Abudinen, K. Ackermann, P. Ahlburg, H. Aihara, M. Albalawi, O. Alonso, L. Andricek, R. Ayad, T. Aziz, V. Babu, S. Bacher, S. Bahinipati, Y. Bai, E. Barberio, T. Baroncelli, T. Baroncelli, A. Basith, G. Batignani, A. Bauer, P. Behera, V. Bertacchi, S. Bettarini, B. Bhuyan, T. Bilka, R. Blanco, F. Bosi, M. Boronat, L. Bosisio, A. Bozek, F. Buchsteiner, C. Camien, A. Caldwell, G. Caria, G. Casarosa, M. Ceccanti, D. Červenkov, V. Chekelian, T. Czank, N. Dash, M. De Nuccio, B. Deschamps, A. Dieguez, J. Dingfelder, Z. Doležal, D. Esperante, P. Fischer, F. Forti, M. Fras, A. Frey, M. Friedl, J. Fuster, M. Gabriel, K. Gadow, U. Gebauer, L. Germic, T. Gessler, D. Getzkow, L. Gioi, B. Gobbo, P. Gomis, J. Grimaldo, K. Hara, M. Heck, T. Hemperek, M. Hensel, T. Higuchi, M. Hoek, C. Irmler, A. Ishikawa, H. Jeon, C. Joo, M. Kaleta, J. Kandra, N. Kambara, K. Kang, P. Kapusta, C. Kiesling, B. Kisielewski, D. Kittlinger, D. Klose, C. Koffmane, T. Kohriki, S. Koike, I. Komarov, I. Konorov, S. Krivokuca, H. Krüger, T. Kuhr, W. Kühn, M. Kumar, R. Kumar, W. Kun, P. Kvasnička, C. La Licata, C. Lacasta, K. Lalwani, L. Lanceri, J. Lange, K. Lautenbach, J. Lee, S. Lee, U. Leis, P. Leitl, D. Levit, J. Libby, G. Liemann, Z. Liu, T. Lueck, F. Lütticke, L. Macharski, P. Mammini, C. Mariñas, A. Martini, S. Mayekar, S. Mccarney, G. Mohanty, T. Morii, H. Moser, D. Moya, F. Mueller, F. Müller, D. Münchow, K. Nakamura, Z. Natkaniec, C. Niebuhr, J. Ninkovic, Y. Onuki, W. Ostrowicz, U. Packheiser, A. Paladino, E. Paoloni, H. Park, B. Paschen, S. Paul, I. Peric, F. Poblotzki, K. Prasanth, A. Profeti, A. Rabusov, I. Rashevskaya, K. Rao, S. Reiter, R. P.K., R. Richter, M. Ritter, M. Ritzert, G. Rizzo, M. Rozanska, S. Rummel, D. Sahoo, J. Sanchez, J. Sasaki, N. Sato, B. Scavino, G. Schaller, M. Schnecke, F. Schopper, H. Schreeck, S. Schultschik, C. Schwanda, B. Schwenker, R. Sedlmeyer, C. Sfienti, F. Simon, S. Skambraks, Y. Soloviev, B. Spruck, R. Stever, U. Stolzenberg, J. Stypula, J. Suzuki, E. Tafelmayer, M. Takahashi, S. Tanaka, H. Tanigawa, G. Taylor, R. Thalmeier, T. Tsuboyama, P. Urquijo, I. Vila, A. Virto, L. Vitale, S. Vogt, M. Vos, C. Wang, S. Watanuki, M. Watanabe, I. Watson, J. Webb, N. Wermes, C. Wessel, J. Wiechczynski, P. Wieduwilt, S. Williams, H. Windel, H. Ye, H. Yin, L. Zani, and J. Zhao. The belle ii vertex detector integration. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 936:616–620, 2019. ISSN: 0168-9002. DOI: 10.1016/j.nima.2018.09.003. Frontier Detectors for Frontier Physics: 14th Pisa Meeting on Advanced Detectors.

[42] I. Kremastiotis, R. Ballabriga, M. Campbell, D. Dannheim, K. Dort, N. Egidos, J. Kröger, L. Linssen, X. Llopart, M. Munker, A. Nurnberg, I. Peric, S. Spannagel, T. Vanat, and M. Williams. Design and characterization of the clictd pixelated monolithic sensor chip. *IEEE Transactions on Nuclear Science*, 67(10):2263–2272, 2020. DOI: 10.1109/TNS.2020.3019887.

[43] I. Kremastiotis, R. Ballabriga Sune, M. Campbell, D. Dannheim, A. Fiergolski, D. Hynds, S. Kulis, and I. Peric. Design and standalone characterisation of a capacitively coupled hv-cmos sensor chip for the clic vertex detector. design and characterisation of a capacitively coupled hv-cmos sensor chip for the clic vertex detector. *JINST*, 12(09):P09012, 2017. DOI: 10.1088/1748-0221/12/09/P09012. arXiv: 1706.04470.

[44] E. Kvaale. Schematic view of imaging and diffraction modes in tem. 2020. URL: https://commons.wikimedia.org/w/index.php?curid=85779398.

[45] W. R. Leo. *Techniques for nuclear and particle physics experiments: a how-to approach*. Springer, 1994. DOI: doi.org/10.1007/978-3-642-57920-2.

[46] G. Lutz. *Semiconductor Radiation Detectors: Device Physics*. Springer Berlin Heidelberg, 2007. ISBN: 9783540716792. DOI: 10.1007/978-3-540-71679-2.

[47] L. Magerand and A. Bartoli. A generic rolling shutter camera model and its application to dynamic pose estimation, Jan. 2010.

[48] Y. Makida, H. Yamaoka, Y. Doi, J. Haba, F. Takasaki, and A. Yamamoto. Development of a superconducting solenoid magnet system for the b factory detector (belle). *Adv. Cryog. Eng.*, 43:221–228, 1998. P. Kittel, editor. DOI: 10.1007/978-1-4757-9047-4_25.

[49] A. Marshall. Fine wire bonding explained. 2020. URL: https://www.inseto.co.uk/fine-wire-bonding-explained-ikb-064/#:~:text=Wedge%20Bonding%3A,forming%20a%20first%20wedge%20bond..

[50] H. Mateos. *Characterization of Sensors and Components for the Construction of an Array of Photodetectors for Dosimetry in Radiotherapy*, 2016. URL: http://ricabib.cab.cnea.gov.ar/585/1/1Mateos.pdf. Presented 2016.

[51] K. G. McKay. Electron-hole production in germanium by alpha-particles. *Phys. Rev.*, 84:829–832, 4, Nov. 1951. DOI: doi.org/10.1103/PhysRev.84.829.

[52] H.-G. Moser. The belle ii depfet pixel detector. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 831:85–87, 2016. DOI: https://doi.org/10.1016/j.nima.2016.02.078. Proceedings of the 10th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors.

[53] F. Müller. *Characterization and optimization of the prototype DEPFET modules for the Belle II Pixel Vertex Detector*, July 2017. URL: http://nbn-resolving.de/urn:nbn:de:bvb:19-210714.

[54] K. Nakamura, K. Hagiwara, K. Hikasa, H. Murayama, M. Tanabashi, T. Watari, C. Amsler, M. Antonelli, D. M. Asner, H. Baer, H. R. Band, R. M. Barnett, T. Basaglia, E. Bergren, J. Beringer, G. Bernardi, W. Bertl, H. Bichsel, O. Biebel, E. Blucher, S. Blusk, R. N. Cahn, M. Carena, A. Ceccucci, D. Chakraborty, M.-C. Chen, R. S. Chivukula, G. Cowan, O. Dahl, G. D'Ambrosio, T. Damour, D. de Florian, A. de Gouvêa, T. DeGrand, G. Dissertori, B. Dobrescu, M. Doser, M. Drees, D. A. Edwards, S. Eidelman, J. Erler, V. V. Ezhela, W. Fetscher, B. D. Fields, B. Foster, T. K. Gaisser, L. Garren, H.-J. Gerber, G. Gerbier, T. Gherghetta, G. F. Giudice, S. Golwala, M. Goodman, C. Grab, A. V. Gritsan, J.-F. Grivaz, D. E. Groom, M. Grünewald, A. Gurtu, T. Gutsche, H. E. Haber, C. Hagmann, K. G. Hayes, M. Heffner, B. Heltsley, J. J. Hernández-Rey, A. Höcker, J. Holder, J. Huston, J. D. Jackson, K. F. Johnson, T. Junk, A. Karle, D. Karlen, B. Kayser, D. Kirkby, S. R. Klein, C. Kolda, R. V. Kowalewski, B. Krusche, Y. V. Kuyanov, Y. Kwon, O. Lahav, P. Langacker, A. Liddle, Z. Ligeti, C.-J. Lin, T. M. Liss, L. Littenberg, K. S. Lugovsky, S. B. Lugovsky, J. Lys, H. Mahlke, T. Mannel, A. V. Manohar, W. J. Marciano, A. D. Martin, A. Masoni, D. Milstead, R. Miquel, K. Mönig, M. Narain, P. Nason, S. Navas, P. Nevski, Y. Nir, K. A. Olive, L. Pape, C. Patrignani, J. A. Peacock, S. T. Petcov, A. Piepke, G. Punzi, A. Quadt, S. Raby, G. Raffelt, B. N. Ratcliff, P. Richardson, S. Roesler, S. Rolli, A. Romaniouk, L. J. Rosenberg, J. L. Rosner, C. T. Sachrajda, Y. Sakai, G. P. Salam, S. Sarkar, F. Sauli, O. Schneider, K. Scholberg, D. Scott, W. G. Seligman, M. H. Shaevitz, M. Silari, T. Sjöstrand, J. G. Smith, G. F. Smoot, S. Spanier, H. Spieler, A. Stahl, T. Stanev, S. L. Stone, T. Sumiyoshi, M. J. Syphers, J. Terning, M. Titov, N. P. Tkachenko, N. A. Törnqvist, D. Tovey, T. G. Trippe, G. Valencia, K. van Bibber, G. Venanzoni, M. G. Vincter, P. Vogel, A. Vogt, W. Walkowiak, C. W. Walter, D. R. Ward, B. R. Webber, G. Weiglein, E. J. Weinberg, J. D. Wells, A. Wheeler, L. R. Wiencke, C. G. Wohl, L. Wolfenstein, J. Womersley, C. L. Woody, R. L. Workman, A. Yamamoto, W.-M. Yao, O. V. Zenin, J. Zhang, R.-Y. Zhu, P. A. Zyla, G. Harper, V. S. Lugovsky, and P. Schaffner. Review of Particle Physics, 2010-2011. Review of Particle Properties. *J. Phys. G*, 37(7A), 2010. DOI: 10.1088/0954-3899/37/7A/075021.

[55] K. Nishimura. The time-of-propagation counter for belle ii. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 639(1):177–180, May 2011. DOI: 10.1016/j.nima.2010.09.164.

[56] A. Panigada and I. Galton. A 130 mW 100 MS/s pipelined ADC With 69 dB SNDR enabled by digital harmonic distortion correction. *IEEE J. Solid-State Circuits*, 44(12):3314–3328, 2009. DOI: doi.org/10.1109/JSSC.2009.2032637.

[57] R. H. Paul Peter Urone. OpenStax, 2022. URL: https://openstax.org/books/college-physics-2e/pages/1-introduction-to-science-and-the-realm-of-physics-physical-quantities-and-units.

[58] I. Peric. A novel monolithic pixelated particle detector implemented in high-voltage cmos technology. *Nuclear Instruments and Methods in Physics Research*, 582, 3, Dec. 2007. DOI: 10.1016/j.nima.2007.07.115.

[59] I. Perić. Design analoger schaltkreise. 2020. URL: https://adl.ipe.kit.edu/downloads/DAS_2020_Text_8_English.pdf.

[60] I. Perić. *Design and Realisation of Integrated Circuits for the Readout of Pixel Sensors in High Energy Physics and Biomedical Imaging*, 2004. URL: https://cds.cern.ch/record/1334577. Presented 2004.

[61] I. Perić, P. Fischer, J. Knopf, and T. H. H. Nguyen. Dcdb and switcherb, the readout asics for belle ii depfet pixel detector. In *2011 IEEE Nuclear Science Symposium Conference Record*, pages 1536–1539, 2011. DOI: 10.1109/NSSMIC.2011.6154365.

[62] I. Perić, P. Fischer, C. Kreidl, H. H. Nguyen, H. Augustin, N. Berger, M. Kiehn, A. K. Perrevoort, A. Schöning, D. Wiedner, S. Feigl, T. Heim, L. Meng, D. Münstermann, M. Benoit, D. Dannheim, F. Bompard, P. Breugnon, J. C. Clemens, D. Fougeron, J. Liu, P. Pangaud, A. Rozanov, M. Barbero, M. Backhaus, F. Hügging, H. Krüger, F. Lütticke, C. Mariñas, T. Obermann, M. Garcia-Sciveres, B. Schwenker, A. Dierlamm, A. La Rosa, and A. Miucci. High-voltage pixel detectors in commercial CMOS technologies for ATLAS, CLIC and Mu3e experiments. *Nucl. Instruments Methods Phys. Res. Sect. A Accel. Spectrometers, Detect. Assoc. Equip.*, 731:131–136, 2013. DOI: doi.org/10.1016/j.nima.2013.05.006.

[63] M. Prathapan. *High Voltage and Nanoscale CMOS Integrated Circuits for Particle Physics and Quantum Computing*. PhD thesis, Karlsruher Institut für Technologie (KIT), 2020. 186 pages. DOI: 10.5445/IR/1000105789. 54.02.03; LK 01.

[64] I. Pshenichnov, I. Mishustin, and W. Greiner. Comparative study of depth–dose distributions for beams of light and heavy nuclei in tissue-like media. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 266(7):1094–1098, 2008. ISSN: 0168-583X. DOI: https://doi.org/10.1016/j.nimb.2008.02.025.

[65] D. E. B. R. Jacob Baker, Harry W. Li. Cmos Fundamentals.

[66] B. Razavi. *Fundamentals of microelectronics / Behzad Razavi.* eng. Wiley, Hoboken, NJ, 2008. ISBN: 9780471478461.

[67] A. Rivetti. *CMOS: Front-End Electronics for Radiation Sensors*. Devices, Circuits, and Systems. CRC Press, 2018. ISBN: 9781466563117. DOI: 10.1201/b18599.

[68] Robert Kohrs. *Development and Characterization of a DEPFET Pixel Prototype System for the ILC Vertex Detector*. PhD thesis, Rheinische Friedrich-Wilhelms-Universität Bonn, 2008. URL: https://hdl.handle.net/20.500.11811/3684.

[69] M. Sampietro, L. Fasoli, and G. Bertuccio. Source follower or charge amplifier? An experimental comparison using a detector with integrated electronics. *IEEE Transactions on Nuclear Science*, 43(4):2413–2418, 1996. DOI: 10.1109/23.531790.

[70] R. Schimassek. *Development and Characterisation of Integrated Sensors for Particle Physics*. PhD thesis, Karlsruher Institut fur Technologie (KIT), 2021. DOI: doi.org/10.5445/IR/1000141412.

[71] R. Schimassek. *Entwicklung und Charakterisierung von Integrierten Sensoren für die Teilchenphysik = Development and Characterisation of Integrated Sensors for Particle Physics*. PhD thesis, Karlsruher Institut für Technologie (KIT), 2021. 215 pages. DOI: 10.5445/IR/1000141412.

[72] C. Schömers, E. Feldmeier, J. Naumann, R. Panse, A. Peters, and T. Haberer. Patient-specific intensity-modulation of a slowly extracted beam at the hit-synchrotron. In pages 2944–2946, Sept. 2013.

[73] J. R. Schwank. Basic mechanisms of radiation effects in the natural space radiation environment, June 1994. URL: https://www.osti.gov/biblio/10158182.

[74] J. Seco, B. Clasie, and M. Partridge. Review on the characteristics of radiation detectors for dosimetry and imaging. *Physics in Medicine and Biology*, 59(20):R303–R347, Sept. 2014. DOI: 10.1088/0031-9155/59/20/r303.

[75] S. Smith. MOS Devices and Basic Circuits. *Des. VLSI Syst. — A Pract. Introd.*, 2010. DOI: doi.org/10.1007/978-1-349-18700-3_2.

[76] W. J. Snoeys, T. A. Palacios Gutierrez, and G. Anelli. A new NMOS layout structure for radiation tolerance. *IEEE Trans. Nucl. Sci.*, 49 I(4):1829–1833, 2002. DOI: doi.org/10.1109/TNS.2002.801534.

[77] A. L. Steinhebel, H. Fleischhack, N. Striebig, M. Jadhav, Y. Suda, R. Luz, C. A. Kierans, R. Caputo, H. Tajima, R. Leys, I. Peric, J. Metcalfe, and J. S. Perkins. AstroPix: novel monolithic active pixel silicon sensors for future gamma-ray telescopes. Technical report, 2022. DOI: 10.48550/arXiv.2209.02631.

[78] H. D. Suit, T. Delaney, S. Goldberg, H. Paganetti, B. M. Clasie, L. E. Gerweck, A. Niemierko, E. J. Hall, J. Flanz, J. Hallman, and A. V. Trofimov. Proton vs carbon ion beams in the definitive radiation treatment of cancer patients. *Radiotherapy and oncology : journal of the European Society for Therapeutic Radiology and Oncology*, 95 1:3–22, 2010.

[79] D. M. S. Sultan, S. Gonzalez-Sevilla, D. Ferrere, G. Iacobucci, E. Zaffaroni, W. Wong, M. Kiehn, and M. Benoit. Electrical characterization of 180 nm ATLASPix2 HV-CMOS monolithic prototypes for the high-luminosity LHC. *Journal of Instrumentation*, 15(05):P05022–P05022, May 2020. DOI: 10.1088/1748-0221/15/05/p05022.

[80] G. C. Temes. In *Analog Circuit Design: Low-Noise, Low-Power, Low-Voltage; Mixed-Mode Design with CAD Tools; Voltage, Current and Time References*. J. H. Huijsing and W. M. C. van de Plassche Rudy J. and Sansen, editors. Springer US, 1996, pages 45–64. DOI: 10.1007/978-1-4757-2462-2_3.

[81] A. Thompson. *X-Ray Data Booklet*. Lawrence Berkeley National Laboratory, University of California, 2009. URL: https://cxro.lbl.gov//PDF/X-Ray-Data-Booklet.pdf.

[82] H. Tsujii. Overview of carbon-ion radiotherapy. *Journal of Physics: Conference Series*, 777:012032, June 2017. DOI: 10.1088/1742-6596/777/1/012032.

[83] R. Turchetta. *Analog Electronics for Radiation Detection*. Devices, Circuits, and Systems. CRC Press, 2017. ISBN: 9781498703574. DOI: 10.1201/b20096.

[84] *Vertical Cavity Surface Emitting Laser*. (OPV300). Rev. C. TT Electronics. July 2018.

[85] A. Weber, F. Ehrler, R. Schimassek, and I. Perić. High-voltage cmos active pixel sensor chip with counting electronics for beam monitoring. *IEEE Transactions on Nuclear Science*, 69(6):1288–1298, 2022. DOI: 10.1109/TNS.2022.3173807.

[86] A. L. Weber. *Development of Integrated Circuits and Smart Sensors for Particle Detection in Physics Experiments and Particle Therapy*. PhD thesis, Karlsruher Institut für Technologie (KIT), 2021. 171 pages. 54.12.01; LK 01.

[87] H. [Zhang. *Entwicklung integrierter Detektoren für geladene Teilchen und Photonen*. PhD thesis, Karlsruhe, 2022. DOI: 10.5445/IR1000143574. aa.

[88] Y. Zhang. Pn-junction diode. In *The Tao of Microelectronics*, 2053-2571, 2-1 to 2–15. Morgan and Claypool Publishers, 2014. DOI: 10.1088/978-1-6270-5453-9ch2.

[89] D. Zhu, H. Shi, C. Wu, and X. Zhang. An electron counting algorithm improves imaging of proteins with low-acceleration-voltage cryo-electron microscope. *Communications Biology*, 5(321):2399–3642, 2022. DOI: 10.1038/s42003-022-03284-1.

Attended courses

Thanks to the Marie Skłodowska-Curie Organizations and the Horizont-2020 program[1], during my time as a fellow I was able to attend several courses to improve and deepens my knowledge on semiconductors and chip design, as well as soft skills:

- Europractice course on Analog Design 25.11.2019 – 27.11.2019
- Secondment at University of Geneva and CERN 02.09.2019 – 13.09.2019
- MEAD Advance CMOS IC Design 26.08.19 – 30.08.19
- MEAD Low Power IC Analog Design 24.06.19 – 28.06.19
- Secondment at Thermo Fisher 29.04.19 – 03.05-19
- EAMTA Conference and Course in Analog Design 09.03.19 – 15.03.19
- Workshop on CV Writing and Interviews 24.01.19
- PRINCE2 Project Management Course 14.01.19 – 18.01.19
- ICTP Advance Workshop on FPGA-Based System-on-Chip for Scientific Instrumentation 26.11.18 – 07.12.18
- Europractice course in Verilog and SystemVerilog 06.11.18 – 9.11.18
- STREAM Joint Training Course and Workshop on Entrepreneurship 19.06.18 – 20.06.18
- Hands-on Characterization of Solid-State Image Sensors 21.05.18 – 25.05.18
- Secondment at Thermo Fisher 09.04.18 – 13.04.18
- German Courses (A1.1 – A1.2 – A2.1 – A2.2 – B1) during 2018 and 2019.
- STREAM Winter School 06.11.17 – 22.11.17

[1]Smart Sensor Technologies and Training for Radiation Enhanced Applications and Measurements (STREAM) have received funding from the "European Union's Horizon 2020 Research and Innovation Programme" under the Grant Agreement No 675587

Acknowledgements

I would like to thank Prof. Dr. Ivan Perić for giving me the chance of pursuing a Ph.D. under his supervision. This thesis would have not been possible without all his outstanding support and help. He has proven over and over that he is a great Professor, supervisor and person.

Also special thanks to Prof. Dr. Ulusoy Ahmet Cagri from the "Elektrotechnik und Informationstechnik" (ETIT) institut at KIT for taking the time to read and evaluate my dissertation as a second supervisor.

I would like to use this opportunity to thank my colleges from ADL group, specially Dr. Rudolf Schimassek, Dr. Richard Leys, and Dr. Felix Ehrler for all the support and help along the path. Their expertise in programming as well as in physics were invaluable to the development of this thesis. Also I would like to mention the help of my colleges Nicolas Striebig and Sigrid Scherl for helping to perform measurements with HINT sensor when COVID-19 disabled me to do so.

A special mention needs to be done to Andrea Ferreti and Luigi Mele, who I worked along the development of HPIXEL. Both, as the experts in electron microscopy and being the link between both institutions (KIT and Thermo Fischer Scientific), made possible to carried the project forward, always helping and guiding.

I would also like to thank Benjamin Layrer and Pia Steck, their expertise in wire bonding made possible to use the sensors developed as well as to learn how to wire bond myself.

I want to give a special shout-out to my family, whose support and guidance alongside my life have meant the world to me. Without them, I wouldn't be here today. They've always been there for me. I can't thank them enough for believing in me every step of the way.

Finally I want to thank and dedicate this thesis to my wife, Dr. M.Sc. Sofía Belén García Fracaro, for her unconditional support along the path. For being my companion during this time and for being by my side any time I was feeling down, pushing me to move forward.

Karlsruhe, October 18, 2023