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A New Resistive Adaptive Gate-Driving Concept with Automated Identification of Operational Parameters

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Abstract

This paper proposes a new adaptive gate-driving concept based on parallel-connected resistive driving stages, which allows the modification of the effective gate-resistance for every turn-on and turn-off event during operation. By selecting the appropriate gate-resistance, the switching behavior can be optimized individually for each specific operating point $(V_{\mathrm{sw}}, I_{\mathrm{sw}}, T_{\mathrm{j}})$. As a result, higher efficiency under partial load can be achieved. The selection of effective gate-resistance is based on the results of a here introduced automatic optimization method, which takes constraints such as dv/dt- and di/dt-limits into account. Subject of this paper is also the comparison of the new approach with the widely used single-stage resistive driver.

1 Introduction

Resistive gate-drivers with one output stage comprising one turn-on gate-resistor $R_{\mathrm{G,on}}$ and one turn-off gate-resistor $R_{\mathrm{G,off}}$ are still dominant in industry due to their low-cost and simplicity [1], [2]. The two gate-resistance have to be chosen such that the power semiconductor never leaves its Safe-Operating Area (SOA) during normal operation. In other words, the design parameters are optimized for only the „worst-case“ operating point of the semiconductor device. Qualitatively, this operating point occurs at high blocking voltages V_{sw}, high load currents I_{sw} and comparably low junction temperatures T_{j}, mainly temperatures below common operating temperatures.

Many applications, like electric cars or inverters used in renewable energies, mainly operate under partial load conditions and at temperatures T_{j} way higher than in the worst-case operating point. Consequently, the switching behavior of the system is mostly suboptimal, especially in terms of efficiency.

Adaptive gate-drivers have the ability to tackle that issue by allowing more degrees of freedom (DOF). They can be classified into open-loop and closed-loop drivers [3], [4]. Closed-loop drivers actively control the switching transient, for instance quantities like dv/dt and di/dt [4]. Such drivers require very fast measurement and control systems since the switching trajectories need to be acquired and controlled in real-time. Note that the duration of switching transients of modern wide-bandgap power semiconductors can be in the range of tens of nanoseconds, which makes such concepts difficult to realize from an economical point of view.

Open-loop drivers generally do not require such measurement circuits and are therefore often the less costly and less complex approach. In order to utilize the high DOF, one needs to define a control strategy. One possible way is to optimize the trajectory of the gate's state variables v_{GE} and/or i_{G}. In [5] such a trajectory optimization scheme is presented. The objective was to minimize the switching losses, whilst limiting the surge voltage of the switching transient. Thereby the optimization was conducted for a single operating point. Note that trajectory optimization can be of very high dimension and therefore time-consuming, especially if one has to determine an optimal trajectory for many operating points.

A simpler and less complex method is to optimize the operational parameters of the gate driver. Depending on the applied gate-driver topology, this can be for instance the gate current i_{G} or the gate resistance R_{G}. In [6] the gate current i_{G} is varied load current dependent using a commercially available driver to optimize the turn-on losses in a variable frequency drive. Thereby, dv/dt was constrained to limit insulation stress and EMI. [7] or [8] proposes a novel converter-based driver topology, where the constant gate current was adjusted such that the surge voltage is optimized for a wide operating range.

It is also possible to combine trajectory optimization with operating point dependent switching in a limited fashion. In [9] the concept from [5] was expanded by an operating point dependent action. Below a certain load current threshold, the gate driver applies constant current to the gate. Above the threshold, an optimized gate current trajectory was applied to limit the surge voltage.

In this paper, an open-loop driver topology with variable gate resistance is proposed. The topology is hereby similar to the topologies summarized in [3] and [4]. The operation strategy is to choose an optimal gate resistance individually for each operating point $(V_{\mathrm{sw}}, I_{\mathrm{sw}}, T_{\mathrm{j}})$ based on a here introduced optimization problem. The latter has the objective to minimize the switching losses with respect to constraints, like maximum surge voltage and surge current, maximum dv/dt and di/dt. In contrast to previous works [6]–[9] more constraints are taken into account. Further, the optimization is done for a larger operating range and is done automatically.

In order to apply the proposed gate driving concept to a converter system, the operating point can be either determined by the built-in measurement system or by employing low-cost measurement circuits on the gate-driver itself. There is no high bandwidth requirement on the measurement system, because it is sufficient to determine the operating point once per switching period. Therefore it is possible to apply the concept to modern fast-switching wide-bandgap power semiconductors, such as GaN or SiC. If the optimization is carried out conservatively, the accuracy requirement can be lowered.

2 Proposed Gate-Driver Circuit

The proposed gate-driver circuit (fig. 1) consists of several commercially available voltage-source gate-driver-stages such as [10]. The latter usually comprise a push-pull output stage, whose output can assume either their positive supply voltage $V_{\mathrm{S}+}$ (on-state) or their negative supply voltage $V_{\mathrm{S}-}$ (off-state). Each driver-stage is connected to the gate-terminal of the power semiconductor through a diode and a resistor. There are N_{on} driver-stages comprising a serial-connected diode belonging to the turn-on-stages. The remaining N_{off} stages with anti-serial-connected diodes belong to the turn-off-stages.

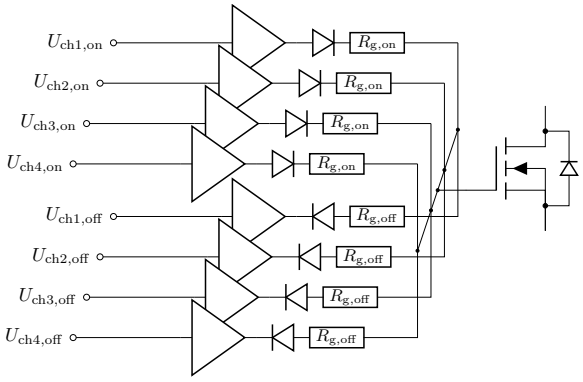

Fig. 1: Simplified schematic of the proposed gate-driver

The value of N_{on} and N_{off} depends on the desired quantization of the resulting equivalent turn-on resistor $R_{\mathrm{G,on}}$ and turn-off resistor $R_{\mathrm{G,off}}$. Besides that, the peak current $I_{\mathrm{g,peak}}$ of a single driver stage and the required total maximum gate-current $I_{\mathrm{G,peak}}$ yield the minimum for N_{on} and N_{off}.

Under the assumption that every driver-stage has the same $I_{\mathrm{g,peak}}$, it is meaningful that their $R_{\mathrm{g,on}}$ and $R_{\mathrm{g,off}}$ are of equal value for optimal device utilization. The possible turn-on resistance $R_{\mathrm{G,on}}$ and turn-off resistance $R_{\mathrm{G,off}}$ are then

$$R_{\mathrm{G,on}} := \left\{ \frac{R_{\mathrm{g,on}}}{k} \middle| k \in [1, N_{\mathrm{on}}] \text{ and } k \in \mathbf{N} \right\}, \quad (1)$$

$$R_{\mathrm{G,off}} := \left\{ \frac{R_{\mathrm{g,off}}}{k} \middle| k \in [1, N_{\mathrm{off}}] \text{ and } k \in \mathbf{N} \right\}. \quad (2)$$

Thus the number of possible $R_{\mathrm{G,on}}$ equals N_{on}. The same applies to the possible number of $R_{\mathrm{G,off}}$.

For turning the semiconductor on, the desired number k of the N_{on} turn-on stages have to be switched on. Further, all N_{off} turn-off stages

have to be switched on as well to prevent a current flowing through $R_{\mathrm{G,off}}$. In order to turn the semiconductor off, the desired k of N_{off} turn-off stages have to be switched off. To prevent a current flowing through $R_{\mathrm{G,on}}$, additionally all turn-on stages have to be switched off.

Instead of using push-pull drivers, the same functionality can be achieved by employing P-channel MOSFETs in the turn-on path and N-channel MOSFETs in the turn-off path of the power semiconductor, as proposed in [4].

3 Hardware Prototype

For validation of the gate-driver concept from fig. 1 together with the introduced control strategy, a hardware prototype (fig. 2) has been designed. As device under test (DUT), a custom *DCM1000X*-module [11] from *Danfoss*, employing eight *EPM3-1200-0017D*-Chips [12] from *Wolfspeed* is used. The module has a maximum current capability $800\,\mathrm{A}$ and features a maximum blocking voltage of $1200\,\mathrm{V}$.

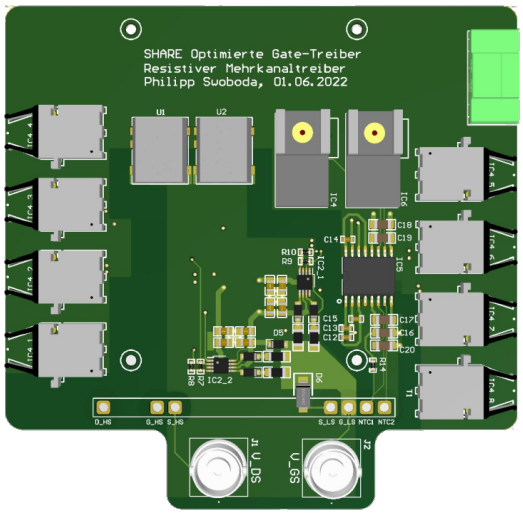

Fig. 2: Hardware implementation

The initial design requirement was to feature a peak gate current $i_{\mathrm{G,peak}}$ of about 20 A for a gate-source voltage swing $\Delta V_{\mathrm{G}} = V_{\mathrm{S+}} - V_{\mathrm{S-}} = 15\,\mathrm{V} - (-5\,\mathrm{V}) = 20\,\mathrm{V}$ and minimum equivalent gate resistance $R_{\mathrm{G,on}}$ resp. $R_{\mathrm{G,off}}$ of $1.4\,\Omega$ each. Using the commercially available *EiceDRIVER 2EDN8524R* [10] from *Infineon*, each consisting of two $5\,\mathrm{A}$ driver-stages, the resulting number of stages for turn-on and turn-off amounts $N_{\mathrm{on}} = N_{\mathrm{off}} = 4$. For optimal device utilization and equal load of the driver stages, $R_{\mathrm{g,on}} = R_{\mathrm{g,off}} = 5.6\,\Omega$ was chosen as stage resistance. Note that besides the resulting $R_{\mathrm{G,on}}$ or $R_{\mathrm{G,off}}$, the total gate resistance $R_{\mathrm{G,total}}$ also consists of the internal gate resistance $R_{\mathrm{G,int}}$ of the power semiconductor and the output impedance of the driver stages.

The gate signals for the driver stages are generated using a custom logic on the programmable logic part of the modular signal processing system introduced in [13]. Besides that, a Sigma-Delta-Converter digitizes the temperature sensor of the DCM1000X-module. For better EMI properties, all signals are transmitted using fiber optics.

For the identification of operational parameters and for the validation of the concept, double pulse measurements were conducted using the (modified) test setup introduced in [14]. The signal processing completely controls the double pulse test setup and therefore knows the current operating point of the power semiconductor. Using the optimization results from the next section, the signal processing system can select the optimal gate resistance for each switching event.

4 Automated Identification of Operational Parameters

4.1 Optimization Problem

The choice of $R_{\mathrm{G,on}}$ and $R_{\mathrm{G,off}}$ (and thus k) for each specific operating point $(V_{\mathrm{sw}}, I_{\mathrm{sw}}, T_{\mathrm{j}})$ can be determined by solving the following optimization problem:

$$J(R_{\mathrm{G},l}) = E_{\mathrm{sw},l}(R_{\mathrm{G},l}) \rightarrow \min \tag{3}$$

subject to

$$V_{\mathrm{sw,max}}(R_{\mathrm{G},l}) - V^{*}_{\mathrm{sw,max}} \leq 0, \tag{4}$$
$$I_{\mathrm{sw,max}}(R_{\mathrm{G},l}) - I^{*}_{\mathrm{sw,max}} \leq 0, \tag{5}$$
$$|\dot{v}_{\mathrm{sw}}(R_{\mathrm{G},l})| - \dot{v}^{*}_{\mathrm{sw,max}} \leq 0, \tag{6}$$
$$\left|\dot{i}_{\mathrm{sw}}(R_{\mathrm{G},l})\right| - \dot{i}^{*}_{\mathrm{sw,max}} \leq 0, \tag{7}$$
$$\Delta v_{\mathrm{sw}}(R_{\mathrm{G},l}) - \Delta v^{*}_{\mathrm{sw,max}} \leq 0, \tag{8}$$
$$\Delta i_{\mathrm{sw}}(R_{\mathrm{G},l}) - \Delta i^{*}_{\mathrm{sw,max}} \leq 0, \tag{9}$$

where $l = \{\mathrm{on}, \mathrm{off}\}$. The optimization algorithm therefore has to choose $R_{\mathrm{G},l}$ such that the switching energies $E_{\mathrm{sw},l}$ both for turn-on and turn-off are minimized without violating the constraints (4) to (9).

The constraints have the following purpose:

- Constraints (4) and (5) ensure that the power semiconductor never leaves its SOA.
- Constraints (6) and (7) limit the maximum allowed $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$. This is useful to mitigate insulation stress [6] or to meet EMI requirements [15].
- Constraint (8) limits the surge voltage occurring when turning the device off, caused by the stray inductance L_σ of the commutation loop [1] and $\mathrm{d}i/\mathrm{d}t$.
- Constraint (9) limits the surge current when turning the device on, caused by the voltage dependent reverse recovery charge Q_{rr}.

A graphical explaination of the constraints in connection with the switching transients is depicted in fig. 3 and 4.

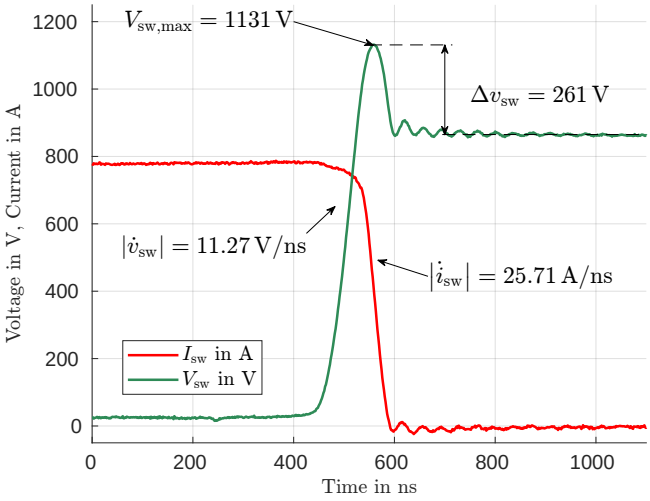

Fig. 3: Turn-off transient for $R_{\mathrm{G,off}} = 2.8\,\Omega$

If one considers the exemplary constraints from table 1, one can see that all constraints are satisfied for the turn-on transient. For the turn-off transient it is noticeable, that the constraints (4), (6) and (7) are not met.

Note that the switching losses decrease with decreasing $R_{\mathrm{G},l}$. Therefore, the objective function (3) is a monotonically decreasing function. Apart from that, the constraints increase with decreasing $R_{\mathrm{G},l}$. This is because the constraints (6) and (7) increase with increasing gate-current i_{G} [7] and also affect the other constraints to increase.

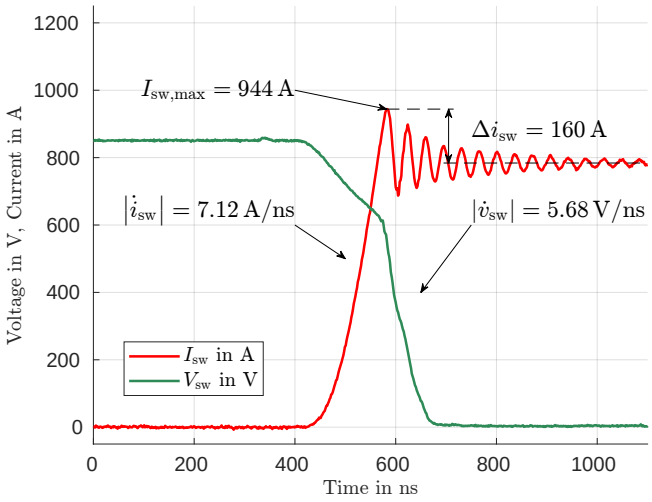

Fig. 4: Turn-on transient for $R_{\mathrm{G,on}} = 2.8\,\Omega$

4.2 Optimization Algorithm

In order to solve the given optimization problem defined by equations (3) to (9) one theoretically needs to know the switching transients for every possible operating point $(V_{\mathrm{sw}}, I_{\mathrm{sw}}, T_{\mathrm{j}})$. Further, equations (3) to (9) are theoretically required as continuous functions of $R_{\mathrm{G},l}$.

However, the optimization has to be based on real measurement data or a circuit simulation, because accurate analytical models for eq. (3) to (9) don't exist. Both methods can be quite time-consuming. Therefore it is reasonable to limit the number of operating points by means of discretization. For the operating points, we chose steps of 50 A and 50 V in the range of

$$V_{\mathrm{sw}} \in [450, 850]\,\mathrm{V}, \tag{10}$$
$$I_{\mathrm{sw}} \in [100, 800]\,\mathrm{A} \tag{11}$$

and an operating temperature T_{j} of $25\,^{\circ}\mathrm{C}$. This results in a total number of 135 operating points for each the optimization problem has to be solved.
In the given case, values of equations (3) to (9) for a specific $R_{\mathrm{G},l}$ are determined by evaluating the switching transients obtained from double-pulse measurements. From a single double-pulse measurement one obtains the switching transients for turn-on and turn-off. With $N_{\mathrm{on}} = N_{\mathrm{off}} = 4$, the required number of such measurements amounts 540.

As described in the previous section, the objective function (3) is monotonically decreasing whereas the constraints increase monotonically

with $R_{\mathrm{G},l}$. Keeping this into mind, constrained optimization algorithms like *Nonlinear Quadratic Programming* are not necessary. A simple optimization algorithm as described in fig. 5 is sufficient. It works as follows:
First one has to select an operating point, where the optimization is to be applied. Next, one selects the lowest possible $R_{\mathrm{G},l}$. Then eq. (3) attains its lowest and eq. (4) to (9) their highest values. The next steps are to measure and evaluate the switching transients. Subsequently, the constraints have to be checked for satisfaction. If the latter is the case, the optimal $R_{\mathrm{G},l}$ has been found. If not, the whole procedure has to be performed again with the next higher possible $R_{\mathrm{G},l}$. In case the highest possible $R_{\mathrm{G},l}$ is reached, the optimizer will always consider the current configuration as optimal, regardless if there is any constraint violation. The constraint violation will thereby be kept as small as possible. However, such operating points should be flagged by the algorithm.

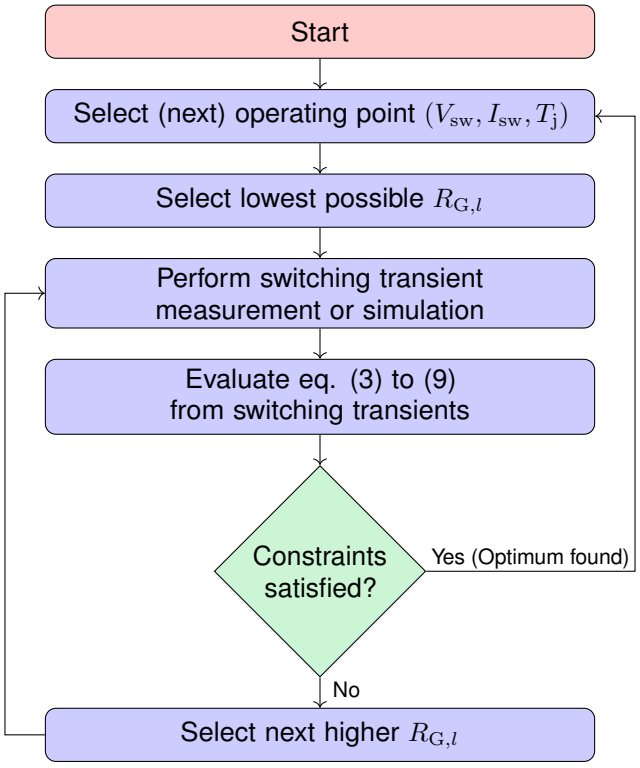

Fig. 5: Optimization algorithm

The optimization procedure can be almost completely automated. However, special care must be taken when selecting the lowest value of $R_{\mathrm{G,off}}$, because the resulting surge voltage might exceed the absolute maximum rating V_{sw} of the power semiconductor. It is therefore required to select $R_{\mathrm{G,off}}$ manually for the worst case operating point. As mentioned earlier, that operating point generally occurs at low operating temperature, highest operating voltage and current.

4.3 Optimization results from exemplary constraints

For the comparison with a conventional gate driver, optimization results based on appropriate constraints are needed. The constraints are given in table 1. The dv/dt-constraint (6) is a typical value in automotive electric drive systems [16].

Eq.	Constraint	Constraint value
(4)	$V^*_{\mathrm{sw,max}}$	1100 V
(5)	$I^*_{\mathrm{sw,max}}$	1200 A
(6)	$\dot{v}^*_{\mathrm{sw,max}}$	10 V/ns
(7)	$\dot{i}^*_{\mathrm{sw,max}}$	20 A/ns
(8)	$\Delta v^*_{\mathrm{sw,max}}$	350 V
(9)	$\Delta i^*_{\mathrm{sw,max}}$	350 A

Tab. 1: Exemplary constraints

Constraints (4) and (5) were chosen to ensure safe operation of the DUT. Thereby, the maximum current $I_{\mathrm{sw,max}}$ can be set as the maximum allowed pulsed drain current of the module, since the current surge is of very short duration. Constraint 7 is chosen to ensure a safe operation of the device, for instance to limit the feedback in the gate loop from the common source inductance of the module.

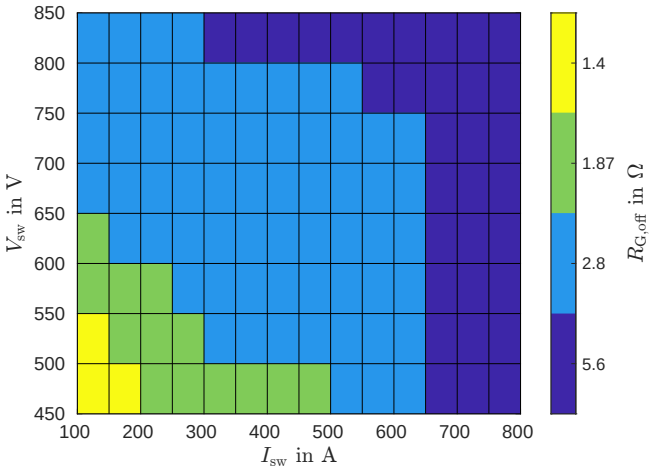

Fig. 6: Decision boundaries for turn-off

Figure 6 shows the decision boundaries for the choice of the effective gate resistance $R_{\mathrm{G,off}}$ dependent on the switching voltage and the switching current for a temperature T_{j} of $25\,^{\circ}\mathrm{C}$. It can be

seen, that $R_{\mathrm{G,off}}$ increases with increasing current and voltage. During the optimization procedure, no constraint violations occurred. In fig. 12 and 14 the dv/dt at turn-off and the turn-off surge voltage Δv_{sw} is plotted over the current I_{sw} for different voltages V_{sw}. One can see that those constraints are satisfied for the depicted operating points.

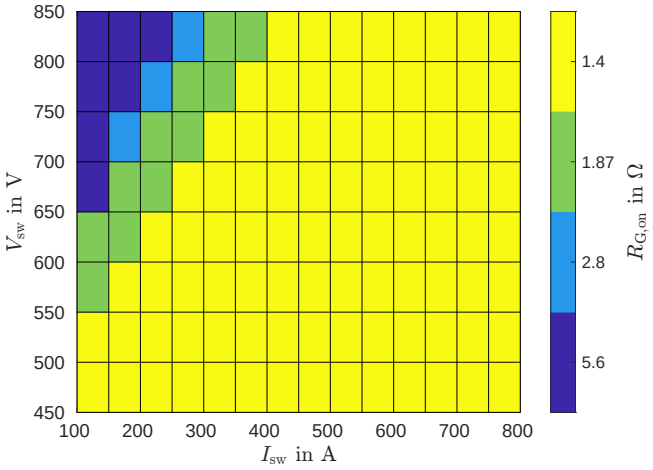

Fig. 7: Decision boundaries for turn-on

Figure 7 shows the decision boundaries for turn-on at $25\,^{\circ}\mathrm{C}$. Because of the high dv/dt at low currents and high voltages, the optimizer limited the switching speed. Similar results were obtained in [6]. For most of the other operating points, the lowest on-resistance $R_{\mathrm{G,on}}$ can be used.

In figures 13 and 15, the dv/dt for turn-on and the turn-on surge current Δi_{sw} are plotted over the current for different voltages. It is noticeable, that the dv/dt-constraint is violated for higher voltages and small currents. In that case, the optimizer already has chosen the highest $R_{\mathrm{G,on}}$ to keep the violation as small as possible.

5 Comparison of the New Concept with a Conventional Driver

Using the optimization results from the last section, the proposed gate driver circuit from fig. 1 can be compared with a conventional gate driver consisting of one turn-on and one turn-off gate resistor. Thereby the hardware prototype imitates a conventional driver by choosing the optimal (constant) resistance values $R_{\mathrm{G,on}}$ and $R_{\mathrm{G,off}}$ for the worst-case operating points. As one can see from fig. 6 and 7, the highest resistance value needs to be considered both for turn-on and turn-off, namely $R_{\mathrm{G,on}} = R_{\mathrm{G,off}} = 5.6\,\Omega$.

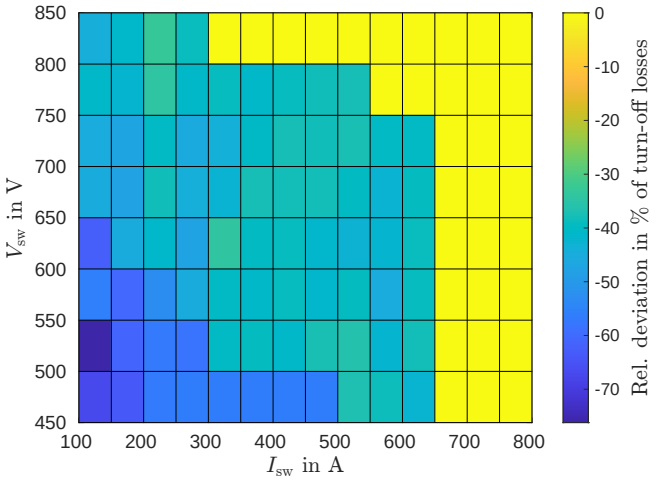

Fig. 8: Relative improvement of turn-off losses

In fig. 8 the relative improvement of turn-off losses is depicted graphically. It is noticeable, that the switching losses can be reduced under partial load conditions by at least $30\,\%$. For low currents between $100\,\mathrm{A}$ and $200\,\mathrm{A}$, the improvement even amounts $60\,\%$ to $70\,\%$. For currents larger than $650\,\mathrm{A}$, no improvements are possible, because the highest gate-resistor $R_{\mathrm{G,off}}$ has to be used to satisfy the constraints. In this case, especially the maximum-voltage-constraint (4) becomes critical, as can be seen in fig. 14. With increasing voltage V_{sw}, that constraint becomes more critical and one needs to use the highest $R_{\mathrm{G,off}}$ even below $650\,\mathrm{A}$.

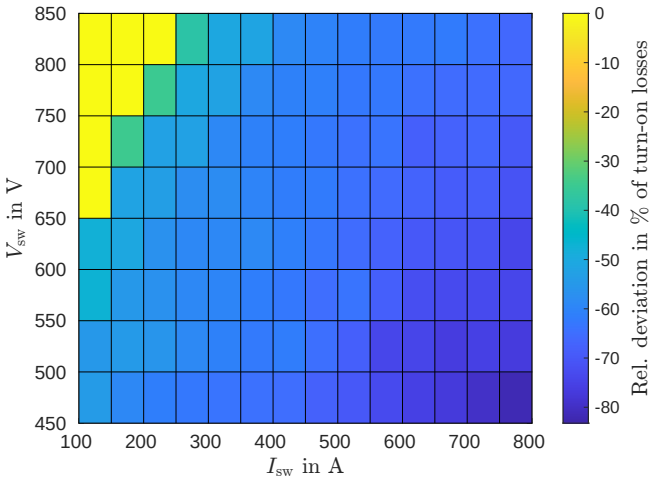

Fig. 9: Relative improvement of turn-on losses

Figure 9 shows the relative improvement of turn-on losses. As already mentioned, it is difficult to satisfy the dv/dt constraint (see fig. 13) for low currents and high voltages. At such operating points, no improvements can be achieved, because the highest $R_{\mathrm{G,on}}$ has to be chosen.

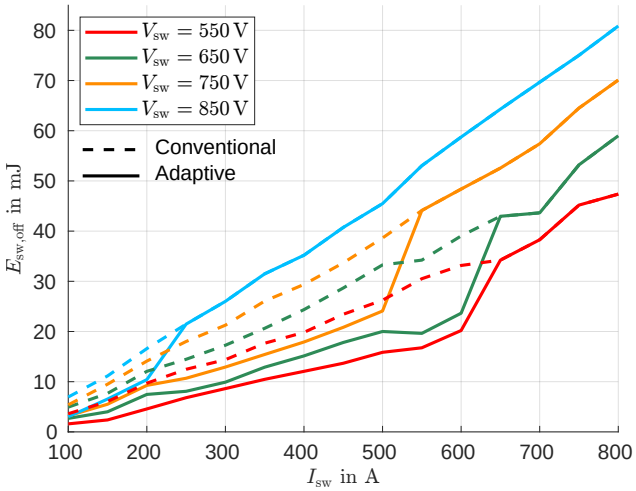

Fig. 10: Comparison of turn-off energies

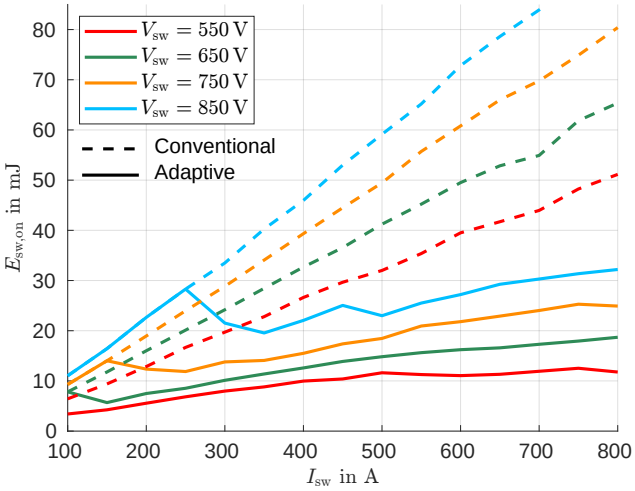

Fig. 11: Comparison of turn-on energies

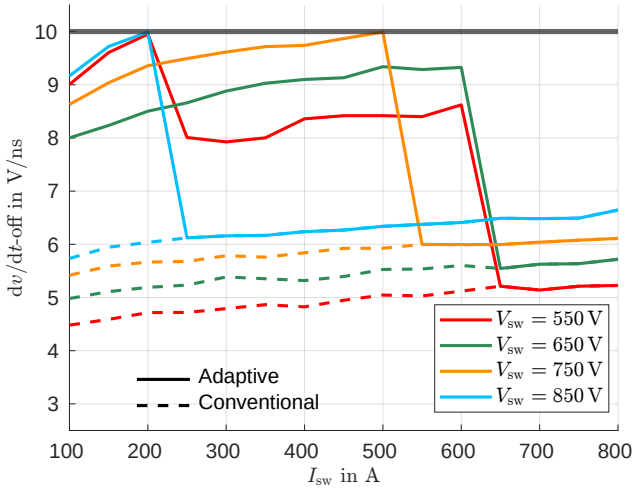

Fig. 12: Comparison of turn-off dv/dt

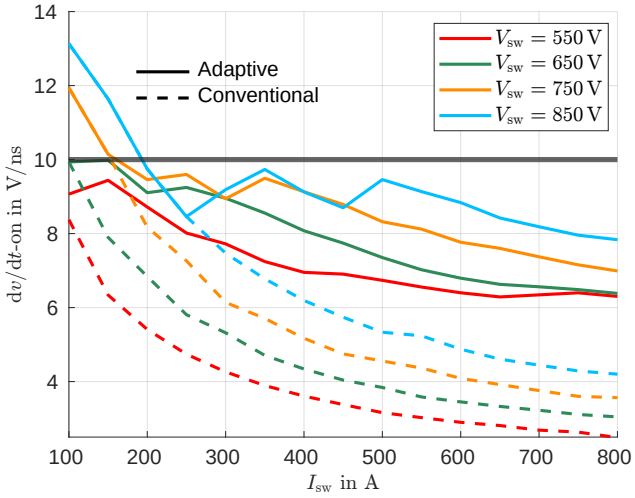

Fig. 13: Comparison of turn-on dv/dt

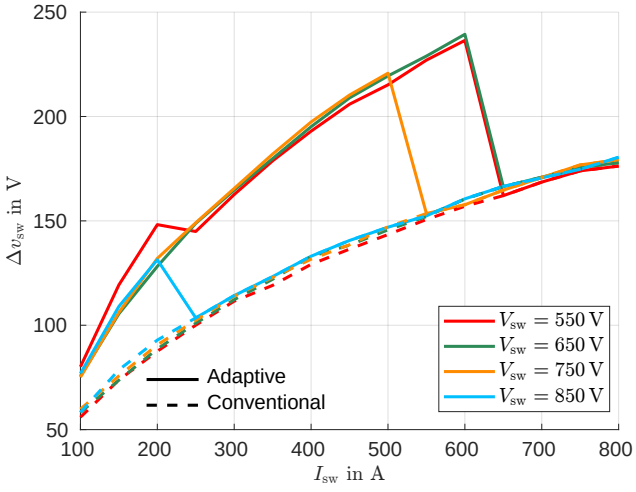

Fig. 14: Comparison of turn-off Δv_{sw}

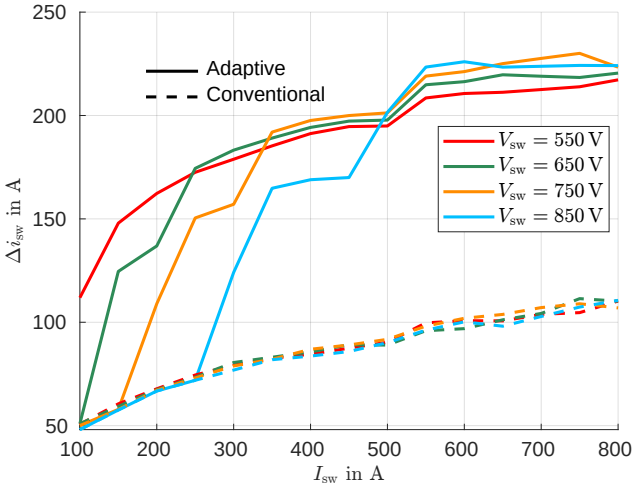

Fig. 15: Comparison of turn-on Δi_{sw}

On almost all other operating points, the fastest switching speed can be chosen, which results in a very high loss reduction of up to $80\,\%$. However, this result should be considered with caution, because when using conventional drivers, the $\mathrm{d}v/\mathrm{d}t$ constraint is difficult to meet. In this case, one chooses a trade-off between low $\mathrm{d}v/\mathrm{d}t$ and low switching losses. Due to this, the use of the proposed control strategy could also have positive effects on the life expectancy of the load's insulation. For the sake of completeness, figure 11 and 10 compare the absolute losses of the adaptive and the conventional driver.

6 Conclusion

In this paper, a new adaptive gate-driving concept with automated identification of operational parameters is proposed. It was shown, that the total switching losses of a SiC-module can be reduced significantly under partial load conditions, which is usually the case for many power electronic applications. This advantage comes especially into effect in AC-applications, because the maximum switching current is rarely reached due to the sinusoidal output current, even at high RMS currents. If there is a varying voltage on the DC-side, as the case in automotive or photovoltaic applications, the potential of the proposed concept can be fully enabled.

The new concept is technically simple and can be realized using widely used low-cost electronic components. This is especially the case, because no high-speed components are required, even if fast switching wide-bandgap semiconductors are used. Further, the proposed automatic optimization method simplifies the design process of the concept significantly and could be also used for gate resistance determination of conventional gate-drivers.

Until now, the concept is validated for only one temperature at $T_\mathrm{j} = 25\,^\circ\mathrm{C}$. Therefore, a validation for more temperatures may be interesting for future work.

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