Hybrid Implementation of Cascade Control for GaN-Based Modular Multilevel Converter for Low-Voltage Grid

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***Index Terms*—Modular Multilevel Converters (MMC), Grid-connected converter, Control strategy, Proportional Resonant Control, Fault ride-through**

***Abstract*—A hybrid control system implementation for a Modular Multilevel Converter (MMC) prototype is presented in this paper. The cascade control using an ARM processor for the energy controller and a field programmable gate array (FPGA) for the current controllers, allows the GaN semiconductors to generate an output current with an effective ripple frequency of 200 kHz. The MMC system model and the partitioning of the cascade control are shown. With its dynamic current limit, implemented in the FPGA, the MMC is able to provide AC currents above the nominal current. Finally, prototype measurements of an emulated grid fault are shown.**

I. Introduction

The Modular Multilevel Converter (MMC) was presented for the first time in [1]. Due to its modular design with numerous submodules connected in series, the MMC offers a high output voltage quality and allows the use of power semiconductors whose blocking voltage is several times lower than the system output voltage. Compared to other multilevel topologies, such as flying capacitor inverters [2, 3], the MMC half-bridge or full-bridge cells allow for smaller commutation loops. This is especially beneficial in case of fast switching SiC or GaN semiconductors, which can only unfold their high efficiency potential in case of a low parasitic inductance

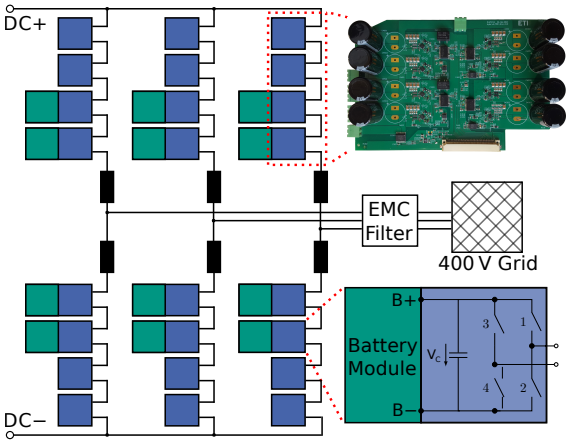

Fig. 1. MMC prototype overview

in the commutation loop. However, the high amount of capacitors, the high level of system complexity and the significant control effort contradict the previously mentioned advantages. In this paper, the control system for an MMC for the low-voltage grid is shown using a hardware prototype, which was presented in [4]. It uses a compact GaN-based arm PCB with four full-bridge cells as shown in Fig. 1. A central System-on-Chip (SoC) for the signal processing allows the reduction of the system complexity, as the 24 cells are directly controlled by the FPGA of the SoC, thus avoiding local control units on the MMC cells. A hybrid control approach is chosen, where complex control algorithms are executed in the ARM processor of the SoC for reduced implementation time and simple but fast control algorithms are executed in the FPGA of the SoC. Compared to [5], the FPGA additionally runs the current controllers and the grid voltage, frequency and phase detection.

The battery modules depicted in Fig. 1 are not yet implemented, thus the MMC in this paper only uses

identical capacitor-based cells.

In Section II, the MMC model is derived to provide a mathematical basis for controller design. In Section III, the controllers for the inner arm current control loop are explained and the cascade control structure is shown. Finally, in Section IV the control design and its hybrid implementation are verified by measurements with a Power-Hardware-in-the-Loop (PHIL) grid emulator. Thereby, a grid fault is emulated and the response of the presented MMC prototype and its controller is shown.

II. MMC Model

To control an MMC, a system model has to be derived. In Fig. 2 the schematic of the MMC is shown. All cells in each MMC arm are combined and modeled as an ideal voltage source. This is valid because the modulation frequency of $100\,\mathrm{kHz}$ is several magnitudes higher than the output frequency of $50\,\mathrm{Hz}$ in grid applications and the inductors are sufficiently large to smooth the current. The MMC schematic consists of three main parts. Firstly, the DC side is located on the left, which is modeled as a split DC voltage source. Secondly, the main MMC part is located in the middle. Thirdly, on the right, there are the AC side filter inductors L_a with their parasitic resistance R_a, which are connected to the AC grid.

As it is shown in [6], the system equations can be written in state space notation:

$$\dot{i}_{1-6} = \mathbf{A}\, i_{1-6} + \mathbf{B}\, v_{1-6} + \mathbf{F}\, z_{1-4} \tag{1}$$

Where $\mathbf{A}$ is the system matrix consisting of inductances and resistances. The input matrix $\mathbf{B}$ and the disturbance matrix $\mathbf{F}$ only contain inductive elements. The disturbance vector z_{1-4} consists of the DC voltage and the grid voltages.

The system is highly coupled and thus, no simple control scheme can be applied. Changing one voltage out of v_{1-6}, affects all currents in the system. Therefore, in [6] a 6×6 decoupling matrix $\mathbf{T}$ was derived. This matrix allows the decoupling of the currents i_{1-6} and the voltages v_{1-6}. Instead of the physical quantities, the system is described in transformed quantities marked with a tilde $\tilde{}$ after applying the decoupling matrix $\mathbf{T}$ to (1). The transformed system can be written as:

$$\dot{\tilde{i}}_{1-6} = \tilde{\mathbf{A}}\, \tilde{i}_{1-6} + \tilde{\mathbf{B}}\, \tilde{v}_{1-6} + \mathbf{T}\,\mathbf{F}\, z_{1-4} \tag{2}$$

After the decoupling, there are six transformed currents, of which five currents are relevant, because one current cannot flow, since the neutral point of the grid is not

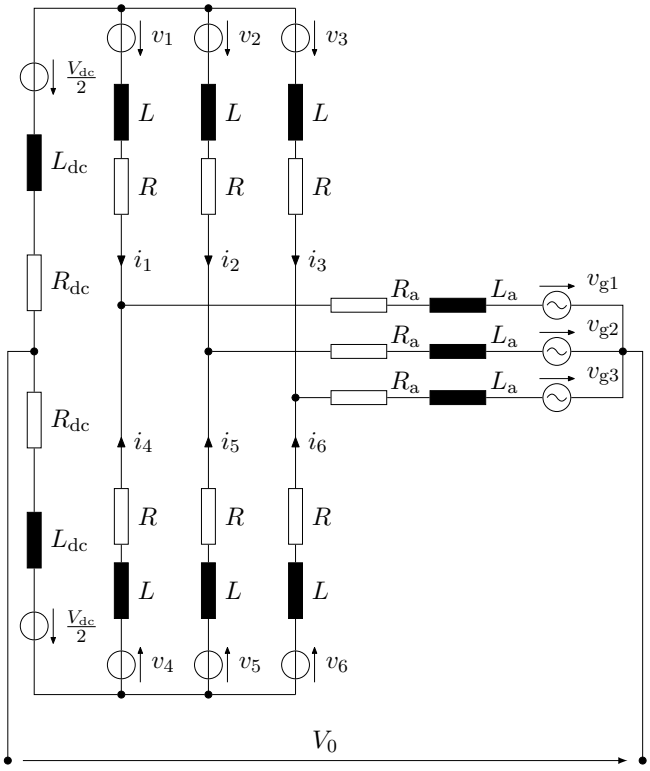

Fig. 2. Schematic of an MMC

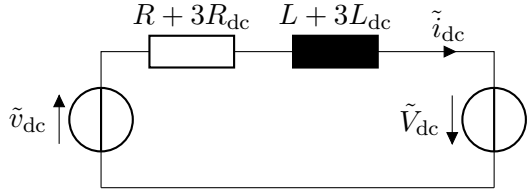

Fig. 3. Equivalent DC circuit

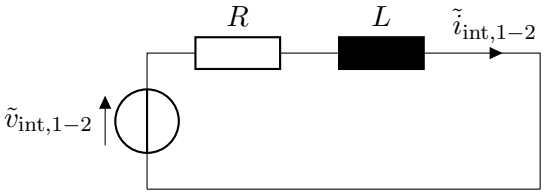

Fig. 4. Equivalent internal circuit

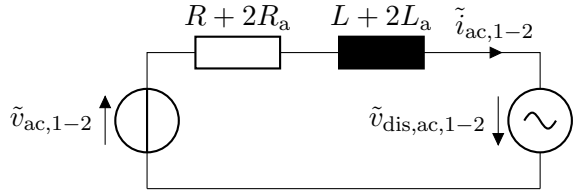

Fig. 5. Equivalent AC circuit

connected. All vectors and matrices are shown in the appendix. Two currents $\tilde{i}_{\mathrm{ac},1-2}$ describe the currents towards the AC grid, similar to i_α and i_β from the well known Clarke transformation. Two internal currents $\tilde{i}_{\mathrm{int},1-2}$ allow the energy transfer within the MMC itself, e.g., for arm energy balancing. And one current $\tilde{i}_{\mathrm{dc}}$ describes the current transfer with the DC side. In the generalised case, this current could also be AC when full-bridge cells are used [7].

The resulting decoupled subsystems are shown in Fig. 3 - Fig. 5. The transformed voltage sources of the MMC are located on the left. In Fig. 3 and Fig. 5, there are also voltage sources on the right, representing the transformed disturbance variables.

III. Control System Design

The decoupling of the subsystems enables the design of classic controllers, like proportional-integral (PI) controllers for the MMC, especially for the current controllers. The superimposed MMC control is implemented in the ARM processor to ensure symmetric energy distribution in the arms of the MMC required for the stable operation of the MMC. It is adapted from [8] and not focused in this contribution. For the AC side currents and voltages, the decoupled subsystem of Fig. 5 is sufficient as long as the high-level control and the cell capacitors provide enough voltage reserve. Thus, the MMC can then be analysed as any other two- or three-level converter from an AC control design perspective.

A. Control Implementation

MMCs need a powerful signal processing system, which is capable of processing a high amount of input signals from the cells, calculating the setpoints for the cell voltages and driving the semiconductors of the cells. In this work, the control of the MMC is implemented on a Xilinx Zynq 7030 SoC, which combines an FPGA with a dual core ARM processor on a single chip. The SoC is embedded in the in-house developed ETI-SoC-System, which is shown in Fig. 6 and was presented in [9]. The MMC arm PCBs are plugged directly into the ETI-SoC-System, as shown in Fig. 6.

The used Zynq 7030 SoC is well suited for a cascade control approach, where fast but simple control loops can be outsourced to the FPGA and more complex, but less time-sensitive tasks can be run on the ARM processor. By utilizing the C-Code generation feature of *Matlab Simulink*, the development process and the implementation time of the complex energy controller can be significantly reduced [9]. For the design of some complex FPGA algorithms, the *Vitis High-Level Synthesis (HLS)* tool from Xilinx has been used, where the algorithms can be developed using C++.

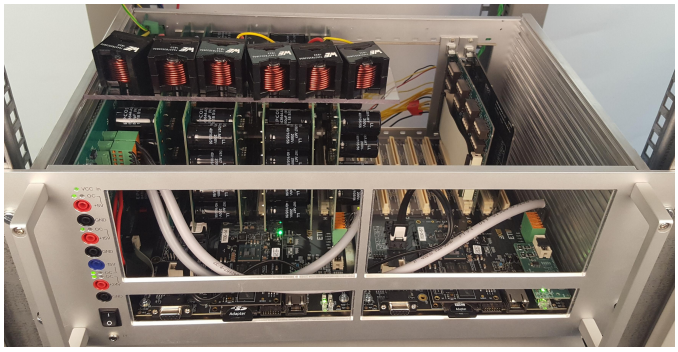

Fig. 6. MMC prototype in the 19-inch rack of the ETI-SoC-System

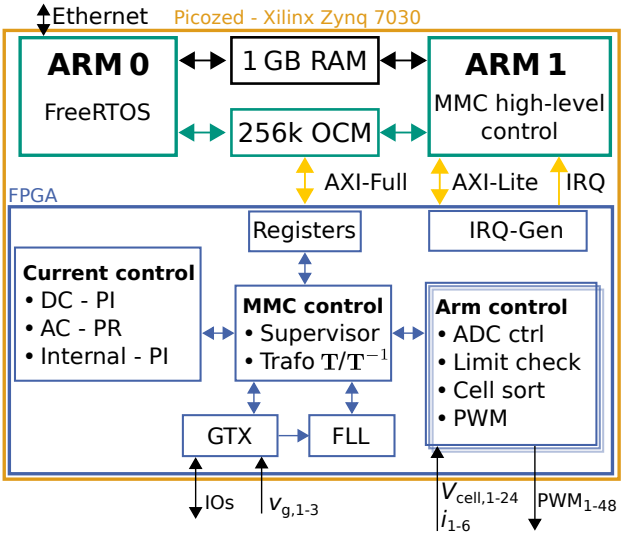

Fig. 7. Control system partitioning

The partitioning of the SoC is shown in Fig. 7. The green arrows indicate connections within the processing system of the SoC. Memory mapped interfaces between the processing system and the FPGA are marked with yellow arrows and blue arrows denote connections inside the FPGA, which use the AXI-Stream protocol [10]. Black arrows mark the connections to the rest of the prototype's hardware as well as to the computer used for monitoring and data logging.

ARM core 0 runs an operating system, which is used to set reference values and receives the system's setpoints via Ethernet. If valid, the reference values are written to the On-Chip Memory (OCM), which can be accessed from the other ARM core. ARM core 1 runs the high-level control, such as the main state machine of the MMC, as well as the energy controller and the voltage controller for the DC side. The energy balancing between

TABLE I
FPGA RESOURCE UTILIZATION

Resource	Utilization	Available	Utilization (%)
LUT	28929	78600	36.8
LUTRAM	1916	26600	7.2
FF	40722	157200	25.9
BRAM	15	265	5.7
DSP	86	400	21.5

the arms of the MMC is part of the outer control loop of the cascade control approach and runs at $10\,\mathrm{kHz}$. The inner control loop includes the current controllers and the feedforward voltage generation for the DC and the grid voltages. It is executed with an update rate of $100\,\mathrm{kHz}$ in the FPGA of the SoC. Thus, the control period is $T_\mathrm{c} = 10\,\mu\mathrm{s}$, which is also used as the PWM period.

All the MMC cells are connected to one SoC, but due to physical space constraints, a second SoC is used for the IO signals for the contactors and the measurement of the grid voltages. The two systems are coupled with a high speed serial connection (GTX) with a net data rate of $5\,\mathrm{Gbit/s}$. In a future design, a larger carrier board could implement the functionality of the second SoC, so only one SoC needs to be programmed. The main SoC has sufficient processing capacity and the resource utilization on the FPGA is low, as shown in Table I.

B. Current Controllers

1) Design: For the DC current, a PI controller is used, which is tuned using the magnitude optimum method [11, 12]. When employing classical control approaches such as PI control for the $50\,\mathrm{Hz}$ grid currents, they have to be used in a rotating reference frame (DQ) to ensure stationary accuracy and sufficient disturbance rejection capabilities. Alternatively, a proportional-resonant (PR) controller can be used in the stationary reference frame. The design of a PR controller seems more complicated than tuning a PI controller in the DQ system with well known methods, like the magnitude optimum method. Similar to [13, pp. 382–384], the equivalence of a PR controller in the stationary reference frame and a PI controller in the rotating reference frame is shown, so the same well established design methods can be applied.

The transfer functions of an ideal PI and an undamped PR controller are

$$G_{\mathrm{c,PI}}(s) = K_\mathrm{p} + \frac{K_\mathrm{i}}{s} \tag{3}$$

and

$$G_{\mathrm{c,PR}}(s) = K_\mathrm{p} + \frac{2K_\mathrm{i}s}{s^2+\omega_0^2}\,, \tag{4}$$

respectively. If (4) is restructured as

$$G_{\mathrm{c,PR}}(s) = K_\mathrm{p} + \frac{K_\mathrm{i}(s+\omega_0) + K_\mathrm{i}(s-\omega_0)}{(s-\omega_0)(s+\omega_0)} \tag{5}$$

$$= \underbrace{\frac{K_\mathrm{p}}{2} + \frac{K_\mathrm{i}}{(s-\omega_0)}}_{G_{\mathrm{c,PI,pos}}} + \underbrace{\frac{K_\mathrm{p}}{2} + \frac{K_\mathrm{i}}{(s+\omega_0)}}_{G_{\mathrm{c,PI,neg}}}\,, \tag{6}$$

it can be seen, that the PR controller is equal to the sum of two PI controllers in reference frames that rotate in opposite directions. One PI controller frame rotates in the positive direction, while the other one rotates in the negative direction. For asymmetrical grid faults, where the negative sequence has to be controlled as well, the PR controllers require less implementation effort compared to two rotating reference frames with PI controllers and their decoupling. To overcome the more difficult parameter tuning for the PR controller, the similarity shown in (4) and (6) is used and the magnitude optimum is applied to determine the parameters K_p and K_i.

To improve the numerical stability, the damped version of the PR controller

$$G_{\mathrm{c,PR,d}}(s) = K_\mathrm{p} + \frac{2K_\mathrm{i}\omega_\mathrm{c}s}{s^2+2\omega_\mathrm{c}s+\omega_0^2} \tag{7}$$

is implemented in the FPGA as recommended in [14]. The additional damping factor ω_c affects the gain of the controller, especially at the nominal frequency. However, ω_c can be tuned to match the gain of the undamped PR controller in the rest of the frequency band by choosing $\omega_\mathrm{c} = 1\,\mathrm{rad/s}$, as shown in Fig. 8. For a better disturbance rejection, a different value of $\omega_\mathrm{c} = 2\pi\,\mathrm{rad/s}$ is chosen, which is within the range of $5\,\mathrm{rad/s}$ to $15\,\mathrm{rad/s}$, recommended by [14].

The internal current controllers have to control the balancing currents. These contain AC and DC components but have no high demands regarding disturbance rejection or stationary accuracy. So PI controllers are used.

The dedicated current controllers for each relevant component of the current vector $\tilde{i}_{1-6}$ are shown in Fig. 9. The star * denotes reference values, which should be generated by the MMC. The high-level control generates the reference currents $\tilde{i}^*_{1-5}$. The measured currents i_{1-6} are transformed into the state space model with the transformation matrix $\mathbf{T}$. The outputs of all controllers are combined with the feedforward voltages $\tilde{v}^*_{10\,\mathrm{kHz}}$ from the high-level control (for pre charging purpose) and grid

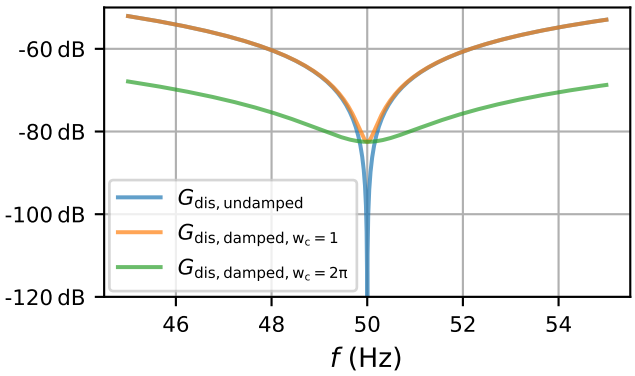

Fig. 8. Disturbance transfer function of PR controller

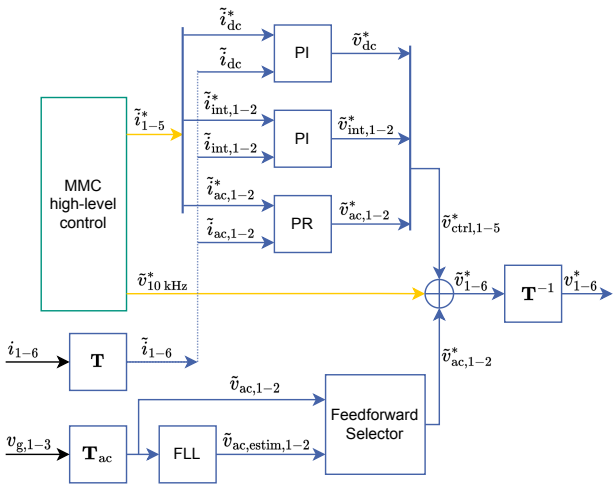

Fig. 9. Cascade control structure

TABLE II
PARAMETERS OF THE MMC

Parameter	Value	Parameter	Value
L	80 µH	P_{ac}	7 kW
L_{a}	20 µH	V_{cell}	160 V
L_{dc}	1 µH	V_{dc}	460 V
R	70 mΩ	$V_{\mathrm{g},1-3}$	230 V
R_{a}	20 mΩ	I_{dc}	15.2 A
R_{dc}	5 mΩ	I_{ac}	10.2 A

feedforward voltage $\tilde{v}^*_{\mathrm{ac},1-2}$. The voltage vector $\tilde{v}^*_{1-6}$ is then transformed back into the physical quantities and fed to the PW modulator.

2) Parameterization: For the calculation of the controllers' parameters, the values from Table II are used. The arm inductors L are selected to limit the current ripple for the internal currents. The inductors L_{a} and L_{dc} are selected for high dynamics. When the MMC should comply with grid standards, L_{a} has to be increased, a LCL-filter has to be used or an adjusted modulation scheme with an increased switching frequency should be carried out. Nevertheless, the low inductance of the prototype shows the capabilities of the control system, which can be useful in case of larger but saturating inductors.

In the prototype, a phase disposition PWM scheme is used. Two arms in one phase of the MMC use the same digital triangle carrier seen in Fig. 13. The maximum difference between the desired voltage and the actual full-bridge voltage occurs at a duty cycle of $d = 0.5$, because the unipolar modulation of the full-bridge cell allows three levels. Natural doubling of the PWM leads to an effective PWM period of $T_{\mathrm{nat}} = \frac{T_{\mathrm{c}}}{2} = 5\,\mu\mathrm{s}$. This PWM period in combination with the parameters of the MMC from Table II leads to a maximum current ripple of a single arm of

$$\Delta I = \Delta T \cdot V_{\mathrm{cell}} \cdot \frac{1}{L} \tag{8}$$

$$= d \cdot \frac{T_{\mathrm{c}}}{2} \cdot (0.5 \cdot 160\,\mathrm{V}) \cdot \frac{1}{80\,\mu\mathrm{H}} = 2.5\,\mathrm{A}\,. \tag{9}$$

This leads to a relative current ripple related to the nominal arm current in the nominal operating point at $\hat{I}_{\mathrm{ac}} = 14.35\,\mathrm{A}$ and $I_{\mathrm{dc}} = 15.22\,\mathrm{A}$ of

$$r = \frac{\Delta I}{I_{\mathrm{arm,nom}}} = \frac{\Delta I}{\frac{I_{\mathrm{dc}}}{3} + \frac{\hat{I}_{\mathrm{ac}}}{2}} = \frac{2.5\,\mathrm{A}}{12.2\,\mathrm{A}} = 20.4\,\%\,. \tag{10}$$

C. Arm Control

The reference voltages from Fig. 9 have to be translated into gate signals for the semiconductors. As each element in the reference voltage vector v^*_{1-6} represents one arm voltage of the MMC, each arm can be processed in a separate block. This block is designed as an intellectual property core (IP core) in the FPGA development environment *Xilinx Vivado*. The IP core is called *Arm control* and is instantiated six times as it is indicated in Fig. 7. A sorting network in each core processes the actual cell voltages and chooses which cells contribute to the arm voltage in the next modulation period. The cell sorting is based on the deviation of the actual cell voltages and the desired cell voltage of the individual cell which can differ in case of connected battery modules. Each IP core also includes four full-bridge PW modulators, which run at 250 MHz and use a double data rate (DDR) register to allow a duty cycle time resolution of 2 ns, which is equivalent to 64 mV.

The *Arm control* IP core also includes an ADC interface for a 16 bit / 5 MSps SAR ADC. The ADC samples a $\pm 50\,\mathrm{A}$ AMR current sensor, which has a $3\,\mathrm{dB}$ bandwidth of $1.5\,\mathrm{MHz}$.

Fault handling capabilities:
The datasheet of the EPC2215 eGaN FET specifies a maximum pulse current of $162\,\mathrm{A}$ for $300\,\mu\mathrm{s}$ at $25\,^{\circ}\mathrm{C}$. The current sensor includes an internal overcurrent detection triggering at $60\,\mathrm{A}$ and disabling the gate driver enable signals of the respective arm within $200\,\mathrm{ns}$, in case the FPGA fails. During normal operation, overcurrent conditions are detected in the FPGA.

In case of grid faults, like voltage drops, it is necessary to stay connected to the grid for up to $3\,\mathrm{s}$ at $85\,\%$ of the nominal grid voltage according to the grid codes [15]. In case of a voltage drop below $15\,\%$ of the nominal voltage, the converters are allowed to disconnect from the grid. Otherwise, the converters have to stay connected for $150\,\mathrm{ms}$ if the grid voltage stays at $15\,\%$ [15]. However, the voltage drop equals a huge disturbance from a control perspective. If the disturbance transfer function of the controller does not provide infinite damping, as it is the case with the damped PR controller shown in Fig. 8, the grid current will also deviate from the reference values.

In order to allow transient currents which occur immediately after the grid fault, a dynamic approach for the current limit detection is chosen. The components are designed to carry a continuous arm current $I_{\mathrm{rms,cont}} = 11\,\mathrm{A_{rms}}$ due to the passively cooled arm PCB shown in Fig. 1 and [4]. In the FPGA, a maximum arm current of $30\,\mathrm{A}$ is allowed for $2\,\mu\mathrm{s}$, which equals to 10 ADC samples and avoids noise triggering an overcurrent fault. Based on the thermal capacity of the used EPC2215 GaN semiconductors [16], another limit, given as the extra loss energy $E_{\mathrm{extra,max}}$ is checked. This extra energy can be tolerated in the nominal operating point and increases the die temperature by $17\,\mathrm{K}$. Assuming the die material is mainly composed of silicon, this energy calculates to:

$$E_{\mathrm{extra,max}} = m_{\mathrm{die}} \cdot c_{\mathrm{silicon}} \cdot \Delta T \tag{11}$$

$$= 0.0089\,\mathrm{g} \cdot 0.7\,\frac{\mathrm{J}}{\mathrm{g}\cdot\mathrm{K}} \cdot 17\,\mathrm{K} = 0.106\,\mathrm{J} \tag{12}$$

This assumption is safe, since it underestimates the extra energy. GaN has much higher density of $6.15\,\mathrm{g\,cm^{-3}}$ compared to silicon with $2.33\,\mathrm{g\,cm^{-3}}$, whereas the specific heat of GaN with $0.49\,\mathrm{J\,kg^{-1}\,K^{-1}}$ is not that much smaller than silicon with $0.7\,\mathrm{J\,kg^{-1}\,K^{-1}}$.

The FPGA estimates the dissipated power in the semiconductors using the arm currents in every control step k. In the nominal operating point, a die resistance of $R_{\mathrm{DS(on)}} = 10\,\mathrm{m\Omega}$ is assumed. If the power exceeds the nominal power loss, the extra amount

$$P_{\mathrm{extra}}[k] = R_{\mathrm{DS(on)}} \cdot (i[k]^2 - I^2_{\mathrm{rms,cont}}) \tag{13}$$

accumulates according to the following equation:

$$E_{\mathrm{extra}}[k] = \max\{(E_{\mathrm{extra}}[k-1] + P_{\mathrm{extra}}[k] \cdot T_{\mathrm{c}}), 0\} \tag{14}$$

If $E_{\mathrm{extra}}[k]$ rises above $E_{\mathrm{extra,max}}$, a current fault condition is triggered.

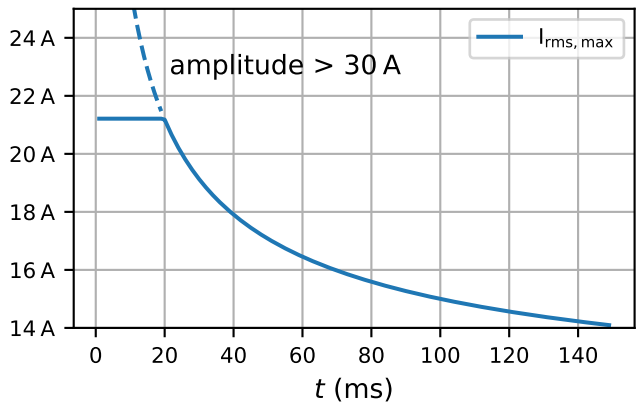

Fig. 10. Dynamic current limit for each arm

The resulting time current limitation is shown in Fig. 10. If no other current, like circulating or DC side current flows in the MMC, both arms of each phase can provide nearly $36\,\mathrm{A_{rms}}$ for two $50\,\mathrm{Hz}$ grid periods. With a more detailed thermal model, this value could be further increased, but the used technique provides a fast solution to provide overcurrents, despite the passively cooled and very small GaN chips, measuring only $4.6\,\mathrm{mm}$ x $1.6\,\mathrm{mm}$ x $0.518\,\mathrm{mm}$.

D. Grid Voltage Detection

To provide stable grid phase and frequency detection in grid following and also grid forming control, a tracking mechanism is needed. A Second-Order Generalized-Integrator Frequency-Locked-Loop (SOGI-FLL) is used to detect grid voltage, grid frequency and phase angle [17]. The SOGI-FLL provides stable tracking and fast response in case of symmetrical, asymmetrical and distorted grid faults. However, there is always a trade-off between stable phase information, and the response time of the grid voltage detection.

In case of a hard single phase voltage drop to $20\,\%$ of the nominal value, the response of the SOGI-FLL grid voltage estimation nearly matches the grid after $10\,\mathrm{ms}$, as shown in Fig. 11.

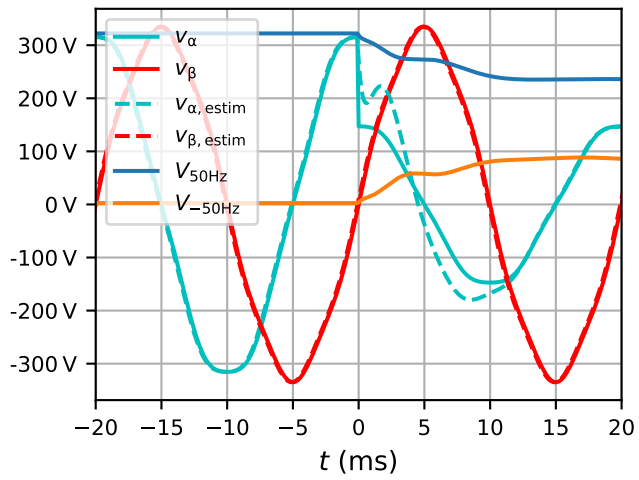

Fig. 11. Response of the SOGI-FLL to a single phase voltage drop

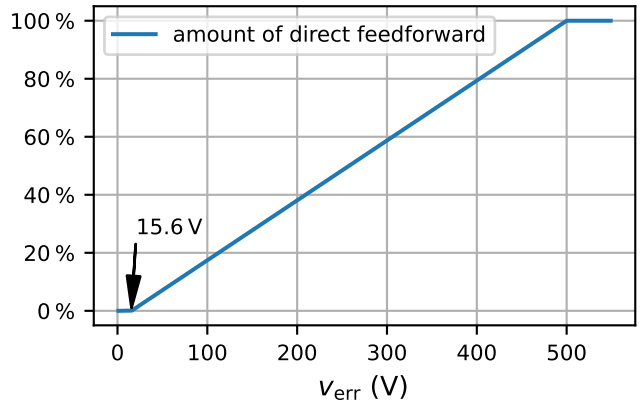

Fig. 12. Transition function of the feedforward selector

During this adjustment period, there would be a large feedforward voltage error. To minimize the disturbance for the PR controller, a linear transition function to a direct feedforward is implemented. The transition function blends the output of the SOGI-FLL with the measured grid voltage, depending on the deviation between both. The transition is shown in Fig. 12. At an error of 500 V the slope reaches its maximum and only the actual grid voltage is used as the feedforward signal. This may destabilize the system in case of weak grids, because the direct feedback resulting from the voltage drop at the grid impedance closes a weakly damped control loop. In the future, the problem will be solved by increasing the systems output filter, which is also necessary to lower the switching current ripple at the output and comply with the grid codes.

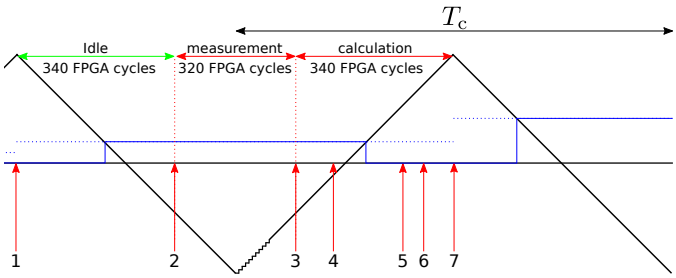

Fig. 13. FPGA control execution process

E. Controller Timing

To achieve a dynamic system response, the control system is designed with minimum latency. The FPGA control execution process is timed with the triangular PWM counter shown in Fig. 13. The deadtime for the controller design can be reduced to one 100 kHz PWM period. Besides the PWM triangle counter which runs at 250 MHz, the control logic in the FPGA uses a 100 MHz clock resource to simplify timing constraints.

The *MMC control* block in Fig. 7 controls all FPGA operations and is triggered when the PWM counter reaches its maximum value.

The modulation period can be divided into seven events:

1) The *tready* AXI signal of the PW modulator starts the process counter, which waits for 340 clock cycles.
2) 16 samples of the current measurement are acquired from each *Arm control* core.
3) The mean values of the current samples from each arm are calculated. Multiplication of these values with the transformation matrix **T** is started. Once that is finished, the current controllers are executed.
4) The SOGI-FLL is triggered and takes 200 clock cycles.
5) All voltages $\tilde{v}^*_{1-6}$ are calculated and the inverse transformation $\mathbf{T}^{-1}$ is executed to get the set point values of the arm voltages v^*_{1-6}.
6) The arm symmetry controller is started. The sorting network determines the cells to be used for the arm voltage generation. It takes 41 cycles to finish, including the duty cycle calculation.
7) The PWM duty cycles are loaded into the modulator and the process counter is restarted.

IV. Experimental Results

A. Prototype Setup

To validate the control design, measurements with the MMC prototype [4] in Fig. 6 and a 30 kVA PHIL

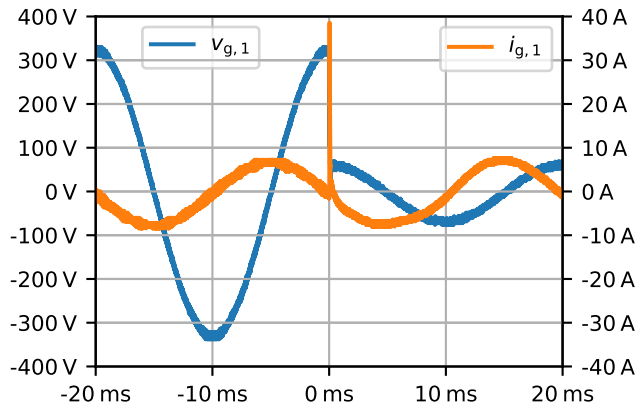

Fig. 14. Symmetric grid fault

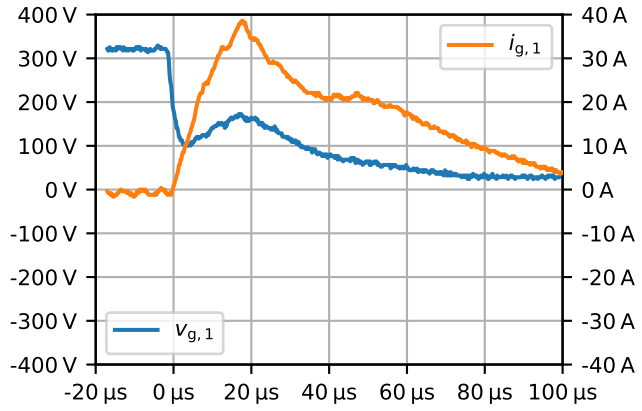

Fig. 15. Zoomed view of symmetric grid fault

grid emulator from Spitzenberger & Spies are carried out. The emulator is programmed to emulate a 400 V, 50 Hz three-phase grid with an impedance of 100 mΩ and 100 µH.

The grid currents are measured with the TCP312 100 MHz current probe from Tektronix, which supports a continuous current of 30 A and a peak current of 50 A for 10 µs.

B. Prototype Measurements

The MMC is running in Static Synchronous Compensator (STATCOM) mode with a reactive current of 5 A. In Fig. 14, a symmetric grid fault is shown, where the voltage drops to 20 % in the middle of the graph. The fault occurs exactly at the maximum of $v_{g,1}$. Thus, phase one shows the most interesting transients. The MMC is programmed to restore the setpoint of 5 A immediately, but it would be also possible to set the current to zero as it is required in the grid code [15].

In Fig. 15, it can be seen that the phase current rises up to nearly 40 A within two control periods due to the low impedance between the grid emulator and the voltage sources of the MMC. However, the disturbance rejection of the PR controllers, the grid-voltage feedforward selector and the dynamic current limit avoid tripping of an inverter fault and keep the inverter within its safe operating area.

While this response may be appropriate from a control design perspective, it may not necessarily be desired from the perspective of a grid system operator. The fast response allows the MMC to stay connected to the grid in case of grid fault and thereby provides the basis to meet the grid code [15]. However, according to [18], grid converters should provide an instantaneous response during abnormal grid conditions. Thus, a behaviour similar to a synchronous machine is desired, where the converter keeps delivering high currents in a fault condition to trip fuse elements within the grid. These features can be implemented in the future, while this work demonstrates the dynamics of the PR controller and the adapted feedforward control.

V. Conclusion

This paper demonstrates that a mathematical decoupling of the physical values of the MMC simplifies the control design. The current controllers for the AC side and the DC side can be designed independently. It was shown, that PR controllers can be used for the grid current control, as they are mathematically equivalent to two PI controllers in rotating reference frames. This reduces the implementation effort.

The paper also showed the partitioning of the control implementation on a SoC, where the highly dynamic parts are implemented on an FPGA and the slower, but more complex parts of an MMC control are implementend on the ARM processor.

Finally, an MMC prototype was used to verify the dynamic response of the implemented control with a hard grid fault in the microsecond range, emulated by a PHIL grid emulator.

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APPENDIX

A. Transformation Matrices

$$\mathbf{T} = \begin{bmatrix} \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} \\ -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & -\frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} \\ \frac{1}{2} & -\frac{1}{2} & 0 & -\frac{1}{2} & \frac{1}{2} & 0 \\ \frac{1}{2\sqrt{3}} & \frac{1}{2\sqrt{3}} & -\frac{1}{\sqrt{3}} & -\frac{1}{2\sqrt{3}} & -\frac{1}{2\sqrt{3}} & \frac{1}{\sqrt{3}} \\ -\frac{1}{2} & \frac{1}{2} & 0 & -\frac{1}{2} & \frac{1}{2} & 0 \\ -\frac{1}{2\sqrt{3}} & -\frac{1}{2\sqrt{3}} & \frac{1}{\sqrt{3}} & -\frac{1}{2\sqrt{3}} & -\frac{1}{2\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix}$$

$$\mathbf{T}_{\mathrm{ac}} = \begin{bmatrix} -1 & 1 & 0 \\ -\frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix}$$

B. Transformed System Matrices

$$\tilde{\mathbf{A}} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{R+3R_{\mathrm{dc}}}{L+3L_{\mathrm{dc}}} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{R}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{R}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{R+2R_{\mathrm{a}}}{L+2L_{\mathrm{a}}} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{R+2R_{\mathrm{a}}}{L+2L_{\mathrm{a}}} \end{bmatrix}$$

$$\tilde{\mathbf{B}} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L+3L_{\mathrm{dc}}} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L} & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{L} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{L+2L_{\mathrm{a}}} & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{L+2L_{\mathrm{a}}} \end{bmatrix}$$

$$\tilde{\mathbf{F}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{\sqrt{6}}{2L+6L_{\mathrm{dc}}} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{L+2L_{\mathrm{a}}} & -\frac{1}{L+2L_{\mathrm{a}}} & 0 & 0 \\ \frac{\sqrt{3}}{3L+6L_{\mathrm{a}}} & \frac{\sqrt{3}}{3L+6L_{\mathrm{a}}} & -\frac{2\sqrt{3}}{3L+6L_{\mathrm{a}}} & 0 \end{bmatrix}$$

$$\tilde{\mathbf{C}} = \begin{bmatrix} 2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 2 \end{bmatrix}$$

C. Transformed Voltages and Currents

$$\tilde{v}_{1-6} = \begin{bmatrix} \tilde{v}_0 \\ \tilde{V}_{\mathrm{dc}} \\ \tilde{v}_{\mathrm{int},1} \\ \tilde{v}_{\mathrm{int},2} \\ \tilde{v}_{\mathrm{ac},1} \\ \tilde{v}_{\mathrm{ac},2} \end{bmatrix}$$

$$\tilde{i}_{1-6} = \begin{bmatrix} \tilde{i}_0 \\ \tilde{i}_{\mathrm{dc}} \\ \tilde{i}_{\mathrm{int},1} \\ \tilde{i}_{\mathrm{int},2} \\ \tilde{i}_{\mathrm{ac},1} \\ \tilde{i}_{\mathrm{ac},2} \end{bmatrix}$$