Continuous Sinusoidal Output Voltage Generation with a Single Phase Cascaded H-Bridge Converter

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***Index Terms*—Cascaded H-Bridge, Modular Multilevel Converters (MMC), Dual Active Bridge (DAB), Voltage Control, Envelope Amplifier.**

***Abstract*—This paper introduces an algorithm to calculate the trajectories of both, the output voltages of a Cascaded H-Bridge converter and the controlled voltage of the supplying Dual Active Bridge to provide a perfectly smooth output voltage with only very small filter components. In this contribution the principle is demonstrated by the generation of a sinusoidal output voltage. After presenting the necessary topology of the converter the mathematical description for the equations for the continuous output operation mode are explained. Measurements at a $8\,\mathrm{kW}$ prototype verify the working principle.**

I. Introduction

Multilevel converters are used in a variety of applications, such as active filters, feed-in converters for renewable energy, converters on ships and for high voltage direct current (DC) transmission [1]–[4]. All these applications benefit from the advantages of multilevel converters, such as lower electromagnetic interference (EMI) and total harmonic distortion (THD) of the output voltage and thus of the output current. In addition, there are lower blocking voltage requirements for the semiconductors used, while higher output voltages are achieved [5]. Another typical application for multilevel converters is as a voltage source for test benches, e.g. for testing other converters or electrical machines [6], [7]. This is made possible by the fact that the multilevel converter achieves a low distortion factor and thus a precise replication of a desired voltage curve in combination with a very high bandwidth. Due to the low THD [5], only a small output filter is required, thus achieving a low internal impedance of the voltage source, which is also critical for test benches to reduce the influence of the converter under test on the output voltage. To optimize the multilevel converter for use as a test converter, where high bandwidth and low THD are required, the switching frequency or number of output levels is typically increased. This results in higher material costs, more complex control algorithms, and a larger system footprint. The method and mathematical description presented in this paper offers a new approach that allows to reduce the THD values without additional hardware effort to provide a continuous, generic output waveform for a single phase Cascaded H-Bridge (CHB) converter. For this purpose, the inherent degrees of freedom of the converter, provided by a Dual Active Bridge (DAB) [8] to dynamically control the voltage of each power module, are used to provide the expected output voltage with low switching effort on the CHB cell. Both the output stage of the CHB cell and the capacitor voltage of each individual power module are controlled to precisely achieve the required output voltage. The result is a dynamically controllable, bidirectional and bipolar voltage source with low THD. Various other methods to reduce the THD have been proposed in the literature, such as modified switching patterns of a space vector modulation (SVM). [9] and selective harmonic elimination [10]. However, none of these systems take advantage of the inherent flexibility provided by the adjustable voltage of the power module.

According to [11] and [12], the topology in combination with the control method proposed in this paper can be seen as a hybrid power amplifier operating in envelope configuration. In contrast to a hybrid power amplifier

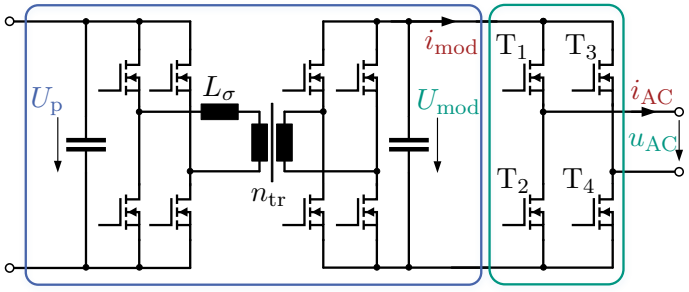

Fig. 1: Power module with DAB stage for power supply (blue) and CHB cell output stage (green)

with a discrete and inefficient linear power stage, such as that shown in [13], no additional hardware is required.

II. Topology

The topology used is a CHB cell structure with each cell individually supplied by a galvanically isolated DAB. The overall topology is explained in more detail in [14]. A single power module consisting of a CHB cell and the DAB stage is shown in fig. 1. The DAB, highlighted in blue, provides unrestricted bidirectional power flow. In addition, DABs also operate in highly efficient buck or boost mode to achieve a wide operating range of output voltage [15], [16]. The CHB cell, highlighted in green, provides the alternating current (AC) output of each individual power module. These AC outputs of the power modules are connected in series to provide the AC output of the entire converter, while all DAB stages of each power module are connected in parallel to a DC power supply. The overall topology of the prototype is shown in fig. 2. The prototype is configured with four power modules. The DAB stages are connected in parallel and are supplied by a bidirectional voltage source with an output voltage U_{p}. The output U_{out} of the converter is provided by a series connection of the CHB cells.

The CHB cell of each power module, consisting of four MOSFETs T_1 to T_4, provides three discrete voltage levels ($+U_{\mathrm{mod}}$, $-U_{\mathrm{mod}}$ or $0\,\mathrm{V}$) depending on the switching state of the MOSFETs, as shown in Table I. The topology of a single power module is shown in fig. 1.

III. Analysis

An example of a sinusoidal output voltage is used in this section to introduce the analysis and formal description of the method. For simplicity, only the rising edge of the positive half-wave is used. For symmetry reasons, a complete sinusoidal signal can be derived

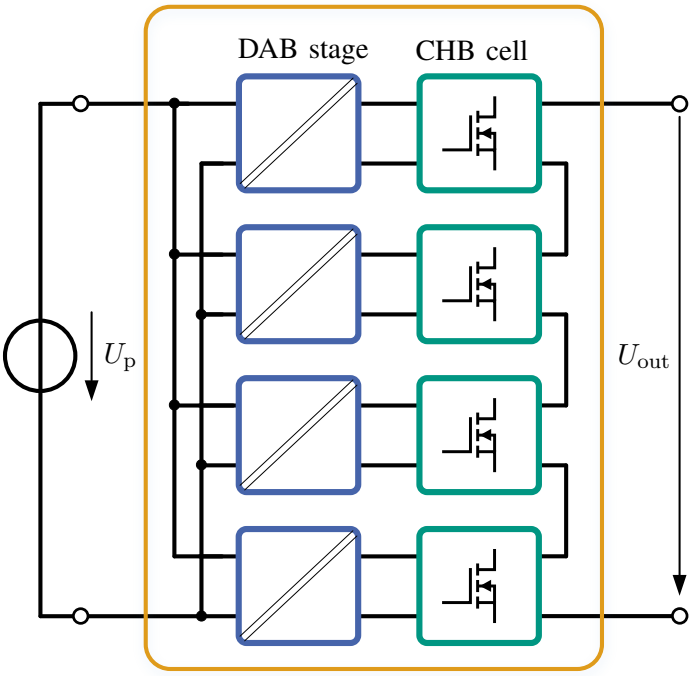

Fig. 2: Test setup with four power modules connected in input serial output parallel connection

TABLE I
Switching states of the CHB cell

State	Conducting	Blocking	Output voltage u_{AC}	Module current i_{mod}
Positive	$\mathrm{T}_1, \mathrm{T}_4$	$\mathrm{T}_2, \mathrm{T}_3$	U_{mod}	i_{AC}
Negative	$\mathrm{T}_2, \mathrm{T}_3$	$\mathrm{T}_1, \mathrm{T}_4$	$-U_{\mathrm{mod}}$	$-i_{\mathrm{AC}}$
Bypass 1	$\mathrm{T}_1, \mathrm{T}_3$	$\mathrm{T}_2, \mathrm{T}_4$	$0\,\mathrm{V}$	$0\,\mathrm{A}$
Bypass 2	$\mathrm{T}_2, \mathrm{T}_4$	$\mathrm{T}_1, \mathrm{T}_3$	$0\,\mathrm{V}$	$0\,\mathrm{A}$

in a similar way. Furthermore, the method is valid for any arbitrary signal that is continuous and limited to a maximum dynamic defined by the maximum dynamic of the DAB.

A. Introduction of variables

One DAB is controlling the module voltage $U_{\mathrm{mod},n}$ of one power module n within the minimum and maximum module voltages $U_{\mathrm{mod,min}}$ and $U_{\mathrm{mod,max}}$, respectively. The resulting, possible voltage variation U_Δ is calculated according to (1).

$$U_\Delta = U_{\mathrm{mod,max}} - U_{\mathrm{mod,min}} \tag{1}$$

The variables $\mu_{1,n}$ and $\mu_{2,n}$ defined in (2) and (3), are introduced to indicate the current switching direction and the module voltage $U_{\mathrm{mod},n}$ of power module n,

respectively. Consequently, $\mu_{1,n}$ is a finite set with three elements, since the output voltage can only be positive (+1), negative (-1) or zero (0), if the CHB cell is in one of the two bypass states. The variable $\mu_{2,n}$ is a rational number between 0 and 1 as defined in (3). Where $\mu_{2,n} = 0$ means the voltage of module n is equal to the minimum $U_{\mathrm{mod},n} = U_{\mathrm{mod,min}}$ and $\mu_{2,n} = 1$ means it is equal to the maximum module voltage $U_{\mathrm{mod},n} = U_{\mathrm{mod,max}}$. In (4) the equation describing the resulting module voltage $U_{\mathrm{mod},n}$ is given.

$$\mu_{1,n} := \{-1, 0, 1\} \tag{2}$$

$$\mu_{2,n} := [0, 1] = \{k | k \in \mathbb{Q}, 0 \leq k \leq 1\} \tag{3}$$

$$U_{\mathrm{mod},n} = (U_{\mathrm{mod,min}} + \mu_{2,n} \cdot U_{\Delta}) \tag{4}$$

The combination of (2) and (4) gives (5), which describes the output voltage at the CHB cell terminals. To calculate the resulting generated output voltage of the phase U_{out} with m power modules, (5) is extended to (6).

$$u_{\mathrm{AC,n}} = \mu_{1,n} \cdot U_{\mathrm{mod},n} = \mu_{1,n} \cdot (U_{\mathrm{mod,min}} + \mu_{2,n} \cdot U_{\Delta}) \tag{5}$$

$$U_{\mathrm{out}} = \sum_{n=1}^{m} u_{\mathrm{AC,n}} \tag{6}$$

$$= \sum_{n=1}^{m} (\mu_{1,n} \cdot (U_{\mathrm{mod,min}} + \mu_{2,n} \cdot U_{\Delta})) \tag{7}$$

Therefore, the equation to calculate the maximum output voltage of a phase can be written as shown in (8):

$$U_{\mathrm{out,max}} = m \cdot U_{\mathrm{mod,max}} \tag{8}$$

B. Assumptions

For the mathematical description two assumptions are made to reduce the complexity of the explanation. If the system does not satisfy both assumptions, the general methodology still works, but modifications of the equations are required.

(a) Assumption one (A_1):
The voltage ratio of the maximum module voltage and the minimum module voltage is defined as $\frac{U_{\mathrm{mod,max}}}{U_{\mathrm{mod,min}}} = \frac{p+1}{p},\ p \in \mathbb{N}$.

(b) Assumption two (A_2):
The amount of power modules m is an even number.

C. Generating a sinusoidal output voltage

Instead of using hardware such as capacitors and inductances to filter the high frequency output of the multilevel converter to create the sinusoidal voltage, the inherent degrees of freedom of the DAB output voltage in combination with the switching states of the CHB cells are used to provide the expected output voltage. The main principle of sinusoidal output voltage generation is as follows. A summary of the methodology is shown in the flowchart in fig. 3. The focus of the algorithm is set on low necessary dynamics of a single DAB. This means that the $\frac{\mathrm{d}U}{\mathrm{d}t}$ of the capacitor voltage of a power module is as small as possible.

1) Increasing output voltage: In normal operation mode, the output voltage is increased as expected by the output voltage setpoint U^*_{out}. The following steps are used to create a continuous output voltage. Without loss of generality, we start with $U^*_{\mathrm{out}} = 0\,\mathrm{V}$.

(a) All module voltages are set to the mean voltage of U_{max} and U_{min}, i.e. $\mu_{2,n} = 0.5$.

(b) Since A_1 holds, there is an even number of power modules. The lower half of the power modules is set to the positive state, i.e. $\mu_{1,l} = 1, l = \{1, 2, ..., \frac{m}{2}\}$, and the upper half of the power modules is set to the negative state, i.e. $\mu_{1,u} = -1, u = \{\frac{m}{2} + 1, ..., m\}$.

(c) While U^*_{out} is rising, the module voltages of power modules in positive state $\mu_{1,n} = 1$ are increased and the module voltages of modules in negative state $\mu_{1,n} = -1$ are decreased as long as it is possible, i.e. $0 \leq \mu_{2,n} \leq 1$. The setpoint voltage change for each power module is calculated by dividing the output voltage setpoint change $U^*_{\Delta,\mathrm{out}} = U^*_{\mathrm{out}} - U^*_{\mathrm{out,old}}$ by the number of power modules that can change their voltages n_{var}, see (10) and (11).

(d) The voltage of bypassed power modules is not changed.

Without changing $\mu_{1,n}$, the possible increase of the output voltage in the current state $U_{\Delta,\mathrm{inc}}$ can be calculated with (9). The number of power modules that can be used to vary the output voltage n_{var} can be calculated using (10).

$$U_{\Delta,\mathrm{inc}} = \sum_{n=1}^{m} \left(\mu_{1,n} \cdot \frac{\mu_{1,n} + 1}{2} - \mu_{1,n} \cdot \mu_{2,n} \right) \cdot U_{\Delta} \tag{9}$$

$$n_{\mathrm{var}} = \sum_{n=1}^{m} \left(|\mu_{1,n}| \cdot \left\lceil \frac{\mu_{1,n} + 1}{2} - \mu_{1,n} \cdot \mu_{2,n} \right\rceil \right) \tag{10}$$

Using (10) and the actual change in output voltage $U^*_{\Delta,\mathrm{out}}$, the new but mathematically temporary setpoint for each power module can be calculated with (11).

$$\mu_{2,n,\mathrm{temp}} = \mu_{2,n} + \mu_{1,n} \cdot \frac{U^*_{\Delta,\mathrm{out}}}{n_{\mathrm{var}} \cdot U_\Delta} \tag{11}$$

For computational reasons, the actual setpoint must be limited to the system-specific maximum and minimum module voltages according to (12).

$$\mu_{2,n} = \begin{cases} 1 & ,\text{if } \mu_{2,n,\mathrm{temp}} > 1 \\ 0 & ,\text{if } \mu_{2,n,\mathrm{temp}} < 0 \\ \mu_{2,n,\mathrm{temp}} & ,\text{otherwise} \end{cases} \tag{12}$$

2) Transition events: Some setpoints of the output voltage U^*_{out} cannot be reached by increasing the output voltage U_{out} because all power modules are either at their maximum or minimum. In this case (9) leads to a result of $0\,\mathrm{V}$. Therefore, transition events of the CHB cells are necessary to provide further margin of the output voltage while the output voltage is continuous. This case is achieved with the 'no' path of the yellow decision tree in fig. 3. The process to evaluate the new switching states $\mu_{1,n}$ is as follows.

(a) To achieve U^*_{out}, as many power modules with $U_{\mathrm{mod}} = U_{\mathrm{mod,min}}$ as possible are switched in positive direction and as many power modules with $U_{\mathrm{mod}} = U_{\mathrm{mod,max}}$ as possible are switched in negative direction. If U^*_{out} cannot be reached with this method, power modules with $U_{\mathrm{mod}} = U_{\mathrm{mod,max}}$ are switched to bypass or positive state (set $\mu_{1,n} = 0$ or $\mu_{1,n} = 1$) to reach U^*_{out} or modules with $U_{\mathrm{mod}} = U_{\mathrm{mod,min}}$ are switched to bypass state (set $\mu_{1,n} = 0$).

(b) To reduce the necessary dynamics of the module voltages, power modules that are not used due to (a) can be switched to one of the active states with the following restriction: An even number of unused power modules with equal voltage levels $\mu_{2,i} = \mu_{2,j}$ can be switched to an active state with alternating signs ($\mu_{1,i} = 1$, $\mu_{1,j} = -1$). As a result, the total output voltage does not change, but more modules are in an active state to provide dynamics.

(c) All other power modules are switched to bypass state $\mu_{1,n} = 0$.

After the transition event, the algorithm described in section III-C1 is applied. However, since some power modules are switched in the positive direction and others in the negative direction at the same time, the total losses increase. By choosing a transition strategy that reduces both the number of anti-serial modules and the losses, the required module dynamics are increased.

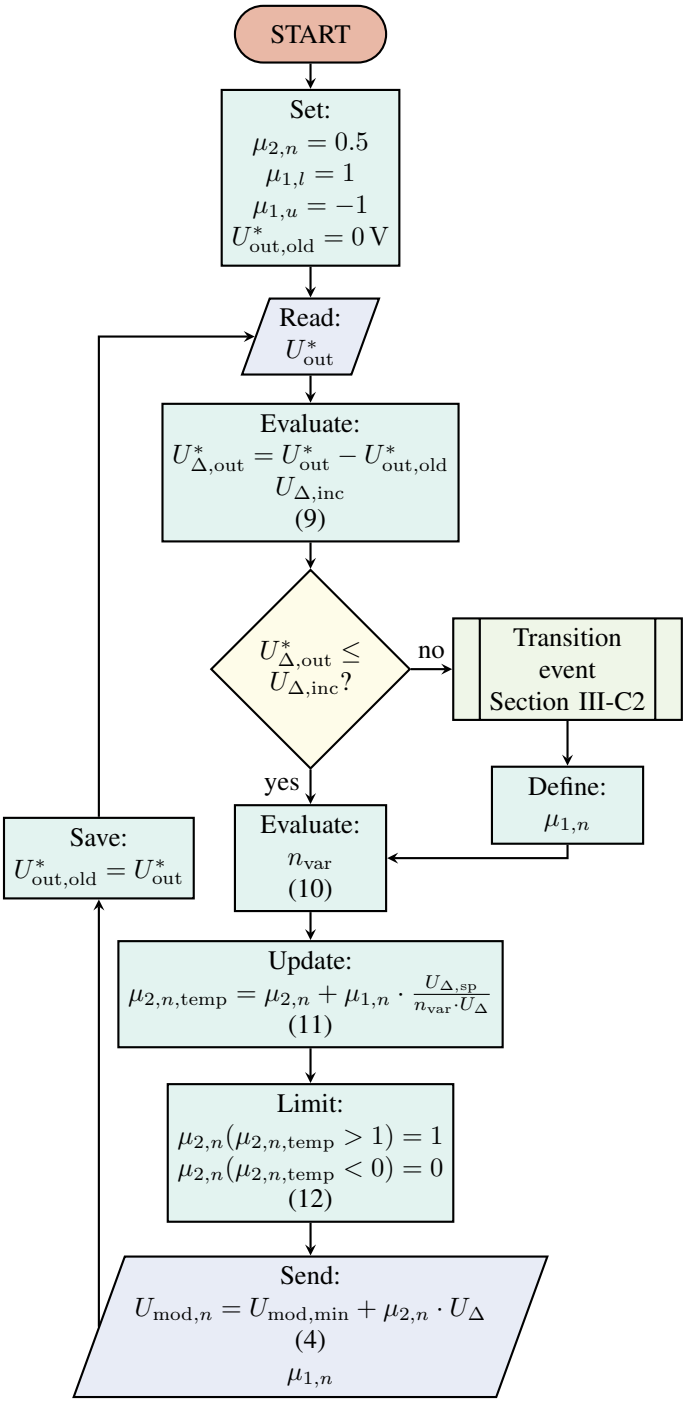

Fig. 3: Flowchart of the continuous voltage adaption trajectory

D. Necessary minimum amount of power modules

To achieve a smooth and continuous sinusoidal output voltage, it is necessary to have enough power modules m and a sufficient voltage variation range U_Δ of each module. In the following, a minimum number of necessary power modules is derived depending on the system parameters. While the setpoint of the output voltage U^*_{out} increases, starting from $0\,\mathrm{V}$, the power modules increase their module voltages in positive direction ($\mu_{1,n} = 1$), i.e. $\mu_{2,n}$ increases. At the same time, the power modules in negative direction ($\mu_{1,n} = -1$) decrease their module voltages, i.e. $\mu_{2,n}$ decreases. This rule holds until all modules have reached either their maximum ($U_{\mathrm{mod,max}}$) or their minimum ($U_{\mathrm{mod,min}}$) voltage. Then, a CHB cell transition is required because there is no possibility to increase the output voltage further. The maximum generated output voltage U_{out} at this transition can be calculated as shown in (13).

$$U_{\mathrm{out}} = \frac{m}{2} \cdot U_{\mathrm{mod,max}} - \frac{m}{2} \cdot U_{\mathrm{mod,min}} = \frac{m}{2} \cdot U_\Delta \quad (13)$$

After the transition at least one power module with $U_{\mathrm{mod}} = U_{\mathrm{mod,min}}$ must be switched to positive direction or at least one power module with $U_{\mathrm{mod}} = U_{\mathrm{mod,max}}$ must be switched to negative direction. This allows to further increase the output voltage. To get a continuous, stepless output voltage, the minimum output voltage that must be reached with the initial switching states is $U_{\mathrm{out}} = U_{\mathrm{mod,min}}$. Accordingly, the required minimum number of power modules m_{min} can be derived as shown in (14) using (13) and the assumption A_2.

$$\begin{aligned}
U_{\mathrm{out}} &\geq U_{\mathrm{mod,min}} \\
\frac{m_{\mathrm{ph,min}}}{2} \cdot U_\Delta &\geq U_{\mathrm{mod,min}} \\
m_{\mathrm{min}} &\geq \frac{2 \cdot U_{\mathrm{mod,min}}}{U_\Delta} \\
m_{\mathrm{min}} &\geq \frac{2 \cdot U_{\mathrm{mod,min}}}{U_{\mathrm{mod,max}} - U_{\mathrm{mod,min}}} \\
m_{\mathrm{min}} &\geq \frac{2}{\frac{U_{\mathrm{mod,max}}}{U_{\mathrm{mod,min}}} - 1} \\
m_{\mathrm{min}} &\geq \frac{2}{\frac{p+1}{p} - 1} \\
m_{\mathrm{min}} &\geq 2p \qquad (14)
\end{aligned}$$

After this first transition event, the output voltage can continue to increase until no more opportunity for the next transition is found.

E. Maximum continuously generable output voltage

The maximum output voltage $U_{\mathrm{out,con,max}}$ that can be continuously generated depends on both the number of power modules m and the maximum and minimum module voltages $U_{\mathrm{mod,max}}$ and $U_{\mathrm{mod,min}}$. $U_{\mathrm{out,con,max}}$ can be calculated as shown in (15).

$$\begin{aligned}
U_{\mathrm{out,con,max}} = &\left(m - \left\lceil \frac{U_{\mathrm{mod,min}}}{2 \cdot U_\Delta} \right\rceil \right) \cdot U_{\mathrm{mod,max}} \\
&- \left\lfloor \frac{U_{\mathrm{mod,min}}}{2 \cdot U_\Delta} \right\rfloor \cdot U_{\mathrm{mod,min}} \qquad (15)
\end{aligned}$$

Equation (15) is valid for the method explained in section III-C. An analytical proof of this equation is pending. However, extensive simulations show that this equation and the calculation method are valid for a realistic and practical number of power modules m and module voltage range ($U_{\mathrm{mod,min}}$ and $U_{\mathrm{mod,max}}$). If the setpoint voltage U^*_{out} is higher, the output voltage can still be reached, but not continuously. In this case the CHB cells work in normal switching mode and additional filters would be necessary.

TABLE II
System specification

Parameter	Symbol	Value
Amount of power modules	m	4
Minimum module voltage	$U_{\mathrm{mod,min}}$	40 V
Maximum module voltage	$U_{\mathrm{mod,max}}$	60 V
Module voltage range	U_Δ	20 V
Primary voltage	U_{p}	750 V
Transformer winding ratio	n_{tr}	14.11:1
DAB switching frequency	f_{DAB}	50 kHz
Maximum phase voltage (15)	$U_{\mathrm{con,max}}$	140 V
Rated power of DAB	P_{DAB}	2 kW
System control frequency	f_{sys}	50 kHz
Grid frequency	f_{grid}	50 Hz

IV. Results

Both the calculation results and the measurements in the following subsections are generated using the system parameters of table II. A more detailed explanation and characterization of a single power module is shown in [17].

A. Hardware setup

Figure 4 shows the hardware setup of a single power module. It consists of the DAB stage and the CHB cell, current, voltage and temperature measurement systems and a plug-in field-programmable gate array (FPGA) controller board. The capacitor voltage of each power module is controlled by a high performance controller described in [18]. The single phase CHB converter topology consists of $m = 4$ power modules, each with a rated power of $P_{\mathrm{DAB}} = 2\,\mathrm{kW}$. The DC side is powered by a power supply with $U_{\mathrm{p}} = 750\,\mathrm{V}$.

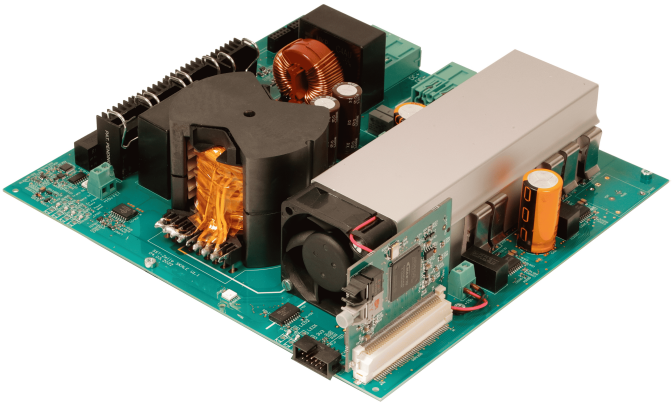

Fig. 4: Hardware of the power module with a DAB stage and a CHB cell

A superimposed controller calculates both the setpoint voltages of each module $U^*_{\mathrm{mod},n}$ and the switching states of the CHB cells at an update rate of $f_{\mathrm{sys}} = 50\,\mathrm{kHz}$ to generate the total output voltage U_{out} as defined by the setpoint U^*_{out}. However, each power module has its own FPGA to calculate the control variables and generate the switching pattern for the DAB. This controller operates at a frequency of $f_{\mathrm{DAB}} = 50\,\mathrm{kHz}$ to reach the set voltage $U_{\mathrm{mod},n}$ as quickly as possible. Since the expected output frequency f_{grid} is 50 Hz and the control frequency $f_{\mathrm{DAB}} = 50\,\mathrm{kHz}$, there are $C_{\mathrm{cyc}} = \frac{f_{\mathrm{DAB}}}{f_{\mathrm{grid}}} = \frac{50\,\mathrm{kHz}}{50\,\mathrm{Hz}} = 1000$ control cycles per grid period. This means that the setpoint resolution is high enough to produce a smooth output signal.

B. Simulation and measured results

Figure 5 shows the resulting module voltage trajectories, according to section III-C, for the system as specified before. In orange, the calculated setpoint of the output voltage of each power module $u^*_{\mathrm{AC},n}$ is shown. The measured output voltage of each module $u_{\mathrm{AC},n}$ is depicted in blue. The measured data shows that each controller is able to follow the module voltage setpoint $U^*_{\mathrm{mod},n}$ within a small deviation range.

The sum of all module output voltages $u_{\mathrm{AC,n}}$ results in the generated output voltage U_{out} as shown in blue in fig. 6. The setpoint of the sinusoidal output voltage is shown in orange. In the figure, the moment of the actual switching events is highlighted with black circles. During these eight switching events, there are brief voltage variations in the output voltage. They are caused by not perfectly synchronized switching events of the power modules. This problem can be solved both by optimizing the synchronization of the switching events

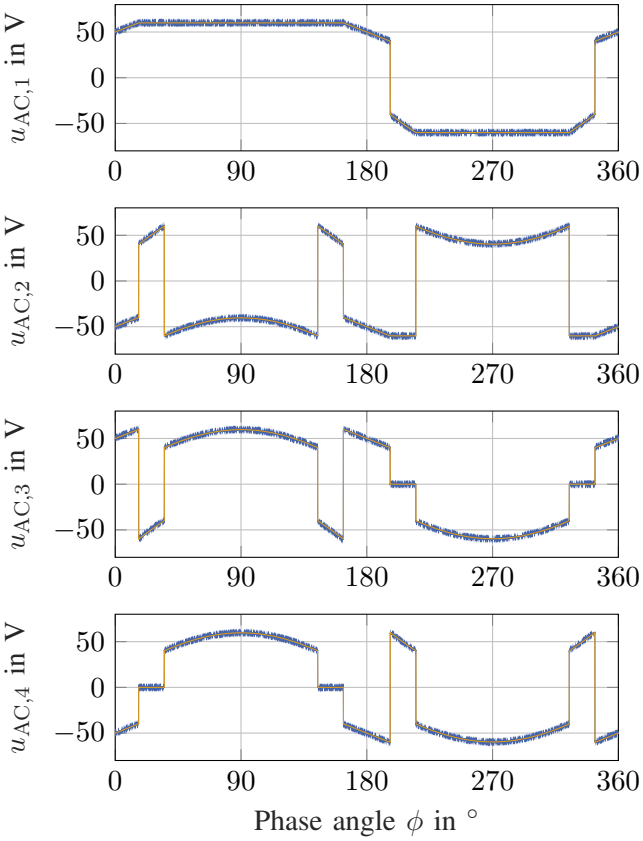

Fig. 5: Calculated setpoint voltage for each power module $u^*_{\mathrm{AC},n}$ (orange) and measured output voltage $u_{\mathrm{AC},n}$ (blue) of $m = 4$ power modules to create a continuous sinusoidal output voltage.

and by adding a small filter at the output of the converter. It can be seen that the resulting measured output voltage U_{out} almost perfectly follows the setpoint U^*_{out}. The calculation of the THD leads to a value of less than 1 %.

To validate the maximum achievable dynamics of both hardware and software, the maximum dynamics of a single power module must be measured. The results are shown in fig. 7. The dynamics required to generate the sinusoidal output voltage with a peak value of $U_{\mathrm{out,max}} = 140\,\mathrm{V}$, an output frequency of $f_{\mathrm{grid}} = 50\,\mathrm{Hz}$ and $m = 4$ power modules is calculated with Matlab. The blue curve shows the absolute value of the derivative of the output voltage $|\frac{\mathrm{d}U^*_{\mathrm{out}}}{\mathrm{d}t}|$. The maximum dynamic is about $44\frac{\mathrm{V}}{\mathrm{ms}}$. The focus of the algorithm is to use as many power modules simultaneously as possible. Therefore, usually more than one power module is actively changing its voltage, and they share the overall dynamics. As a result, the required dynamics of each power module $|\frac{\mathrm{d}U_{\mathrm{mod}}}{\mathrm{d}t}|$ is reduced, as shown in orange. The green curve shows

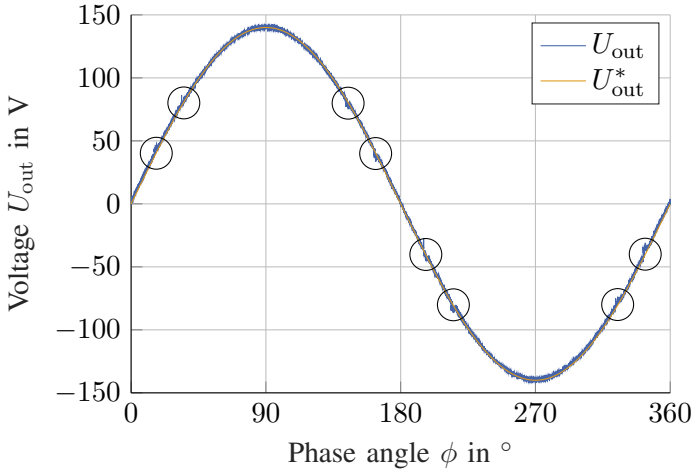

Fig. 6: Generated, measured output voltage U_{out} (blue) and setpoint voltage U^*_{out} (orange)

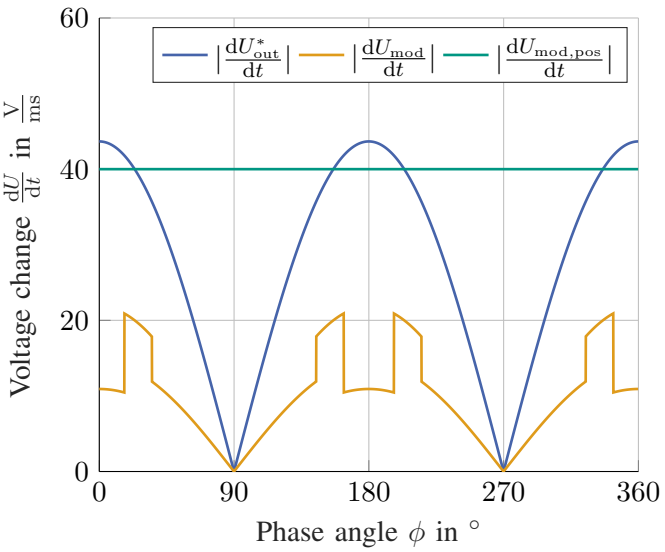

Fig. 7: Comparison of necessary and possible dynamics of the power module's voltage control. Absolute value of the derivation of the setpoint voltage $|\frac{dU^*_{\text{out}}}{dt}|$ (blue). Maximum necessary dynamics of each DAB module voltage $|\frac{dU_{\text{mod}}}{dt}|$ (orange). Measured maximum possible dynamics of the module voltage $|\frac{dU_{\text{mod,pos}}}{dt}|$.

the maximum possible dynamics of the module voltage $|\frac{dU_{\text{mod,pos}}}{dt}|$ according to measurements of the step response to both pulses and sinusoidal input signals. Since the required dynamics (orange) is always lower than the maximum possible dynamics (green), the power module voltages can be controlled fast enough. The available dynamic range is about a factor of two. This means that either the frequency of the output voltage can be increased by a factor of two or additional harmonics with lower amplitudes can be generated and superimposed on the fundamental wave. Figure 8 shows the bode plot of the voltage control of the power module being used. The setpoints of the power module voltage are sinusoidal in the range from $U_{\text{mod,min}} = 40\,\text{V}$ to $U_{\text{mod,max}} = 60\,\text{V}$. The frequencies are varied from $f_{\text{min}} = 10\,\text{Hz}$ to about $f_{\text{max}} = 3100\,\text{Hz}$. The bode plot of a power module helps to substantiate the above statements and to get an estimate of the possible dynamics. Since the voltage control gain of the power module is close to 1 and the phase is less than 7° at a frequency of 200 Hz, the system is able to provide the dynamics to generate a continuous output voltage with a single phase CHB converter.

V. Conclusion

With the CHB converter topology and the algorithm described in this paper, a dynamically controllable, galvanically isolated output voltage can be generated. However, the capacitor voltage of each power module must be individually and dynamically controlled by a DAB. The algorithm can be used to generate continuous output voltages, e.g. a sinusoidal waveform, without the need for a high switching frequency of the CHB cells. The measurement results show that the possible dynamic

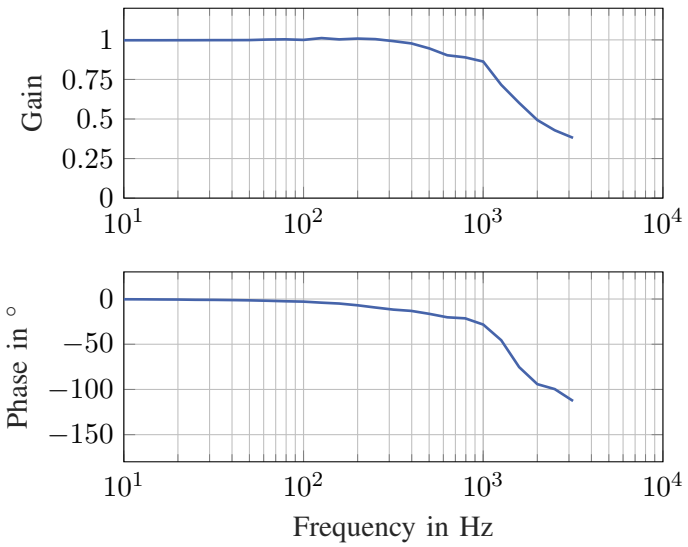

Fig. 8: Bode plot of the large signal voltage transfer function of a single DAB $G_{\text{DAB}}(s) = \frac{U_{\text{mod}}(s)}{U^*_{\text{mod}}(s)}$.

range of the module's voltage control is high enough to generate a sinusoidal output voltage with low THD. In addition, any other output voltage can be generated if its dynamics remain within the possible limits. However, special attention must be paid to the synchronization of the transition events and the control of the module voltages.

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