Inductive Adder for Driving Kicker Magnets Terminated in a Short-Circuit

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Kurzfassung

Im Teilchenbeschleunigerkomplex des CERN werden schnell gepulste Magnetsysteme für den Transfer des Teilchenstrahls zwischen den Beschleunigerstufen eingesetzt. Transmission-line-type Kicker-Magnete werden in vielen dieser Systeme verwendet, um die geladenen Teilchen mit Hilfe eines gepulsten Magnetfelds abzulenken, das einen wohldefiniert flachen Verlauf und eine schnelle Anstiegs- und Abfallzeit aufweist. Einige transmission-line-type Kicker-Magnete haben eine Kurzschluss-Terminierung, um bei gegebener Systemimpedanz, Aperturgröße und Magnetlänge durch Verdoppelung des Stroms im Kicker-Magnet eine doppelt so starke Ablenkung des Teilchenstrahls zu erzielen.

Die derzeit zur Ansteuerung dieser Kicker-Magnete verwendeten Impulsgeneratoren auf der Basis von pulsformenden Leitungen oder pulsformenden Netzwerken und Thyratronschaltern sollen in naher Zukunft ersetzt werden, da die verwendeten Thyratronschalter veraltet sind und das in den pulsformenden Leitungen verwendete SF_6-Gas die Umwelt belasten kann.

Im Rahmen der vorliegenden Arbeit wurden erstmals die Grundlagen erarbeitet, um zu zeigen, dass mit einem induktiven Spannungsaddierer eine Ansteuerung eines transmission-line-type Kicker-Magneten mit Kurzschluss-Terminierung möglich ist und dies eine vielversprechende Alternative zur veralteten Technik darstellt.

Um die Wanderwelle zu beherrschen, die vom Kurzschluss zurück in den induktiven Spannungsaddierer reflektiert wird, wurde im Rahmen eines neuen Entwurfsansatzes ein Zweigmodul entworfen und aufgebaut. Aufgrund der auftretenden Signalreflexion verfügt das Zweigmodul über eine neuartige Topologie mit zwei unabhängig voneinander gesteuerten Halbleiterschaltern. Dies ermöglicht

es, zunächst Energie in das Verbindungskabel und den Kicker-Magneten einzuspeisen, dann den resultierenden Strom in einem Freilaufintervall zirkulieren zu lassen und schließlich die Energie am Ende des Impulses zu absorbieren. Diese neue Betriebsart ermöglicht es, die Querschnittsfläche der magnetischen Kerne des induktiven Spannungsaddierers nur nach der doppelten Signallaufzeit in der Last zu bemessen, die aus dem Verbindungskabel und dem transmission-line-type Kicker-Magneten besteht. Dadurch kann im Vergleich zu einer herkömmlichen Anordnung die Querschnittsfläche der magnetischen Kerne für die üblichen Betriebsfälle deutlich reduziert werden, da die Kernquerschnittsfläche nun nicht mehr für die gesamte Impulslänge ausgelegt werden muss. Darüber hinaus ist im Gegensatz zu einem konventionellen Entwurf ein Betrieb mit höherer Pulswiederholrate möglich, da mit der neuen Betriebsart ein Zurücksetzen der magnetischen Kerne nicht erforderlich ist.

Wesentlich für die Anwendung ist, dass die Schaltvorgänge für die gepulste Energieeinspeisung und -entnahme durch den induktiven Spannungsaddierer zu genau definierten Zeitpunkten stattfinden, die durch die Signallaufzeiten in der Last festgelegt sind. Die hierfür erforderlichen kurzen Schaltzeiten konnten durch die Implementierung eines Gate-Boosting-Betriebs von SiC-MOSFETs erfüllt werden. Dabei wurden Anstiegszeiten von Spannung und Strom von $5\,\mathrm{ns}$ bei einer Spannung von $1.2\,\mathrm{kV}$ und einem Strom von $120\,\mathrm{A}$ für ein Zweigmodul erzielt.

Das Zweigmodul und die neue Betriebsart wurden erfolgreich mit einer Ersatzlast mit Kurzschlussterminierung getestet. Die Versuchsergebnisse bestätigen die Vorteile des neuartigen Entwurfs, des Schaltungskonzepts für das Zweigmodul und der neuen Betriebsart.

Abstract

In the CERN particle accelerator complex, fast pulsed magnet systems are used to transfer the particle beam between accelerator stages. Transmission line type kicker magnets are used in many of these systems to deflect the charged particles using a magnetic field pulse with a well-defined flat top and a fast rise and fall time. Some kicker magnets are terminated with a short-circuit for the advantage of twice the kick-strength for a given system impedance, aperture size, and magnet length, due to the doubling of the current in the kicker magnet. The pulse generators based on pulse forming lines or pulse forming networks and thyratron switches, currently used to drive these kicker magnets, should be replaced in the near future, due to the obsolescence of the thyratron switches employed and because of the environmental impact of SF_6 gas which is used in the pulse forming lines.

As a promising alternative, an inductive adder for driving these kicker magnets terminated in a short-circuit is investigated in this work.

In order to deal with the wave reflected from the short-circuit back into the inductive adder, as part of a new design approach, a specifically tailored branch module has been designed and built. To account for the reflection at the short-circuit, the branch module features a novel topology with two independently controlled semiconductor switches. This allows to first inject energy into the connecting cable and the kicker magnet, then to circulate the resulting current in a free-wheeling interval, and, finally, to absorb the energy at the end of the pulse. This new mode of operation makes it possible, to design the cross-sectional area of the magnetic cores of the inductive adder according to only twice the signal propagation time along the connecting cable and the kicker magnet, rather than according to the whole pulse length as in a conventional design. This allows for a

significant reduction in the cross-sectional area of the magnetic cores for the usual operating cases. In addition, in contrast to a conventional design, an operation at a higher pulse repetition rate is possible, as a reset of the core is not required with the new mode of operation.

It is essential for the application that the operation of the switches for the pulsed energy injection and extraction by the inductive adder results in steep edges at exactly defined times, which are determined by the signal propagation times in the connecting cable and the kicker magnet. These requirements have been met by implementing the gate boosting operation of SiC MOSFETs, resulting in a rise time of both voltage and current of $5\,\mathrm{ns}$ for a voltage of $1.2\,\mathrm{kV}$ and a current of $120\,\mathrm{A}$ per branch module.

The branch module and the new mode of operation have been tested successfully with a short-circuit terminated replacement load. The experimental results confirm the advantages of the novel design, the circuit concept of the branch module and the new mode of operation.

Contents

1 Introduction

The CERN laboratory features the world's largest and most powerful particle accelerator complex. It is situated in Geneva, Switzerland, and consists of several accelerator stages, each designed to accelerate particles to higher energies. Figure 1.1 shows a schematic of the complex [1]. The proton chain includes the Linac 4, the Proton Synchrotron Booster (PSB), the Proton Synchrotron (PS), the Super Proton Synchrotron (SPS), and finally the Large Hadron Collider (LHC). The PS accelerates protons and other charged particles to an energy of either $12.9\,\mathrm{GeV}$, $14\,\mathrm{GeV}$ or $26\,\mathrm{GeV}$, while the SPS further accelerates them to either $400\,\mathrm{GeV}$ or $450\,\mathrm{GeV}$. Thereby, the $26\,\mathrm{GeV}$ injection energy into the SPS and the $450\,\mathrm{GeV}$ extraction energy out of the SPS correspond to the beam required for the LHC [2]. The LHC, the most powerful accelerator in the complex, accelerates protons to an energy of up to $6.8\,\mathrm{TeV}$ [3] and is used for experiments in high-energy physics, such as the discovery of the Higgs boson [4].

1.1 Kicker Systems at CERN

In order to achieve high energies for charged particles in a large particle accelerator complex, multiple accelerator stages, such as circular accelerators, are cascaded, since each individual accelerator has a limited dynamic range [5]. Transferring the particle beams between accelerator stages via a beam transfer line, requires a way to extract particles from one accelerator and to inject them into the next stage. Figure 1.2 provides a simplified schematic of an injection kicker system used in circular accelerators showing a septum and a kicker magnet. The acceleration of particles in circular accelerators occurs by passing them through resonant cavities

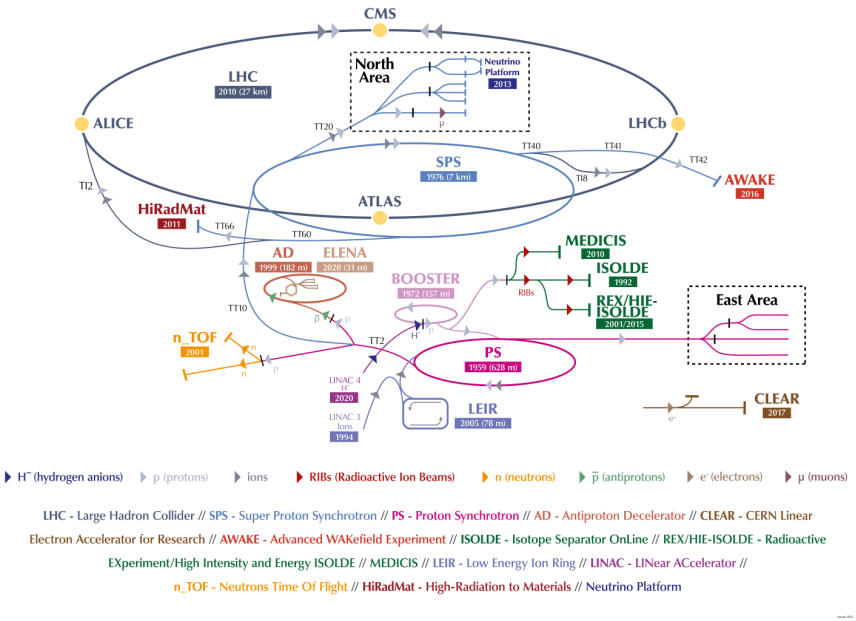


Figure 1.1: The CERN accelerator complex [1].

(not shown in fig. 1.2) that provide an electric field to accelerate the particles. However, the acceleration process is not continuous as the cavities operate in a resonant mode with a specific frequency, leading to the particle beam being divided into bunches with gaps in between. The septum is used to bring the injected beam as close as possible to the circulating beam. It contains a region with a deflecting electric or magnetic field, and a field-free region separated by a thin septum blade. The field in a septum is usually constant or slowly pulsed. The final adjustment of the injected beam trajectory into the circulating orbit is performed using fast, pulsed kicker magnets. Fast, pulsed magnets are required to ensure that only the injected beam, and not the circulating beam is deflected. Thereby, both the septum and the kicker magnet can consist of a group of modules arranged one behind the other. Each kicker magnet module is then driven by its own pulse generator.

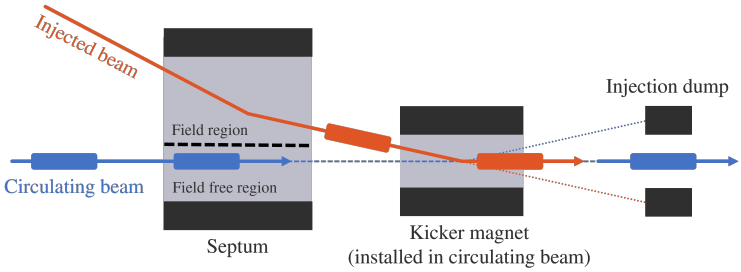


Figure 1.2: Kicker magnet installed with the circulating beam in the aperture of the magnet. The particles in the beam are arranged into bunches. The circulating beam is shown in blue, the injected beam in orange.

1.1.1 Kicker Magnets

Kicker magnets are used to deflect a defined number of bunches either from their incoming transfer line trajectory into the circulating orbit or from the circulating orbit into the extraction channel. Kicker magnets use the Lorenz force (eq. 1.1 [6]) to deflect charged particles with a charge q and a velocity v close to the speed of light as they pass through the magnetic field B in the kicker magnet.

$$F = q * v \times B \tag{1.1}$$

Although the field needs to be constant and well defined while a particle bunch traverses the kicker magnet, fast rise and fall times are important when a high degree of filling of the accelerator ring and thus a short gap between bunches is desired. In some extraction kicker systems at CERN, where the entire beam is extracted, a fast fall time is not required [7].

Another application for kicker magnets is in the beam dump system of an accelerator. In case of an emergency, the beam must be extracted and dumped onto a specifically designed target in order to quickly empty the accelerator ring. For this purpose, the target is designed in such a way, that it is able to absorb the total energy of the beam, which is e.g. in the case of the LHC up to $470\,\mathrm{MJ}$ per beam. This design includes a dilution kicker system to spread the beam over an

area of the dump target in order to distribute the energy to an absorption volume of sufficient capacity [8]. As the accelerator ring is emptied completely after the beam is extracted, for the kickers employed in the dump system, the fall time is not important. To be able to activate the beam dump system with sufficiently low latency at any time, the pulse generators for driving the kicker and deflection magnets of the beam dump system are kept charged to a voltage which is dependent upon the beam energy, and ready for operation [9].

1.1.1.1 Transmission line type kicker magnets

At CERN most fast kicker magnets are set up as transmission line type kicker magnets [7]. Figure 1.3 shows an exemplary picture of a transmission line type kicker magnet used to inject beams into the SPS. It consists of inductive segments formed by a parallel conductor and return-conductor around several ferrite yokes interleaved with capacitances to ground. This setup creates an LC-chain, approximating a broadband transmission-line with a characteristic impedance Z_0 [7]. An impedance matched cable is used to connect the kicker magnet to the pulse generator.

Figure 1.3: Photo of a transmission line type kicker magnet [10].

At present, most kicker magnets at CERN are driven by pulse generators based on pulse forming lines (PFL) or pulse forming networks (PFN) [11] in combination with thyratron switches [7]. The output impedance of a PFL- or PFN-based pulse generator is matched to the characteristic impedance of the kicker magnet. Therefore, the impedance of the matched source and the load impedance form a voltage divider, causing a reduction in driving voltage by half and requiring a charging voltage twice that of the voltage applied to the kicker magnet. Due to design constraints, a maximum charging voltage of $80\,\mathrm{kV}$ and limited space, SF_6 gas is used in the insulation of many of the cables serving as pulse forming lines. Since SF_6 gas is known to be harmful to the environment [12] these systems should be replaced in the near future [13]. In addition, thyratron switches can sometimes turn on spontaneously without a trigger signal applied, which can cause miskicks of the beam and damage to accelerator components; they are also becoming increasingly difficult to source [7].

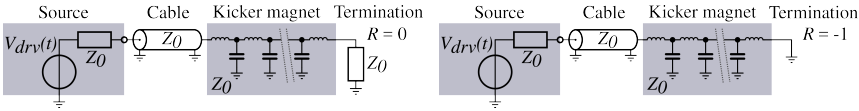
1.1.1.2 Transmission line type kicker magnet with a short-circuit termination

The simplified circuit diagram in fig. 1.4 illustrates a transmission line type kicker magnet connected to a pulse generator via a transmission line. Many kicker magnets at CERN are terminated in a matched impedance, as shown in fig. 1.4(a), which absorbs the wave traveling from the pulse generator through the kicker magnet and the connecting cable. The reflection coefficient R for a transmission line with characteristic impedance Z_0 terminated in an impedance Z is defined according to eq. 1.2. For Z = Z_0 the reflection coefficient R equals zero.

$$R = \frac{Z - Z_0}{Z + Z_0} \tag{1.2}$$

Some kicker magnets, however, are specified to be terminated in a short-circuit, as shown in fig. 1.4(b). For a very low terminating impedance approximating $0\,\Omega$, the reflection coefficient R becomes -1. The reflection at the short-circuit

termination, results in a doubling of the current flowing through the kicker magnet compared to a kicker with a matched termination. Thereby, this current doubling also doubles the amplitude of the deflecting magnetic field in the kicker magnet for a given system impedance, aperture dimensions, and magnet length. Hence, the advantages of this setup are a doubling of the kick strength in relation to the voltage applied to the kicker magnet, as well as savings on space along the beam line. However, since the full current in the magnet is only flowing after the wave has traversed the kicker magnet twice, the field rise time, i.e. the time needed to establish the magnetic field along the whole length of the magnet, is increased.



(a) Terminated in a matched impedance **(b)** Terminated in a short-circuit

Figure 1.4: Simplified circuit diagram of a transmission line type kicker magnet connected to a pulse generator.

The deflection angle Θ of a charged particle is the main design parameter for a kicker magnet. For a given design of a transmission line type kicker magnet, in the idealized case, Θ is proportional to the magnetic flux Φ_{kicker}. Neglecting losses, the time integral of the difference between the voltages at the input and output ports of the transmission line type kicker magnet, $V_{m,in}(t)$ and $V_{m,out}(t)$, respectively, gives the magnetic flux $\Phi_{kicker}(t)$, as shown in eq. 1.3 [7].

$$\Phi_{kicker} = \int \left(V_{m,in}(t) - V_{m,out}(t)\right) dt \propto \Theta \tag{1.3}$$

For a kicker magnet terminated in an ideal short-circuit, the voltage at the magnet's output $V_{m,out}(t)$ is zero. So, for a lossless transmission line type kicker magnet terminated in a short-circuit, the field in the magnet, and thus the deflection angle Θ is proportional to the integral of the voltage at the kicker magnet's input as shown in eq. 1.4.

$$\Phi_{kicker,SC}(t) = \int (V_{m,in}(t))\, dt \propto \Theta \tag{1.4}$$

The rise of the field in the kicker magnet starts once the rising slope of the in-going wave arrives at the magnet input, and is completed when the rising slope of the reflected wave has fully passed the magnet input terminal again. Therefore, as worst case estimate, the field rise time in a short-circuit terminated kicker magnet $t_{fieldrise,SC}$ consists of two times the one-way signal propagation time of the kicker magnet τ_k and the rise time of the driving voltage pulse $t_{rise,p}$ (eq. 1.5).

$$t_{fieldrise,SC} = 2 * \tau_k + t_{rise,p} \tag{1.5}$$

A more accurate estimate of the field rise time in a transmission line type kicker magnet terminated in a matched impedance $t_{fieldrise,term}$ is given in [14] as the power function shown in eq. 1.6.

$$(t_{fieldrise,term})^x = t_{rise,p}^x + (M * \tau_k)^x \tag{1.6}$$

The parameters M and x in eq. 1.6 depend on the definition of the field rise time and have been determined by simulation in [14] for different definitions, e.g. for a field rise time definition from $10\,\%$ to $90\,\%$ M = 0.8 and x = 2.33. With strict rise time requirements of $0\,\%$ to $100\,\%$, both parameters M and x approach one.

1.2 Inductive Adder

In previous work, a semiconductor-based pulse generator using an inductive adder topology has been identified as a promising possibility to replace pulse-forming line-based generators with thyratron switches [15]. Due to its modularity, the inductive adder topology has the advantage of excellent scalability in both voltage and current [7]. Compared to a Marx generator, less parasitic capacitance to

ground has to be charged during pulse generation since the stages remain at ground potential. The ground referenced stages also make the distribution of control signals to the stages easier.

1.2.1 Setup of an Inductive Adder for Driving a Kicker Magnet

Figure 1.5 shows a simplified equivalent circuit of an inductive adder. It comprises

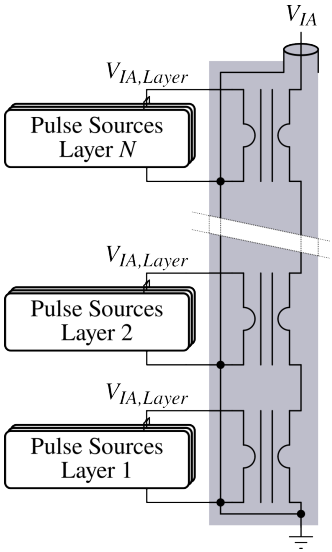


Figure 1.5: Inductive adder comprising pulse sources driving the primary winding of transformers. The secondary windings of these output transformers are connected in series.

pulse sources, each driving the primary winding of a transformer. Advantageously for the application of driving a kicker magnet, each transformer has a transformer ratio of one with one turn for each winding (see 1.2). The secondary windings of these transformers are connected in series. Hence, the output voltage of the inductive adder $V_{IA,layer}$ is the sum of the voltages of the primary pulse sources

$V_{IA,layer}$. With $V_{IA,layer}$ equal for all layers, the output voltage V_{IA} is $V_{IA,layer}$ times the number of layers N_{layers} (eq. 1.7).

$$V_{IA} = N_{layers} * V_{IA,layer} \tag{1.7}$$

The current that an inductive adder can deliver can be scaled up by paralleling multiple primary pulse sources, called branch modules, in each layer that share the current equally. Thereby, the total current at the output of the inductive adder I_{load} is the current of one branch module I_{branch} times the number of branch modules per layer $N_{branches}$ (eq. 1.8).

$$I_{load} = N_{branches} * I_{branch} \tag{1.8}$$

Figure 1.6 shows a coaxial design of an inductive adder useful for driving a kicker magnet [16]. The magnetic cores of the output transformers are encased in a conductive core housing that serves as the single turn primary winding. The bottom half of each core housing is connected to ground by rods that run through the inductive adder stack on the outside of the magnetic cores (fig. 1.6). A center conductor, called stalk, functions as the series connected secondary windings. Depending on the design of the stalk, which is described in more detail in section 1.2.2, the stalk can be grounded at either end, to select the polarity of the output pulse [17]. For the example shown in fig. 1.6, the stalk is grounded at the bottom of the inductive adder stack, with the top end being the output of the inductive adder. The primary pulse sources of each layer consist of branch modules slotted into gaps between these core housings (fig. 1.6). Each layer comprises multiple such nominally identical branches, that drive the respective output transformer in parallel and thereby share the load current I_{load}.

The axisymmetric arrangement of the branch modules in each layer and equal impedances in each module foster equal current sharing between the branches [20]. When assuming equal current distribution between the branch modules, eq. 1.9 describes the branch current I_{branch}, which each branch module has to

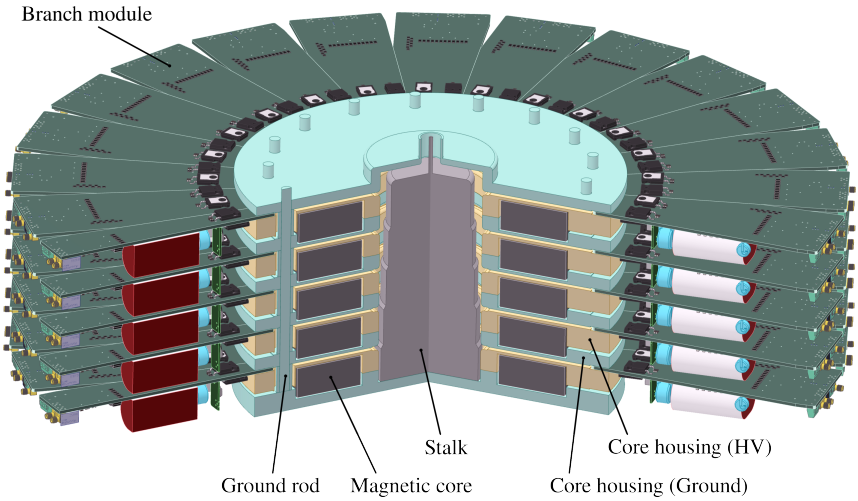


Figure 1.6: Sectional view of a coaxial setup of a five-layer inductive adder [18, 11, 19].

deliver, as a fraction of the total current through the load, I_{load}, according to the number of branch modules per layer $N_{branches}$. The voltage per layer V_{layer} is according to eq. 1.10 a fraction of the voltage, which the load current I_{load} causes across the load impedance Z_{load} divided by the number of layers N_{layers}. Thus, the load impedance Z_{branch}, for which each branch module has to be designed, is given by eq. 1.11.

$$I_{branch} = \frac{I_{load}}{N_{branches}} \tag{1.9}$$

$$V_{layer} = \frac{Z_{load} * I_{load}}{N_{layers}} \tag{1.10}$$

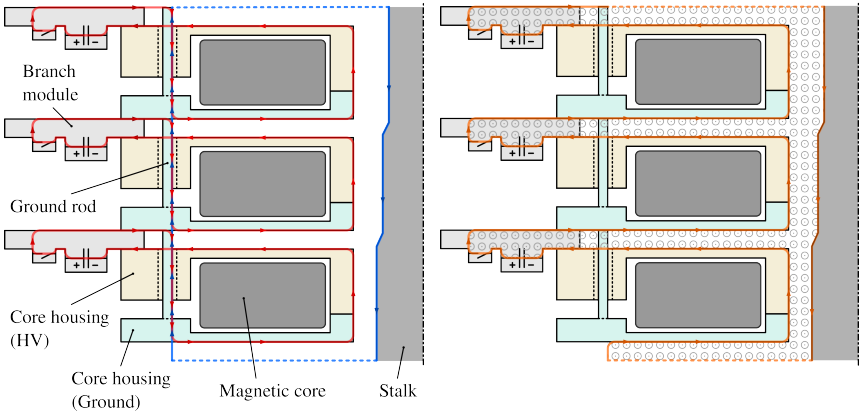
$$Z_{branch} = \frac{V_{layer}}{I_{branch}} = \frac{Z_{load} * N_{branches}}{N_{layers}} \tag{1.11}$$

Figure 1.7(a) shows the current paths of the primary currents through the assembly in red color, as well as the path of the secondary current in blue color. The secondary current superimposed with the primary currents sum to zero in some branches of the circuit under the assumption of the ideal case, that the primary currents and the secondary current are equal. In a real design, however, this ideal case can only be approximated, e.g. due to the magnetizing current of the cores and the non-ideal coupling between the primary and secondary sides. For this illustration a very high permeability of the magnetic cores and an ideal coupling between the primary and secondary current and, therefore, a negligibly small magnetizing current is assumed. The superposition of the primary and secondary currents leads to a resulting current as shown in fig 1.7(b). This arrangement combines the advantages of the mechanical designs presented in [19] and [16]. The current through the ground return rods is almost completely compensated and mainly flows in the center conductor and the primary circuits only. For equal primary currents and secondary current, the magnetic field is constrained to the gap between the stalk and the core housing, the insulating gap between the layers, and the primary circuit as highlighted in fig. 1.7(b).

The mechanical setup is modular, and the branch modules can be simply plugged in around the outside of the inductive adder stack. This allows for easy replacement of modules.

1.2.2 Wave Propagation along the Inductive Adder Stack

Since the rise times of the primary pulse sources can be of a similar order of magnitude to the signal propagation times in the mechanical structure of an inductive adder, the consideration of wave propagation along the inductive adder stack is useful. In literature [21, 11] there are two design approaches for an impedance matched mechanical setup of an inductive adder. Both use the capacitances between the stalk and the core housings together with inductances present in the setup to approximate a transmission line with a specific characteristic



(a) Primary current paths (red) and secondary current path (blue).

(b) Sum of primary- and secondary current paths (excluding magnetizing current).

Figure 1.7: Coaxial setup of an inductive adder.

impedance to match the traveling wave impedance of the inductive adder to the characteristic impedance of its intended load.

1.2.2.1 Constant diameter stalk

The design approach described in [21] and used in previous inductive adder designs at CERN [16, 22] uses a constant diameter stalk, and has the same characteristic impedance for each layer of the coaxial structure. The inductive adder structure is modeled as an LC-chain where each layer represents one cell, as shown in fig. 1.8.

The capacitance of each layer is provided by the cylindrical capacitor between the stalk and the core housing. According to the equivalent circuit of a transformer [23], the inductance of each layer can be described as the series connection of the secondary inductance of the coaxial structure per layer $L_{layer,sec}$ and the inductance of the primary circuits of one layer $L_{layer,pri}$ translated to the secondary side by the layer-transformer, which has a transformer ratio of one in the considered design. Thereby, the magnetizing current of the core is considered

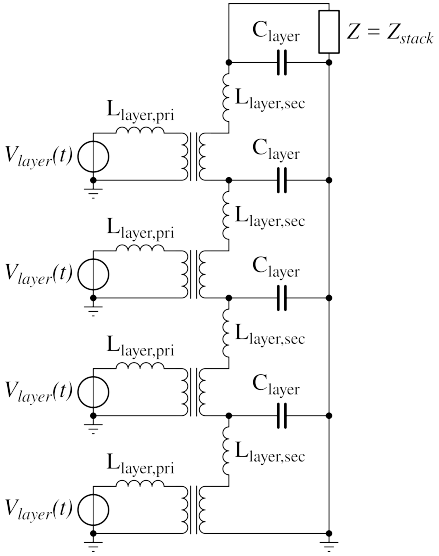


Figure 1.8: Four layer inductive adder stack modeled as an LC-chain. The primary inductances are part of the LC-chain.

to be negligibly small. Therefore, the primary inductance has to be considered for matching the characteristic impedance of this LC-chain Z_{stack} to a load impedance according to eq. 1.12 [21].

$$Z_{stack} = \sqrt{\frac{L_{layer,sec} + L_{layer,pri}}{C_{layer}}} \tag{1.12}$$

For a given dielectric material used between the stalk and the core housing with the material properties ϵ_r and μ_r, the inductance $L_{layer,sec}$ and the capacitance C_{layer} of the secondary side coaxial structure can be calculated for the mechanical height of one layer h_{layer} as per eqs. 1.13 and 1.14 [24] depending on the ratio of the inner diameter of the core housing d_{ch} and the outer diameter of the stalk d_{stalk}. Thereby, the structure has been approximated as a coaxial transmission line.

$$C_{layer} = 2\pi\epsilon_0\epsilon_r * \frac{h_{layer}}{\ln\left(\frac{d_{ch}}{d_{stalk}}\right)} \tag{1.13}$$

$$L_{layer,sec} = \frac{\mu_0\mu_r}{2\pi} * h_{layer} * \ln\left(\frac{d_{ch}}{d_{stalk}}\right) \tag{1.14}$$

By multiplying equations 1.13 and 1.14 together and rearranging, the secondary inductance $L_{layer,sec}$ of the coaxial structure can be expressed independent of $\frac{d_{ch}}{d_{stalk}}$ as a function of C_{layer} and the parameters ϵ_r, μ_r and h_{layer}, which depend on the setup of the inductive adder (eq. 1.15).

$$L_{layer,sec} = \frac{\epsilon_0\epsilon_r * \mu_0\mu_r * h_{layer}^2}{C_{layer}} \tag{1.15}$$

Substituting eq. 1.15 into eq. 1.12, and solving for C_{layer} allows to calculate the required C_{layer} depending on the primary inductance $L_{layer,pri}$, the characteristic impedance of the inductive adder stack Z_{stack} and the design parameters ϵ_r, μ_r and h_{layer}, as per eq. 1.16.

$$C_{layer} = \frac{L_{layer,pri} + \sqrt{4\epsilon_0\epsilon_r\mu_0\mu_r * Z_{stack}^2 * h_{layer}^2 + L_{layer,pri}^2}}{2Z_{stack}^2} \tag{1.16}$$

For generating an output pulse, all layers are triggered simultaneously. This leads to two traveling waves emanating from each individual layer, one propagates up along the inductive adder stack, the other wave with the opposite sign travels downwards along the stack. The downwards traveling waves are reflected at the grounded bottom end of the stack with a reflection coefficient of minus one and travel back up towards the output of the inductive adder. Only once all traveling waves have reached the output, at the top of the inductive adder, the full output voltage $N_{layers} * V_{layer}$ is reached over an impedance matched load. So, the rise

time of an inductive adder stack, with a constant diameter stalk in a configuration as outlined, is at least twice the signal propagation time in the stack. The formula for the rise time of the inductive adder stack, neglecting the rise time of the primary pulse sources, is given in [21] as shown in eq. 1.17.

$$t_{rise,cd} = 2N_{layers} * \sqrt{(L_{layer,sec} + L_{layer,pri}) * C_{layer}} \tag{1.17}$$

With the capacitance C_{layer} determined by the input parameters $L_{layer,pri}$, ϵ_r, μ_r, h_{layer} and Z_{stack}, the ratio between the outer diameter of the stalk d_{stalk} and the inner diameter of the core enclosures d_{ch} is fixed via the relation described in eq. 1.13. Rearranging eq. 1.13 yields eq. 1.18 for the inner diameter of the core housings d_{ch}.

$$d_{ch} = d_{stalk} * \exp\left(\frac{2\pi\epsilon_0\epsilon_r * h_{layer}}{C_{layer}}\right) \tag{1.18}$$

In the top layer the capacitor C_{layer} needs to withstand the full output voltage of the inductive adder $V_{gen,max}$. With a larger primary inductance a larger capacitance between the core housing and the stalk is required, to reach the designed characteristic impedance. Hence, a large primary inductance makes the design of this insulation more challenging. Equation 1.19 [25] gives the electric field strength $E(r)$ inside a cylindrical capacitor as a function of the radius r.

$$E(r) = \frac{V_{gen,max}}{r * \ln\left(\frac{d_{ch}}{d_{stalk}}\right)} \tag{1.19}$$

Thereby, the electric field strength is highest at the radius of the stalk. The maximum electric field strength E_{max} in the insulation gap between the stalk and the core housing is therefore given by eq. 1.20.

$$E_{max} = \frac{V_{gen,max}}{\frac{d_{stalk}}{2} * \ln\left(\frac{d_{ch}}{d_{stalk}}\right)} \tag{1.20}$$

By solving eq. 1.20 for d_{ch}, eq. 1.21 is obtained as a constraint for d_{ch}, dependent on d_{stalk} and the maximum electric field strength E_{max} in the insulation medium between the core casing and the stalk for a given maximum output voltage $V_{gen,max}$ of the inductive adder.

$$d_{ch} = d_{stalk} * \exp\left(\frac{2 * V_{gen,max}}{E_{max} * d_{stalk}}\right) \tag{1.21}$$

By equating eq. 1.18 and eq. 1.21 and rearranging for d_{stalk}, eq. 1.22 is obtained for the diameter of the stalk.

$$d_{stalk} = \frac{2 * V_{gen,max} * C_{layer}}{E_{max} * 2\pi\epsilon_0\epsilon_r * h_{layer}} \tag{1.22}$$

1.2.2.2 Tapered stalk

An alternative design approach for an impedance matched inductive adder is described in [11]. The mechanical setup differs from the previously described one, by a stalk that features a decreasing diameter towards the output of the inductive adder; this will be referred to as a tapered stalk. The inductive adder is modeled as stacked pieces of transmission line, representing the coaxial structure of the layers, with the pulse sources in series in between, as shown in fig. 1.9.

The characteristic impedance Z_{layer} of these transmission lines increases from layer to layer from the grounded end (bottom) of the stack to the output end (top). The change in impedance per layer is given by the load impedance Z_0 the inductive adder is matched to, divided by the total number of layers N_{layers}, with the top layer having the impedance Z_0. The characteristic impedance Z_{layer} of each layer n_{layer} is given by eq. 1.23, where n_{layer} = 1 at the bottom of the stack and n_{layer} = N_{layers} at the top of the stack.

$$Z_{layer}(n_{layer}) = \frac{n_{layer} * Z_0}{N_{layers}} \tag{1.23}$$

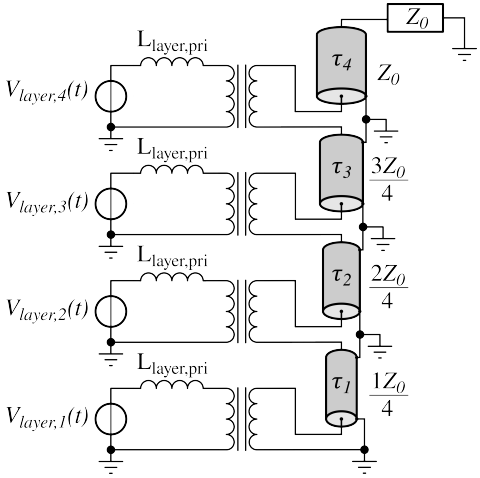


Figure 1.9: Four-layer inductive adder stack modeled as stacked pieces of transmission line. The characteristic impedance increases towards the output.

The pulse sources are triggered in sequence synchronized to the propagation of the wavefront in the inductive adder stack. The triggering of the bottom layer starts a wave traveling upwards along the stalk, and the field from the voltage of each layer adds to the field of the upwards propagating wave. Hence, the voltage between the stalk and the core housings, that form the outer conductor of the coaxial structure, increases from layer to layer. The distance between inner and outer conductor increases such that there are cylindrical equipotential surfaces concentric around the stalk. Because, ideally, there is no gradient in the electric field parallel to the stalk, once the wave has passed a layer, no wave is traveling downwards.

In [11] the sources at the feedpoints are pulse forming lines, i.e. a source with a matched inner impedance. But the principle also works, with low impedance sources, directly driving the feedpoints between layers [26]. Thereby, each pulse source, comprising the primary inductance $L_{layer,pri}$, drives an impedance $Z_{input,layer}$ equal to a fraction of the load impedance Z_0 corresponding to the number of layers N_{layers} (eq. 1.24) [11].

$$Z_{input,layer} = \frac{Z_0}{N_{layers}} \tag{1.24}$$

When the ratio between the voltage of the wave traveling upwards along the stalk at each feedpoint $V_{trav,feedpoint}$ and the voltage of the wave injected at the feedpoint $V_{inj,feedpoint}$ is equal to the ratio of the layer impedance $Z_{layer}(n_{layer})$ and the feedpoint impedance $Z_{input,layer}$ (eq. 1.25), the wave traveling along the stalk is not transmitted into the feedpoint [27].

$$\frac{V_{inj,feedpoint}}{V_{trav,feedpoint}} = \frac{Z_{input,layer}}{Z_{layer}(n_{layer})} \tag{1.25}$$

In this case, the primary pulse sources are not part of the waveguide through which the wave traveling along the stalk propagates. Therefore, with this design approach, the primary inductances are part of the primary pulse sources and do not factor into the mechanical design of the inductive adder stack for a specific characteristic impedance at the output. In contrast, with the constant diameter stalk approach (sec. 1.2.2.1), the primary inductances are part of the LC-chain through which the wave propagates along the stack. To match the characteristic impedance of this LC-chain to the load impedance, the capacitances between the constant diameter stalk and the core housings are increased to compensate for the primary inductances. Thus, for a given output impedance, the maximum electric field strength in the insulation gap between the stalk and the core housing is normally lower for the tapered stalk approach than for the constant diameter stalk design approach, for the same inner diameter of the core housings. As a result, using a tapered stalk with an otherwise given inductive adder design can increase the rated voltage of the inductive adder stack.

Furthermore, with the tapered stalk design, the mechanical length of the stack has no influence on the rise time at the output of the inductive adder. The rise and fall time at the output matches the rise and fall times of the individual stages operating into the impedance $Z_{input,layer}$. Because the signal propagation time between the layers does not factor into the rise time at the output of the generator,

for example, splitting the inductive adder into two stacks connected by cables with matched impedance, would not negatively impact the rise time.

However, one disadvantage of the tapered stalk approach is the increased complexity in controlling the different layers, as they have to be triggered one after another with a delay time in the range of a few $100\,\mathrm{ps}$. Additionally, the constant diameter stalk design allows the stalk to be grounded at either end, to select the polarity of the output pulse. As the tapered stalk has a defined ground and output end, the tapered stalk must be reversed to invert the output polarity of a tapered stalk inductive adder.

Theoretically, the increasing impedance towards the output of the stack, could be achieved by using a constant diameter stalk and using core housings with appropriate inside diameters. However, in practice this would be an expensive approach, as the core housings and cores would need to be individually dimensioned. Therefore, in practice, the stalk is tapered.

The determination of the diameter of the core housings d_{ch} and the stalk diameter at each layer $d_{stalk}(n_{layer})$ can be done analogously to the approach with a constant diameter stalk (sec. 1.2.2.1). Assuming cylindrical equipotential surfaces concentric around the stalk for the tapered stalk design, the highest electric field strength E_{max} occurs at the surface of the stalk at the top layer of the inductive adder stack, where the surface radius is the smallest. With a given maximum output voltage of the inductive adder $V_{gen,max}$ and a maximum permissible E_{max} eq. 1.26, analogous to eq. 1.21, gives a first constraint for d_{ch} as a function of the stalk diameter at the top layer $d_{stalk}(top)$.

$$d_{ch} = d_{stalk}(top) * \exp\left(\frac{2 * V_{gen,max}}{E_{max} * d_{stalk}(top)}\right) \tag{1.26}$$

The characteristic impedance of the transmission line $Z_{layer}(n_{layer})$, formed by the stalk and the core housing of each layer with the diameters $d_{stalk}(n_{layer})$ and d_{ch} is given by eq. 1.27 with the parameters μ_r and ϵ_r of the dielectric between the stalk and the core housings [28].

$$Z_{layer}(n_{layer}) = \frac{1}{2\pi}\sqrt{\frac{\mu_0\mu_r}{\epsilon_0\epsilon_r}}\ln\left(\frac{d_{ch}}{d_{stalk}(n_{layer})}\right) \tag{1.27}$$

For the top layer, the characteristic impedance $Z_{layer}(top)$ is equal to the load impedance Z_0. Rearranging eq. 1.27 for d_{ch} gives eq. 1.28.

$$d_{ch} = d_{stalk}(top) * \exp\left(2\pi * \sqrt{\frac{\epsilon_0\epsilon_r}{\mu_0\mu_r}} * Z_0\right) \tag{1.28}$$

By equating eq. 1.26 and eq. 1.28 and rearranging for $d_{stalk}(top)$, eq. 1.29 is obtained for the diameter of the stalk at the top layer.

$$d_{stalk}(top) = \sqrt{\frac{\mu_0\mu_r}{\epsilon_0\epsilon_r}} * \frac{V_{gen,max}}{\pi * E_{max} * Z_0} \tag{1.29}$$

For this design, the inner diameter of the core housings is constant for all layers and can be calculated from eq. 1.28 with $d_{stalk}(top)$ from eq. 1.29. The stalk diameter for each layer can then be determined by rearranging eq. 1.27 for $d_{stalk}(n_{layer})$ (eq. 1.30).

$$d_{stalk}(n_{layer}) = d_{ch} * \exp\left(-2\pi * \sqrt{\frac{\epsilon_0\epsilon_r}{\mu_0\mu_r}} * Z_{layer}(n_{layer})\right) \tag{1.30}$$

1.2.3 Inductive Adder for Short-Circuit Mode Operation

When operating the kicker magnet with a matched termination, in the idealized scenario, no reflections occur. In this case, the primary pulse sources of an inductive adder can be designed with a single controllable semiconductor switch per branch module [29]. In contrast to this design, if a kicker magnet terminated in a short-circuit is being driven by an inductive adder, a new design approach for the branch module is required to manage the reflections from the termination.

1.2.3.1 Typical parameters of relevant kicker systems at CERN

At CERN, the kicker systems which are of great interest for an upgrade with a short-circuit mode capable inductive adder are those equipped with PFL-based pulse generators and comprising SF_6 gas-filled cables. Table 1.1 shows the parameters of exemplary kicker systems featuring a short-circuit termination and currently in operation in the CERN PS complex [30, 31].

All these short-circuit terminated kicker magnets are of the transmission line type. The currents to drive these magnets are in the order of $3\,\mathrm{kA}$ to $6.4\,\mathrm{kA}$. This refers to the flat top current in the magnet after the current doubling at the short-circuit termination. The characteristic impedance of the designs listed in table 1.1 ranges between $12.5\,\Omega$ and $26.3\,\Omega$. This leads to input voltages of $30\,\mathrm{kV}$ to $40\,\mathrm{kV}$ at the input terminal of the kicker magnet. Due to the voltage divider formed by a pulse generator with a matched characteristic impedance and the impedance of the kicker magnet and the connecting cable, the charging voltage of a PFL/PFN based pulse generator needs to be twice this voltage. These high voltages make the replacement of SF_6 gas filled cables with new cables a challenge, and thus using an inductive adder with a low source impedance is an attractive, but challenging alternative.

1.2.3.2 Previous work on inductive adders for driving a short-circuit terminated kicker magnet

Some first theoretical considerations for adapting an inductive adder for operation with a short-circuit terminated kicker magnet were made in [15]. Figure 1.10 shows a circuit for one layer of an inductive adder that was simulated in [15], which has a matching resistor (Rmatch) with a parallel switch (U3) in series with the pulse capacitor Cp.

While the switch U3 is closed the primary current flows through the switch; from the moment the switch is opened, the current flows through the parallel resistor. The matching switch U3 is opened at the moment the reflected waveform arrives

Table 1.1: Parameters of exemplary kicker systems operated with a short-circuit termination currently in operation in the CERN PS complex [30, 31, 32].

System	KFA45	AD Injection	KFA10
Magnet Type	Transmis. Line	Transmis. Line	Transmis. Line
Magnet Z_0 [Ω]	26.3	15	12.5
Magnet input Voltage [kV]	40	40	30
Magnet Current incl. doubling at short-circuit termination [kA]	3.042	5.3	4.8
One-way signal propagation time of magnet [ns]	33	72 .. 83	36
Cable length between pulse generator and kicker magnet [m]	46.5 .. 64.5	44 .. 67.6	34
Flattop duration [µs]	2.6	0.7	1.6
Field rise time 5 %-95 % [ns]	80	163 .. 185	88
Flat top ripple (peak) [%]	±2	±2	±2
Post pulse ripple [%]	5.6		
Generator type	PFL	PFL	PFL
Uses SF_6 gas	Yes	Yes	Yes

at the inductive adder the first time [15]. However, as the simulations in [15] show, once the reflected wave arrives at the inductive adder, the freewheeling diode D1 starts to conduct. Therefore, the resistor Rmatch only serves to limit the current through the switch U1,U2 as it remains closed. The energy provided by the pulse capacitor after the arrival of the reflected wave at the pulse generator is thereby fully dissipated in the matching resistor. As long as the current through

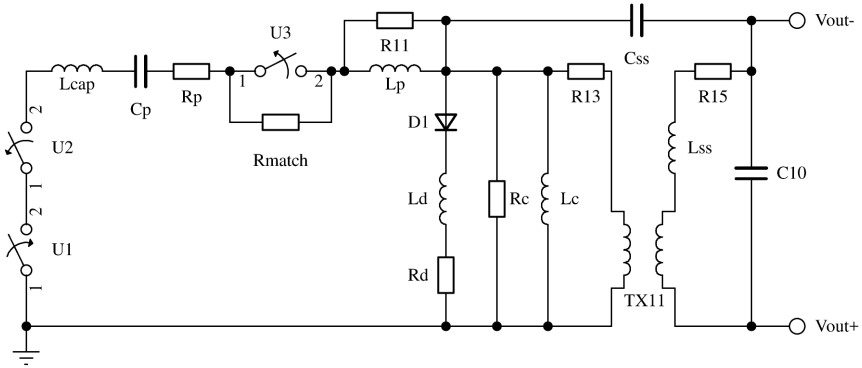


Figure 1.10: Inductive adder layer with additional resistor (Rmatch) and switch (U3) [15].

the generator exceeds the current through the switch U1,U2, the freewheeling diode D1 conducts and the matching resistor has no effect on the impedance at the generator interface. Once the main switch opens, the entire generator current commutates into the freewheeling diode. Therefore, the current flowing in the pulse generator, the connecting cable and the kicker magnet slowly decays due to losses and voltage drops over the diodes and can not be actively switched off. Therefore, this circuit is not suitable for applications where a fast fall time of the pulse is required.

1.3 Structure of the Work

Until now, inductive adders have been employed for applications comprising a matched load where no reflections occur. However, an inductive adder circuit suitable for operation with a short-circuit terminated load, must be able to deal with a wavefront reflected back from the load.

Although in [15] a first approach for a circuit for dealing with the reflections from a short-circuit termination is described, the circuit has never been set up and tested, and unfortunately is not suitable for many kicker applications as the current cannot be interrupted.

Despite a thorough literature search, no existing solution for the operation of an inductive adder with a load terminated in a short-circuit has been found. Therefore, research on the design of such an inductive adder has been initiated.

As a first step, a system comprising a kicker magnet with a short-circuit termination, a connecting cable, and an inductive adder has been analyzed. Based on the results obtained, the requirements for the operation of an inductive adder for driving a kicker magnet terminated with a short-circuit have been worked out. Tailored to these requirements, a novel mode of operation has been defined and verified by simulations. The results are described in chapter 2.

Subsequently, a circuit suitable for the requirements has been designed, set up and tested, as described in chapter 3.

Finally, the design has been experimentally verified successfully. The results are presented in chapter 4.

2 Inductive Voltage Adder for Short-Circuit Mode Operation

2.1 Mode of Operation

For first considerations of the process of driving a kicker magnet terminated in a short-circuit, the setup is modeled as shown in the simplified equivalent circuit diagram in fig. 2.1. Both the connecting cable and the kicker magnet are represented by a lossless transmission line with the characteristic impedance Z_0. Thereby, the one-way signal propagation times in the connecting cable and the kicker magnet are τ_c and τ_k, respectively. The kicker magnet is terminated in an ideal short-circuit leading to a reflection coefficient of $R = -1$ at the end of the transmission line. The pulse generator is modeled as a voltage source with zero internal impedance.

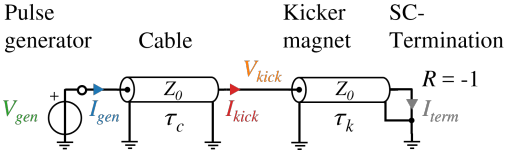


Figure 2.1: Simplified schematic of a kicker magnet terminated in a short-circuit connected to a pulse generator.

2.1.1 Wave Propagation

Figure 2.2 shows the voltages and currents in the simplified kicker system with a short-circuit termination, as shown in fig. 2.1, for a trapezoidal field pulse in the kicker magnet. For this illustration the system parameters have been chosen as follows: The nominal output voltage of the pulse generator V_0 is $10\,\mathrm{kV}$, the connecting cable and the kicker magnet both have a characteristic impedance of $Z_0 = 10\,\Omega$, and a one-way signal propagation time of $\tau_c = 200\,\mathrm{ns}$ and $\tau_k = 50\,\mathrm{ns}$, respectively. The pulse length of the generator pulse has been set to $\tau_p = 1\,\mu\mathrm{s}$: in the ideal case, this will also result in a full width at half maximum (FWHM) pulse length in the kicker magnet of τ_p.

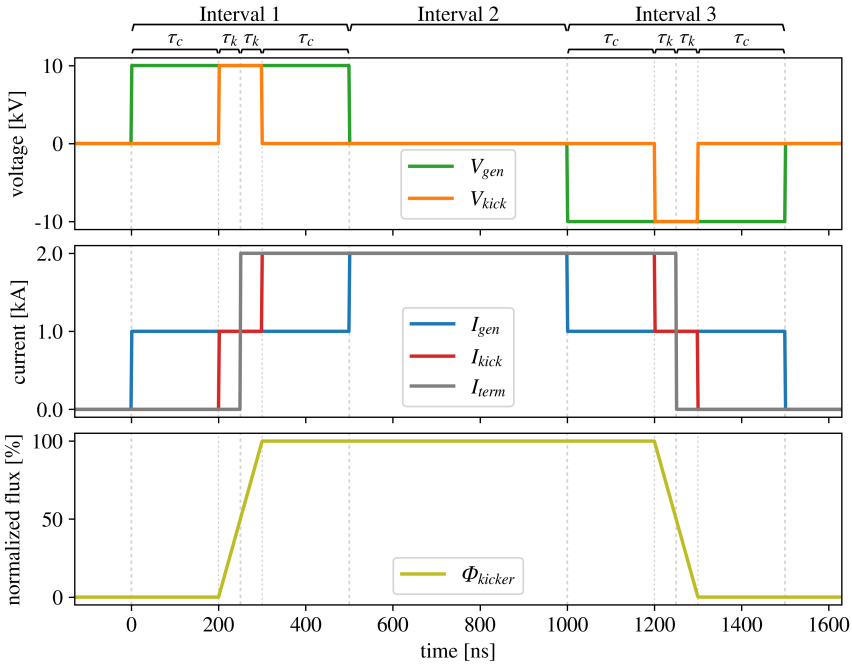


Figure 2.2: Voltages, currents and magnetic flux in an idealized kicker system with a short-circuit termination (fig. 2.1).

At the generator interface the pulse can be divided into the three intervals indicated at the top of fig. 2.2.

In the first interval, the generator outputs a voltage that travels as a wave along the connecting cable and the kicker magnet. From the view of the generator, during this interval, the load comprising the cable and kicker magnet appear as a real impedance, with a characteristic impedance Z_0, which leads to an output current of the generator of $I_{gen} = \frac{V_0}{Z_0}$. Thereby, energy is fed into the load. After the time τ_c = 200 ns the leading edge of the in-going wave reaches the input terminals of the kicker magnet, and the magnetic flux Φ_{kicker} rises as the wave propagates through the magnet. The in-going wave reaches the short-circuit termination of the kicker magnet after the time $\tau_c + \tau_k$ = 250 ns and the wave is then reflected with a reflection coefficient of $R = -1$. Where the in-going and the reflected wave superimpose, the voltage in the transmission lines adds to zero and the current $2 * \frac{V_0}{Z_0}$ flows. Once the reflected wave has passed the input terminal of the kicker magnet again (after $\tau_c + 2 * \tau_k$ = 300 ns) the full current flows in the entire magnet, and the flux in the magnet reaches its flat top value. Interval one ends, when the reflected wave reaches the pulse generator, so, the total length of this interval is $2 * (\tau_c + \tau_k)$ = 500 ns.

From the beginning of interval two on, the doubled current $I_{gen} = 2 * \frac{V_0}{Z_0}$ flows both in the kicker magnet and through the pulse generator. The generator switches the voltage at its output V_{gen} to 0 V to prevent the current from rising above $I_{gen} = 2 * \frac{V_0}{Z_0}$. Consequently, in the second interval, the pulse generator also acts as a short-circuit termination, and the traveling wave is reflected at the generator without any more energy being added. During this interval, the energy in the cable and the kicker magnet is stored as magnetic energy and is kept constant, neglecting losses.

Finally, at the end of the pulse in the third interval, after the time τ_p = 1 µs, the wave traveling in the cable and the kicker magnet is absorbed by the pulse generator. To achieve this, the generator switches to a matched impedance state at the beginning of the third interval. The voltage at the output of the generator becomes negative with respect to the first interval, while the direction of the

current remains the same. Thereby, the energy stored in the cable and the kicker magnet is extracted by the generator.

2.1.1.1 Pulse lengths shorter than the two-way signal propagation time in the connecting cable and the kicker magnet

If the desired (FWHM) pulse length τ_p is smaller than the two-way signal propagation time in the connecting cable and the kicker magnet $2 * (\tau_c + \tau_k)$ the sequence described above changes. Figure 2.3 shows the voltages, currents and flux in the kicker system for this case. The FWHM pulse length is set to $300\,\mathrm{ns}$, while $2 * (\tau_c + \tau_k) = 400\,\mathrm{ns}$.

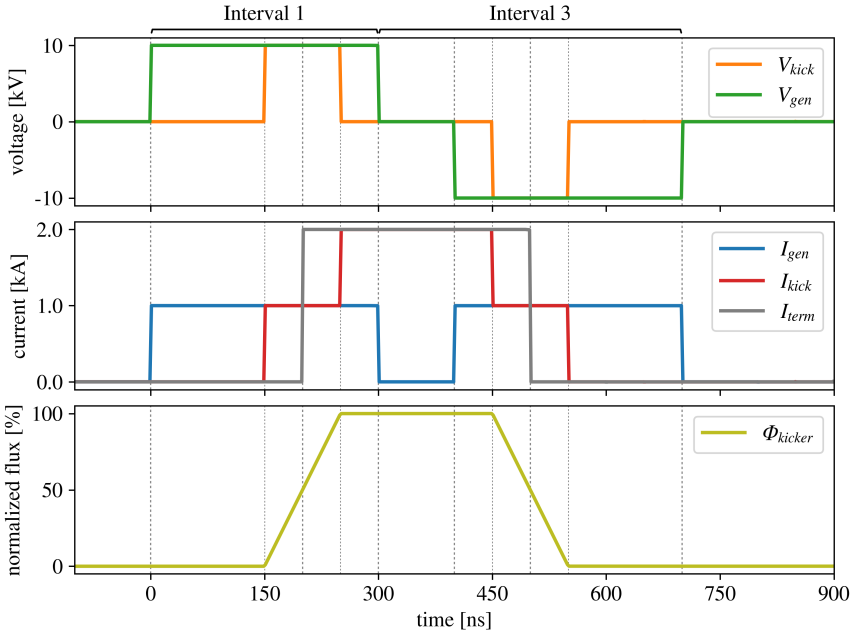


Figure 2.3: Voltages, currents and flux in an idealized kicker system with a short-circuit termination (fig. 2.1). The pulse length $\tau_p = 300\,\mathrm{ns}$ is shorter than the two-way signal propagation time in the connecting cable and the kicker magnet $2 * (\tau_c + \tau_k) = 400\,\mathrm{ns}$.

Interval one is shortened to the desired pulse length τ_p then the generator switches directly into the matched state to absorb the reflected pulse once it arrives back at the generator after $2 * (\tau_c + \tau_k)$. Interval two is skipped, so, the pulse generator does not need to conduct the doubled load current. This mode can be used as the default mode when operating an inductive adder with a short-circuited kicker magnet. However, the long cables with $2*(\tau_c+\tau_k) > \tau_p$ would be costly and lead to losses and frequency dependent attenuation of the signal [15]. Additionally, the pulse generator still needs the capability to absorb the wave reflected at the short-circuit termination via a matched state if the pulse can not be allowed to be reflected back into the kicker magnet at the pulse generator. A mismatched impedance state of the pulse generator, when the reflected pulse returns, would also lead to an increased current or voltage at the generator interface, depending on the reflection coefficient.

2.1.2 Layer Switching Pattern for an Inductive Adder in Short-Circuit Mode with a Tapered Stalk

Figure 2.4 shows a simplified simulation model of a four layer inductive adder with a tapered stalk driving a short-circuit terminated kicker magnet. The simulation results have been obtained using the circuit-simulation tool LTspice [33]. All transmission lines are considered to be lossless, and parasitic elements have been neglected. For better visualization of the timing sequence of the voltage sources driving the individual layers, shown in fig. 2.5 in the top graph, the signal propagation time τ_l between the layers was set to $10\,\mathrm{ns}$.

For the rising edge of the initial pulse, the stages need to be synchronized to the propagation of the wave from the bottom of the inductive adder stack towards the generator interface. However, for the falling edge the layers need to be switched off in reverse order, to track the reflected wave propagating from the generator interface towards the bottom of the stack. Therefore, the pulse length for the initial pulse, is not constant for the layers but must be increased in duration by two times the signal propagation time from the respective layer to the generator interface.

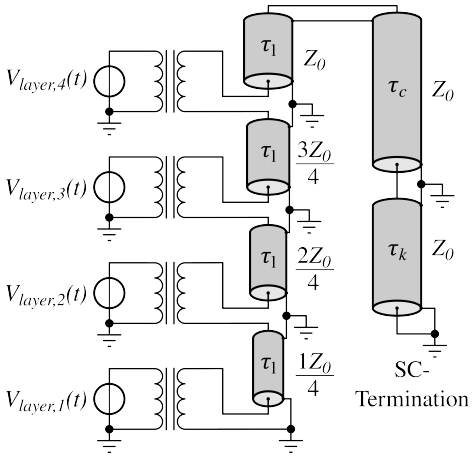


Figure 2.4: Four-layer inductive adder stack modeled as stacked pieces of transmission line with the connecting cable and the kicker magnet also modeled as lossless transmission lines.

So, in contrast to an inductive adder concept with a resistive load (1.2.2.2), a simple delay of the layer control signals is not sufficient for controlling the layers. The pattern for the layer voltages to generate the negative voltage pulse in interval three is the same as in interval one.

The bottom graph in fig. 2.5 shows the secondary voltages at each layer at the top of the respective transmission line. Thereby, $V_{sec,4}$ is the output voltage of the inductive adder. V_{kick} is the voltage at the input of the transmission line representing the kicker magnet. It can be seen how the secondary voltages at the layers add up with the propagation of the in-going and reflected waves. The simulation shows, that the rise and fall times of the voltage waveforms at the layers, the generator output and at the kicker magnet input match the rise and fall time of the primary voltage sources and no unwanted reflections occur.

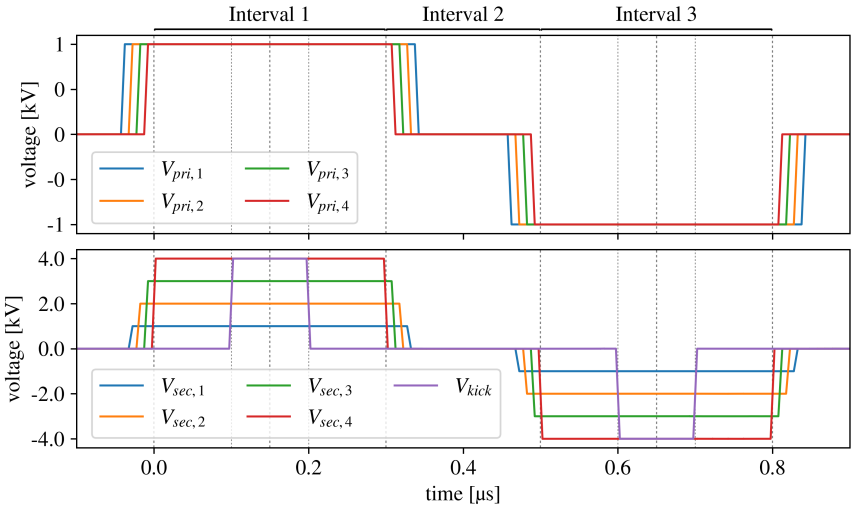


Figure 2.5: Simulation of the primary and secondary voltages for the four layer inductive adder in fig. 2.4 with the parameters $\tau_l = 10\,\text{ns}$, $\tau_c = 100\,\text{ns}$, $\tau_k = 50\,\text{ns}$, $\tau_p = 500\,\text{ns}$. The rise time of the primary voltage sources is set to 5 ns

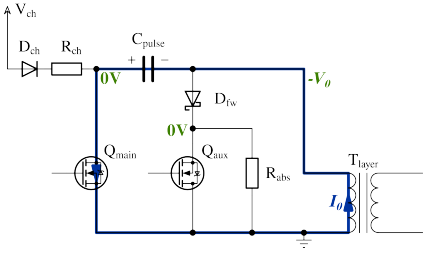
2.2 Circuit Topology for the Branch Module

Figure. 2.6 shows a first approach to a circuit topology for a branch module for an inductive adder operating with a short-circuit terminated kicker magnet. Before the beginning of the pulse the capacitor C_{pulse}, used for energy storage, is charged via D_{ch} and R_{ch}. Thereby, R_{ch} limits the charging current and D_{ch} prevents undesired discharging and current flow between branch modules charged in parallel. The switch Q_{aux} can be closed during charging to limit the voltage drop over the output transformer T_{layer} caused by the charging current. The transformer T_{layer} in fig. 2.6 represents one layer of the inductive adder, to which several branch modules are connected in parallel on the primary side. So, the circuit elements in the diagram can represent multiple paralleled components.

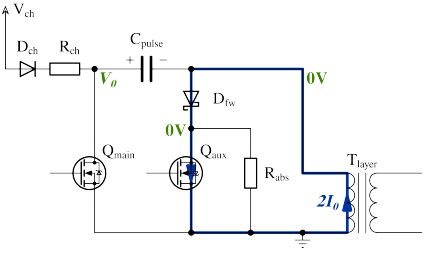
To operate in three intervals, according to the considerations in sec. 2.1.1, the topology comprises the two actively controlled MOSFET switches Q_{main} and

Q_{aux}. The current paths and voltages at the nodes of the circuit for the three intervals are highlighted in the sub-figures of fig. 2.6. To start the pulse, in the first interval, the switch Q_{main} is closed, and energy is transferred from the storage capacitor, via the output transformer T_{layer}, to the cable and the kicker magnet, as shown in fig. 2.6(a). Once the reflected wave reaches the pulse generator, the generator switches its output to zero by opening the switch Q_{main}, and closing the switch Q_{aux}. The opening of Q_{main} causes the current to commutate into the circuit branch comprised of the freewheeling diode D_{fw} and Q_{aux}. Since the output of the pulse generator is zero in the second interval, no more energy is exchanged between the generator and the cable and kicker magnet. The circuit elements that form the freewheeling current path highlighted in fig. 2.6(b) need to conduct twice the current of the first interval. The closing of Q_{aux} can already happen before the start of interval two, e.g. Q_{aux} can remain closed from the capacitor charging phase before the pulse. At the end of the pulse, in the third interval, the energy is extracted from the load: to achieve this, the pulse generator switches into a mode where it represents a matched impedance by opening the switch Q_{aux}. The energy absorbed by the generator is dissipated in the resistor R_{abs}. However, during this interval, twice the output voltage of one layer is present over the switch Q_{main} as indicated in fig. 2.6(c). The value of the capacitor C_{pulse} is chosen sufficiently large to keep the output voltage approximately constant during interval one. Consequently, during interval three at the drain terminal of Q_{main} the charging voltage of the capacitor is added to the voltage drop across R_{abs}. So, with this topology, Q_{main} needs to be designed to be capable of blocking this voltage.

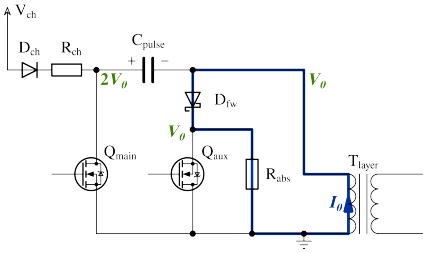
A modified topology, that avoids this disadvantage, is shown in fig. 2.7. The switch Q_{aux} and the parallel resistor R_{abs} have been moved to a position in series with the primary winding of the layer transformer T_{layer}. Hence, during the intervals two and three, the negative terminal of the capacitor C_{pulse} is clamped by D_{fw} to a potential almost equal to ground. With this modification, all circuit elements only need to withstand the output voltage of one layer. However, since the switch Q_{aux} is no longer referenced to ground an isolated gate driver is required. The charging path for the capacitor C_{pulse} now comprises the circuit elements D_{ch}, R_{ch}, and D_{fw}, which shunts the components Q_{aux}, R_{abs} and T_{layer}. In the first interval, shown



(a) Interval 1



(b) Interval 2



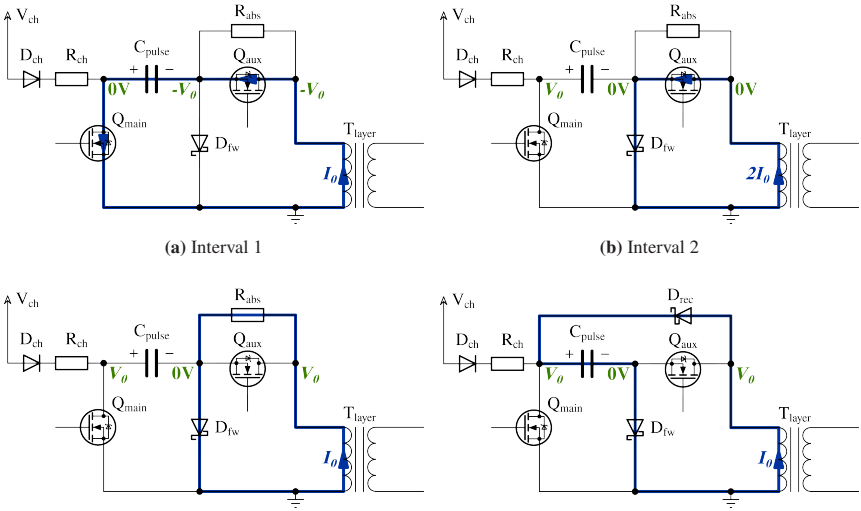
(c) Interval 3 with resistor for dissipating the absorbed energy. Q_{main} has to block twice the output voltage V_0.

Figure 2.6: Circuit topology for a branch module for an inductive adder operating with a short-circuit terminated kicker magnet. Both the switches Q_{main} and Q_{aux} are referenced to ground.

in fig. 2.7(a), both MOSFET switches Q_{main} and Q_{aux} are closed, to transfer the energy from C_{pulse} to the cable and kicker magnet. At the beginning of the second interval, the generator switches into a freewheeling mode by opening the switch Q_{main}, and the current, highlighted in fig. 2.7(b), commutates into the diode D_{fw}. As in the previous topology both the freewheeling diode D_{fw} as well as Q_{aux} need to be designed to conduct twice the current of interval one.

In the third interval, there are two variants for the pulse generator to extract the energy stored in the kicker magnet and cable [34]. The first variant shown in fig. 2.7(c) absorbs and dissipates the energy via a matched resistor R_{abs}. Figure 2.7(d) shows the second variant, where the stored energy is instead absorbed by recuperating it into the pulse capacitor C_{pulse} via the diode D_{rec}. The first and

second intervals are the same for both variants. Neither variant requires any component to withstand more than the charging voltage V_{ch}.



(a) Interval 1

(b) Interval 2

(c) Interval 3 with a resistor R_{abs} for dissipating the stored energy

(d) Interval 3 with a diode D_{rec} for recuperating the stored energy

Figure 2.7: Modified topology with one ground referenced switch Q_{main} and one floating switch Q_{aux}. All circuit elements only need to withstand the output voltage V_0 of one layer.

2.2.1 Inaccuracy in Timing

2.2.1.1 Inaccuracy in switching time

During the first interval, the main switch is closed, to transfer energy into the kicker magnet and the connecting cable. Thereby, the turn off of Q_{main} must coincide precisely with the arrival of the reflected wave, and therefore, twice the one-way signal propagation time in the kicker magnet and the cable. Inaccuracy in this switching time will result in an unwanted energy exchange between the pulse generator and the load. Figure 2.8 depicts a circuit simulation [33] where delaying

the switch-off of the generator's output voltage by $5\,\mathrm{ns}$ after the reflected wave arrives at the generator injects additional energy into the load. The model for the simulation is the same as shown in fig. 2.1 with the system impedance being $10\,\Omega$, and a one-way signal propagation time of $150\,\mathrm{ns}$ for the connecting cable, and $50\,\mathrm{ns}$ for the kicker magnet. The delay causes a unipolar voltage and current spike to travel through the kicker magnet and cable, which is repeatedly reflected at both the generator and the short-circuit termination during the second interval. While traveling through the kicker magnet, this spike causes an unwanted increase of the magnetic flux in the magnet by $5\,\%$ for the example shown in fig. 2.8. Hence, precise timing of the turn-off moment of $\mathrm{Q_{main}}$ is crucial [35]. In this simulation the transmission line is driven by an ideal voltage source with a negligibly small inner impedance in all intervals as shown in fig. 2.1, like when using the topology variant with recuperation of the absorbed energy in the third interval. Thereby, no true matched impedance state absorbs the reflected pulse, instead, it is countered by a fixed voltage. Any differences to this voltage in the reflected pulse are reflected back into the load. Therefore, the disturbances in the wave traveling inside the load caused by inaccuracies in switching times, are not absorbed and persist after the end of interval three.

2.2.1.2 Influence of the slopes

With the kicker magnet and cable modeled as ideal transmission lines terminated in a short-circuit, the absolute rise and fall times of the pulse generator's output voltage waveform V_{gen}(t) do not lead to perturbations in the magnet's flux, if the slopes in $V_{gen}(t)$ are matched to each other. However, if the rise and fall times at the beginning and end of interval one or three are different, the difference in the generator's output voltage waveform, and the waveform of the reflected wave leads to perturbations being emitted back towards the kicker magnet. In the simulation in fig. 2.9, the rise time of the output voltage $V_{gen}(t)$ at the beginning of interval one is $10\,\mathrm{ns}$, while the fall time at the end of interval one is $20\,\mathrm{ns}$, with the switching processes centered on the ideal times.

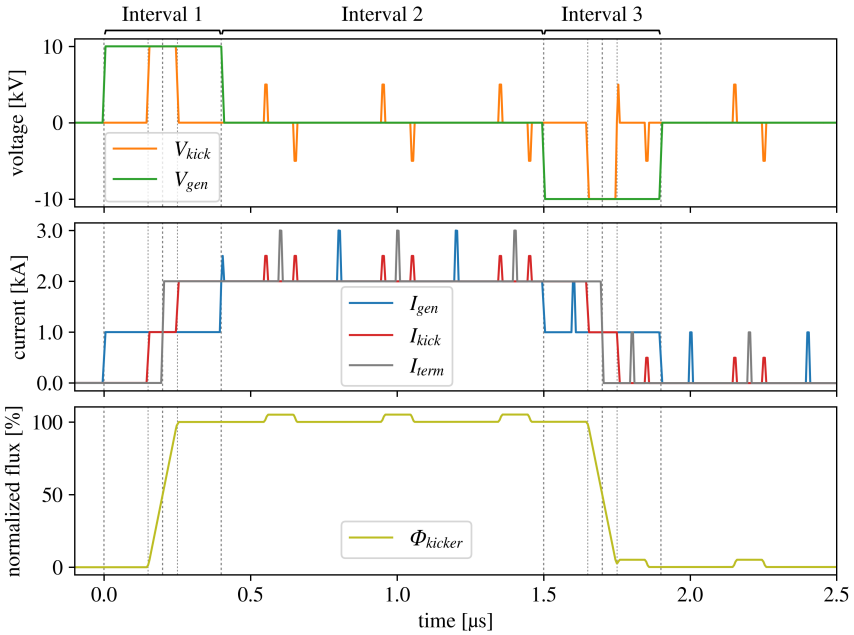


Figure 2.8: Inaccuracy in switching time: Turn off of the switch at the end of interval one is delayed by 5 ns

The simulation shows that a mismatch between the slope of the returning wave at the end of the first interval and the falling edge of $V_{gen}(t)$ causes a bipolar and symmetric disturbance in the wave traveling through the kicker magnet and cable. In the lossless case, the magnetic flux $\Phi_{kicker}(t)$ inside a kicker magnet terminated in an ideal short-circuit is proportional to the integral of the voltage $V_{kick}(t)$ on its input terminal (eq. 1.4). Due to their bipolar and symmetric nature, the disturbances in the traveling wave only cause perturbations in the flux $\Phi_{kicker}(t)$ as they are passing the input terminal of the magnet. For the example shown in fig. 2.9 the perturbations in $\Phi_{kicker}(t)$ have a magnitude of $\pm 1.2\,\%$. So, the impact of a mismatch in the rise and fall times is well mitigated by the integrating behavior of the kicker magnet. For the auxiliary switch Q_{aux}, the timing of the turn on is not critical as it can be turned on before the pulse starts. It stays on during the first interval and the freewheeling phase in interval two. The

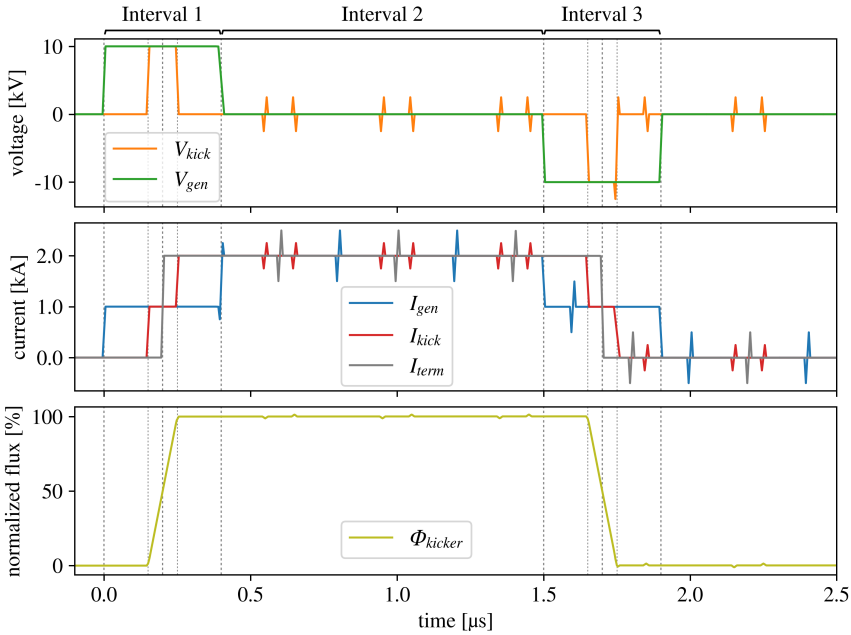


Figure 2.9: Different rise- and fall time in interval one: rise time 10 ns, fall time 20 ns

turn off of Q_{aux} determines the end of the pulse and leads to the extraction of the energy.

2.2.2 Loss Compensation

Losses in the system comprising the pulse generator and the load consisting of the connecting cable and the kicker magnet have not been considered so far. However, if there is no more energy fed into the load in the second interval, the unavoidable losses in the system lead to a decrease in the magnetically stored energy and, thereby, the current circulating in the system. Figure 2.10 shows a simplified simulation model with the cable and kicker magnet modeled as lossy transmission lines T_{cable} and T_{kicker}. In interval one and two, the switch Sw_1 is closed and the load is driven by a voltage source $V_1(t) = 1\,\mathrm{kV}$ in interval one, and

$V_1(t) = 0\,\mathrm{V}$ in interval two. In interval three, $\mathrm{Sw_1}$ is opened and the resistor $\mathrm{R_{abs}}$, of $10\,\Omega$, matching the characteristic impedance of the connecting cable $\mathrm{T_{cable}}$ and the kicker magnet $\mathrm{T_{kicker}}$, is used to absorb the energy in the load. The losses in the pulse generator are represented by a the resistor $\mathrm{R_{gen}}$ with a resistance of $100\,\mathrm{m}\Omega$.

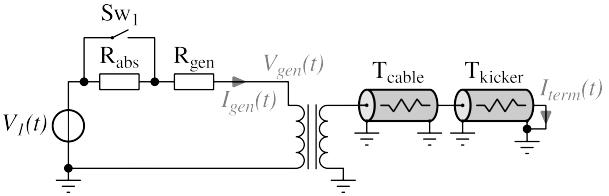


Figure 2.10: Simulation model with the connecting cable $\mathrm{T_{cable}}$ and the kicker magnet $\mathrm{T_{kicker}}$ modeled as lossy transmission lines [33].

A simulation of the current at the generator and at the kicker termination is shown in fig. 2.11. To represent $\mathrm{T_{cable}}$ and $\mathrm{T_{kicker}}$, LTspice's lossy transmission line model [33] with frequency-independent distributed elements is used. The distributed elements have been set to $R' = 7.7\,\mathrm{m}\Omega\,\mathrm{m}^{-1}$, $L' = 41.5\,\mathrm{nH}\,\mathrm{m}^{-1}$ and $C' = 420\,\mathrm{pF}\,\mathrm{m}^{-1}$. These values correspond to five $50\,\Omega$ coaxial cables of type CK50 [36] connected in parallel at an operating frequency of $1\,\mathrm{MHz}$, which are later used as a replacement load for measurements (sec. 4.1). The lengths of the transmission line models in the simulation are set to $36\,\mathrm{m}$ for $\mathrm{T_{cable}}$ and $12\,\mathrm{m}$ for $\mathrm{T_{kicker}}$.

For considering the compensation of the loss induced degradation of the current waveform, it is useful to divide the attenuation of the pulse shape into two categories. The "flattop current" in the second interval is made up of back-to-back reflections of the pulse shape injected into the connecting cable and the kicker magnet in the first interval. While traveling through the connecting cable and the kicker magnet, this pulse shape can be altered by non-linear and frequency-dependent losses. Deviations from an ideal trapezoidal pulse of the pulse shape of the wave traveling in the system at the end of the first interval result in a ripple in the flattop current in the second interval with a periodicity of the two-way signal

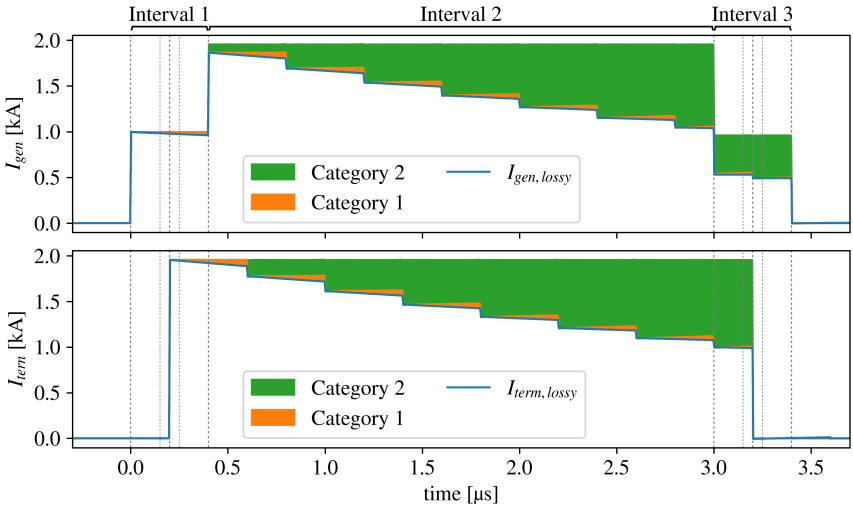


Figure 2.11: Simulation of the degradation of the current waveform at the generator and the kicker termination with the cable and kicker modeled as lossy transmission lines.

propagation time in the cable and the kicker magnet. These effects, which make up category one, are highlighted in orange in fig. 2.11.

In the second category, highlighted in green in fig. 2.11, are the effects of linear ohmic losses, dependent on the DC-bulk of the flattop current and proportional to the total current. These losses cause the current to decrease stepwise with each round trip of the traveling wave. Thereby, any ripple, part of category one, superimposed on this bulk DC current is assumed to be negligibly small compared to the total current. The losses of category two can be compensated by applying a constant voltage of the same sign as in the first interval to the load during the second interval [37].

Figure 2.12 shows a simulation of the current flowing in the system for different driving voltage waveforms $V_{gen}(t)$. The simulation model is the same as in fig. 2.11.

The simulation shows, that injecting a constant voltage into the load during the second interval (loss comp. 2) serves to compensate the step wise decrease in the

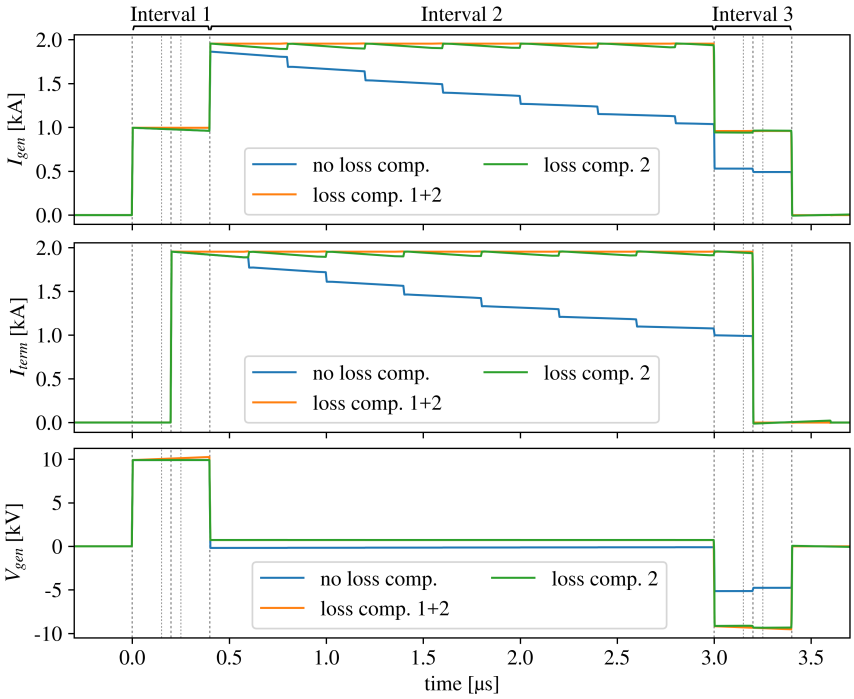


Figure 2.12: Simulation with the cable and kicker modeled as frequency independent lossy transmission lines driven by the ideal voltage waveform for the lossless case (blue), with an additional DC voltage injected during interval two (green), and with an additional slope in the first interval (orange).

current, leaving only a ripple in the flattop, caused by the attenuation of the shape of the traveling wave during the first interval.

For the system in this simulation, this remaining ripple can be compensated as well, by countering the deterioration of the waveform incurred during the first round trip of the wave in interval one. Adding a rising slope of the right magnitude to the voltage in interval one, as shown in fig. 2.12 (loss comp. 1+2), makes the first reflection of the wave square shaped. For the following circulations of the traveling wave, as the current is constant, the losses are constant as well, and can be compensated by a constant voltage in the second interval.

The lossy transmission line model of LTspice does not model the frequency dependent attenuation of signals existing in a real transmission line. Therefore, for a more complete picture of the behavior of such a system, the replacement load of five paralleled type CK50 coaxial cables (T_{cable} and T_{kicker}) was modeled including frequency dependent changes in the distributed elements as described in [38]. Thereby, the interpolation points for the values for L', C', R' and G' part of the model were determined using a 2D field simulation of the coaxial geometry of the cable with appropriate material parameters. Figure 2.13 shows a simulation using the more complete simulation model for the connecting cable and the kicker magnet.

The frequency-dependent attenuation of the waveform traveling in the cable results in a lowpass-like degradation of the leading edge of the pulse on its first pass through the transmission line. As in the previous simulation, the loss in current with each round trip is approximately proportional to the total current and can be compensated with a constant voltage in interval two (loss comp. 2). The remaining ripple in the current flattop represents high-frequency signal components and is attenuated by losses that increase with frequency as the wave travels in the transmission line. The compensation of the remaining ripple by countering the effect of the load on the waveform at the generator output is more complex than in the previous case. To achieve a good flat top in the load current in interval two along the transmission line, a compensation voltage has to be applied both in the first interval, as well as for one round trip time after interval one, during the first reflection of the wave at the pulse generator. However, depending on the losses and the frequency response of the system as well as the requirements for the flat top stability, simple compensation via a constant voltage in interval two may be sufficient.

2.2.2.1 Application of loss compensation with an inductive adder

There are two obvious approaches to output a low constant compensation voltage during the second interval with an inductive adder. The first option is an extension of the branch module topology for all the normal layers of the inductive adder,

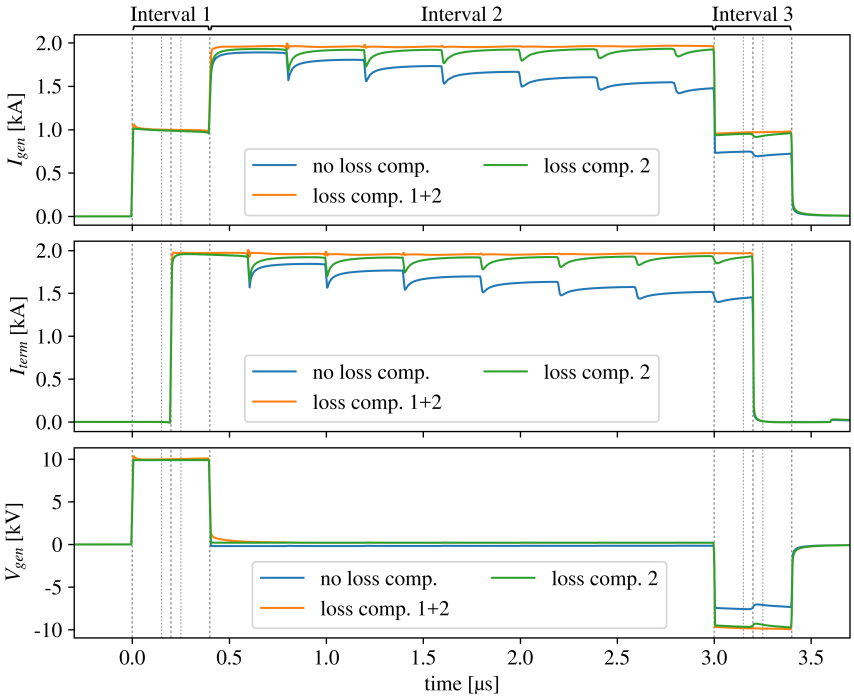


Figure 2.13: Simulation with the cable and kicker modeled as lossy transmission lines (T_{cable} and T_{kicker}) with frequency dependent distributed elements. The load is driven in three variants: by the ideal voltage waveform for the lossless case (blue), with an additional DC voltage injected during interval two (green), and with an additional compensation for the frequency dependent attenuation of the waveform (orange).

so that an additional lower output voltage can be provided. A possible topology for such an extended branch module is shown in fig. 2.14. It has an additional circuit branch comprising switch Q_{comp}, diode D_{comp} and capacitor C_{comp}. By switching on Q_{comp} during interval two, the voltage of C_{comp} is provided at the output. Therefore, this additional circuit branch needs to conduct the doubled load current. C_{comp} is charged to an appropriate negative voltage via $D_{ch,comp}$ and $R_{ch,comp}$. D_{comp} prevents a short-circuit when both Q_{main} and Q_{comp} are on. Q_{main} has to be able to block the sum of the voltages of C_{comp} and C_{pulse}, Q_{comp} only needs to block the voltage of C_{comp}.

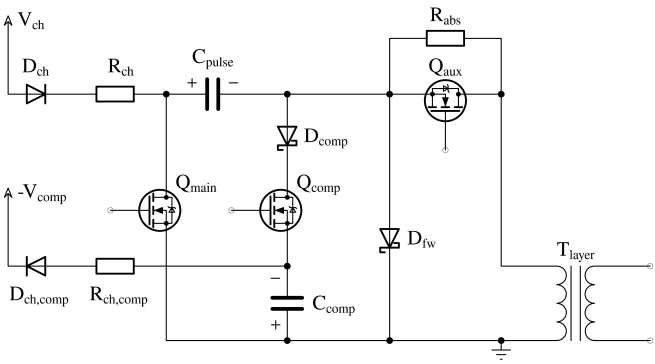


Figure 2.14: Branch module topology with third switch (Q_{comp}) and energy storage (C_{comp}) for applying a compensation voltage during interval two.

However, this extended topology makes the circuit of the branch module more complex, and requires an additional control signal and supply voltage for each layer.

The second approach is to inject the compensation voltage via one or more separate dedicated layers of the inductive adder. The branch modules of these layers can have the same topology as for an inductive adder operating with a terminated load. The voltage time integral of the compensation voltage has to be considered in the design of the magnetic cores of the inductive adder (see section 2.3). For the total additional magnetic core cross-sectional area or energy storage required, it does not matter whether the compensation voltage is introduced distributed over many layers or a few dedicated layers. Therefore, the trade-off is between the increased complexity of the pulse circuit and the need for more layers in the inductive adder setup for loss compensation. For the investigations presented in this work, loss compensation via a separate layer has been chosen as the simpler and more flexible approach. The compensation of the remaining flattop ripple with frequency-dependent losses requires complex arbitrary voltage waveforms. The active modulation layers presented in [39] might serve for this purpose.

2.3 Magnetic Core Requirements for an Inductive Adder in Short-Circuit Operation

Normally in an inductive adder driving a kicker magnet, the required pulse length is one of the main driving parameters for the required size of the magnetic cores [15]. A first estimation of the required effective cross section of the core A_{Fe} can be obtained according to eq. 2.1 with the maximum of the integral of the output voltage over time $V_{IA,layer}(t)$, of one layer of the inductive adder and the available magnetic flux density swing of the core ΔB_c.

$$A_{Fe} = \frac{\max(\int V_{IA,layer}(t)dt)}{\Delta B_c} \tag{2.1}$$

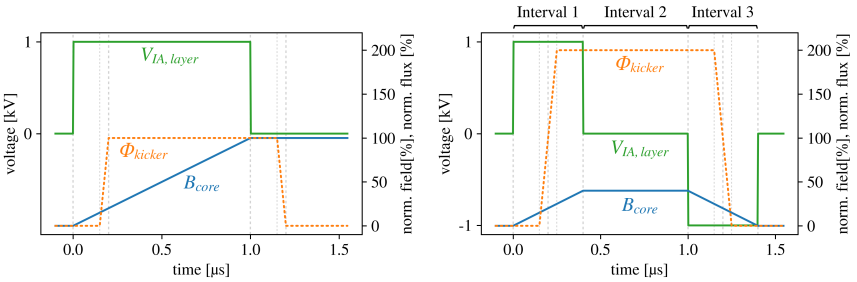
With an inductive adder operating into a load with a matched termination and a rectangular output pulse shape this leads to eq. 2.2 with the charging voltage of the layer V_{ch} and the full width half maximum pulse length of $\tau_{p,FWHM}$ of the output pulse.

$$A_{Fe,term} = \frac{V_{ch} * \tau_{p,FWHM}}{\Delta B_c} \tag{2.2}$$

Figure 2.15 shows two idealized simulations, one for an inductive adder with a matched impedance terminated kicker magnet, and one for a short-circuit terminated kicker magnet, both with a FWHM pulse length of the field in the kicker magnet of $1\,\mu s$. Both are using the same parameters for the kicker magnet with a one-way delay τ_k of $50\,\mathrm{ns}$ and the connecting cable with a one-way signal propagation time τ_c of $150\,\mathrm{ns}$. The flux density B_{core} is calculated from eq. 2.3, with the effective cross section A_{Fe} of the core being the same for both simulations and assumed to be constant. The flux density in the core at the beginning of the pulse $B_{core}(0)$ is assumed to be zero.

$$B_{core}(t) = \frac{\int V_{IA,layer}(t)dt}{A_{Fe}} + B_{core}(0) \tag{2.3}$$

As can be seen in fig. 2.15(a), the flux density in the core increases over the entire duration of the pulse to a much higher magnitude than in 2.15(b). For the short-circuit terminated case (fig. 2.15(b)), since the output voltage is zero during the second interval, the magnetic field of the core does not increase during this part of the pulse. Only in the first interval there is an output voltage, that increases the magnetic field in the cores. The length of the first interval is twice the one-way signal propagation time in the kicker magnet and the cable connecting the kicker magnet to the generator.



(a) Kicker magnet terminated in a matched impedance.

(b) Kicker magnet terminated in a short-circuit.

Figure 2.15: Idealized simulations of the magnetic flux density and the magnetic flux in the kicker magnet.

So, with this mode of operation, in the lossless case, the required size of the magnetic cores is not determined by the length of the pulse, but two times the sum of the one-way signal propagation times in the kicker magnet τ_k and the connecting cable τ_c, as shown in eq. 2.4.

$$A_{Fe,SC} = \frac{V_{ch} * 2 * (\tau_c + \tau_k)}{\Delta B_c} \tag{2.4}$$

Since these signal propagation times can be much shorter than the typical pulse length requirements for kicker systems at CERN (e.g. 1.6 µs flattop duration and $2 * (\tau_c + \tau_k) \approx 412\,\text{ns}$ for KFA10 in table 1.1), this mode of operation offers

the advantage of allowing for smaller cheaper magnetic cores for a given required pulse length.

Some dependence of the required core size for the respective layers on the pulse length is introduced by the compensation of losses via a DC voltage in interval two, as it adds a DC component to the output voltage of the inductive adder in short-circuit mode. However, this dependence is still much less than for the terminated mode, as only the losses in the system need to be compensated.

2.3.1 Pulsed Magnetisation of Nanocrystalline Tapewound Magnetic Cores

Both for an inductive adder in terminated mode, as well as in the first interval in short-circuit mode, the magnetic cores are magnetized by unipolar rectangular voltage pulses. To have the full flux density swing from positive to negative saturation available, the core can be biased towards the opposite saturation flux density by driving a current through a winding around the core [17]. Different options for magnetic cores were investigated in [15] and a nanocrystalline tapewound core with a square shaped BH-curve was selected as best suited for inductive adder applications at CERN. The custom made VAC T60009-L2282-V387 core [40] has been selected for its steep square shaped BH-loop, very high remanent magnetization and large saturation flux density. It is a toroidal core with a rectangular cross section and a height of $30\,\mathrm{mm}$, an outer diameter of $282\,\mathrm{mm}$ and an inner diameter of $146\,\mathrm{mm}$. The ribbons making up the core are made from Vitroperm 500Z alloy and have a thickness of $20\,\mu\mathrm{m}$.

2.3.1.1 Bias current

The required magnetomotive force to saturate the core depends on its reluctance and, thereby, the geometry and the material parameters of the core. Figure 2.16 shows the achievable change in core flux for a core driven by a rectangular voltage pulse for different applied DC bias currents. The bias current was driven by a DC

power supply through a dedicated secondary winding around the core. A toroidal air coil with an inductance of 1.9 mH was used to provide transient insulation between the DC power supply and the voltage induced in the secondary winding during the pulse.

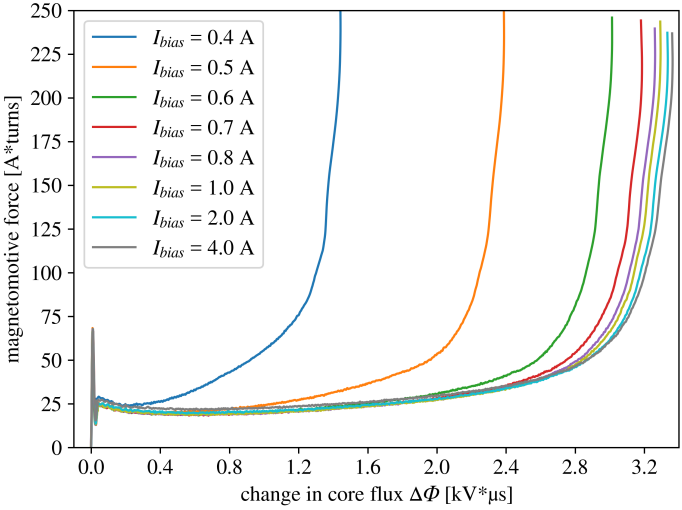


Figure 2.16: Magnetomotive force vs. change of magnetic flux in the core for different DC bias currents. The core is driven by a rectangular voltage pulse of 1 kV.

As the pulse is applied, the biasing current, imposed by the 1.9 mH inductor, flows through the pulse source, which leads to a higher primary current for higher biasing currents before the onset of saturation effects. Increasing the biasing current above 1 A only provides marginal gain in the available voltage time integral. Based on these measurements, considering some margin for parameter tolerance and inaccuracy, a bias current of 1 A was chosen as a good compromise between losses due to the current flow and available $\Delta\Phi$.

The bias current can be applied via a secondary winding passing through all layers, either the stalk [41], or a dedicated secondary winding [39], and a large inductance as transient insulation. Since the biasing current sources are exposed to the layer

voltage of the layers through which their current flows, with this arrangement, this insulation inductance needs to withstand the full output voltage of the inductive adder. By using one smaller inductance per layer, and applying the bias current per layer via the primary winding, the insulation requirements for the biasing inductors can be reduced to the layer voltage. However, an independent current source for each layer would be required.

2.3.1.2 Magnetisation rate

To qualify the cores for the intended application they have been tested with a unipolar pulsed excitation using rectangular pulses at different voltages. The primary current was measured using a shunt resistor and the flux in the core was determined by integrating the voltage of a secondary winding via an RC-integrator with a time constant of 10 ms.

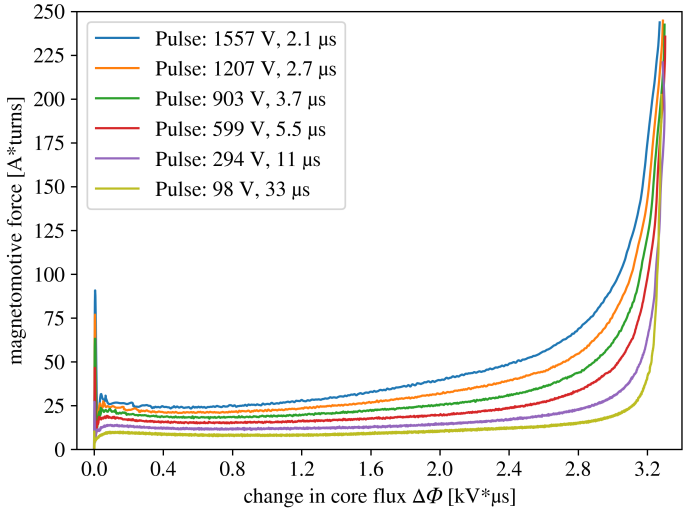


Figure 2.17: Magnetomotive force vs. change of magnetic flux in the core when the core is driven by rectangular pulses of different voltages. The core is biased towards negative saturation with a constant current of 1 A.

The shape of the flux versus magnetomotive force response of the magnetic core, shown in fig. 2.17, changes significantly with magnetization rate [42]. The change of the core response is caused by a displacement of the magnetic field from the individual ribbons of which the core is composed, due to eddy currents induced by the change in magnetization. Thus, the magnetic cross-sectional area becomes available only gradually during the pulse, with the progression of the magnetisation into the ribbons from the outside in [43]. Both the initial step in the magnetizing current and the steepness of the rise in the flat pre-saturation region of the curve increase with higher magnetization rate. These effects can be attributed to increased losses due to the establishment, and eddy current controlled movement, of magnetic domain walls [44]. However, the voltage time integral, for which the core approaches saturation is nearly constant at $3.3\,\mathrm{kV\,\mu s^{-1}}$ for the considered magnetization rates.

2.3.1.3 Remanent magnetisation

The selected core has a high remanent magnetization close to the saturation flux density. This magnetic memory of the core allows for alternative biasing schemes, where the biasing is done separated in time e.g., using a switch for disconnecting the biasing current source before the start of a pulse. This way, the relatively bulky inductors for transiently insulating the bias power supplies may be avoided. Figure 2.18 shows a comparison between pulses with a continuous DC biasing current of $1\,\mathrm{A}$ applied during the pulse, and a corresponding pulse where the biasing was switched off five minutes before the application of the pulse.

The comparison shows, that turning off the biasing before the pulse makes very little difference in the available voltage time integral, and without excitation, the core remains very close to its last state. However, this behavior makes a reset of the core essential, as the core does not return to a demagnetized state on its own.

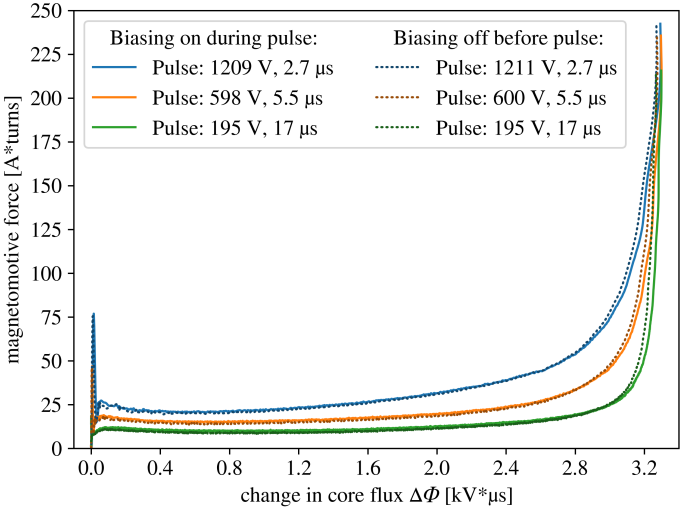


Figure 2.18: Comparison of magnetomotive force vs. change of magnetic flux in the core for a continuous bias current of 1 A applied during the pulse (solid lines) and a bias current of 1 A applied before the pulse but turned off 5 min before applying the pulse (dotted lines). The core is driven by rectangular voltage pulses.

2.3.1.4 Pulse repetition rate and biasing in short-circuit mode

In an inductive adder operating with a terminated load, outputting unipolar pulses, the resetting of the magnetic cores is a limiting factor in the achievable pulse repetition rate [41]. After the pulse the magnetizing current flowing in the primary windings has to decay. The time at which this magnetizing current decays is determined by the voltage $V_{reset}(t)$, with opposite polarity compared to the preceding pulse, over the layer transformer. Normally, in a solid state inductive adder this voltage depends on voltage drops caused by the magnetizing current over parasitic resistances and a freewheeling diode part of the primary pulse sources. Since the sum of these voltages over each layer also appears at the output of the inductive adder, the post pulse ripple requirements may limit how fast the core can be demagnetized. After the decay of the magnetizing current, the same limitations apply for the voltage necessary to drive the biasing current for bringing the core into a state ready for the next pulse. To bring the core into the same

magnetic state as before the pulse, the voltage time integral of the pulse, and the voltage with opposite polarity after the pulse have to be equal [41].

For the inductive adder operating in short-circuit mode, the total voltage time integral of the layer voltage waveform (neglecting loss compensation) is close to zero (fig. 2.15(b)). Therefore, the magnetic state of the core before and directly after the pulse is approximately the same. When using a core with a high remanent magnetization, the core can remain near the opposite saturation between pulses even without biasing. For initially bringing the core into a defined state, and to avoid drift in the pre-pulse core magnetisation, biasing may nevertheless be useful. However, neglecting losses, the requirements for the core reset voltage $V_{reset}(t)$ does not restrict the duty cycle of the inductive adder in short-circuit mode operation.

2.3.2 Influence of Magnetic Core Parameters During Lossy Energy Absorption from the Load

As a first approximation, the output transformer of each layer of the inductive adder can be modeled as its magnetizing inductance $L_{mag,layer}$ and a parallel resistor $R_{coreloss,layer}$, modeling core losses, parallel to an ideal transformer [45]. When using a resistor R_{abs} in the third interval to absorb the energy at the end of the pulse, these elements are not driven by a low impedance source, and can therefore have an effect on the output voltage of the inductive adder. Figure 2.19 shows a simplified simulation model for estimating the influence of magnetic core parameters in an inductive adder with matched impedance state.

The simulation model uses lossless transmission lines to model the connecting cable and the kicker magnet: the inductive adder is modeled as a voltage source in the first two intervals and a matched resistance R_{abs} in the third interval. Thereby, the circuit elements of the individual layers are assumed to be equal, and have been lumped together for the simulation model. The voltage source $V_1(t)$ provides the layer voltage times the number of layers in interval one and $0\,\mathrm{V}$ after interval one. The resistor $R_{abs} = Z_0$ represents the absorbing resistor distributed equally over

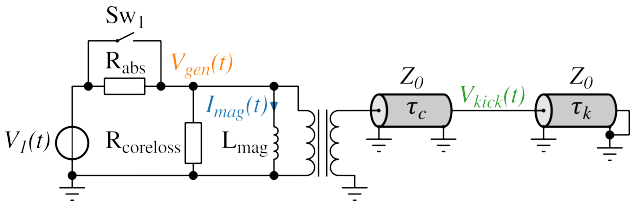


Figure 2.19: Simulation model for estimating the influence of magnetic core parameters in an inductive adder with matched impedance state

the layers; the magnetizing inductance has a value of $L_{mag} = N_{layers} * L_{mag,layer}$ to represent the series connection of the magnetizing inductances of the output transformer of each layer, and $R_{coreloss} = N_{layers} * R_{coreloss,layer}$ represents the core losses of all layers connected in series.

2.3.2.1 Core losses

In interval three, the absorbing resistor R_{abs} is used to match the inductive adder to the characteristic impedance Z_0 of the cable and kicker magnet. The resistor representing core losses, $R_{coreloss}$, is then parallel to R_{abs} and reduces the impedance the inductive adder represents. As shown in section 2.3.1.2, the core losses and, thereby, the value of R_{abs}, depend on both the magnetization rate, and the closeness of the core to saturation. Therefore, by increasing the absorbing resistor, so that $R_{abs}||R_{coreloss} = Z_0$ only the portion of the impedance mismatch caused by core losses that is constant for the intended operating range of the inductive adder can be compensated.

The equivalent core loss resistance for one core estimated from the initial current step, in relation to the excitation voltage in the measurements shown in fig. 2.17, is $25\,\Omega$ at a pulse voltage of $294\,\mathrm{V}$, $39\,\Omega$ at $599\,\mathrm{V}$, and $47\,\Omega$ at $1207\,\mathrm{V}$. As a worst-case estimate for the dynamics of the core loss equivalent resistance, the entire current flow in fig. 2.17 after a pulse with a voltage time integral of $2.4\,\mathrm{kV\,\mu s}$ is interpreted as caused by core losses (although in reality a considerable amount of magnetization current is present). Thereby, the voltage time integral of $2.4\,\mathrm{kV\,\mu s}$ has been chosen as a possible working range for the magnetization of the core.

With this estimate, the equivalent core loss resistance for one core decreases to $25\,\Omega$ at a pulse voltage of $294\,\mathrm{V}$, $18\,\Omega$ at $599\,\mathrm{V}$, and $31\,\Omega$ at $1207\,\mathrm{V}$ by the end of the pulse. The resistor $\mathrm{R_{abs}}$ for absorbing the energy at the end of the pulse is equally distributed over the layers. Therefore, as the fraction of $\mathrm{R_{abs}}$ per layer is lower for a higher number of layers, a given core loss equivalent resistance per core has less impact with a lower system impedance or a higher number of layers. For a 30-layer inductive adder and a system impedance of $12.5\,\Omega$ the absorption resistance per layer is $0.42\,\Omega$ in the ideal case without core losses. With the core loss resistance estimated from the first current step taken into account in the dimensioning of the absorption resistor, the dynamics of the core losses as per the values above, would change the impedance of the generator between $0.6\,\%$ and $0.7\,\%$ as the pulse progresses. This is within acceptable tolerances for the matched state of the pulse generator in interval three.

2.3.2.2 Magnetizing inductance

Figure 2.20 shows a simulation for visualizing the effects of the magnetizing inductance on the output voltage of the inductive adder and the flux in the kicker magnet, when using an absorption resistor in interval three. For the simulation in fig. 2.20 the parameters were set to Z_0 = $10\,\Omega$, L_{mag} = $50\,\mu\mathrm{H}$, τ_c = $150\,\mathrm{ns}$, τ_k = $50\,\mathrm{ns}$ and $V_{gen}(Interval\ 1)$ = $1\,\mathrm{kV}$. For these considerations, $R_{coreloss}$ is assumed to be constant, and combined with R_{abs} so that $R_{abs}||R_{coreloss} = Z_0$. The output voltage of the inductive adder during the first interval V_{gen} causes a magnetizing current $I_{mag}(t)$ in the magnetizing inductance L_{mag} of the output transformers according to eq. 2.6, assuming $I_{mag}(0) = 0$.

$$I_{mag}(t) = \frac{\int V_{gen}(t)dt}{L_{mag}} + I_{mag}(0) \tag{2.5}$$

The magnetizing current reaches its maximum $I_{mag,max}$ (eq. 2.6) at the end of the first interval.

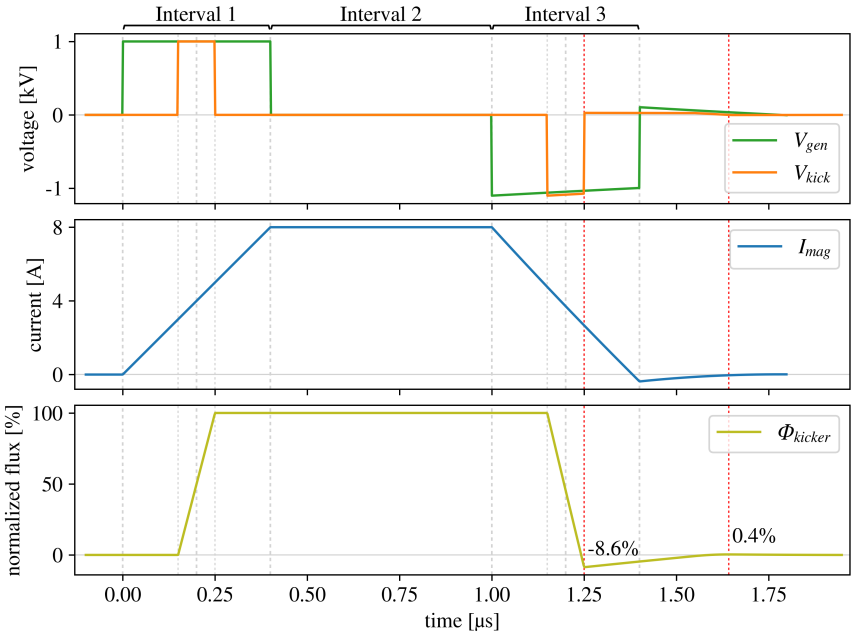


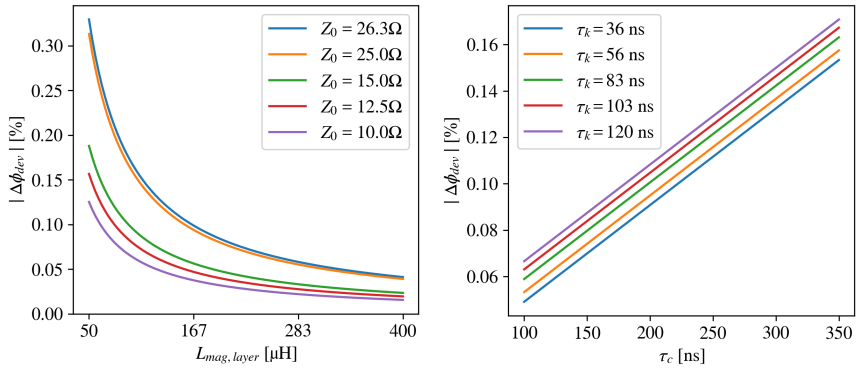
Figure 2.20: Perturbations caused by the magnetizing current after the nominal end of the pulse. Extreme case for visualization: $Z_0 = R_{abs}||R_{coreloss} = 10\,\Omega$, $L_{mag} = 50\,\mu H$, $\tau_c = 150\,ns$, $\tau_k = 50\,ns$, $V_{gen}(Interval\ 1) = 1\,kV$

$$I_{mag,max} = \frac{V_{gen}(Interval\ 1) * 2 * (\tau_c + \tau_k)}{L_{mag}} \tag{2.6}$$

In interval two, where the voltage over L_{mag} is approximately zero, $I_{mag}(t)$ remains near $I_{mag,max}$. As a consequence, in interval three, $I_{mag}(t)$ causes an additional voltage drop over R_{abs} which superimposes a downward ramp shaped over-voltage on the output voltage of the generator. This results in an additional energy transfer to the load, and, subsequently, perturbations, i.e. the deviation of the flux Φ_{kicker} from the ideal case shown in fig. 2.2, after the nominal end of the pulse. With these parameters the magnetic flux in the kicker magnet, calculated from integrating the voltage at the input terminals of the kicker magnet according to eq. 1.4, exhibits an undershoot of $8.6\,\%$. With the simplified model considered

here, the relative magnitude of this undershoot decreases with a lower system impedance, a higher total magnetizing inductance or lower signal propagation times in the kicker magnet and the connecting cable.

In order to study different cases in a realistic parameter range, the absolute value of the deviation of the flux from the ideal case $|\Delta\phi_{dev}|$ is considered. To estimate if the perturbations of the magnetic flux in the kicker magnet caused by the magnetizing inductance need to be addressed, fig. 2.21 shows $|\Delta\phi_{dev}|$ simulated for a range of the relevant parameters. A realistic value for the magnetizing inductance L_{mag} of the core between $160\,\mu\text{H}$ and $367\,\mu\text{H}$ is presented in [15]. It has been derived from BH-curve measurements with low magnetisation rate. To account for a possible reduction of L_{mag} due to a higher magnetization rate or possible parameter variations for other reasons, in the simulation in fig. 2.21 the parameter range for L_{mag} has been extended to span an interval between $50\,\mu\text{H}$ and $400\,\mu\text{H}$. Since the simulation in fig. 2.20 is based on a parameter set in an extreme range to obtain a large perturbation with a $|\Delta\phi_{dev}|$ of $8.6\,\%$ in the realistic cases shown in fig. 2.21 the deviation $|\Delta\phi_{dev}|$ is much smaller.



(a) $R_{abs}||R_{coreloss} = Z_0$, fixed parameters: $\tau_c = 170\,\text{ns}$, $\tau_k = 36\,\text{ns}$, $N_{layers} = 30$

(b) fixed parameters: $R_{abs}||R_{coreloss} = Z_0 = 12.5\,\Omega$, $L_{mag,layer} = 100\,\mu\text{H}$, $N_{layers} = 30$

Figure 2.21: Quantitative impact of the magnetizing inductance for selected parameter ranges

As an example, the value of the post-pulse ripple parameter for the KFA45 kicker system (table 1.1) has been reported in [32], for the system currently in use, based on direct field measurements at a PFL-voltage of $40\,\mathrm{kV}$ at $5.6\,\%$. As fig. 2.21 shows, even with the worst-case assumptions for the relevant parameters in a full-scale inductive adder, the relative magnitude of the perturbations $|\Delta\phi_{dev}|$ remains well below $0.5\,\%$ and is therefore deemed acceptable for the system under consideration.

One possibility to prevent the magnetizing inductance from affecting the output voltage of the inductive adder, is for the primary pulse sources to represent a low impedance source in all intervals, like the circuit variant with recuperation of the absorbed energy presented in section 2.2. Thereby, the magnetizing current does not cause a significant voltage drop over the primary pulse sources.

3 Short-Circuit Mode Branch Module Design Process

3.1 Circuit Requirements

The requirements for a single branch module can be derived from the requirements of the kicker system the inductive adder is designed to drive. The general design of the proof-of-concept short-circuit mode branch module described in this chapter should be suitable to be used as part of various inductive adders to drive any of the kicker systems shown in the table 1.1. The main design parameters for the branch module are summarized in 3.1.

Table 3.1: Design parameters for a branch module suitable for an inductive adder to drive the kicker systems shown in table 1.1.

Parameter	Value
Module output voltage	1.2 kV
Number of branch modules per layer	24
Current per module with doubling at short-circuit termination	220 A
Equivalent impedance the module operates into during the first interval	10.5 Ω
Current rise time into resistive load	<6 ns
Pulse length (interval 1, see fig. 2.2)	1 µs
Pulse repetition rate	10 Hz

The layer voltage of the inductive adder, and thereby the charging voltage of the branch module, has been chosen to V_{layer} = 1.2 kV. This provides a reasonable margin of safety considering the 1.7 kV rated SiC MOSFET switches available in suitable packages at the time of this study. In addition, this voltage specification allows the use of pulse capacitors that have been manufactured to specification for previous inductive adder investigations [39] (sec.3.7).

The mechanical dimensions of one branch module are derived from the dimensions of the inductive adder assembly and the magnetic cores (sec. 2.3), which are also available from a previous inductive adder prototype at CERN [46] and suitable for these first investigations into an inductive adder operating with a short-circuit terminated kicker load. As described in 1.2, the branch modules are arranged in circular layers that are plugged into the metal shells that form the primary winding around the magnetic cores of the inductive adder. This gives 167 mm as the inner radius of the ring formed by the branch modules. For good flexibility, and to minimize the cost per module for the initial proof-of-concept development phase, the module was designed to be the smallest practical unit, with one pulse capacitor per module. The branch module PCB has a wedge shape with an angle of 15 degrees. In this case, 24 branch modules are arranged in a ring and operate in parallel to form the primary pulse source of one layer of the inductive adder. The maximum required output current I_{load} of an inductive adder for the kicker systems considered in these investigations is 5.3 kA for the AD injection kicker system. According to eq. 1.9, this results in a current per branch module of 110 A in the first interval and 220 A when the current is doubled during the second interval.

To achieve the required output voltage of 40 kV for the KFA45 and the AD injection kicker systems (table 1.1) with the selected layer voltage, the inductive adder must have at least 34 layers (neglecting redundancy). For the 30 kV of the KFA10 kicker system, a 25 layer inductive adder is required. The equivalent load impedance Z_{branch} for which each branch module has to be designed (eq. 1.11) is 18.8 Ω for KFA45, 10.5 Ω for AD Injection, and 12 Ω for KFA10. Assuming equal current sharing between the modules in a layer and equal layer voltage for all layers, this impedance is the impedance into which the module operates during

the first interval. Neglecting the core loss equivalent parallel resistance of each layer, Z_{branch} is also the required value of the absorbing resistor $R_{abs,branch}$ per branch module, so that the inductive adder represents a matched impedance Z_{laod} during interval three. In the following chapters, Z_{branch} = 10.5 Ω has been chosen for testing single branch modules.

The rise time requirement for the output pulse of the inductive adder can be derived from the field rise time requirement of the corresponding (short-circuited) kicker system $\tau_{fieldrise,SC}$ and the one-way signal propagation time of the kicker magnet τ_k. With the worst case estimate given in eq. 1.5, the required rise time of the driving voltage pulse at the magnet terminals $\tau_{rise,p}$ is 14 ns for KFA45, 19 ns for AD Injection, and 16 ns for KFA10. To leave some margin for rise time degradation, e.g. due to the inductive adder stack and frequency dependent attenuation of the pulse in the connecting cable, the design target for the rise time of the voltage and current at the module output was set to less than 6 ns into a resistive load equivalent to the impedance seen by each module in the first interval. This necessitates fast switching and a low inductance design of the pulse circuit.

The pulse length for which the branch module must supply energy from its storage capacitor is given by the length of the first interval, which is two times the one-way signal propagation time in the connecting cable and the kicker magnet. Assuming a one-way signal propagation time of 5 ns m^{-1} in the connecting cables, the length of the first interval is 0.53 µs to 0.71 µs for KFA45, between 0.58 µs and 0.84 µs for AD Injection, and 0.41 µs for KFA10. To leave some margin, the pulse length requirement (interval one) was set to 1 µs. Thereby, a kicker system can comprise multiple kicker magnets with a range of cable lengths, as shown in table 1.1, between the kicker magnet and respective generator.

The pulse repetition rate requirement for the branch module was set at 10 Hz, which is significantly higher than required for the kicker systems considered in these investigations.

Fault conditions such as flashover in the kicker magnet, saturation of the magnetic cores due to an issue with the biasing of the magnetic cores, or failure to transition from interval one to interval two in time can cause excessive current in the inductive

adder. Therefore, a fast overcurrent protection is required to prevent the branch module from being damaged by an overcurrent.

3.2 Related Metrology

The time domain data presented here was recorded using a Tektronix DPO5054 [47] oscilloscope with a $-3\,\mathrm{dB}$ bandwidth of $500\,\mathrm{MHz}$, a sample rate of $5\,\mathrm{GS/s}$, and a resolution of $8\,\mathrm{Bit}$. For voltage measurements voltage probes of type 10076C [48] and tpp0500 [49], both with a $-3\,\mathrm{dB}$ bandwidth of $500\,\mathrm{MHz}$, have been employed. The voltage probes were compensated for the input capacitance of the respective oscilloscope channel prior to all measurements, and the signal propagation time in the different signal paths was compensated for all signals with a difference in delay time of less than $1\,\mathrm{ns}$ between channels.

To minimize measurement errors due to induced voltages, the measurement loops were kept as small as possible. Sheath currents in the test leads were reduced to a level that did not detectably affect the measurements by using ferrites around the test leads and by using a single ground reference for all devices. The reproducibility of all measurements was ensured by repeating them at least ten times.

Unless otherwise noted, the rise time of a voltage or current pulse in this work is calculated as the time it takes for the quantity under consideration to rise from $10\,\%$ to $90\,\%$ of its final value. To accurately determine the rise time of a pulse, the influence of the limited bandwidth of the measurement system must be taken into account. Assuming Gaussian systems, the total rise time $t_{r,tot}$ of systems with the rise times $t_{r,n}$, cascaded without feedback, can be added geometrically as shown in eq. 3.1 [50].

$$t_{r,tot} = \sqrt{t_{r,1} + t_{r,2} + ...t_{r,N}} \tag{3.1}$$

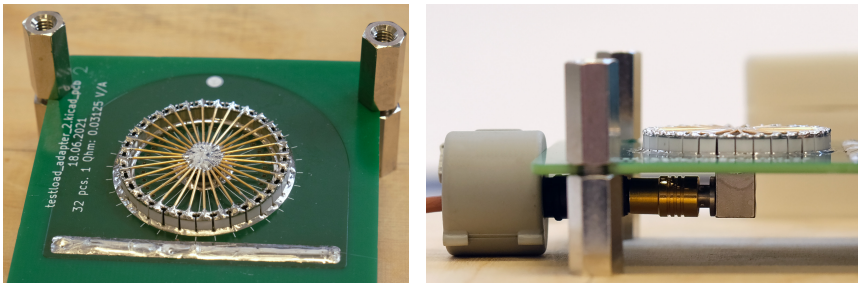
Thereby, the rise time of a system, such as an oscilloscope, is the rise time of the system's step response. The relationship between the rise time t_r of the step response and the $-3\,\mathrm{dB}$ bandwidth Bw of a Gaussian system is given by eq. 3.2 [50].

$$t_r = \frac{0.35}{Bw} \tag{3.2}$$

This results in a rise time of the voltage measurement setup of approximately $1\,\mathrm{ns}$, which is considered to be sufficiently fast for the measurements. The rise times reported in this work are calculated from the measured signal without adjusting for the influence of the measurement system and are therefore slightly slower than the rise time of the real signals. For example, with the above assumptions, if the rise time of the measured signal is $5.0\,\mathrm{ns}$, the rise time of the real signal is $4.9\,\mathrm{ns}$.

3.2.1 Coaxial Shunt Resistor for Current Measurements

The current through the load has been measured by means of a purpose built coaxial current measurement shunt [51]. It is designed to provide high bandwidth, high current measurement capability, and low added inductance when inserted into a circuit. Figure 3.1 shows two photos of the assembled shunt resistor.



(a) Top view. **(b)** Side view.

Figure 3.1: Coaxial current measurement shunt.

The shunt consists of 32 SMD resistors with a value of $1\,\Omega$ and 32 zero ohm bridges soldered upright in two concentric rings. The current to be measured flows through the top layer of the PCB, up the outer ring of $1\,\Omega$ resistors, and back down through the inner ring consisting of zero ohm bridges. The top sides of the SMD resistors and zero ohm bridges are oriented towards each other to minimize the distance between the forward and return paths of the measured current. Both rings are connected at the top via the spokes leading to the center of the arrangement, where the voltage drop over the resistor-ring is measured. Due to the symmetrical design, the center is almost free of magnetic fields caused by the current. Additionally, the inner ring of zero ohm bridges, the spokes, and the copper layers of the PCB form a shielded enclosure around the $50\,\Omega$ resistor used as a series termination for the output signal. With the 32 resistors of $1\,\Omega$ connected in parallel, the coaxial current measurement shunt has an output signal of $31.25\,\mathrm{mV\,A^{-1}}$ into a high impedance measurement input.

To validate the performance, the frequency response of the coaxial current shunt was measured using a vector network analyzer (VNA) [52]. Figure 3.2 shows a measurement of the S21 parameter with port 1 of the vector network analyzer connected to the input of the shunt and port 2 connected to the output.

Driving the shunt with a source having an inner impedance of $50\,\Omega$ and coupling the output signal into the $50\,\Omega$ terminated input of the VNA results in a nominal attenuation of $-70.1\,\mathrm{dB}$. This nominal attenuation is shown by the middle dotted line in fig. 3.2. The measurement shows a flat frequency response within $\pm 1.2\,\mathrm{dB}$ from $10\,\mathrm{kHz}$ to $1\,\mathrm{GHz}$. The frequency response first deviates more than $3\,\mathrm{dB}$ from the nominal attenuation at a frequency of $1.25\,\mathrm{GHz}$. The resonances visible in the measurement are above $1.5\,\mathrm{GHz}$ and thus well outside the pass band of the low pass input filter of the oscilloscope used.

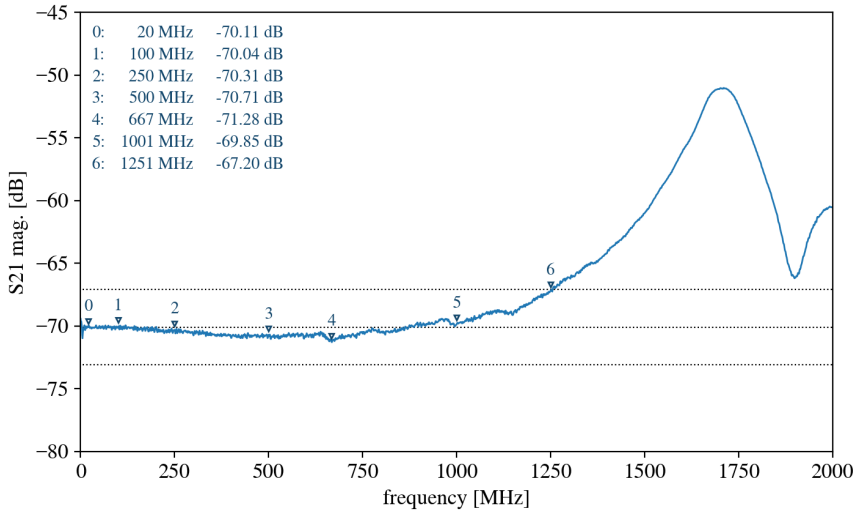


Figure 3.2: VNA measurement of the S21 parameter for the coaxial current measurement shunt.

3.3 Circuit Features and Component Selection

As an overview, fig. 3.3 shows a block diagram of the developed branch module for short-circuit operation.

The circuit is based on the circuit topology presented in sec. 2.2. The two variants for absorbing the stored energy in interval three can be implemented alternatively on the PCB by populating either the diode D_{rec} or the resistor R_{abs}.

The two switches are controlled via two logic level coaxial interfaces and feature a galvanic isolation via digital isolators to prevent problems caused by differences in the reference potential of the pulse circuit and the control signal. The module is powered by a 15 V supply that is isolated from the pulse circuitry by an isolated DC/DC converter. Other voltage levels are generated from this supply voltage, e.g. for the gate drivers of the switches.

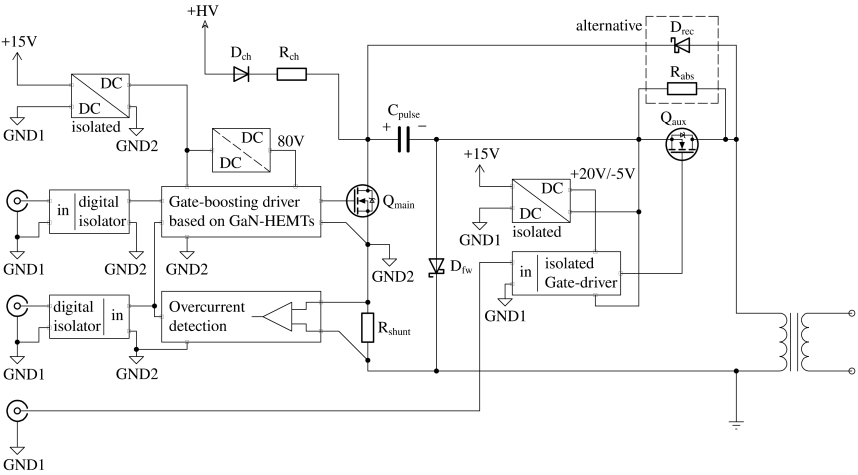


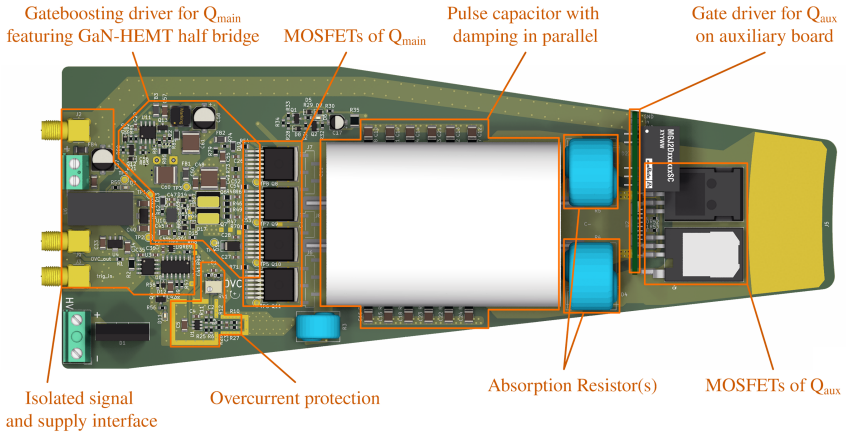
Figure 3.3: Block diagram of the branch module

The pulse capacitor, which serves as energy storage for the branch module, is charged by a high-voltage power supply. The high-voltage charge input is referenced to the pulse circuit ground potential. To prevent unwanted high-frequency ground currents through the charging interface due to the operation of the pulse circuit, an appropriate filter is used in the charging supply connection (not shown).

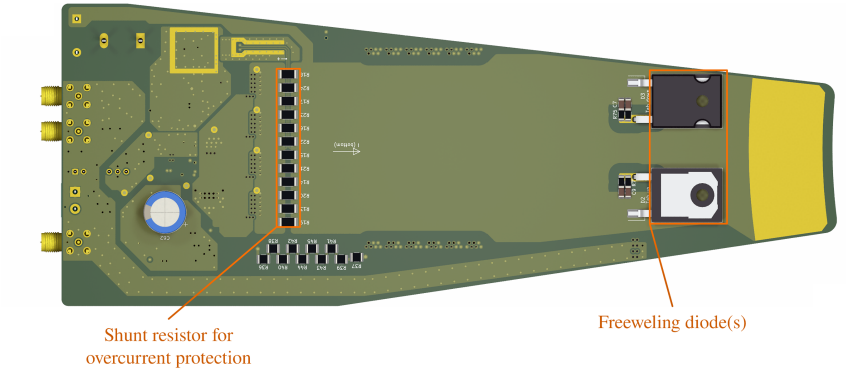
Figure 3.4 shows a top and bottom view of the branch module PCB with the various circuit features labeled. This chapter describes the circuit features in detail.

3.4 Main Switch

Since the switch Q_{main} is only closed in the first interval, it only has to carry the initial current, i.e. 110 A, before the current doubles in the second interval. For switch Q_{main} four paralleled MOSFETs of type G3R160MT17J [53] in a surface mount TO-263 package with a Kelvin source were selected to allow for a low inductance layout of the pulse circuit. The selected MOSFET has a pulsed current



(a) Top view.



(b) Bottom view.

Figure 3.4: Rendered image of the branch module PCB with the various circuit features labeled.

rating of 48 A. With a maximum pulse width of 1 µs and a repetition rate of 10 Hz, the duty cycle of the switch is 0.001 %. This is well within the operating area defined for the pulsed current specification defined in the datasheet [53].

Since the field rise time in the kicker magnet comprises the rise time of the pulse (eq. 1.5), a fast rise of the pulse is crucial to minimize the field rise time for a given kicker magnet design. Since Q_{main} closes after the switch Q_{aux} is already

closed, the switching speed of Q_{main} plays a major role in the rise time of the initial pulse. Therefore, a specialized gate-boosting circuit has been implemented to drive the MOSFETs of Q_{main} [54].

3.4.1 Gate-Boosting Driver

Figure 3.5 shows a simplified schematic of the specialized gate-boosting driver circuit [55] for driving the MOSFET Q_{main}.

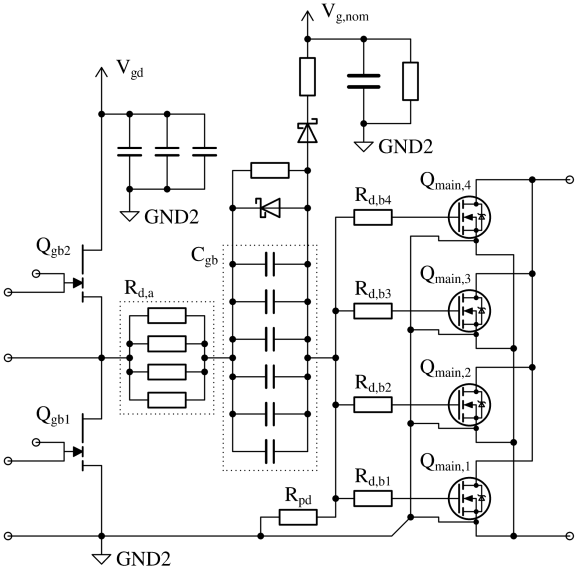


Figure 3.5: Schematic of the gate-boosting driver.

It allows the switching speed of a MOSFET switch to be increased without exceeding the maximum gate voltage specified in the datasheet [53]. The gate drive loop of a MOSFET switch can be represented by a damped RLC series resonant circuit formed by the capacitance of the MOSFET gate C_{gate}, the parasitic inductance of the gate drive loop L_{gl}, and gate resistors inserted for damping. This

RLC resonant circuit is typically aperiodically damped or slightly underdamped to achieve a fast rise time without excessive overshoot at the MOSFET gate. The $10\,\%$ to $90\,\%$ rise time for an aperiodically damped RLC circuit is given by eq. 3.3 [56].

$$t_{r,ap} = 3.36\sqrt{L_{gl}C_{gate}} \tag{3.3}$$

As can be seen, by introducing an additional capacitance C_{gb} in series with the MOSFET gate, the rise time $t_{r,ap}$ of the voltage signal at the MOSFET gate can be shortened. However, the capacitor C_{gb} forms a capacitive divider with the gate capacitance, resulting in a reduced driving voltage at the gate. To offset the effect of this capacitive voltage divider, a driving voltage V_{gd} of $80\,\mathrm{V}$ is used to drive the gate circuit. For providing a fast gate drive signal at this increased voltage, a half-bridge comprising the two GaN-HEMTs Q_{gb1} and Q_{gb2} has been implemented. The GaN-HEMTs of the type GS66506T [57] have a pulsed drain current rating of $48\,\mathrm{A}$ and are used to drive the gates of the four MOSFETs of Q_{main} in parallel. To prevent an overshoot of the gate voltage, the gate drive loop is damped by means of the resistors $R_{d,a}$ and $R_{d,b}$. The resistors $R_{d,b}$ foster equal distribution of the gate driving current among the gates of the four paralleled MOSFETs of Q_{main}.

The total capacitance of C_{gb} is calculated according to eq. 3.4 [55] based on the effective gate capacitance C_g derived from the gate-charge versus gate-voltage plot provided in the datasheet [53], the desired final voltage across the gate capacitance $V_{g,nom}$, and the available gate driving voltage V_{gd}.

$$C_{gb} = \frac{C_g}{\frac{V_{gd}}{V_{g,nom}} - 1} \tag{3.4}$$

Figure 3.6 shows a close-up photo of the MOSFET switch Q_{main} and the gate-boosting driver implemented on the PCB. Care has been taken to design the

layout as compact as possible, using short, wide traces to minimize the parasitic inductance of the gate drive loop.

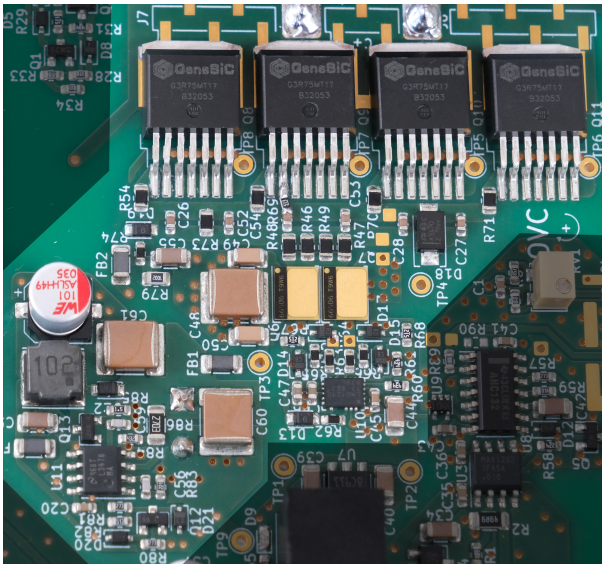
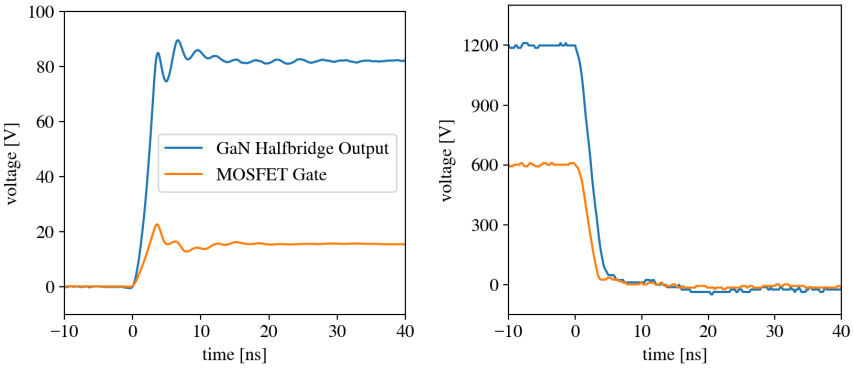


Figure 3.6: The four paralleled MOSFETs of Q_{main} (top) with the gate-boosting driver (center) implemented on the PCB. On the lower left is the DC/DC converter for providing the 80 V for the gate-boosting driver.

3.4.1.1 Measurements

Figure 3.7(a) shows the voltage at the half-bridge output, as well as at the gate of one of the MOSFETs comprising Q_{main}, measured where the gate and Kelvin-source leads enter the package. The output voltage of the GaN-HEMT half bridge has a rise time of 2.33 ns. The voltage at the MOSFET gate leads rises within 2.5 ns to a voltage of 15 V and exhibits an overshoot to approximately 23 V. Measurements in [58] performed directly on the die of an IGBT show, that this voltage spike can be explained by the inductive voltage across the part of the leads inside the package as well as the bond wires that are part of the measurement

shown in fig. 3.7(a). Hence, it can be assumed, that the measured overshoot is not applied to the die. The voltage at the MOSFET gate plateaus to a steady state voltage of 15 V as recommended in the datasheet [53]. Figure 3.7(b) shows measurements of the drain-source voltage across the MOSFETs of Q_{main} for a charging voltage of 600 V as well as at the rated voltage of 1.2 kV. The voltage between the drain and source of the paralleled MOSFETs exhibits a fall time of 2.7 ns at 600 V and 3.4 ns at 1.2 kV with a resistive load of 10 Ω.



(a) Voltage at the output of the GaN-HEMT half bridge and the gate lead of one MOSFET of Q_{main}

(b) Drain-source voltage across the MOSFETs of Q_{main}

Figure 3.7: Gate-boosting driver measurements.

3.4.2 Loss Distribution among the Paralleled SiC MOSFETs of Q_{main}

To detect potential issues with equal current distribution between the four paralleled MOSFET switches of Q_{main}, the heating of the MOSFETs was examined using a thermal imaging camera [59]. In normal operation at the specified pulse repetition rate of 10 Hz and at pulse lengths in the 10 µs range, there is no measurable heating of the switches. Therefore, for this test, the module has been operated with a resistive load of 6.7 Ω at a charging voltage of 700 V at a repetition rate of 10 kHz and a pulse length of 200 ns. This corresponds to an approximate average

total output power of 146 W. A relatively short pulse length was chosen to focus the measurement on switching losses and the initial phase of the pulse, where any current displacement due to skin and proximity effects is expected to be most pronounced. To be able to recharge the pulse capacitor at a sufficient rate, the value of the resistor limiting the charging current was reduced for this test. Nearby parts of the circuit emitting heat, e.g., the DCDC converters were covered up. The thermal image shown in fig. 3.8 was taken after approximately 5 s of operation of the module, after it had been turned off long enough to be at ambient temperature at the start of operation.

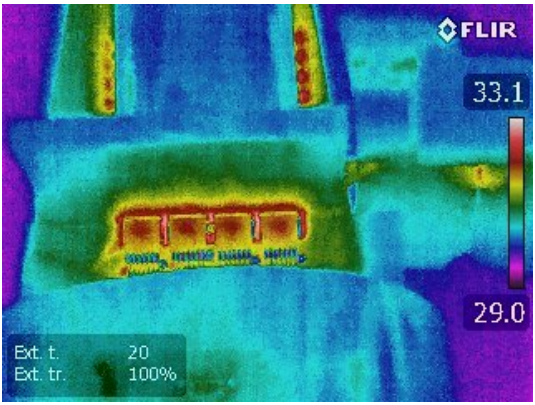


Figure 3.8: Thermal image of the MOSFETs of Q_{main}

In the thermal image, there is no apparent difference in the loss-induced heating of the Q_{main} MOSFET switches.

3.5 Auxiliary Switch

The switch Q_{aux} must be capable of carrying a peak current of 220 A during the second interval. Therefore, two SiC MOSFETs of the type C2M0045170P [60] in parallel configuration were selected to implement Q_{aux}. They each have a pulsed

drain current rating of 160 A. Figure 3.9 shows a photo of the switch Q_{aux} and its gate driver.

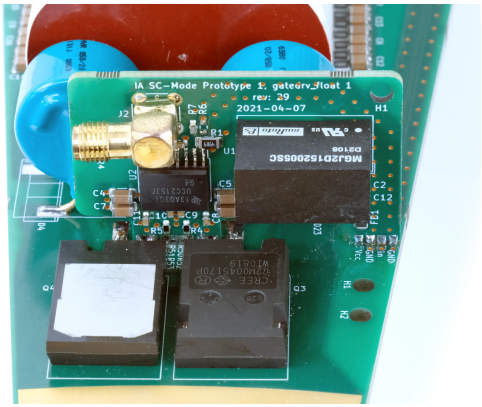


Figure 3.9: The two paralleled MOSFETs of Q_{aux} with the isolated gate driver on an auxiliary PCB.

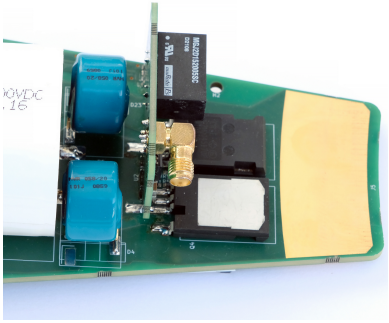
The MOSFETs in the TO-247-4 package are mounted on the top of the board as surface-mount devices. While this mounting method is not standard, it prevents the wide ground return trace on the bottom of the board from being interrupted by the holes for the device leads and the large insulation gap that would be required for the potential difference of 1.2 kV between Q_{aux} and the ground return. Additionally, it allows for smaller, lower inductance current loops to be formed by the device leads.

The turn-on time of Q_{aux} is not important, as it can be turned on before the pulse is initiated via Q_{main}. Hence, a commercial gate driver of the type UCC21530 [61] is used to drive the MOSFETs of Q_{aux}, which provides galvanic isolation as Q_{aux} is electrically floating. The gate driver is implemented on a small auxiliary PCB soldered on the main PCB close to the gate and Kelvin source pins of the two MOSFETs of Q_{aux}. This allows both a small gate drive loop and a shorter pulse circuit compared to implementing the gate drive circuit on the main board. Furthermore, it minimizes the parasitic capacitance between the isolated control and supply side of the gate drive circuit and the potential of Q_{aux}.

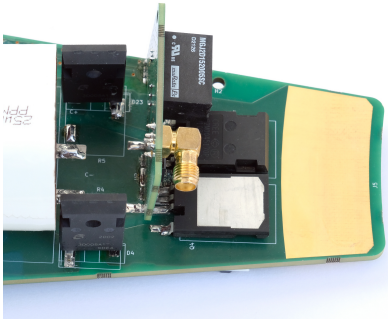
3.6 Absorption Resistor and Recuperation Diode

The branch module allows to test both variants for absorbing the energy stored in the connecting cable and the kicker magnet in the third interval, by either populating the absorption resistor R_{abs} or the recuperation diode D_{rec} (3.3). For R_{abs} two paralleled low inductance ceramic carbon resistors of type AB 058 [62] have been chosen. They have a thermal mass large enough to adiabatically absorb the required energy in interval three (72 mJ per resistor, for two parallel 20 Ω resistors and a voltage of 1.2 kV in interval three with a length of 1 µs) and are rated to dissipate the average power at a pulse repetition rate of 10 Hz (0.72 W). The resistors are positioned near the end of the module, to keep the series inductance as low as possible during the matched state in the third interval. Figure 3.10(a) shows a photo of the two resistors of R_{abs} mounted on the PCB.

Alternatively, two SiC diodes of type GB25MPS17-247 [63] can be placed, to feed the energy absorbed in interval three back into the pulse capacitor. Figure 3.10(b) shows a photo of the two SiC diodes of D_{rec} mounted on the PCB.



(a) Resistors mounted on the PCB to dissipate the absorbed energy.



(b) Diodes mounted on the PCB to recuperate the absorbed energy into the pulse capacitor.

Figure 3.10: Diodes or resistors can be alternatively mounted to absorb the energy stored in the connecting cable and the kicker magnet during the third interval.

3.7 Pulse Capacitor

A foil capacitor with a capacitance of $25\,\mu\mathrm{F}$ and a voltage rating of $1500\,\mathrm{V}$ was selected as the main energy storage device in each branch module. This capacitor has been made to CERN specifications, and has been used in previous inductive adder projects [15]. It offers a good compromise in pulsed current capability and energy density, while having appropriate mechanical dimensions with a height of $35\,\mathrm{mm}$.

The discharge of the pulse capacitors into the connecting cable and the kicker magnet, during the first interval, causes a droop in the capacitor voltage and thus in the output voltage of the inductive adder. As described in sec. 2.2.2, deviation from a rectangular shape of the output voltage of the pulse generator in interval one, can contribute to ripple in the current flattop during the second interval. Therefore, a large capacity of the pulse capacitor is preferable, to keep voltage droop as low as possible. Assuming a constant current $I_{branch,i1}$ being sourced from the pulse capacitor of each branch module during the first interval, the capacitor droop ΔV_{droop} can be calculated according to eq. 3.5 [25].

$$\Delta V_{droop} = \frac{I_{branch,i1} * t_{i1}}{C_{pulse}} \tag{3.5}$$

With $I_{branch,i1}$ = $110\,\mathrm{A}$, the duration of interval one t_{i1} = $1\,\mu\mathrm{s}$ and C_{pulse} = $25\,\mu\mathrm{F}$, ΔV_{droop} is $4.4\,\mathrm{V}$. This is sufficiently low for the present application.

Due to the relatively high series inductance measured at $28\,\mathrm{nH}$ in [15], a low-inductance parallel current path consisting of twelve ceramic capacitors with a capacitance of $100\,\mathrm{nF}$ each was initially foreseen. The goal of this configuration is to achieve a low voltage drop across the parasitic inductance of the foil capacitor during the fast rise and the initial phase of the pulse.

3.7.1 Damping of Oscillations in the Pulse Circuit

For a first commissioning of the pulse circuit, the module was tested directly connected to a resistive load of $10.5\,\Omega$ without the use of an output transformer. This load of $10.5\,\Omega$ corresponds to the intended operating point of the module during the first interval, where the kicker magnet and the connecting cable appear as resistive load from the point of view of the pulse generator. A picture of the test setup is shown in fig. 3.11.

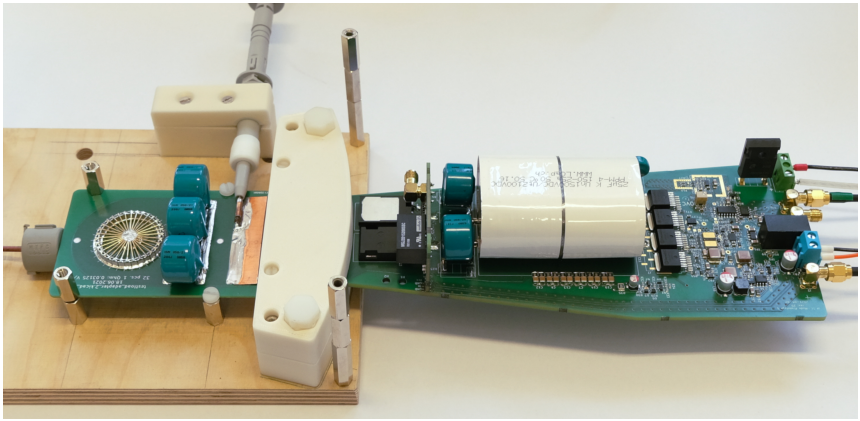
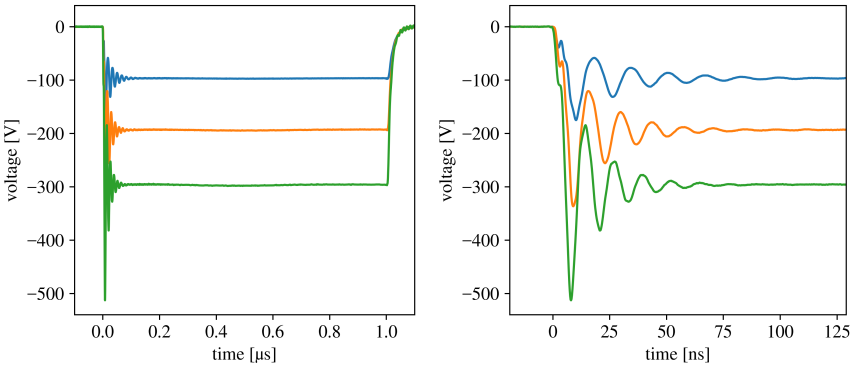


Figure 3.11: Test setup for operation of the branch module with a resistive load.

The measurements revealed that the pulse waveform at the output of the module exhibits an overshoot with a damped oscillation in the leading edge of the pulse. Figure 3.12 shows a measurement of the voltage across the load resistor for three different charging voltages of $100\,\mathrm{V}$, $200\,\mathrm{V}$ and $300\,\mathrm{V}$. As can be seen in fig. 3.12(b), the frequency of the oscillations increases with a higher charging voltage. The frequency of these oscillations was estimated to be $62\,\mathrm{MHz}$ at $100\,\mathrm{V}$, $72\,\mathrm{MHz}$ at $200\,\mathrm{V}$, and $79\,\mathrm{MHz}$ at $300\,\mathrm{V}$. This indicates the presence of a parasitic resonant circuit with at least one voltage-dependent circuit element. A measurement with only one of the two parallel diodes forming the freewheeling

diode (see sec. 3.8) populated identified the voltage-dependent capacitance of the freewheeling diode as part of this resonant circuit.



(a) Pulse with a length of 1 µs.

(b) Detail of the leading edge of the pulse.

Figure 3.12: Measurement of the output voltage of the module with a resistive load of 10.5 Ω for the charging voltages 100 V, 200 V and 300 V

To further investigate the cause of the oscillations, a simulation model of the pulse circuit including parasitic elements has been set up. The considered parasitic elements are highlighted in red in fig. 3.13.

In the real circuit, the pulse capacitor consists of one foil capacitor $C_{pulse,m}$ with a capacitance of 25 µF in parallel with twelve ceramic capacitors of 100 nF each, together considered as $C_{pulse,f}$. The capacitance $C_{p,Dfw}$ of fig. 3.13 represents the voltage-dependent capacitance of the two parallel SiC diodes of the free-wheeling diode D_{fw}. It behaves as a decreasing capacitance with increasing blocking voltage across the diode and has been modeled using a voltage versus charge table based on the information given in the datasheet [63].

The inductances $L_{p,Cpulse,f}$, $L_{p,Cpulse,m}$, $L_{p,Qmain}$, $L_{p,Dfw}$ and $L_{p,O}$ highlighted in fig. 3.13 model the parasitic inductances of the components and PCB traces of their respective circuit branch. The inductances of the components were initially roughly estimated based on a value of $10\,\mathrm{nH\,cm^{-1}}$ [64]. The connections between the components of the pulse circuit are designed as wide traces, with both the

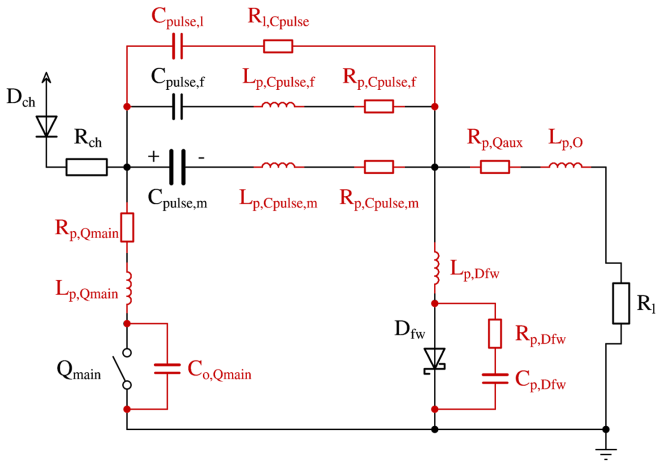


Figure 3.13: Simulation model of the pulse circuit including parasitic elements.

go and return conductors having approximately the same width. Therefore, to estimate the inductance L of these traces, they have been approximated as parallel plate transmission lines with width w, spacing h, and length l according to eq. 3.6 [28].

$$L = \mu_0 \frac{h}{w} * l \tag{3.6}$$

For modeling the losses of the circuit branches resistors have been employed. The initial values for these resistors were based on data sheet information of the respective components, where available, and on reasonably estimated values otherwise. Thereby, a frequency dependency of the losses has not been considered. However, some damping of very high frequency components has been implemented in the simulation via the capacitance $C_{pulse,l}$ and the resistor $R_{l,pulse}$. Subsequently, both the parasitic inductances, and the resistors modeling the losses, were then iteratively adjusted to match measurements at different points of the circuit and under different operating conditions. The four paralleled MOSFETs of switch Q_{main} have been modeled using LTspice's [33] switch model with a voltage-dependent parallel capacitance $C_{o,Qmain}$ according to the output capacitance plot given in the

datasheet [53]. The switch Q_{aux} is closed throughout the measurement and is therefore represented by its on-resistance $R_{p,Qaux}$. Its parasitic inductance is part of $L_{p,O}$. The ceramic capacitors that make up $C_{pulse,f}$ have a reduced capacitance at higher charging voltages [65], so a value of $C_{pulse,f} = 800\,\mathrm{nF}$ was used for the simulations. The final adjusted values of the parasitic elements used in all simulation runs, are given in table 3.2.

Table 3.2: Values for the parasitic elements used in all simulation runs.

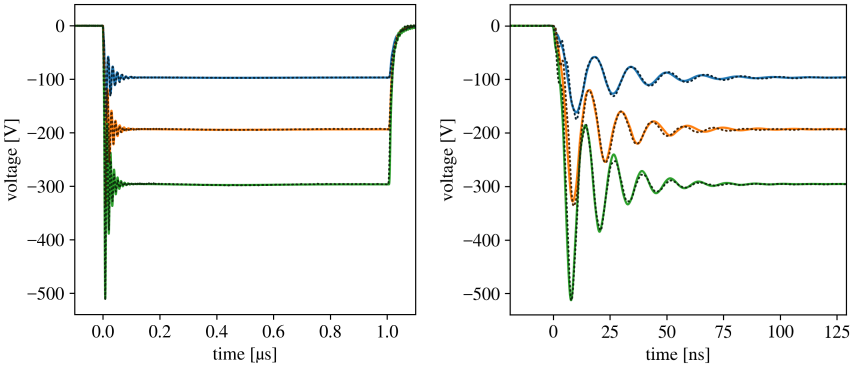
Element	Value	Element	Value
$C_{pulse,l}$	$100\,\mathrm{pF}$	$R_{l,Cpulse}$	$200\,\mathrm{m\Omega}$
$L_{p,Cpulse,f}$	$2.5\,\mathrm{nH}$	$R_{p,Cpulse,f}$	$50\,\mathrm{m\Omega}$
$L_{p,Cpulse,m}$	$12\,\mathrm{nH}$	$R_{p,Cpulse,m}$	$20\,\mathrm{m\Omega}$
$R_{p,Qaux}$	$15\,\mathrm{m\Omega}$	$L_{p,O}$	$12\,\mathrm{nH}$
$R_{p,Qmain}$	$30\,\mathrm{m\Omega}$	$L_{p,Qmain}$	$4.5\,\mathrm{nH}$
$L_{p,DfW}$	$1.8\,\mathrm{nH}$	$C_{o,Qmain}$	voltage dependent [53]
$R_{p,Dfw}$	$200\,\mathrm{m\Omega}$	$C_{p,Dfw}$	voltage dependent [63]

The solid lines in fig. 3.14 show the simulation of the voltage across the load resistor R_l for an initial charging voltage of the capacitor C_{pulse} of $100\,\mathrm{V}$, $200\,\mathrm{V}$, and $300\,\mathrm{V}$.

The dotted lines superimposed on the simulation result are the previously obtained measurements in the test setup with a restistive load. The excellent agreement between measurement and simulation confirms the assumptions made for the model. Subsequently, the model is employed to identify and implement means of damping the oscillations.

3.7.1.1 Damping measures

To suppress the oscillations, damping resistors have been added to the circuit [66]. The circuit elements added for damping are highlighted in green in fig. 3.15.



(a) Pulse with a length of 1 µs.

(b) Detail of the leading edge of the pulse.

Figure 3.14: Simulation of the output voltage of the branch module into a resistive load of 10.5 Ω for the charging voltages 100 V, 200 V and 300 V (solid lines). The respective measurements are overlaid as dotted lines for comparison.

The simulation revealed that the oscillating current passes almost completely through the low inductance path comprising the capacitors $C_{pulse,f}$. Therefore, damping was only added to this path in the form of $R_{d,Cpulse,f}$ and not to the main current path through $C_{pulse,m}$. Thereby, no additional losses are incurred for the large discharge current through capacitor $C_{pulse,m}$ during the majority of the pulse in normal operation. In addition, an RC circuit consisting of $R_{d,D}$ and $C_{d,D}$ has been added in parallel to the freewheeling diode D_{fw}. The values of these three components were iteratively adjusted in the simulation to minimize the oscillations in the output voltage. This resulted in the following values for the damping elements: $R_{d,Cpulse,f} = 4.2\,\Omega$, $R_{d,D} = 8.3\,\Omega$, and $C_{d,D} = 880\,\mathrm{pF}$. For the simulation the parasitic inductance $L_{p,d,D}$ of the new circuit branch comprising $R_{d,D}$ and $C_{d,D}$ was set to $1\,\mathrm{nH}$. The simulation showed that with the damping resistors in series with the capacitor $C_{pulse,f}$, the circuit branch comprising $C_{pulse,f}$ carries current only during the first tens of nanoseconds of the pulse, until the full load current has commutated to the main current path through $C_{pulse,m}$. Therefore, the capacitance of $C_{pulse,f}$ can be significantly reduced from approximately $800\,\mathrm{nF}$ to $C_{pulse,f} = 30\,\mathrm{nF}$ without affecting the performance of the module.

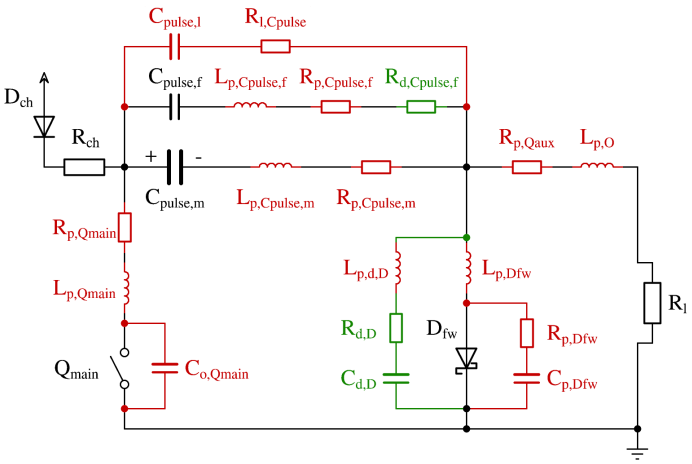
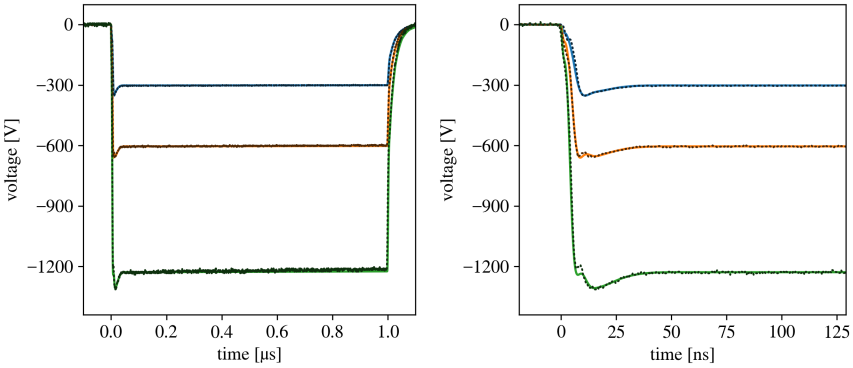


Figure 3.15: Simulation model of the pulse circuit including parasitic elements, and added damping measures.

A simulation of the voltage across the load resistor, with damping elements having the above values, is shown in fig. 3.16 as the solid lines. The corresponding measurements of the branch module with the improvements implemented on the PCB are overlaid as dotted lines.

Both the simulation results and the measurements are shown for the nominal charging voltage of the branch module of 1.2 kV in addition to the voltage levels of 600 V and 300 V. The measurements are in excellent agreement with the simulation and show the same aperiodic behavior as predicted by the simulation results.

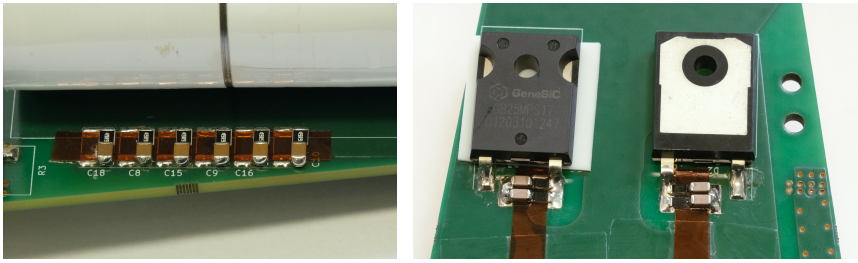
Figure 3.17 shows pictures of the damping elements as they were added to the printed circuit board.



(a) Pulse with a length of 1 µs

(b) Detail of the leading edge of the pulse.

Figure 3.16: Simulation of the output voltage of the branch module with added damping measures into a resistive load of 10.5 Ω for the charging voltages 300 V, 600 V and 1200 V (solid lines). The measurements from the modified module overlaid as dotted lines match the improvements predicted by the simulation.



(a) Damping in parallel to the pulse capacitor.

(b) Damping in parallel to the freewheeling diode.

Figure 3.17: Damping measures implemented on the branch module.

3.8 Freewheeling Diode

Along with the switch Q_{aux}, the freewheeling diode D_{fw} conducts the doubled current of 220 A during the second interval. Diode D_{fw} consists of two parallel SiC diodes of type GB25MPS17-247 [63] each rated for a repetitive peak forward surge current of 162 A.

The diodes of D_{fw} are positioned close to the output of the branch module, to minimize losses during the second interval. However, this increases the distance between the switch Q_{main} and the freewheeling diode. When Q_{main} opens at the end of the first interval, the load current flowing through the branch module commutates into D_{fw}. Thereby, energy stored in the parasitic inductance of the pulse capacitor and in the traces between D_{fw} and Q_{main} is mainly absorbed by the output capacitance of Q_{main}. This parasitic inductance is represented by L_p in fig. 3.18.

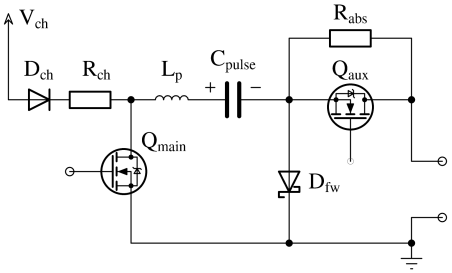
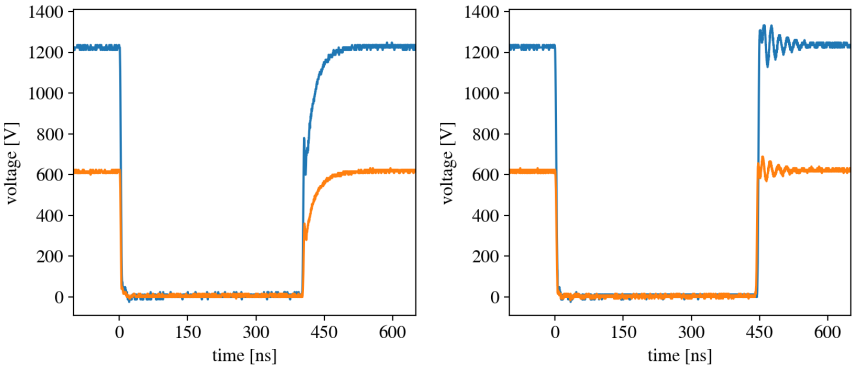


Figure 3.18: Simplified schematic including the parasitic inductance L_p of the loop formed by Q_{main}, C_{pulse} and D_{fw}.

Depending on the size of L_p and the output capacitance of Q_{main}, this can lead to an inductive overvoltage across Q_{main}. To make the parasitic inductance L_p as small as possible, wide copper planes are used for the connection between D_{fw}, C_{pulse} and Q_{main}. Additionally, the pulse capacitor features a low inductance parallel path comprising smaller capacitors and damping(sec. 3.7). To ensure that no additional measures, such as a snubber across Q_{main}, are required to prevent an overvoltage at Q_{main} the voltage across Q_{main} was measured with both a resistive load of $10.5\,\Omega$, as well as with a short-circuit mode replacement load with a characteristic impedance of $10\,\Omega$ (sec. 4.1). The measurements are shown in fig. 3.19.

In fig. 3.19(a)), with the resistive load, there is an initial steep rise and a small voltage spike during the rising edge of the drain-source voltage of Q_{main} as the energy stored in L_p charges the output capacitance of Q_{main} as it opens. With



(a) Operation with a resistive load of $10.5\,\Omega$

(b) Operation with a short-circuit mode replacement load with a characteristic impedance of $10\,\Omega$ (sec. 4.1)

Figure 3.19: Drain source voltage of the switch Q_{main} with a charging voltage of $618\,V$ and $1225\,V$.

the resistive load, the voltage at the output of the module, and thus, the negative terminal of C_{pulse} rises relatively slowly (fig. 3.16) due to the large capacitance of the freewheeling diode in relation to the parasitic inductance of the loop formed by the load resistor Q_{aux} and D_{fw}. Since the voltage spike across Q_{main} caused by L_p is superimposed on this slow rise, the drain-source voltage of Q_{main} does not exceed the charging voltage of C_{pulse}.

With the short-circuit mode replacement load, the voltage at the negative terminal of C_{pulse} rises rapidly, as the capacitance of D_{fw} is charged by the reflected wave returning from the short-circuit termination. As can be seen in fig. 3.19(b), this leads to an overshoot and a damped oscillation in the drain-source voltage of Q_{main}. The overshoot reaches a maximum of $688\,V$ for a charging voltage of C_{pulse} of $618\,V$ and a maximum of $1330\,V$ for a charging voltage of C_{pulse} of $1225\,V$. The input capacitance of $3\,pF$ of the oscilloscope probe [48] used for the measurements is thereby negligibly small compared to the combined output capacitance of $128\,pF$ at $V_{DS} = 1\,kV$ of the four parallel MOSFETs of Q_{main} [53].

The overshoot is judged to leave enough margin to the rated voltage of Q_{main} of $1700\,V$ to not require a snubber for Q_{main}.

3.9 Overcurrent Protection

To prevent the branch module from being damaged by an overcurrent, a fast overcurrent protection is important. An overcurrent can occur due to various fault conditions. For example, flashovers can sometimes occur in a kicker magnet [67][68]. A flashover effectively brings the short-circuit termination closer to the pulse generator, and the reflected wave returns earlier than expected. In this scenario, as long as the switch Q_{main} remains closed, the current increases in steps each time the reflected wave from the short-circuit arrives at the generator. Thus, for every two-way signal propagation time from the pulse generator to the location of the flashover, the current increases by two times the current of the first interval (neglecting droop of the capacitor voltage).

Similarly, if the switch Q_{main} is not opened in time as the wave reflected from the short-circuit termination arrives at the generator at the nominal end of the first interval, e.g. due to a control malfunction, the current will rise to three times the current of the first interval.

Another possible scenario leading to an overcurrent is the saturation of the magnetic core of one of the layers of the inductive adder. This can happen, for example, if the core is not being properly biased towards the opposite saturation at the beginning of the pulse. The behavior when approaching saturation of the magnetic cores used for the inductive adder is shown in sec. 2.3.

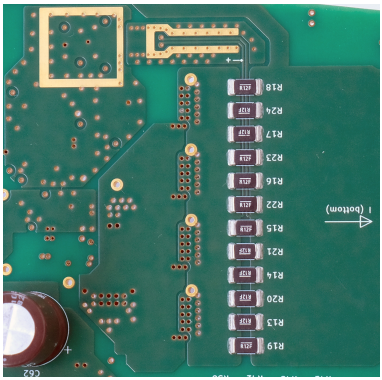
In all these cases, the fault current increase is driven by the energy supplied by the pulse capacitor via the switch Q_{main} and can be detected by monitoring the current through Q_{main}. Therefore, an overcurrent protection is implemented only for the switch Q_{main}.

Several options have been considered for implementing overcurrent detection. One possibility is to monitor the drain-source voltage of a MOSFET while it is in the on state [69]. As the current through the switch increases, the drain-source voltage of the MOSFET increases due to the on-resistance of the MOSFET. While no modification to the pulse circuitry is required, a blanking time after the

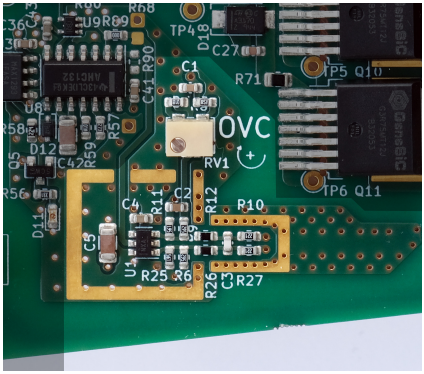
MOSFET is turned on is usually required to avoid false triggering. The blanking time is typically on the order of a few 100 ns [70]. This time can be too long if the branch module starts to pulse into an inductive adder layer with a saturated magnetic core.

Another option is to measure the current through the switch using a current transformer [71] or a Rogowski coil realized with PCB traces and vias around a terminal of the semiconductor switch [72]. However, these were considered impractical to insert into the pulse circuit of the branch module without an unwanted increase in inductance, or to fit into the limited space of the PCB layout.

The method chosen to implement the overcurrent protection for the branch module is to measure the current through a shunt resistor in the ground return path, which is evaluated by a fast comparator [73]. Figure 3.20(a) shows the shunt resistor as implemented on the PCB. It consists of twelve low-inductance metal strip resistors distributed over the wide ground return trace on the bottom of the PCB.



(a) Shunt resistor consisting of twelve 120 mΩ metal strip resistors distributed over the wide ground return trace on the bottom side of the module.



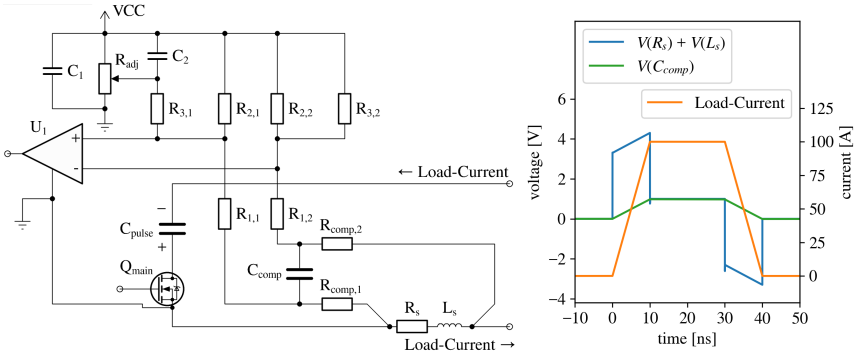
(b) RC circuit for compensating the parasitic inductance of the shunt and the comparator with its input network.

Figure 3.20: Overcurrent detection circuit implemented on the branch module PCB.

Considering the distributed shunt resistor as a section of a parallel plate transmission line with a width of 47 mm, a conductor spacing of 3.2 mm, and a length

of $5.5\,\mathrm{mm}$, the value of the parasitic inductance L_s of the shunt resistor can be estimated to be $514\,\mathrm{pH}$. The designed current rise rate of $110\,\mathrm{A}$ in $6\,\mathrm{ns}$ causes a voltage drop of $9.4\,\mathrm{V}$ across $\mathrm{L_s}$. This voltage is significantly higher than the voltage drop across the shunt's ohmic resistance of $10\,\mathrm{m\Omega}$ caused by the load current, which is $1.1\,\mathrm{V}$ at $110\,\mathrm{A}$. Therefore, to obtain an accurate measurement despite the high di/dt, the effects of the inductance $\mathrm{L_s}$ are compensated by an RC circuit.

A simplified schematic of the overcurrent protection is shown in fig. 3.21(a). By matching the time constant $\tau_{shunt} = L_s/R_s$ of the shunt resistor $\mathrm{R_s}$ with its parasitic inductance $\mathrm{L_s}$ and the time constant $\tau_{comp} = R_{comp} * C_{comp}$ of the RC circuit the effects of $\mathrm{L_s}$ can be fully compensated. This is illustrated in the simulation in Figure 3.21(b), which shows the voltage across the shunt resistor $\mathrm{R_s}$, including its parasitic inductance $\mathrm{L_s}$, as well as the voltage across the capacitor $\mathrm{C_{comp}}$ of the RC circuit used to compensate for the effects of $\mathrm{L_s}$. The voltage drop



(a) Simplified schematic of the overcurrent detection.

(b) Simulation of the voltage across the shunt resistor $\mathrm{R_s}$ and its parasitic inductance $\mathrm{L_s}$ ($V(R_s) + V(L_s)$) and the voltage across the capacitor $\mathrm{C_{comp}}$ ($V(C_{comp})$) for a Load-Current pulse of 100 A with a rise/fall time of 10 ns.

Figure 3.21: Overcurrent protection.

across $\mathrm{L_s}$ during the rising and falling edges of the load current is filtered out in the voltage across $\mathrm{C_{comp}}$ that is evaluated by the comparator U1.

To minimize interference inductively coupled into the measurement signal, the traces of the differential current measurement signal are routed in parallel and close together. In addition, the comparator input network is symmetrical, with a balanced impedance of the comparator input signals to the comparator reference potential. Guard traces and ground planes are used to shield the traces and comparator circuit from capacitively coupled interference.

3.9.1 Test of Overcurrent Protection

To test the performance of the overcurrent protection, the branch module was operated with a load consisting of a resistor of $8\,\Omega$ in parallel with a saturable inductor. Figure 3.22 shows the measurements of the load current.

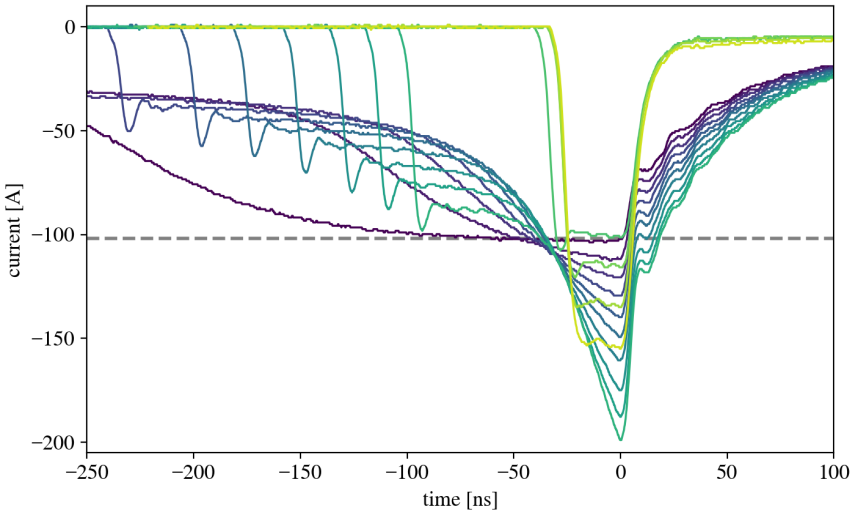


Figure 3.22: Measurement of the output current of the branch module for different charging voltages between 800 V and 1200 V, operated with a load consisting of a $8\,\Omega$ resistor in parallel with a saturable inductor. The dashed line shows the threshold of the overcurrent protection adjusted to 102 A.

The test was performed with various different charging voltages from 800 V to 1200 V. The overcurrent threshold was adjusted to 102 A for all measurements, indicated by the dashed line in fig. 3.22. As a result, the load current rises at different rates to the point where it exceeds the overcurrent threshold. The current waveforms in fig. 3.22 have been aligned by the time the current starts to decrease due to the main switch being turned off by the overcurrent protection. The measurements show, that the overcurrent protection turns off an overcurrent condition within approximately 40 ns for the slower rising load current waveforms and within approximately 25 ns for the fast rising load current waveforms. The overcurrent protection does not react to a fast rising initial current peak of 98 A that only comes close to the threshold of 102 A, while tripping when the threshold is crossed later at a lower current rise rate. This verifies that the effects of the shunt's parasitic inductance are well compensated.

3.10 Test of the Board with a Resistive Load

Figures 3.23 and 3.24 show the output voltage of the branch module and the current through a resistive load connected to the branch module with low inductance.

A picture of the test setup is shown in fig. 3.11 in sec. 3.7. The measurements are shown for a charging voltage of 600 V and 1200 V. The value of the resistive load has been selected to be 10.5 Ω. This results in a current of 114 A with a charging voltage of 1200 V corresponding to the designed operating point of the module in the inductive adder before the arrival of the reflected wave front in the first interval. For the tests the total pulse length has been adjusted to 400 ns. The rise time for both voltage and current has been measured to be 5.4 ns for a charging voltage of 600 V and 5.0 ns for a charging voltage of 1200 V as shown in fig. 3.24. This fulfills the requirement of a rise time of the load current with a resistive load of less than 6 ns.

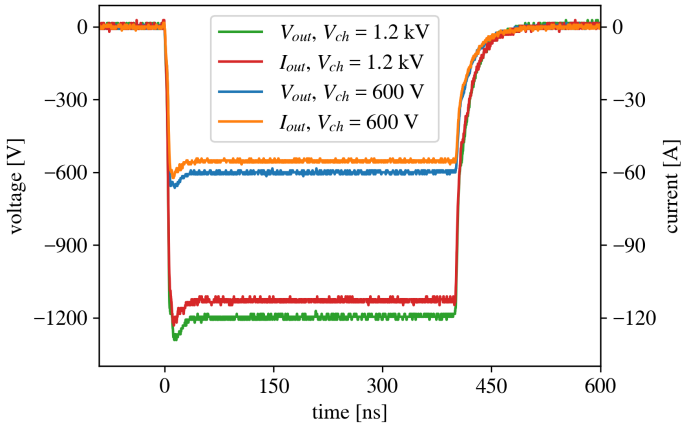


Figure 3.23: Output voltage V_{out} of the branch module and load current I_{out}, operated with a resistive load of 10.5 Ω for the charging voltages V_{ch} 600 V and 1200 V.

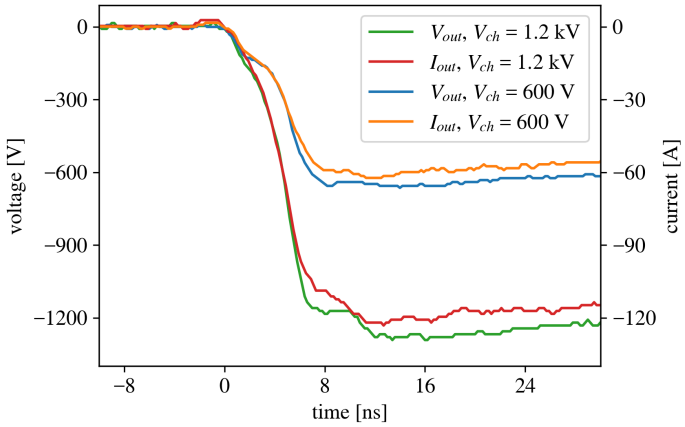


Figure 3.24: Zoom on the rising edge of the measurements shown in fig. 3.23.

4 Tests with a Short-Circuit Mode Replacement Load

4.1 Short-Circuit Mode Replacement Load

As described in sec. 1.1.1.1, a transmission line type kicker magnet approximates a broadband transmission line. Therefore, to test the branch module and the behavior of an inductive adder with a short-circuit terminated load, a replacement load consisting of five $50\,\Omega$ coaxial cables connected in parallel is used. Figure 4.1 shows a photo of the short-circuit mode replacement load. The coaxial cables of type CK50 [36] have a length of approximately $50\,\mathrm{m}$ and are connected in parallel at the input end. At the other end, each cable is individually terminated with a short-circuit, and the lengths of the cables are matched to provide an equal one-way signal propagation time of $208\,\mathrm{ns}$ with a tolerance of less than $100\,\mathrm{ps}$. Thereby, these parallel coaxial cables represent both a transmission line type kicker magnet with a characteristic impedance of $10\,\Omega$ and an impedance matched connecting cable. The one-way signal propagation time of $208\,\mathrm{ns}$ is approximately equal to that of the KFA10 kicker system (table 1.1). The characteristic impedance of $10\,\Omega$ is approximately the equivalent impedance that a single branch module is designed to operate into, making this replacement load useful for tests with single branch modules.

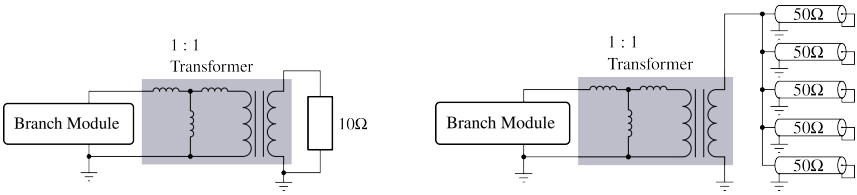
Figure 4.1: Five 50 Ω coaxial cables used as a replacement load for a short-circuit terminated kicker system with a characteristic impedance of 10 Ω. The cables are connected in parallel on the input side, individually short-circuit terminated, and have a matched one-way signal propagation time of 208 ns.

4.2 Pulse Length and Core Saturation

To demonstrate the possibility of longer pulses with a given magnetic core in short-circuit mode, as described in sec. 2.3, comparative tests were performed with the branch module connected via an output transformer to a resistive load and to the short-circuit mode replacement load.

4.2.1 Test Setup

Simplified schematics of the two test setups are shown in fig. 4.2. A short-circuit mode branch module is connected to a single layer of an inductive adder assembly, used as an output transformer with a single turn primary and secondary winding. The magnetic core is a nanocrystalline tapewound core made of Vitroperm 500F



(a) Test setup with a resistive load.

(b) Test setup with the short-circuit mode replacement load.

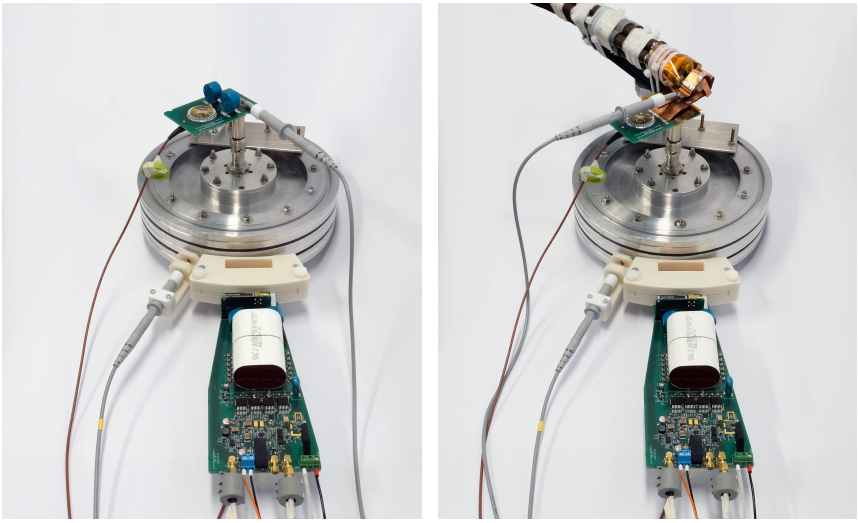
Figure 4.2: Simplified schematics of the test setup to demonstrate the possibility of longer pulses with a given magnetic core in short-circuit mode.

[74] material. The toroidal magnetic core has a height of $20\,\mathrm{mm}$, an inner diameter of $102\,\mathrm{mm}$ and an outer diameter of $160\,\mathrm{mm}$ and is operated without biasing. The nominal voltage-time integral of the core is $0.48\,\mathrm{kV\,\mu s^{-1}}$. The secondary winding is connected either to a resistive load of $10\,\Omega$ or to the short-circuit mode replacement load (sec. 4.1) with a characteristic impedance of $10\,\Omega$. Thereby, the resistive load of $10\,\Omega$ is a replacement load for a kicker system with a characteristic impedance of $10\,\Omega$ terminated with a matched impedance. For the resistive load test, the switch Q_{aux} (fig. 3.3) is closed during the test. For the short-circuit mode test, the branch module uses a matched resistor R_{abs} (fig. 3.3) of $10\,\Omega$ to dissipate the energy absorbed in the third interval (sec. 2.2). Figure 4.3 shows photos of both test setups.

4.2.2 Results

Figure 4.4 shows the measurements of the primary voltage V_{prim}, the secondary voltage V_{sec}, the primary current I_{prim} and the secondary current I_{sec} for both tests.

The tests were performed with a charging voltage of $1\,\mathrm{kV}$. The difference between I_{prim} and I_{sec} shows the current through the magnetizing inductance of the output transformer superimposed with a current due to core losses. For the resistive load, the magnetic core begins to saturate after approximately $500\,\mathrm{ns}$, as can be seen from the steeply rising magnetizing current, in the lower left graph in fig. 4.4.



(a) Resistive load. **(b)** Short-circuit mode replacement load.

Figure 4.3: Photos of the test setup to demonstrate the possibility of longer pulses with a given magnetic core in short-circuit mode.

For the test with the short-circuit mode replacement load, both the I_{sec} and V_{sec} show the expected general shape described in 2.1. Due to losses in the test setup, I_{prim} and I_{sec} show a stepwise decrease as described in 2.2.2. The length of the first interval has been set to $416\,\mathrm{ns}$, which is the two-way signal propagation time of the short-circuit mode replacement load. During interval one, the primary current follows the primary current in the test with the resistive load. However, as can be seen from the difference between I_{prim} and I_{sec} in the lower right graph in fig. 4.4, the magnetizing current does not increase further during interval two, where V_{prim} and V_{sec} are zero. The combined length of interval one and interval two is equal to the FWHM pulse width of the field in the kicker magnet. For the measurement in fig. 4.4 this time has been adjusted to $2\,\mu\mathrm{s}$. The measurements show that the inductive adder in short-circuit mode allows for an increased pulse length, for a given magnetic core, compared to a system terminated in a matched impedance [75].

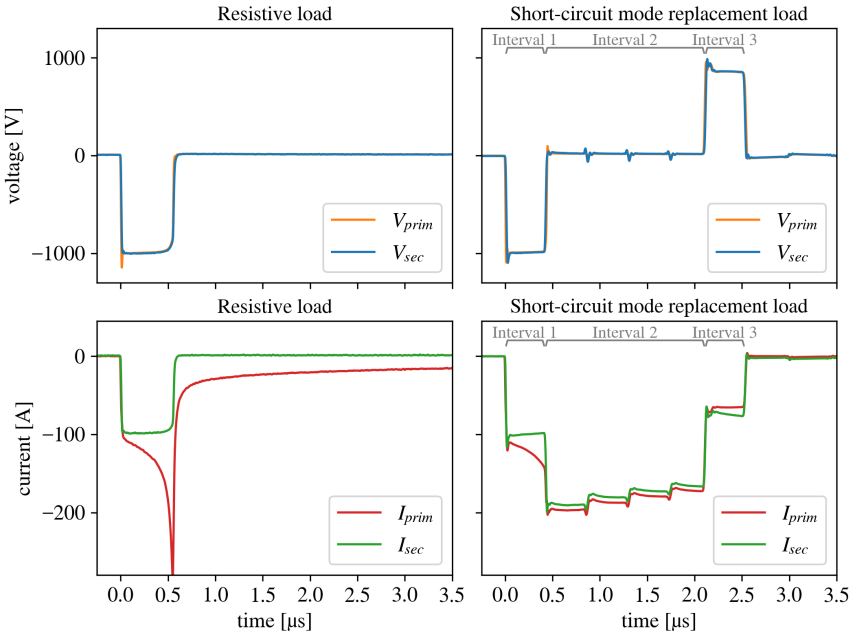


Figure 4.4: Primary and secondary voltages (top row) and currents (bottom row) for a single layer (output transformer) of an inductive adder. Comparison between a resistive load (left column) and the short-circuit mode replacement load (right column).

4.3 Loss Compensation

Figure 4.5 shows a simplified schematic of a test setup for investigating the compensation of losses during the second interval by injecting a constant voltage into the load via a separate layer of an inductive adder, as described in sec. 2.2.2. A picture of the test setup is shown in fig. 4.6.

One branch module is connected in the top layer, of a five-layer inductive adder stack, and another branch module is connected in the second layer from the top. The primary windings of the unused three layers at the bottom of the stack are shorted using copper plates inserted into the slots of the aluminium core housings. The inductive adder stack used as a testbed comprises the cores described in

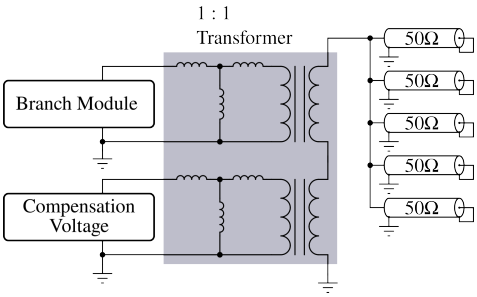


Figure 4.5: Simplified schematic of a test setup to investigate the compensation of losses during interval two by a constant voltage applied to the load via a separate layer of an inductive adder (sec. 2.2.2).

sec. 2.3 and uses a cylindrical stalk with air as dielectric between the stalk and the core housings. The magnetic cores are biased using a current of $1\,\mathrm{A}$ via a separate secondary winding connected to a power supply with a $1.9\,\mathrm{mH}$ inductor in between for transient insulation.

The upper branch module is equipped with a resistor $\mathrm{R_{abs}}$ of $10\,\Omega$ and operates in short-circuit mode as described in sec. 2.2. The lower branch module is used to output a rectangular voltage pulse during interval two to counteract losses in that interval. The magnitude of the compensation voltage is set by the charging voltage of the branch module used for loss compensation.

Measurements are taken of the output voltage of the inductive adder V_{sec}, the primary voltage of the layer used for loss compensation V_{comp}, the secondary current I_{sec} and the current at the short-circuit termination of one of the coaxial cables making up the short-circuit mode replacement load $I_{term}/5$. The parallel connection of the coaxial cables of the short-circuit mode replacement load at the output of the inductive adder, and the nominally equal characteristic impedance and signal propagation time in the cables, foster equal waves propagating in all the cables. Therefore, the current measured at the short-circuit termination of one of the cables represents one fifth of the current at the termination of an

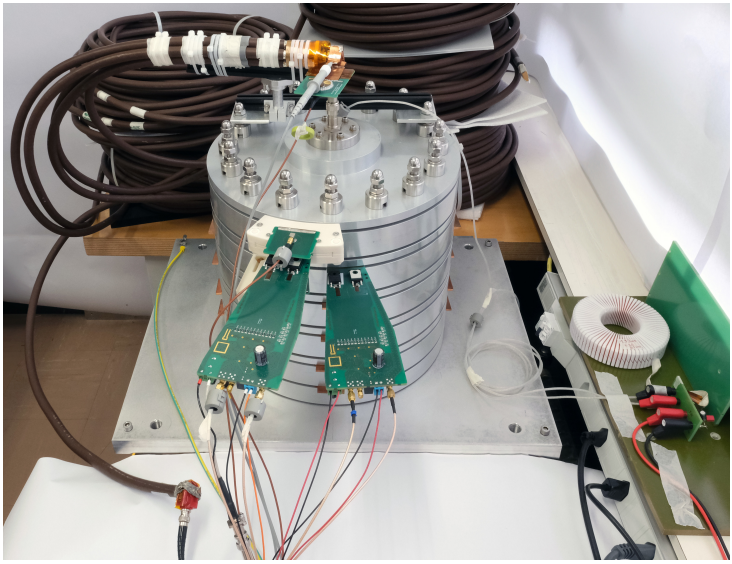


Figure 4.6: Photo of the test setup used to investigate the compensation of losses during interval two by a constant voltage applied to the load via a separate layer of an inductive adder (sec. 2.2.2).

equivalent system with a characteristic impedance of $10\,\Omega$ and only one short-circuit termination. The current at the short-circuit termination is measured using a current transformer of type CT-B1.0B [76].

As a reference, fig. 4.7 shows a measurement using the test setup shown in fig. 4.6 with the compensation voltage V_{comp} set to $0\,\mathrm{V}$. The charging voltage for the branch module in short-circuit mode was set to $1.2\,\mathrm{kV}$, the pulse length (Interval 1 + Interval 2) was set to $3\,\mu\mathrm{s}$. Both the current at the output of the inductive adder I_{sec} and the current at the short-circuit termination $I_{term}/5$ show a loss-induced stepwise decrease with a superimposed rising slope during each step due to the frequency-dependent attenuation of the pulse during its first pass through the transmission line, as described in sec. 2.2.2.

For the measurement shown in fig. 4.8, a compensation voltage of $63\,\mathrm{V}$ was applied during interval two via the branch module of the second from the top

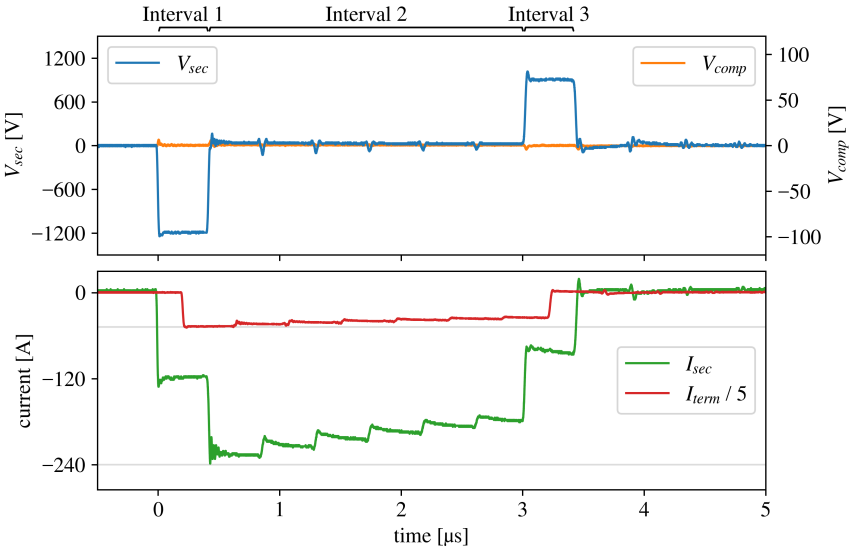


Figure 4.7: Measurement of a 3 µs pulse with the test setup in fig. 4.6 without loss compensation. The branch module operating in short-circuit mode is equipped with a resistor R_{abs}.

layer of the inductive adder. The value of the compensation voltage was adjusted iteratively until I_{sec} and $I_{term}/5$ were as flat as possible for the test setup used. The 63 V is approximately 5 % of the short-circuit mode branch module voltage.

Figure 4.9 shows a measurement with the pulse length set to 5 µs and with the same compensation voltage of 63 V. The measurements show, that the loss-induced stepwise decrease of I_{sec} and $I_{term}/5$ is well compensated, using this method, even for a longer pulse.

4.4 Magnetic Core Reset in Short-Circuit Mode

As described in sec. 2.3.1.4, for an inductive adder operating with a load terminated in a matched impedance, a reset of the magnetic cores is required between pulses to avoid saturation of the cores. For the inductive adder operating in short-circuit

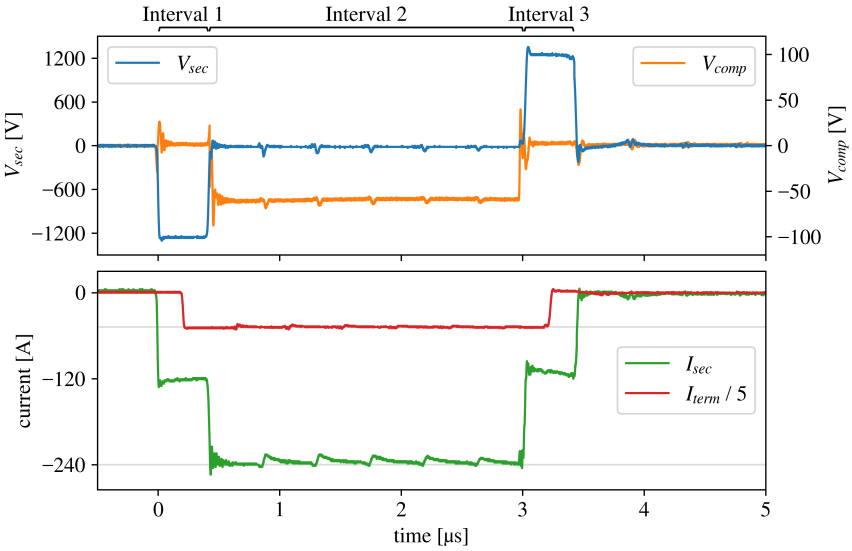


Figure 4.8: Measurement of a 3 µs pulse with the test setup in fig. 4.6 using a loss compensation voltage of V_{comp} = 63 V. The branch module operating in short-circuit mode is equipped with a resistor R_{abs}.

mode, the total voltage time integral of the layer voltage is close to zero. Therefore, the magnetic state of the core is approximately the same before and immediately after the pulse. To demonstrate this, the test setup shown in figs. 4.5 and 4.6 was used to generate a burst of 120 pulses with a FWHM pulse width of 800 ns at a pulse repetition rate of 300 kHz into the short-circuit mode replacement load. The branch module operating in short-circuit mode is equipped with a resistor R_{abs}, and no loss compensation is used. The biasing of the cores was turned off before the start of the measurement. Figure 4.10 shows a measurement of the inductive adder's output voltage V_{sec}, the primary current I_{prim}, the secondary current I_{sec} and the current at one of the short-circuit terminations of the load $I_{term}/5$.

Because the current $I_{term}/5$ exceeds the maximum $I*t$ of the current transformer [76] used, the measurement of $I_{term}/5$ is distorted for the second half of the lower graph of fig. 4.10 (dashed line). The amplitude of the pulses at the output of the inductive adder (V_{sec}) decreases from pulse to pulse due to a decrease in the

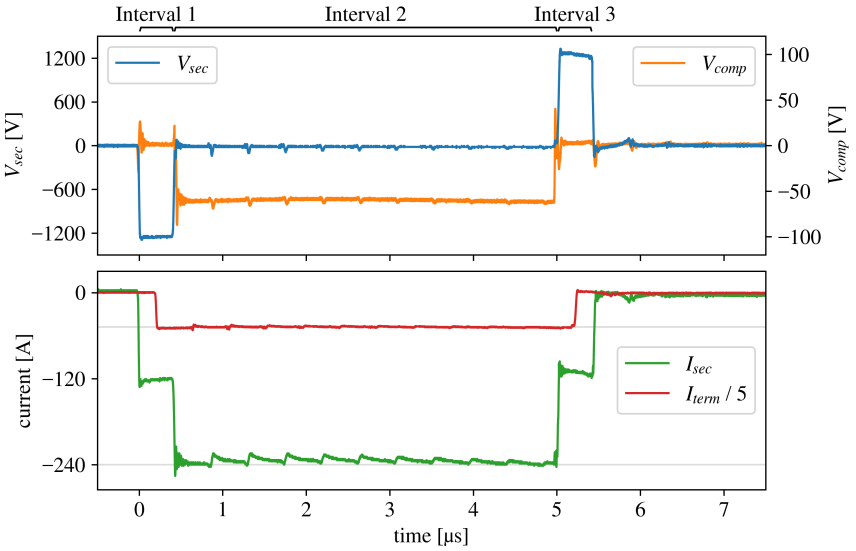


Figure 4.9: Measurement of a 5 µs pulse with the test setup in fig. 4.6 using loss compensation voltage V_{comp} = 63 V. The branch module operating in short-circuit mode is equipped with a resistor R_{abs}.

voltage of the pulse capacitor and its charging circuit not being designed for the mode of operation used in this test. Nevertheless, the measurements show that the magnetizing current ($I_{prim} - I_{sec}$) remains approximately the same throughout the burst, and is close to 0 A between pulses. This indicates that the magnetic core is approximately reset after each pulse in short-circuit mode.

4.5 Operation with Recuperation in the Third Interval

The short-circuit mode branch module developed in this work allows for two variants for handling the energy absorbed from the load in the third interval (sec. 2.2). In the previous measurements, a matched resistor R_{abs} was used for this purpose, which dissipates the absorbed energy. In order to investigate the use

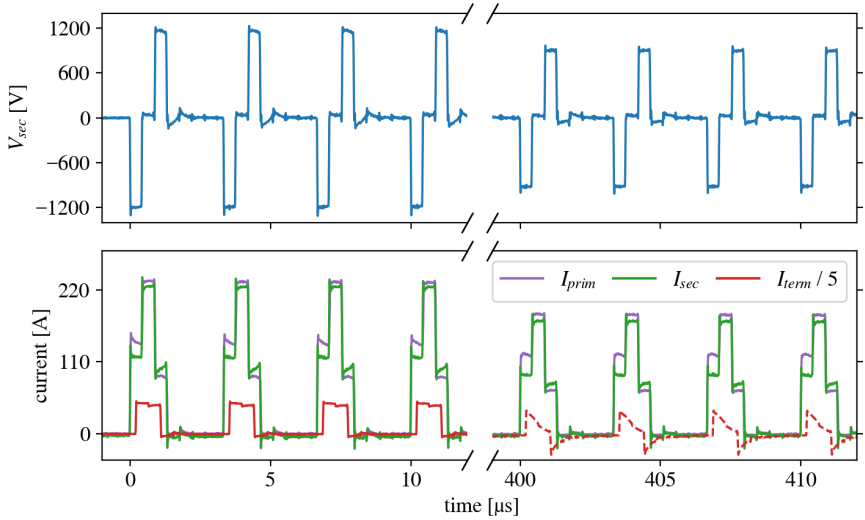


Figure 4.10: Operation with a burst of 120 pulses with a pulse width of 800 ns at a pulse repetition rate of 300 kHz to demonstrate core reset requirements in short-circuit mode. The current measurement at the termination of one of the five cables of the short-circuit mode replacement load ($I_{term}/5$) is skewed for the second half of the graph (dashed line) due to the signal exceeding the max. $I * t$ of the current transformer [76] used.

of a diode D_{rec} to recuperate the absorbed energy back into the pulse capacitor, the branch module operating in short-circuit mode, which is part of the test setup shown in figs. 4.5 and 4.6, was equipped with a diode D_{rec}.

Figure 4.11 shows a measurement without the use of loss compensation. During interval three, the recuperation diode D_{rec} is conducting (sec. 2.2) and the voltage of the pulse capacitor is applied across the load. This does not represent a true matched state, and the traveling wave arriving at the pulse generator in interval three is absorbed without reflections only if the amplitude of the incoming wave and the voltage of the pulse capacitor match. Since the amplitude of the traveling wave has decreased due to losses at the beginning of the third interval, the difference between the voltage of the pulse capacitor and the amplitude of the wave is reflected back into the load during interval three. This can be seen in the

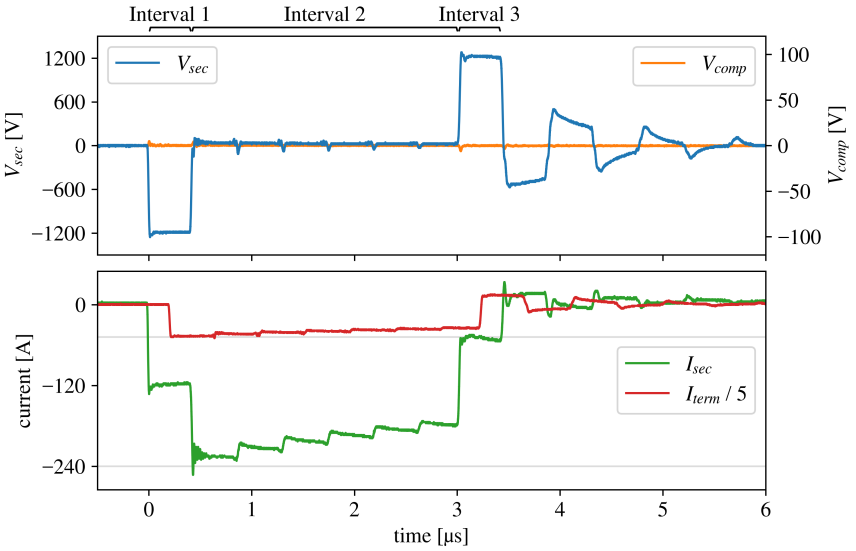


Figure 4.11: Measurement of a 3 µs pulse with the test setup in fig. 4.6 without loss compensation. The branch module operating in short-circuit mode is equipped with a diode D_{rec}.

traveling wave oscillation of the inductive adder output voltage V_{sec} after the end of the pulse.

Figure 4.12 shows a measurement using recuperation with loss compensation via a constant voltage applied. Since the branch module behaves the same as with a resistor R_{abs} during the first two intervals, the same compensation voltage of 63 V is used. The measurement shows that with loss compensation using a constant voltage in interval two, the reflections remaining after interval three are significantly reduced. Because the remaining ripple in the current flattop in interval two is not compensated (sec. 2.2.2) in this test, some reflections still occur in interval three. However, the test shows that the principle of using a diode to recuperate the energy absorbed from the load in interval three into the pulse capacitor is valid.

Figure 4.13 shows a comparison of the output voltage of the inductive adder using a branch module equipped with a resistor R_{abs} and a branch module equipped

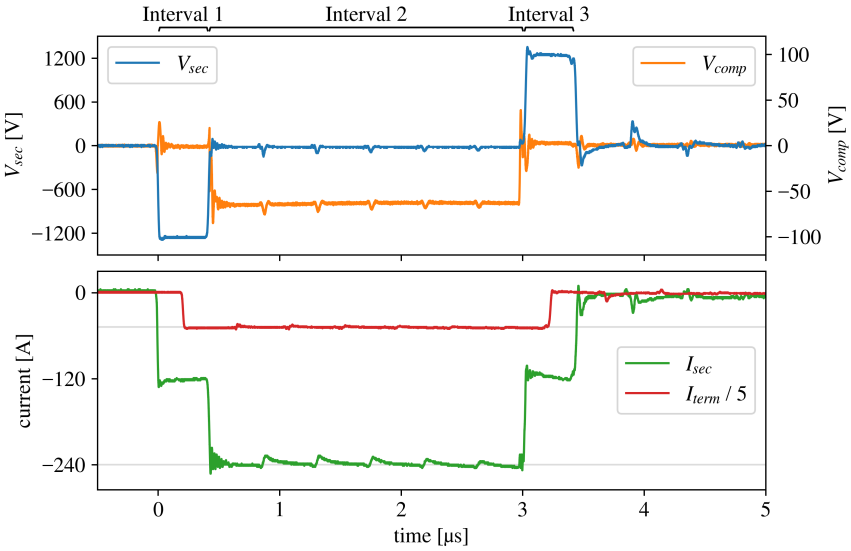


Figure 4.12: Measurement of a 3 µs pulse with the test setup in fig. 4.6 using the loss compensation voltage V_{comp} = 63 V. The branch module operating in short-circuit mode is equipped with a diode D_{rec}.

with a diode D_{rec}. The inductive adder is operated in a burst of 240 pulses at a pulse repetition rate of 300 kHz without the use of loss compensation. A short pulse length of 800 ns (FWHM) is used to reduce the losses during the pulse. The initial charging voltage of the pulse capacitor is 700 V for both tests. During the tests, the charging power supply was disconnected. The measurement shows that the voltage of the pulse capacitor after the burst, visible from the amplitude of the negative pulses (interval one), has decreased less for the measurement with recuperation of the absorbed energy (D_{rec}) compared to the measurement with dissipation of the absorbed energy (R_{abs}). This shows that for the branch module equipped with a diode D_{rec}, some energy is recovered during the third interval.

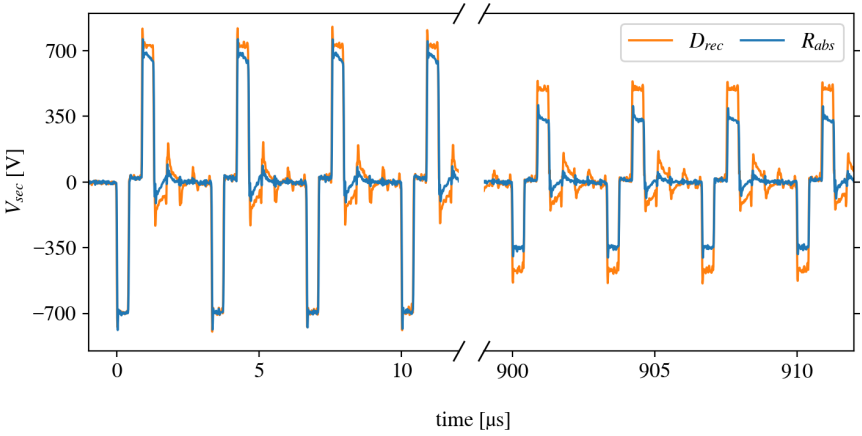


Figure 4.13: Comparison of the output voltage of the inductive adder (a) operated with a branch module using a diode D_{rec} and (b) operated with a branch module using a resistor R_{abs} for handling the energy absorbed in interval three. The inductive adder is operated in a burst of 240 pulses with an FWHM width of 800 ns at a pulse repetition rate of 300 kHz. The initial charging voltage for both tests is 700 V.

5 Summary and Outlook

In the frame of this work, the basic principles of an inductive adder for driving a transmission line type kicker magnet with a short-circuit termination have been developed. In this mode of operation, the inductive adder needs to handle the reflected wave from the short-circuit. As a novel approach, the inductive adder first injects energy into the connecting cable and the kicker magnet, then circulates the resulting current during a free-wheeling interval, and at the end of the pulse absorbs the energy. This new mode of operation allows for designing the magnetic cores based on the signal propagation time in the connecting cable and the kicker magnet rather than the length of the pulse. This enables the use of magnetic cores with a smaller cross-section than required for a comparable inductive adder operating into a matched load. Moreover, when using cores with a high remanent flux density, the cores are reset during pulse generation, and hence, are ready for the next pulse shortly after the previous pulse.

A novel circuit for a branch module for an inductive adder, suitable for the new mode of operation, has been designed and built. It features a topology with two actively controlled switches to handle reflections from the short-circuit termination. A precise modeling of the pulse circuit in simulations, enabled to effectively suppress oscillations in the output voltage by implementing specialized damping measures.

To protect the module, an overcurrent detection has been implemented and successfully tested, which is capable of stopping the current rise in less than $40\,\mathrm{ns}$ in the event of an overcurrent.

Using the gate-boosted operation of SiC-MOSFETs a fall time of $3.4\,\mathrm{ns}$ has been measured between the drain and the source of the MOSFETs, with an output

voltage of $1.2\,\mathrm{kV}$ and a current of $120\,\mathrm{A}$. A voltage and current rise time of $5\,\mathrm{ns}$ is achieved at the module output under equal conditions.

The branch module has been tested thoroughly and successfully in a test setup with a short-circuit terminated replacement load including the compensation of losses. The core reset during pulse generation, as part of the new mode of operation, was demonstrated successfully by operating the module at a pulse repetition of up to $300\,\mathrm{kHz}$. In addition, the recuperation of some of the energy from the load at the end of the pulse has been shown.

To demonstrate the use of magnetic cores with a smaller cross-sectional area, according to the new mode of operation, pulses have been generated which were much longer than they could have been when operating the core conventionally in an inductive adder connected to a matched load. This clearly demonstrates the advantage of shrinking the cross-sectional area of the magnetic core when using the new mode of operation.

The use of a tapered stalk in an inductive adder connected to a short-circuit terminated load has been investigated. Simulations showed that using a tapered stalk, the limit in rise time, due to wave propagation in the inductive adder assembly that occurs in the case of a cylindrical stalk, can be overcome. However, the scheme for controlling the semiconductor switches needs to implement sophisticated timing considering the propagation of the outgoing and reflected wave along the tapered stalk. The setup of an appropriate control circuit is planned for a later stage of the project. In the future, it is planned to build a full-scale inductive adder to be operated in one of the kicker systems at CERN. Future research will also focus on implementing compensation of the ripple induced by frequency-dependent losses in the system.

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