Decoupled Control Structure of a Modular Solid State Transformer

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***Index Terms*—Solid-State Transformer, Multi-level converters, Cascaded H-Bridge, Control strategy, AC-DC converter**

***Abstract*—This paper proposes a new control strategy for a three phase modular Cascaded-H-Bridge based Solid-State Transformer operating with a wide output voltage range. The control scheme incorporates AC grid side control, output voltage control and distributed cell voltage balancing. The balancing is assisted by feed forward of the oscillating phase powers. The cascaded structure enables highly dynamic and decoupled control of the DC output and AC grid side while limiting the cell voltage deviation. Measurements on a five-level laboratory prototype validate the control concept.**

I. Introduction

Solid State Transformers (SSTs) are power electronic systems which incorporate one or multiple Medium Frequency Transformers (MFTs) for galvanic isolation. In recent years, SSTs have attracted much attention due to their advantages over Line Frequency Transformers (LFTs), such as smaller size, ability to compensate for reactive power and harmonics, as well as controllability of voltage and power flow [1]. Due to these advantages, SSTs are applied for data centers, in smart grids, for renewable energy integration and as replacements for conventional LFTs. This paper considers an SST for interfacing a DC microgrid with the Medium Voltage Alternating Current (MV-AC) grid. The two-stage topology shown in Fig. 1a) was proposed in [2] and is based on a three phase Cascaded H-Bridge (CHB) converter in star connection. Each of the series connected CHB cells shown in Fig. 1b) consists of a full bridge on the AC side for AC-DC conversion and a Dual Active Bridge (DAB) to provide the galvanic isolation to the DC side.

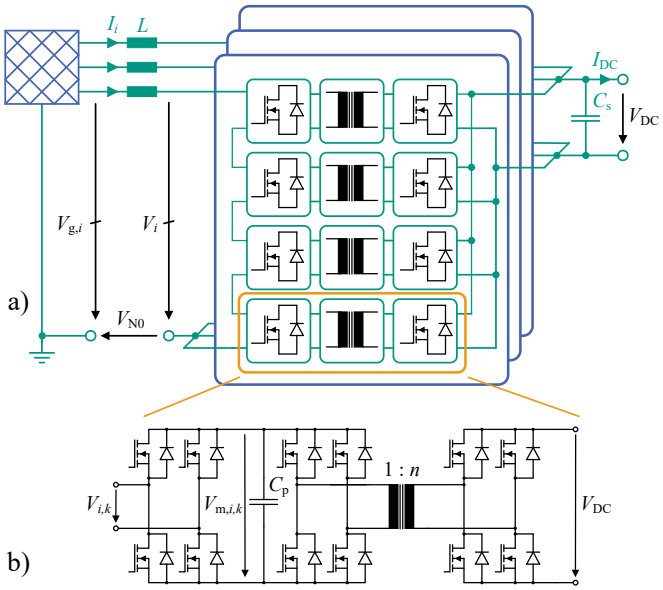

Fig. 1: a) Structure of the modular SST system and b) Schematic of the SST cell

The considered SST has two external ports: a three phase AC port and a DC port.

Due to the complex system structure of the considered SST, a sophisticated control scheme is necessary. Depending on the application, the SST needs to control the voltage or current of one or both of the external ports. Additionally, a voltage and power balancing scheme of the series connected cells needs to be incorporated.

Various approaches for the control structure of CHB based SSTs have been discussed in the literature, which can be divided into two main groups depending on applied voltage balancing algorithm. The conventional approach utilises a Pulse Width Modulation (PWM)-scheme for the CHB cells to balance the cell volt-

ages, adjusting the duty cycle of the individual cells. It was described for Static Synchronous Compensators (STATCOMs) [3], [4], active rectifiers [5], [6] and SSTs [7]–[10]. However, as described in [11] and [12], the adjustment of the duty cycles of each CHB cell leads to additional lower frequency harmonics in the output voltage spectrum if combined with Phase-Shift Pulse Width Modulation (PS-PWM). Additionally, the control bandwidth of the CHB cell voltage balancing is limited.

The second control structure approach uses the DABs feeding the CHB cells to balance the CHB cell voltages $V_{\mathrm{m},i,k}$. This strategy enables the usage of arbitrary CHB cell modulation schemes without limitations or drawbacks imposed by the cell voltage balancing. Furthermore, this approach provides better power balancing [13] and routing [11], improved output voltage spectrum [12] and higher control bandwidth [14], [15].

Besides the voltage balancing, the DABs can also be used to control the output voltage V_{DC}. In this case, the CHB converter needs to control the sum of the cell voltages [13]. Therefore, the DABs are responsible for two objectives: Control the voltage V_{DC} and balance the cell voltages $V_{\mathrm{m},i,k}$.

In most SST applications, the DABs operate in a narrow voltage band, since the DC output voltage and the cell voltages are fixed. In these cases, the DABs work in unity gain with Singe Phase Shift (SPS) modulation, which is favourable due to the low circulating current and soft switching operation [16]. However, in wide voltage gain scenarios, e.g. a direct battery connection on the Direct Current (DC) port or high power charging for commercial vehicles, more advanced modulation schemes may become necessary [17]. This paper introduces a control scheme which enables cell voltage balancing and provision of reactive power to the AC side while offering output voltage control in a wide range for a three phase CHB converter system.

II. Three phase SST model

The analysed converter topology, a the three phase, star connected SST system is shown in Fig. 1a. Each of the phases is build up from identical SST cells, which are connected in series on the MVAC side and connected in parallel on the LVDC side. Each SST cell consists of the input CHB cell, a DC-link capacitor and two full bridges, connected via a MFT, which form a DAB. The DAB is necessary to provide a galvanically isolated power supply for the CHB cell. In contrast to resonant DCDC converters, the DAB can operate in a wide voltage range and easily control the transferred

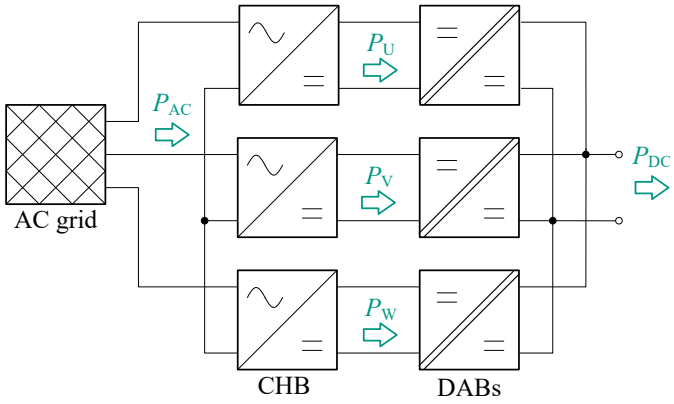

Fig. 2: Simplified model of the three-phase SST

power. The series connected CHB cells operate as a rectifier to the AC grid.

The analysis of the SST converter is carried out for lossless converter operation in steady state condition, assuming ideal sinusoidal grid current and grid voltage. The simplified SST model, which neglects the intra phase cell voltage balancing, is shown in Fig. 2. Although the power P_{AC} obtained from the AC grid and transferred to the DC port is constant, each of the converter phases (U,V,W) will experience a variable instantaneous power. The power of each converter phase for a symmetric AC grid is described by (1).

$$\begin{aligned} P_i(t) =& \frac{\hat{I}\hat{V}_{\mathrm{g}}}{2} \begin{bmatrix} \cos(\varphi) + \cos(2\omega t + \varphi) \\ \cos(\varphi) + \cos(2\omega t - \frac{2\pi}{3} + \varphi) \\ \cos(\varphi) + \cos(2\omega t - \frac{4\pi}{3} + \varphi) \end{bmatrix} \\ & - \frac{\hat{I}V_{\mathrm{N0}}(t)}{2} \begin{bmatrix} \cos(\omega t + \varphi) \\ \cos(\omega t + \frac{2\pi}{3} + \varphi) \\ \cos(\omega t + \frac{4\pi}{3} + \varphi) \end{bmatrix} \end{aligned} \tag{1}$$

The amplitudes of the grid voltage and grid current are denoted as $\hat{V}_{\mathrm{g}}$ and $\hat{I}$. φ describes the phase displacement between the converter output voltage and the grid current, $\omega = 2\pi f_{\mathrm{grid}}$ is the grid frequency and $v_{\mathrm{N0}}(t)$ is the zero voltage component, which describes the voltage difference between the converter star point and the grid star point. It can be observed that the instantaneous power consists of three components: a constant component, which is dependent on the power factor $\cos(\varphi)$, a component which oscillates with twice the grid frequency and a component which is dependent on the grid current and the zero voltage component. Fig. 3 shows the grid voltage, current and the phase power for an operation point with $\cos(\varphi) = 0.9$ and a triangular zero voltage component v_{N0}.

Applying the Clarke Transformation [18] to (1) re-

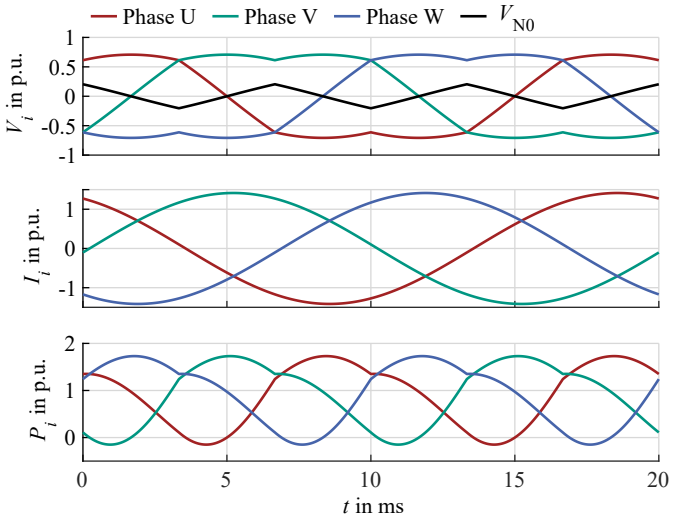

Fig. 3: Idealized AC-side voltages and currents as well as phase power of the SST converter

sults in (2).

$$P_{\alpha\beta 0}(t) = \frac{\hat{I}\hat{V}_{\mathrm{g}}}{2}\begin{bmatrix}\cos(2\omega t+\varphi)\\ \sin(2\omega t+\varphi)\\ \cos(\varphi)\end{bmatrix} + \frac{\hat{I}V_{\mathrm{N0}}(t)}{2}\begin{bmatrix}\cos(\omega t+\varphi)\\ -\sin(\omega t+\varphi)\\ 0\end{bmatrix} \tag{2}$$

With this representation, the constant power, which is transferred from the AC grid to the DC port, is expressed by $3P_0$ while P_α and P_β describe the reactive power, which is oscillating internally between the converter phases and is influenced by the double frequency ripple and the zero voltage component. The oscillating power needs to be supplied by the DABs, which can result in reduced efficiency [19], or can be buffered by the DC-link capacitors. Since the frequency of the oscillating power is relatively small, buffering of the power leads to bulky DC-link capacitors C_{p}, which increases the total costs and the required space. Here, the converter control with small DC-link capacity is investigated.

The power distribution within a phase depends on the CHB modulation scheme and the power routing scheme, which specify the mean cell AC output voltage $V_{i,k}$. The power $P_{i,k}$ of an individual cell can be calculated using

$$P_{i,k} = \frac{V_{i,k}}{\sum_{k=1}^{N} V_{i,k}} P_i \tag{3}$$

where $i = \{1,2,3\} \mathrel{\widehat{=}} \{U,V,W\}$ denotes the phase index, k the index of the cell and N the total number of cells per phase.

Fig. 4 shows the steady state model for a single phase with two cells, which is introduced in [14]. The AC side of the CHB converter is modelled from the grid voltage

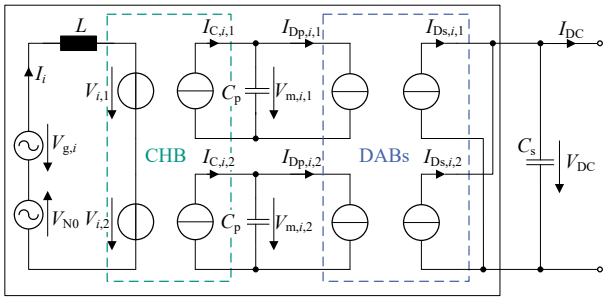

Fig. 4: Equivalent circuit diagram for a single phase of the SST converter

$V_{\mathrm{g},i}$, the zero voltage V_{N0}, the grid inductance L and the series connection of the cell AC output voltages $V_{i,k}$. The CHB cell is modelled as a current source on the DC-link side. The voltage and current sources are linked by the duty cycle $D_{i,k} \in [-1,1]$ of the CHB cell:

$$V_{i,k} = D_{i,k} \cdot V_{\mathrm{m},i,k} \tag{4}$$

$$I_{\mathrm{C},i,k} = D_{i,k} \cdot I_i \tag{5}$$

The DAB is modelled with two current sources. For the steady state, the ratio between the DAB currents $I_{\mathrm{Dp},i,k}$ and $I_{\mathrm{Ds},i,k}$ is given by:

$$I_{\mathrm{Ds},i,k} = \frac{V_{\mathrm{m},i,k}}{V_{\mathrm{DC}}} I_{\mathrm{Dp},i,k} \tag{6}$$

These steady state relationships are used to design the converter control and the feed forward structure.

III. Three Phase SST Control Structure

The proposed control structure includes the following parts:

- DC output voltage control
- CHB DC-link voltage control
- AC current control
- Distributed DC-link voltage balancing

In the following, the different parts of the control structure are explained.

A. Output Voltage Control

The SST controls the DC output voltage V_{DC} by manipulating the total current transferred by the DABs connected in parallel. The control structure is shown in Fig. 5. A PI controller calculates the total current $I^*_{\mathrm{DAB},0}$. The PI controller is tuned using the Symmetric Optimum [20]. To implement a feed forward for the cell voltage balancing, $I^*_{\mathrm{DAB},0}$ is distributed among the converter phases and cells using information from the CHB modulation. The reactive currents $I_{\mathrm{DAB},\alpha}$ and $I_{\mathrm{DAB},\beta}$,

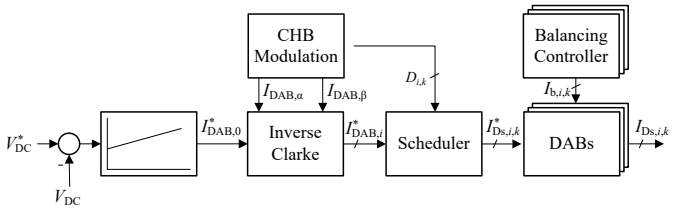

Fig. 5: Output voltage control with oscillating power feed forward

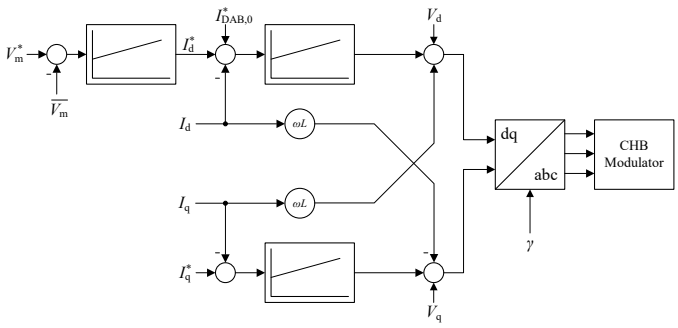

Fig. 6: Grid side control structure with the DC-link voltage controller and two current controllers in the dq-reference frame

which are oscillating between the phases are calculated with (7) by applying the Clarke Transformation to the mean value of the rectified phase current. The rectified phase current is the product of the phase duty cycle D_i, which is calculated using (8) and the measured phase current I_i.

$$\begin{bmatrix} I_{\mathrm{DAB},\alpha} \\ I_{\mathrm{DAB},\beta} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} I_{\mathrm{U}} \cdot D_{\mathrm{U}} \\ I_{\mathrm{V}} \cdot D_{\mathrm{V}} \\ I_{\mathrm{W}} \cdot D_{\mathrm{W}} \end{bmatrix} \tag{7}$$

$$D_i = \frac{1}{N} \sum_{k=1}^{N} D_{i,k} \tag{8}$$

The resulting phase set points $I^*_{\mathrm{DAB},i}$ are then calculated by combining the controller set point $I^*_{\mathrm{DAB},0}$ with the reactive currents $I_{\mathrm{DAB},\alpha}$ and $I_{\mathrm{DAB},\beta}$ and using the inverse Clarke Transformation. Within each phase, the scheduler uses the individual cell duty cycles $D_{i,k}$ to distribute $I^*_{\mathrm{DAB},i}$ between the different cells:

$$I^*_{\mathrm{Ds},i,k} = I^*_{\mathrm{DAB},i} \cdot D_{i,k} \tag{9}$$

B. AC Grid Side Control

Since the DABs control the output voltage V_{DC}, the sum of the cell voltages needs to be controlled by the CHB cells. The cascaded control structure, which consists of an outer voltage control loop and two inner current control loops in a rotating reference frame is shown in Fig. 6. The active power is controlled by the I_{d}-controller, while the reactive power is controlled by the I_{q}-controller. The two PI controllers are decoupled to reduce their interaction. The current controllers are tuned using the Magnitude Optimum to optimise the response to set point changes [20]. A PI controller is used for the outer voltage control loop, which generates the set points for the active power of the converter. The voltage controller is tuned using the Symmetric Optimum [20]. The controller is supported by a feed forward of the set point $I^*_{\mathrm{DAB},0}$ generated by the output voltage controller. This reduces the influence of the output voltage control on the cell voltages $V_{\mathrm{m},i,k}$. The reactive power provided the AC grid is independent from the active power requested on the DC port and can be chosen arbitrarily under consideration of the maximum current of the converter.

C. Cell Voltage Balancing and DAB Modulation Scheme

Due to parameter variation, measurement inaccuracy and parasitic effects of the DABs and CHB cells, voltage differences between the CHB cells can occur. To counteract the voltage difference, the current $I^*_{\mathrm{DAB},0}$ requested by the DC voltage controller needs to be redistributed with regard to the individual cell voltages $V_{\mathrm{m},i,k}$. For each cell, a P controller with gain K_{b} is implemented which calculates a balancing current $I_{\mathrm{b},i,k}$ from

$$I_{\mathrm{b},i,k} = K_{\mathrm{b}} \left(\overline{V}_{\mathrm{m}} - V_{\mathrm{m},i,k} \right) \tag{10}$$

with

$$\overline{V}_{\mathrm{m}} = \frac{1}{3N} \sum_{i=1}^{3} \sum_{k=1}^{N} V_{\mathrm{m},i,k} \tag{11}$$

Using P-controllers for the balancing has the advantage that the sum of all balancing currents $I_{\mathrm{b},i,k}$ equals 0, as shown in (12).

$$\begin{aligned} \sum_{i=1}^{3} \sum_{k=1}^{N} I_{\mathrm{b},i,k} &= \sum_{i=1}^{3} \sum_{k=1}^{N} K_{\mathrm{b}} \left(\overline{V}_{\mathrm{m}} - V_{\mathrm{m},i,k} \right) \\ &= K_{\mathrm{b}} \left(3N \overline{V}_{\mathrm{m}} - \sum_{i=1}^{3} \sum_{k=1}^{N} V_{\mathrm{m},i,k} \right) = 0 \end{aligned} \tag{12}$$

Therefore, the cell balancing is decoupled from the output voltage control. The selection of the controller gain K_{b} is a trade-off between the stationary inaccuracy and the stability of the controller. An analytical derivation of K_{b} is difficult, since the voltage differences arise from to the design variations of the SST cells. Therefore, K_{b} was chosen empirically using measurements. Depending on

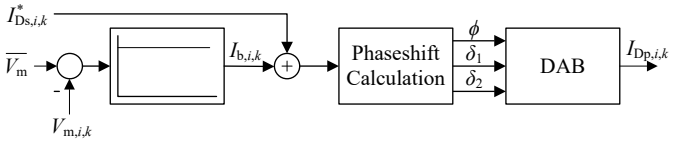

Fig. 7: Balancing controller and phase shift calcualtion of the DAB

TABLE I: Hardware Setup Parameter

Parameter	Value	Parameter	Value
N	2	$V_{\mathrm{m,max}}$	70 V
V_{AC}	125 V	f_{grid}	50 Hz
L	1 mH	P_{nom}	15 kW
f_{CHB}	50 kHz	f_{DAB}	50 kHz
C_p	1.38 mF	C_s	710 µF

the employed CHB-modulation scheme, the remaining deviation between the cell voltages due to the stationary inaccuracy of the P-controllers is acceptable.

Fig. 7 shows the balancing control structure of each cell. The current $I^*_{\mathrm{Ds},i,k}$ calculated by the output voltage controller and the balancing current $I_{\mathrm{b},i,k}$ are used to calculate the phase shifts for the DAB. Depending on the operation point, the controller chooses between SPS and Triangular Current Mode (TCM)-modulation. SPS-modulation is beneficial for unity voltage gain, while TCM allows the efficient operation in wide voltage gain operation points [21]. This enables the SST operation in a wide output voltage range, e.g. for direct connection to a battery storage. A more detailed description of the phase-shift calculation with regard to the wide output voltage range is given in [22].

IV. Implementation / Test Setup

The proposed control structure is implemented on a scaled down laboratory prototype shown in Fig. 8. The parameters of the five-level prototype are shown in Table I. Each phase of the SST consists of two identical converter cells, which incorporate power electronics, galvanic isolation, the necessary measurements and a Field Programmable Gate Array (FPGA) as the Local Control Unit (LCU). The LCU is responsible for communicating with a Central Control Unit (CCU), controlling the power electronics and monitoring the correct operation of the cell. The *ETI-SoC-System*, a modular signal processing platform based on a *Zynq™7030* System on Chip (SoC), is used as the CCU [23]. The CCU is responsible for the system operation, sequence control and central control of the SST.

The CHB cells apply the Phase-Disposition Pulse Width Modulation (PD-PWM) with a fixed modulation period T_A to generate the AC voltage [24]. For each phase, a single CHB cell is operating in PWM-mode, while the other CHB cells have a constant output voltage.

The timing diagram of the control structure is shown in Fig. 9. The digram shows two modulation periods of the SST, each with the duration T_A. The measurements are obtained using a sample and average strategy to reduce the sensors' noise. The sampling occurs symmetrical to the middle of the modulation period. Each LCU measures its CHB cell voltage $V_{\mathrm{m},i,k}$ and the output voltage V_DC, while the CCU measures the grid voltages V_i, the grid currents I_i and the output voltage V_DC.

The LCUs send the measurements via fiber optic links using a Universal Asynchronous Receiver Transmitter (UART)-protocol to the CCU. After receiving all CHB cell voltages, the CCU calculates the average value $\overline{V}_\mathrm{m}$ which is immediately sent back to all LCUs. Each LCU calculates its balancing current $I_{\mathrm{b},i,k}$ and the appropriate phase shifts for its DAB for the modulation period $m+1$ using the measurements from period m, leading to a very low latency for the balancing control loops. The control of the remaining system, including the DC output voltage and the AC grid side, is more complex and therefore consumes more computation time. The CCU calculates the set points $I^*_{\mathrm{DAB},i,k}$ and the duty cycles $D_{i,k}$ for each SST cell cell after receiving the measurements from the LCUs within one modulation period.

The LCUs synchronise their internal timing to the CCU using the data packets received from the CCU. This ensures that the modulation period is synchronised among all parts of the SST, which is necessary to ensure a deterministic behaviour of the converter.

V. Measurement validation

The proposed control scheme is validated using the prototype presented in the previous chapter. The measurements are shown in Fig. 10 to Fig. 12. The top graph shows the measured values V_DC and I_DC on the DC side and the voltage set point V^*_DC. In the second graph the CHB cell voltages $V_{\mathrm{m},i,k}$ are illustrated. The third graph depicts the AC-side currents I_i and the bottom graph shows the output voltages V_i of the SST.

In the first measurement, shown in Fig. 10, shows the change of the set point V^*_DC from 670 V to 720 V is analysed. V_DC has a rise time of 6 ms and a small overshoot. The CHB cell voltages drop initially, since the current rise time of the AC-side is limited by the filter inductance L and therefore slower than the DABs.

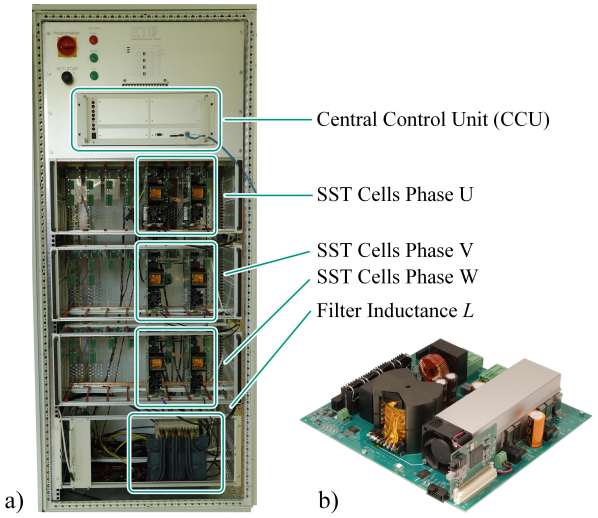

Fig. 8: a) Prototype of the SST converter and b) Single SST cell

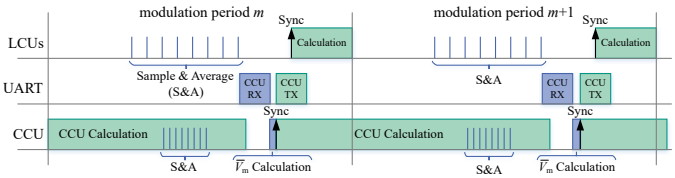

Fig. 9: Timing diagram of the SST

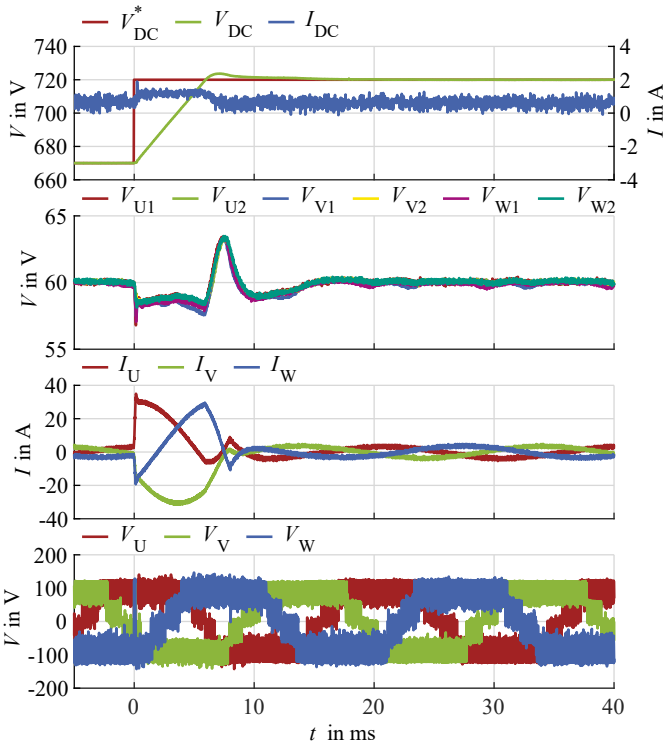

Fig. 10: Set point change of V^*_{DC} from 670 V to 720 V

After V^*_{DC} is reached, the CHB cell voltages rise, since the AC-side continues to supply current while the DABs already reduce their output current. During the whole process, the DC-link voltages are within 1 V of each other, which is a relative deviation of less than 2 %.

Fig. 11 depicts a set point change of I^*_q, causing a reactive power injection into the AC grid. After the set point is changed, both the output voltage V_{DC} and the CHB cell voltages $V_{m,i,k}$ have a small 100 Hz ripple with 180° phase shift, which could be caused by unfavourable parameter variations or the nonlinear transfer characteristic of the DABs [25], leading to a periodic error of $I_{DAB,0}$. This ripple could be reduced by estimating the individual parameters and nonlinearities of the DABs and adapting the control accordingly.

Fig. 12 shows a load step on the DC port. The output current changes from 5 A to −5 A, resulting in an increase of V_{DC}. The output voltage controller counteracts by adjusting $I_{DAB,0}$, which results in an increase of the cell voltages, since the CHB cells are not able to reverse their power fast enough. After 15 ms, the voltage has returned to the desired value and the converter is operating in steady state.

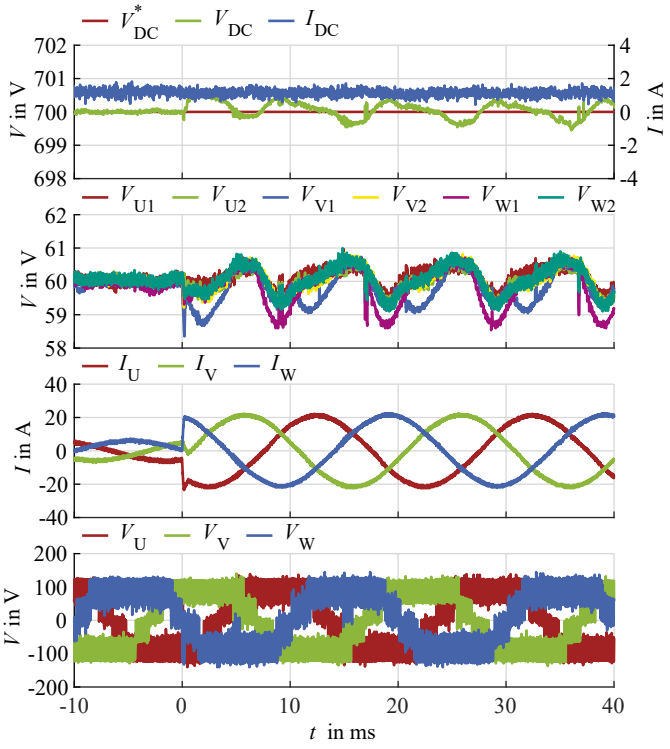

Fig. 11: Set point change of I_q from 0 A to 20 A while maintaining $I_{DC} = 1$ A

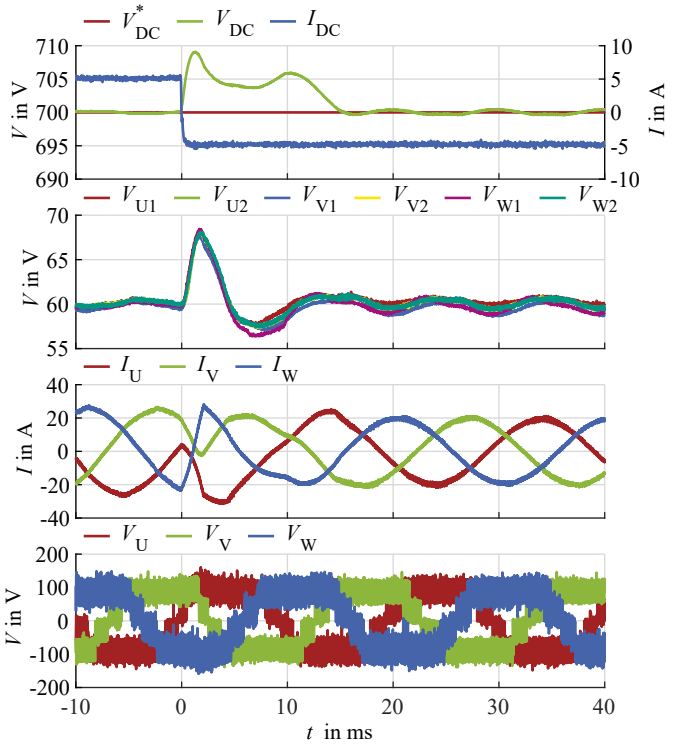

Fig. 12: Converter behaviour for a output load step from $I_{DC} = 5\,A$ to $-5\,A$

Although the three transient events lead to fast changing CHB cell voltages, the feed forward of the internally oscillating reactive power and the balancing controllers are able to keep the voltages deviation between the CHB cells in an acceptable range.

VI. Conclusion

This paper presents a control structure for a modular three phase SST. The control is based on the feed forward of the power oscillating between the converter phases, which is described using the Clarke Transformation of the converter phase powers. The structure allows an accurate control of the output voltage and reactive power while balancing the cell voltages of the CHB cells using the DABs. The parallelisation of the SST cells on the DC output side does not lead to undesirable circulating currents, even for transient operation point changes. The control structure has been tested on a five-level laboratory prototype. The measurements show very good steady state and transient behaviour with very low output voltage ripple and a good decoupling between the DC output and the AC grid side. Hence, the developed SST concept in combination with the applied control structure enables e.g. the direct power supply of large charging station parks from the medium voltage grid.

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