Impedance-based Stability Analysis of a Power Hardware-in-the-Loop for Grid-Following Inverter Testing

Fargah Ashrafidehkordi ¹ Institute of Technical Physics (ITEP) Karlsruhe Institute of Technology (KIT) Karlsruhe, Germany

Xiaochang Liu Powertrain Solutions Bosch Powertrain Systems Co., Ltd. Wuxi, China Xiaochang.LIU@cn.bosch.com Giovanni De Carne Institute of Technical Physics (ITEP) Karlsruhe Institute of Technology (KIT) Karlsruhe, Germany

Abstract—Power Hardware-in-the-Loop (P-HIL) provides a reliable evaluation of real hardware interactions under realistic grid conditions in the Laboratory environment. A P-HIL setup comprises three main sectors: real-time simulator, Hardwareunder-test (HuT), and interfaces. The limitations of interfaces and the delays between the sectors can result in stability issues. Therefore, a precise stability analysis is necessary before conducting laboratory experiments. This paper proposes the impedancebased approach to asses the stability constraints for a P-HIL using a grid-following inverter as HuT. The stability criterion is determined based on the impedances seen by the grid and the inverter at the PCC. The impact of interface dynamics, delays, and controller bandwidth is carefully regarded. All P-HIL components are implemented in Simulink first, then the actual setup with RTDS and linear amplifier has been configured to provide a more realistic reference for impedance verifications. The calculated impedances are verified with both simulations and experiments through frequency response. The comparison between the time domain response and the Nyquist criterion confirms the validity of the given stability criterion.

Index Terms—Power hardware-in-the-loop, impedance-based stability, grid-following inverter, voltage-type ideal transformer method, real-time simulation

I. INTRODUCTION

It is imperative to accurately evaluate the performance of new energy technologies, e.g., grid-connected converters, to assess their viability and potential for widespread adoption. The successful integration of these technologies into existing energy systems depends on the reality and reliability of testing-phase experiments. The contribution of Power Hardware-in-the-Loop (P-HIL) is well-known for de-risking experiments, providing cost-effective testing, validating models, and modeling methodologies [1]. P-HIL applications are growing significantly in many power and energy-associated societies, particularly in power electronics. In literature, a variety of these applications are investigated; namely, electrical motor drives [2], automotive and electric vehicles [3], energy storage [4], and grid converters [5]. As shown in Fig. 1(a),

in a P-HIL setup, the simulated test grid in a digital realtime simulator (DRTS) is replicated at the hardware level through a power amplifier. The sensors then measure physical variables and transmit them back to the DRTS. Analog/digital converters are required in interfacing the DRTS with the analog Hardware-under-Test (HuT). However, the conversion stages mentioned above compel delays, which devaluate the accuracy of test results and deteriorate the closed-loop stability [6]. Typical application-oriented interface algorithms are proposed to achieve higher stabilities and accuracies in [7]; among those Ideal Transformer Method (ITM) is known for its simplicity. This method requires a numerical low-pass filter to increase the system's stability [1]. Voltage-type ITM (V-ITM) is represented in Fig. 1(b), where the amplifier acts as a voltage source, emulating the grid conditions for the HuT, and the hardware current is feedback through the sensors.

The impedance-based method is proposed in [8] for the stability analysis of interactions of grid-connected inverters with the power grid, where the system's stability depends on the impedance ratio at the connection point. It has been shown that the Nyquist criterion can be applied to the impedance ratio for stability evaluation since the ratio represents the system's open-loop transfer function. In [9], the impedancebased method is developed for impedance shaping and stability improvement using bode plots of individual impedances rather than impedance ratio. Most grid-connected VSCs use current control in a rotating (dq) reference frame synchronized with grid voltages using a phase-locked loop (PLL) [10]. However, both the dq-domain current control and the PLL-based grid synchronization introduce nonlinearities in power electronic systems. Researchers in [11] investigate the harmonic linearization method to address this issue. This method directly models the impedance of the three-phase VSC in the phase domain, thereby bypassing the limitations associated with the dq reference frame approach. The current and voltage-type ITM P-HIL stability is studied in [12] through virtual/hardware impedances using passive load as HuT. In [13], the impedance of an AC network and MMC converter are estimated, and the impact of the filter configuration on the stability of a P-

This work was supported by the Helmholtz Association under the program "Energy System Design" and within the Helmholtz Young Investigator Group "Hybrid Networks" (VH-NG-1613).



Fig. 1. (a) Generic Scheme of P-HIL (b) Voltage-type ITM algorithm

HIL setup with the transmission line method (TLM) is shown through bode plots. The approach is further adopted in P-HIL setups, e.g., in [14], where authors employ a V-ITM P-HIL test bench to study the stability challenges of interconnecting grid inverters to a complex simulated power grid with a resonant spike in its impedance. However, an explicit approach must be included to ensure the stable operation of any HuTs in a P-HIL setup before conducting the lab experiments.

This paper provides the necessary and sufficient stability condition for a V-ITM P-HIL setup when a grid-following inverter is tested. This concept can effectively generalize the system's stability to any unknown Hardware under Test (HuT), ensuring robust and reliable stability evaluations across various test scenarios.

The remaining sections of this paper are structured as follows: In section II, the technique of the classic software/hardware impedance ratio in the P-HIL setup is developed for the emulated grid versus a grid-following inverter with an LCL filter, considering the influences of interfaces and inverter controller. In this section, the system is modeled using transfer functions, deliberately avoiding the PLL model. In section III, first, the computed impedances are verified respecting the implemented model in Simulink. Then the stability of the setup is demonstrated by changing the grid-side impedance and using the Nyquist plots. The Nyquist criterion is compared with the Simulink model for stable and unstable cases. Finally, in section IV, experimental results are provided operating an RTDS with a linear amplifier using a gridfollowing converter as HuT to verify calculated impedance validity realistically. Finally, in section IV, experimental results are provided operating an RTDS with a linear amplifier using a grid-following converter as HuT to verify calculated impedance validity realistically.

II. IMPEDANCE MODEL OF THE P-HIL SETUP

This section represents the impedance-based modeling of a V-ITM P-HIL setup, where HuT is a grid-following inverter tied to the DRTS through a linear amplifier. Each section is formulated through their transfer functions, and the equivalent impedance model of the setup is proposed. The Nyquist criterion is then applicable to the calculated impedance ratio of the V-ITM P-HIL setups.

The Thévenin equivalent is used for the virtual grid model in DRTS. As shown in Fig. 1b, it is a voltage source (V_s) with a series impedance (Z_s) . This impedance consists of a resistance and an inducance in series which is formulated in (1). The measured voltage after $Z_s(s)$ is applied to the HuT through a D/A converter and the amplifier with their transfer functions as follows:

$$Z_s(s) = L_s s + R_s \tag{1}$$

$$G_{Amp}(s) = e^{-(T_{Amp})s} / ((1/\omega_0)s^2 + (2D/\omega_0)s + 1)$$
 (2)

$$G_{D/A}(s) = e^{-(T_{D/A})s}$$
 (3)

$$G_{DRTS}(s) = e^{-(T_{DRTS})s} \tag{4}$$

$$G_{ifw}(s) = G_{Amp}(s) \times G_{D/A}(s) \times G_{DRTS}(s)$$
(5)

Where ω_0 and D are the resonant frequency and the damping factor of the amplifier, respectively. T_{Amp} , $T_{D/A}$, and T_{DRTS} are associated delays and $G_{ifw}(s)$ is the forward path within the interface section (Fig.1b).

Similarly, the backward path, $G_{ifb}(s)$ involves:

$$G_{ifb}(s) = G_{Sensor}(s) \times G_{A/D}(s) \times G_{Filter}(s)$$
(6)

$$G_{Sensor}(s) = e^{-(T_{Sensor})s}$$
⁽⁷⁾

$$G_{A/D}(s) = e^{-(T_{A/D})s}$$
 (8)

$$G_{Filter}(s) = \omega_c / (s + \omega_c) \tag{9}$$

Where T_{Sensor} and $T_{A/D}$ are the sensor and A/D converter delays, and ω_c is the cut-off frequency of the low-pass filter. According to Fig.2, the transfer function of the LCL filter $(Z_{HuT}$ in Fig. 1b) is divided respecting the influence of the grid side, $Y_{LCL,V}(s)$ and the converter side $Y_{LCL,V_{HuT}}(s)$:

$$Z_L(s) = L_f s + R_{fl} \tag{10}$$

$$Z_C(s) = 1/(C_f s) + R_{fc}$$
(11)

$$i = Y_{LCL, V_{HuT}}(s) \times V_{HuT} + Y_{LCL, V}(s) \times V \quad (12)$$

$$Y_{LCL,V}(s) = \{i/V\}_{V_{HuT}=0}$$

= $\frac{Z_C(s) + Z_L(s)}{2 \times Z_C(s) \times Z_L(s) + Z_L(s)^2}$ (13)

$$Y_{LCL,V_{HuT}}(s) = \{i/V_{HuT}\}_{V=0} = \frac{Z_C(s)}{2 \times Z_C(s) \times Z_L(s) + Z_L(s)^2}$$
(14)

The controlled variable, i, is the variable connecting the software and hardware sides, and it represents the impedance model of the setup. Through the KVL from V_s to PCC point, V:

$$V = (V_s - G_{ifb}(s) \times Z_s(s) \times i) \times G_{ifw}(s)$$
(15)

$$i = \underbrace{\frac{1}{G_{ifb}(s) \times Z_s(s)}}_{H_{grid}(s)} V_s \underbrace{+ \frac{1}{G_{ifb}(s) \times Z_s(s) \times G_{ifw}(s)}}_{Y_{grid}(s)} V_{grid}(s)}$$
(16)



Fig. 2. Grid-following inverter as HuT



Fig. 3. Current controller structure

According to (16), the current at the PCC point can be presented with chosen coefficients, $H_{grid}(s)$, and $Y_{grid}(s) = 1/Z_{grid}(s)$. According to the Fig. 3, relation between V_{HuT} and reference current, i^* is explained as:

$$V_{HuT} = (i^* - T_d(s) \times i) \times G_{PI}(s) \times T_d(s)$$
(17)

And applying (17) in (12), the effect of the inverter side at PCC can be represented with coefficients, $H_{inv}(s)$ and $Y_{inv}(s) = 1/Z_{inv}(s)$:

$$i = \frac{G_{PI}(s) \times T_{d}(s) \times Y_{LCL,V_{HuT}}(s)}{\underbrace{1 + G_{PI}(s) \times T_{d}(s)^{2} \times Y_{LCL,V_{HuT}}(s)}_{H_{inv}(s)}}_{I_{Hov}(s)} i^{*}$$

$$\underbrace{-\frac{Y_{LCL,V}(s)}{1 + G_{PI}(s) \times T_{d}(s)^{2} \times Y_{LCL,V_{HuT}}(s)}_{Y_{inv}(s)}}_{Y_{inv}(s)} V$$
(18)

Therefore considering (16) and (18), the whole setup can be represented with impedances, $Z_{grid}(s)$ and $Z_{inv}(s)$ and their associated sources, namely, V_{grid} and i_{inv} as:

$$V_{grid} = H_{grid}(s) \times V_s \tag{19}$$

$$i_{inv} = H_{inv}(s) \times i^* \tag{20}$$

$$i = [i_{inv} - \frac{V_{grid}}{Z_{inv}(s)}][\frac{1}{1 + \underbrace{\frac{Z_{grid}(s)}{Z_{inv}(s)}}_{\text{open-loop}}}]$$
(21)

The proposed impedance model is represented in Fig. 4. Since V_{grid} and i_{inv} are stable sources (no right half-plane poles in $H_{grid}(s)$, and $H_{inv}(s)$), the stability only depends on the Z_{grid}/Z_{inv} [7]. This criterion is examined next.

III. STABILITY EVALUATION

Following section II, in this section, first, the validity of the defined impedances is verified through the bode plot. The P-HIL setup with the given parameters in Table I is implemented in Simulink to serve as the reference for verification of calculated $Z_{grid}(s)$. Then to measure $Z_{grid_{ref}}(s)$, the blue color in Fig. 5, the grid source, V_s is short-circuited. Therefore, according to Fig.4, measured voltage over current at PCC equals the inverter side impedance. For a wide frequency range analysis, a disturbance is added on i^* in which its magnitude is constant, but the frequency varies in the 200-1200 Hz frequency range. Then at each frequency, the gain and phase of the PCC voltage and current are measured using the Fourier transformation block, which eventually delivers the gain and phase for the impedance *Simulink* $Z_{grid}(s)$, which is then compared with $Z_{grid}(s)$ bode plot.

Similarly, for Simulink $Z_{inv}(s)$, the inverter source is deactivated, which makes the PCC measurements equal to the inverter side impedance measurement. The attained gain and phase are shown in red in Fig. 5. Then the bode plot of the $Z_{inv}(s)$ is plotted in the same figure to illustrate the excellent matching between the calculated impedance $Z_{inv}(s)$, and its Simulink reference.

The matching between impedances and their references in Fig. 5 confirms the validity of the impedance-based modeling in section II.

For stability analysis, $Z_L(s)$ is held constant, and its parameters are provided in Table I. On the other hand, $Z_s(s)$



Fig. 4. Proposed impedance model



Fig. 5. Impedance verification



 T_{Amp}

 $[\mu s]$

 $T_{A/D}, T_{D/A}$

 $[\mu s]$

 T_{DRTS}

 $[\mu s]$

Fig. 6. Case I: Nyquist plot of Z_{grid}/Z_{inv}

is adjusted according to variations in parameter k, which is defined as follows:

$$k = Z_L / Z_s \tag{22}$$

Variations in k result in variation in the stability criterion given in (21). Two examples of k are chosen to show the stability condition. For example, if k=9, the graph encircles the (-1+0j) in the Nyquist plot (Fig. 6), showing an unstable system whose current waveform also confirms its instability. Whereas, with k=10, the new $Z_s(s)$ eventually updates the Z_{grid}/Z_{inv} ratio and holds the system within the stable region (Fig. 8). As shown in Fig. 9, the current controller exhibits excellent tracking of reference changes.

Thus, the stability of the P-HIL setup is examined through the impedance model, where the information on impedances at the PCC point, as shown in this section, is adequate. This knowledge provides the necessary and sufficient conditions to ensure a stable P-HIL system for any HuTs. By adopting this approach, researchers and engineers in various industries can conduct realistic tests on emerging power technologies using P-HIL, mitigating potential stability problems during their experiments without delving into the intricate details of the HuT model. This streamlined approach offers valuable support, making it easier for practitioners to use P-HIL effectively and confidently in their innovative endeavors.

The following section adds the experimental results from an actual P-HIL setup for further verifications.

IV. EXPERIMENTAL VERIFICATION

As shown in Fig. 10, a P-HIL setup composed of the realtime digital simulator (RTDS), three APS 15000 4-quadrant

Fig. 7. Case I: Time-domain response of the inverter current



Fig. 8. Case II: Nyquist plot of Z_{grid}/Z_{inv}



Fig. 9. Case II: Time-domain response of the inverter current

amplifiers Spitzenberger & Spies, an EA-PSI 91500-30 WR 3U DC supply, Imperix rack consisting of B-Box RCP digital controller, power rack (3 PEB8038 half-bridge modules), and passive filters rack in the Energy Lab 2.0 at Karlsruhe Institute of Technology has been built-up for a realistic experimental validation. Parameters used for the experiment are given in Table II. The rest of the parameters remain the same as the simulation parameters in Table I. The grid model and low-pass filter are executed in RSCAD. To validate the accuracy of the calculated Z_{inv} in (18), the inverter source, i_{inv} , is deactivated.

TABLE I P-HIL SIMULATION PARAMETER

 L_f

[mH]

2.36

 $\omega_c/(2pi)$

[kHz]

2

 R_{fl}

[Ω]

 C_{f}

 $[\mu \dot{F}]$

10 0.05

 R_{fc}

 $[\Omega]$

1

 $\omega_0/(2pi)$

[kHz]

180

D kp ki

0.9 1 40

 T_{Sensor}

 $[\mu s]$



Fig. 10. P-HIL setup at the Energy Lab2.0, KIT

Next, a three-phase disturbance with a magnitude of 2 V is added to V_s in RSCAD. The disturbance frequency is varied from 200 Hz to 1000 Hz with increments of 100 Hz. The resulting voltage and currents at the PCC are measured at each frequency to calculate the impedance at PCC, which equals Z_{inv} . Using the Fourier transform for the measured variables, the gain and phase of $Z_{inv_{ref}}$ are obtained and compared with the given bode plot from Z_{inv} transfer function. This comparison is shown in Fig. 11, proving the correctness of evaluated Z_{inv} .

Similarly, for $Z_{grid_{ref}}$, the disturbance is added to i_{inv} while V_s is set to zero. For the voltage level of 220 V (rms) due to the rise time, the T_{DRTS} is 2 times the chosen time-step T_s . Also, when using the Small Form-factor Pluggable (SFP) connection, the lumped open-loop delay is 4.1 μ s [15]. Since the voltage and current for Z_{grid} calculation are measured in the software sector, another unit delay (50 μ s) interferes with the transformation from the hardware level (PCC) to RSCAD. Hence, the conversion delay, T_{conv} , equals 54.1 μ s.

The comparison results are presented in Fig. 12, demonstrating a remarkable agreement between the model-predicted impedances and the reference values obtained from experimental data.

The experimental impedance verification in this section confirms the accuracy of the impedance model outlined in Section III, and the functionality of the impedance-based approach to evaluate the stability of the P-HIL setup ahead of running lab testing.

V. CONCLUSION

Power Hardware-in-the-Loop (P-HIL) application is significantly increasing due to its reliability and safety. However, conversion delays between the sectors can deteriorate the

TABLE II P-HIL EXPERIMENT PARAMETER

T_S [μs]	$\begin{array}{c} T_{DRTS} \\ [\mu s] \end{array}$	T_{conv} [μs]	L_f [mH]	C_f [μF]	R_{fl} [Ω]	$\begin{array}{c} R_{fc} \\ [\Omega] \end{array}$	$\stackrel{kp}{-}$	$\stackrel{ki}{-}$
50	100	54.1	2.5	12	0.045	1.5	0.1	40



Fig. 11. Experimental inverter impedance verification



Fig. 12. Experimental grid impedance verification

system's stability, causing severe hardware damage when testing. A stability analysis is crucial before running the P-HIL experiment to avoid impairments during the experiment. This paper suggests the impedance-based approach to ensure the stability of a P-HIL setup using a grid-following inverter. The stability condition is determined using the Nyquist criterion, where it has been demonstrated that the open-loop transfer function is the ratio of two divided impedances at PCC, Z_{grid}/Z_{inv} . The impact of interface dynamics and delays, the inverter's controller, and its output LCL filter in the P-HIL setup are considered. A P-HIL setup with RTDS realtime simulator, linear amplifier, and Imperix inverters with Boombox controller has been arranged for realistic verifications. Calculated impedances are verified through bode plots with simulations in Simulink and experiments as references. For stability verification, time and frequency responses are compared to confirm the validity of the impedance model. It has been shown that this method guarantees the P-HIL's stability to avoid erroneous analyses and potential hardware damage without the need for the HuT model.

REFERENCES

- A. Benigni, T. Strasser, G. De Carne, M. Liserre, M. Cupelli, and A. Monti, "Real-time simulation-based testing of modern energy systems: A review and discussion," *IEEE Industrial Electronics Magazine*, vol. 14, no. 2, pp. 28–39, 2020.
- [2] M. Steurer, C. S. Edrington, M. Sloderbeck, W. Ren, and J. Langston, "A megawatt-scale power hardware-in-the-loop simulation setup for motor drives," *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1254–1260, 2010.
- [3] R. German, F. Tournez, A. Bouscayrol, A. Lievre, and B. Lemaire-Semail, "Power hardware-in-the-loop test of low-voltage battery for a plug-in hybrid electric vehicle," in 2022 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), 2022, pp. 1–7.
- [4] S. Karrari, G. De Carne, and M. Noe, "Adaptive droop control strategy for flywheel energy storage systems: A power hardware-in-the-loop validation," *Electric Power Systems Research*, vol. 212, p. 108300, 2022.
- [5] F. Wald, Q. Tao, and G. D. Carne, "Virtual synchronous machine control for asynchronous grid connections," *IEEE Transactions on Power Delivery*, pp. 1–10, 2023.
- [6] F. Ashrafidehkordi and G. De Carne, "Improved accuracy of the power hardware-in-the-loop modeling using multirate discrete domain," in 2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2022, pp. 1–5.
- [7] W. Ren, M. Steurer, and T. L. Baldwin, "Improve the stability and the accuracy of power hardware-in-the-loop simulation by selecting appropriate interface algorithms," in 2007 IEEE/IAS Industrial & Commercial Power Systems Technical Conference, 2007, pp. 1–7.
- [8] J. Sun, "Impedance-based stability criterion for grid-connected inverters," *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3075– 3078, 2011.
- [9] Y. Liao and X. Wang, "Impedance-based stability analysis for interconnected converter systems with open-loop rhp poles," *IEEE Transactions* on Power Electronics, vol. 35, no. 4, pp. 4388–4397, 2020.
- [10] F. D. Freijedo, A. G. Yepes, O. López, A. Vidal, and J. Doval-Gandoy, "Three-phase plls with fast postfault retracking and steady-state rejection of voltage unbalance and harmonics by means of lead compensation," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 85–97, 2011.
- [11] M. Cespedes and J. Sun, "Impedance modeling and analysis of gridconnected voltage-source converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 3, pp. 1254–1261, 2014.
- [12] M. Dargahi, A. Ghosh, and G. Ledwich, "Stability synthesis of power hardware-in-the-loop (phil) simulation," in 2014 IEEE PES General Meeting — Conference & Exposition, 2014, pp. 1–5.
- [13] F. Loku, L. Osterkamp, P. Düllmann, C. Klein, M. Maimer, T. Bergwinkl, M. Kufner, M. Stevic, A. K. K. S., and R. Venugopal, "Utilization of the impedance-based stability criterion for stability assessment of phil interface algorithms," in 2022 IEEE 13th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), 2022, pp. 1–7.
- [14] T. Reinikka, H. Alenius, T. Roinila, and T. Messo, "Power hardware-inthe-loop setup for stability studies of grid-connected power converters," in 2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia), 2018, pp. 1704–1710.
- [15] F. Ashrafidehkordi, D. Kottonau, and G. De Carne, "Multi-rate discrete domain modeling of power hardware-in-the-loop setups," *IEEE Open Journal of Power Electronics*, pp. 1–10, 2023.