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Integrated CPU Monitoring Using 2D Temperature Sensor Arrays Directly Printed on Heat Sinks

*Robert Huber, Daniel Belles, Tim Bücher, Leonard Franke, Hussam Amrouch, and Uli Lemmer**

In today's digital world, the demand for computer security and system reliability is a crucial element. Monitoring the CPU temperature during operation provides valuable insights but is currently limited to the embedded on-chip sensors. The implementation of an extra security layer based on temperature monitoring can detect anomalies in an early stage, identify malware, and help mitigate attacks. The approach of integrating more on-chip temperature sensors into the silicon is avoided due to space, power limitations, and cost constraints. However, the field of printed electronics and sensor technology has recently seen significant progress. This is the first work that introduces a fully-printed temperature sensor array integrated onto the cooling unit of a CPU. It offers a novel approach for the practical implementation of such sensors into an operational computer system. The present sensor array, consisting of 396 sensor pixels, detects local hotspots induced by the underneath CPU cores, leading to an individual thermal fingerprint. This unique method paves the way for addressing pivotal elements of computer security, as deviations from expected thermal behavior can signal malicious activities. Additionally, this innovation facilitates reliability optimization. The detailed thermal map garnered provides insights into which cores are subjected to significant stress over time.

1. Introduction

Living in a world highly dependent on digital infrastructure, its operational availability, hardware security, and reliability have become crucial aspects of our economy and daily life. Methods that fulfill these criteria strive to analyze and record the usage of central processing units (CPUs) and network traffic. Alternatively, monitoring low-level indicators and physical properties of CPUs, such as temperature fluctuations over time of chip-integrated sensors, provide easily accessible parameters. Unfortunately, the embedded on-chip sensors are limited and lack sufficient spatial resolution and coverage to monitor and identify hotspots comprehensively. Additionally, a decrease in the number of embedded sensors can be observed over the past CPU generations, while the number of cores increased steadily. This is in contradiction with the demand for more detailed information and also the extensive research executed in the field of obtaining a detailed thermal map of the CPU. Adding a sensor independent of the system for monitoring would be a straightforward way to address these limitations. Nevertheless, a variety of methods are implemented utilizing the information supplied by the system, which includes data from the built-in on-chip sensors, workload tracking, and power usage. This information is then processed with various models and machine learning algorithms.[1–4] Other approaches monitor the CPU with an external infrared camera, which comes along with increased space requirements and a complex cooling system.[1,5,6] This effort is taken to ensure system reliability, optimize performance, increase cooling efficiency, and detect security threats. The detailed knowledge helps to significantly mitigate heat accumulation and hotspots on the CPU, which significantly affect the aging process of the involved components.[7,8] This issue particularly escalates when taking

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into account the condensed infrastructure in data centers suffering from undetected hotpots. Not only the individual computer components are affected, but this also presents a challenge for the cooling system, resulting in poor efficiency due to unbalanced cooling requirements.[4,7,9] Predicting and detecting the thermal load helps allocate workloads before problems arise. Finally, the detection of anomalies from the heat map can prevent cyber attacks or diminish the damage caused to the affected system. Different types of attacks generate local intensive or periodical hotspots, which can be observed with pattern recognition methods.[5,10–13] Nevertheless, suppose the detection is based on embedded sensors or data generated by the system. In that case, the data acquisition and handling will be executed on the potentially infected personal computer (PC). This also makes the concept susceptible to manipulation. A system-independent temperature sensor array is, therefore, highly advantageous. Presenting a solution of an external, printed high-resolution temperature sensor array, therefore, offers a promising solution to overcome these limitations. By closely monitoring the CPU temperature using an external sensor array, security solutions can detect anomalies, mitigate side-channel attacks, identify malware, and detect physical tampering. Brouchier et al.[14] applied customized software to heat the processor and used the corresponding cooling fan's behavior to encode information. The results effectively proved that an attacker can leverage such heat manipulation to threaten the entire system's security. By simply observing the system's cooling patterns and behavior, an external entity can exploit this information. Masti et al.[15] also demonstrated that processors inside a multicore system could leak or exchange information through the temperature side channel. Using accurate thermal measurements for a commercial multicore processor using an infrared camera,[5] proved that in cyber-physical systems, the repeatedly executed control loop creates a unique "temperature fingerprint". This, in turn, can be leveraged to detect any malicious activities induced by a software/hardware Trojan because such activities will lead to a certain deviation from the expected temperature fingerprint. Nevertheless, a significant challenge persists in obtaining an online thermal map of the chip with a high spatial resolution during run-time. On the one hand, the available on-chip thermal sensors are limited and cannot offer the necessary detailed temperature information for the entire chip. On the other hand, employing an infrared camera on top of the chip at run-time during operation to obtain the necessary thermal maps is impractical. Therefore, we propose and implement in this work the first-of-its-kind temperature sensor array that is directly printed on the heat sink, which can provide a high spatial temperature resolution of the entire processor chip.

Placing an external array of temperature sensors at a relevant position on the CPU die enables detailed and accurate temperature monitoring down to the sub-core level. Modifying existing packages to facilitate such a sensor array is a convincing approach for ease of use. Although traditional semiconductor manufacturing methods still offer better reproducibility and performance, they still lack mechanical flexibility and adaptability. Recent developments in the field of printing technology and additive manufacturing have provided the prospects to manufacture such sensor structures.[16,17] The progress made is reflected in the number of recent works[18,19] and the steadily growing market.[20] Digital and scalable printing processes offer an on-demand and efficient way of fabricating electronic microstructures.[21] Furthermore, technologies such as aerosol jet printing, electrohydrodynamic printing, or ultraprecise deposition have recently enabled feature sizes below 10 µm.[22] They are well suited for printing onto 2.5D substrates or, depending on the configuration, even 3D substrates. In addition, the development of commercial and experimental inks and pastes has progressed in parallel with advances in printing technology. Printed electronics are not only limited to single-layered and passive components but are also applicable to different sorts of sensors[23,24] and active components such as multiplexers and transistors.[25,26]

Conventionally, such sensor systems with micron resolution are fabricated using cost-intensive lithographic techniques. Therefore, achieving this with printing technologies and additive manufacturing methods still presents a significant challenge. This includes the development of suitable sensor layouts and the adjacent implementation in a fabrication process. Three sensing methods are the most commonly used in this context: Thermistors,[27,28] thermocouples,[29,30] and resistance temperature detectors (RTDs).[31,32] Generally, these represent the primary technologies for digital temperature measurements.[33] In the recent work, we could demonstrate the fabrication and performance of fully printed temperature sensor arrays on plastic foils.[34,35]

This work presents a fully printed temperature sensor array specially designed to be mounted on a CPU die. The sensor array features a high spatial resolution that is able to resolve local hot spots induced by the CPU cores. To make the implementation easy, the sensor array was printed directly onto the cooling unit consisting of a metal body with an insulating coating. Compared to a modular sensor system, e.g., printed on a plastic foil, the coating can be made ultra-thin, mitigating the impact on the cooling performance. In general, this approach makes the sensor system more robust and application-save in terms of assembly and alignment. To facilitate the sensor, the cooling unit only required small modifications while also serving as an electrically insulated printing substrate. The sensor array is based on a passive matrix structure and consists of 18x22 electrodes providing 396 sensor pixels within an area of 9x22 mm^2. All layers were printed using an aerosol jet printer. Aerosol jet printing is an emerging direct-write approach gaining attention for rapid and affordable (micro-)additive manufacturing. Its versatility in handling various ink viscosities allows for printing diverse materials, including ceramics, metals, polymers, and biological matter, with high spatial resolution and wide standoff distances. These unique properties make aerosol jet printing an appealing technology for a wide range of application cases for industry and consumer electronics.[36] To demonstrate the sensor's capabilities, the sensor was implemented on a commercial Intel i9 Core 9900K CPU. The approach presents an exciting avenue to enhance both system performance and security.

2. Design and Fabrication

The fabrication of the sensor array is divided into the preparation of the heat sink of the cooling unit and the printing process, including the sintering/curing. **Figure 1**a shows a step-by-step representation of the fabrication process. The CPU is mounted to a cooling system, which originally exhibits a copper plate at the

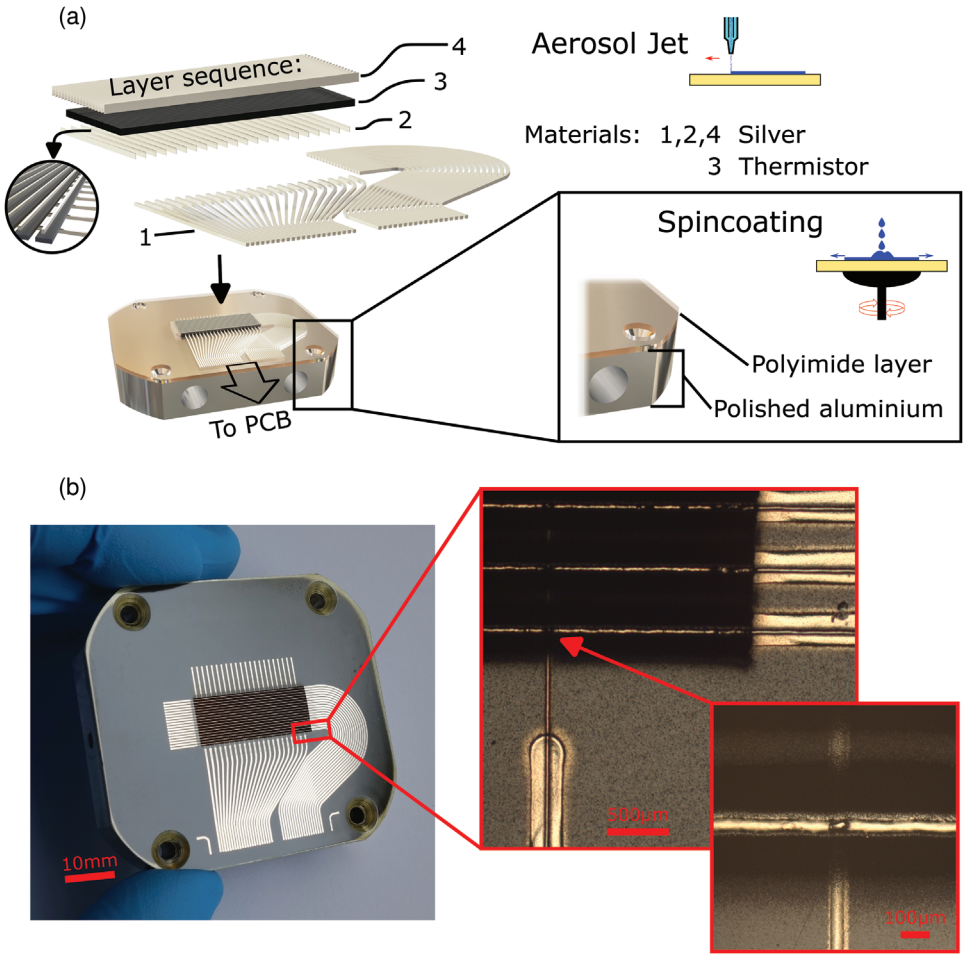

Figure 1. a) Fabrication scheme of the 2D passive matrix printed sensor array: First, the aluminum surface was polished in a lapping process before preparing the polyimide layer. The layer is used for electrical insulation and serves as the layer on which it is printed. Second, all sensor layers were printed successively using an aerosol jet printer starting from bottom to top: (1)-connection lines, (2)-bottom contact lines, (3)-thermistor material, (4)-top contact lines. Each printing step requires a curing or sintering process. b) Image of the fully fabricated sensor array, including a close-up view of a single sensor pixel consisting of the deposited layers.

bottom side being in direct contact with the CPU. The original copper plate was replaced with two specially designed aluminum plates, incorporating two dedicated slots for accommodating external heating probes, along with an external reference Pt100 temperature sensor. These are necessary to conduct the calibration of the sensor and to simulate an additional heat source. The surface pointing toward the sensor array was polished in a lapping process to prevent punctures of the subsequent insulating polyimide layer. This material exhibits optimal properties for the intended purpose. It can withstand temperatures above 200 °C and is highly scratch-resistant. After curing, the deposited polyimide layer is fully compatible with the subsequent fabrication process of the sensor array. The polyimide precursor layer is spin-coated to achieve the thinnest possible design for the layer to minimize the additional thermal resistance between the CPU and heat sink. A layer with a thickness <5 µm and a surface roughness below ±2 µm was achieved. Additionally, the deposited layer offers the benefit as the used inks are optimized and designed for plastic foils composed from polyimide/Kapton, eliminating the need for any modifications. An alternative approach would be to deposit the sensor on the CPU die. In such a scenario, the CPU would also necessitate a polyimide layer for electrical isolation. The fabrication process, however, includes a baking step at 350 °C, posing a risk of damaging the processor. We, therefore, discarded this approach and printed on the heat sink.

The sensor array is connected to the readout electronics by a flat flexible cable (FFC). However, an inherent challenge arises due to the severe limitation imposed by the available space while still maintaining a robust and stable connection. The layout of the connection lines (1, Figure 1a) has to match the connector pattern of the FFC to fulfill the requirement mentioned above. The printing is entirely conducted using an aerosol jet printer (Aerosol Jet 5X System, Optomec, Inc.). The printer offers rapid prototyping combined with precise printing and feature sizes of <10 µm. The operational principle relies on the creation of an ink aerosol through the process of either sonication of the ink or by spraying the ink through an orifice within the ink tank. The ink viscosity mainly determines the chosen process. By applying a nitrogen stream, the aerosol is then guided to the nozzle, where it is focused and compressed with an additional nitrogen sheath gas

stream. Figure 1 shows the layer sequence from bottom to top. All conductive paths are printed with a water-based nanoparticulate silver ink with selected nozzle size and printing parameters depending on the demanded line properties. In general, the lowest possible line resistance is desirable, which can be achieved by increasing the line width/thickness or optimizing the sintering process. Photonic curing was utilized to sinter all deposited silver lines, offering the advantage of achieving enhanced conductivity and producing results free from cracks.[36–39]

First, the connection lines (1, Figure 1a) were printed with a width of 300 µm. One end of the connection lines is designed with a pitch of 0.5 mm with respect to the FFC footprint, while the other end represents the sensor layout with a pitch of 1 mm in the x-direction and 0.5 mm in the y-direction, respectively. The line properties result in a specific line resistance of $<5\ \Omega\ cm^{-1}$. The provided area in the connection lines is then filled with the actual sensor array based on the concept of a passive matrix. Hence, the intersection of the bottom and top electrodes defines the sensor pixels with the line width of the electrodes specifying the pixel's dimensions (here ca. 60 x 60 μm^2). The first set of electrodes (2, Figure 1a) of the sensor stack is printed and forms the bottom electrode of the sensor. At one end, they overlap with the already printed connection lines. Because the line width of the electrodes is significantly narrower than the connection lines (60–80 µm vs. 300 µm), the nozzle was exchanged for a smaller version. A photonic sintering step follows the printing. This method provides several benefits compared to thermal curing, such as time savings and enhanced conductivity of the metal lines.

The thermistor layer is the third printed layer (3, Figure 1a), which is sandwiched between the bottom and top electrodes. This layer defines the properties of the temperature sensor and exhibits a negative-temperature-coefficient (NTC) behavior. As the ink was developed for screen printing, some adjustments to the formulation were necessary. To lower the viscosity to an acceptable level for aerosol jet printing, the ink was diluted with a second solvent. According to the manufacturer's datasheet, the thermistor material used is thermoplastic-based. For our work, the resistance was altered by changing the number of deposited layers, which means that the final layer thickness corresponds to the resistance. In general, it is advantageous to achieve homogeneous resistance values among all pixels, which directly corresponds to the thickness and quality of the thermistor layer. Four specific measures were taken to increase the uniformity from a design and printing point of view. 1) The thermistor layer was printed perpendicular to the bottom electrodes and printed as broad as possible without making contact with the neighboring line. This yields a larger, evenly thick layer in the middle of the thermistor line. 2) We have also observed slight pressure variations in the aerosol jet printer when utilizing the internal shutter. Consequently, this leads to minor fluctuations in the material output during the printing process, resulting in a subtle yet discernible fading effect. This problem was overcome by printing all lines in one continuous meander structure and applying a simple mask (polymer foil) onto the sensor array, cropping the unnecessary sections by removing the mask after the print. The cropping procedure is illustrated in Figure S1 (Supporting Information). 3) Printing multiple layers instead of a single thick layer effectively mitigated the impact of printing fluctuations and resulted in a more consistently formed material stack. 4) Curing the thermistor stack/sample in an oven for several hours provides a more thoroughly cured and homogeneous result than the use of a hotplate.

The deposition of the top electrode lines is the final and fourth layer (4, Figure 1a). They are directly printed and aligned with thermistor lines on top of the thermistor material using the same parameters as the bottom electrode. The printing is again followed by photonic sintering. Due to the subjacent layers, it is a challenging task to find appropriate curing and printing parameters to achieve flawless lines. This can be attributed to different flash absorption properties of the thermistor material, which results in different temperatures and expansion characteristics of involved layers. Finally, the samples were subsequently placed inside an oven to reduce local stress in the materials.

Figure 1b shows the completely fabricated temperature sensor array with a close-up view of the deposited layers. Next to the connection lines, two alignment markers were added to the layout to simplify the positioning of the FFC cable. Taping the FFC to the sample has proven to be the most suitable way to mount the cable to the sensor. It should be noted that a perfect alignment is crucial to avoid short circuits between the individual connection lines. The close-up images reveal the discussed layer stacking. The broad, shiny lines are the connection lines printed in the first step. The thin vertical silver line is part of the bottom electrode, whereas the horizontal ones belong to the top electrode. Both electrodes sandwich the thermistor layer in black, forming pixels at the intersections.[34]

3. Results and Discussion

To facilitate the measurement with the temperature sensor array on an active CPU, the cooling system and mainboard had to be adapted. **Figure** 2a presents the utilized measurement setup. The sensor design was inspired by the originally installed cooling plate of the liquid cooling system. To implement two heating elements and an external reference temperature sensor, a slightly thicker aluminum plate was chosen. For the measurement, it was pivotal to have access to the bare silicon die of the CPU and to mount the sensor on top directly. Therefore, the originally installed heat spreader was removed (delidded), which would otherwise blur out the thermal fingerprint of the cores (**Figure** 3a). With the removal of the heat spreader, it was not possible to use the mounting clamps of the mainboard to fasten the CPU further. Instead, the CPU was pressed into position with the cooler itself. Different from what is shown in Figure 3a, the mounting frame was removed for the actual measurement. The mounting frame caused problems due to a tilted cooling plate and space limitations, resulting in an air gap between the CPU die and the sensor array. For electrical insulation, it is important to implement an ultra-thin PEN foil between the electrically conductive CPU die and the sensor array. Adding thermal paste between the die and PEN foil further enhances the heat transfer into the sensor array/cooler plate and prevents overheating. The cooling plate was mounted onto the liquid cooling unit, replacing the originally installed copper plate. The unit was mounted onto the CPU by the standard mainboard fixture. The increased thickness of the cooling plate comes with an increased standoff distance, which was compensated with extended mounting bolts. The sensor array was connected to the readout device via the FFC taped to the

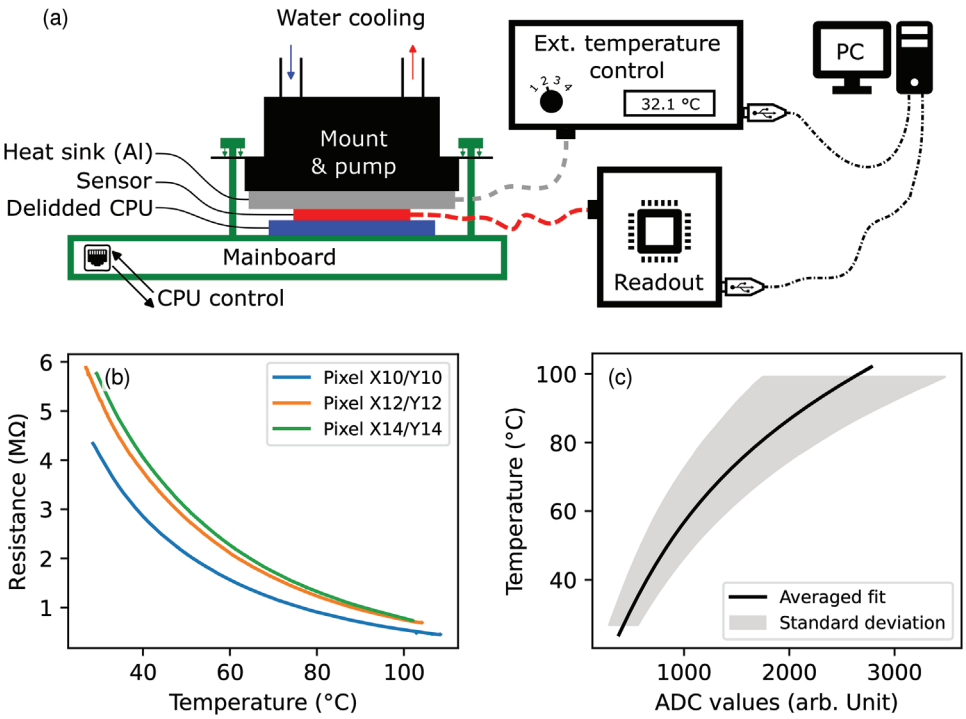

Figure 2. a) Schematic of the test setup comprising the mainboard with CPU, the cooling unit, and the external controls. The sensor array is turned upside-down and mounted on top of the delidded CPU (CPU die). A picture of the real setup is included in Figure S2 (Supporting Information). b) The behavior of three exemplary pixels is shown in the plot exhibiting a non-linear NTC response to temperature change. Despite several measures applied to mitigate inhomogeneities, each pixel features slightly different resistance values. c) The readout device measures the current for a bias voltage of 1 V, which depends on the resistance of the pixel and is converted by an analog-digital converter (ADC). A separate calibration function can be determined for each sensor pixel using a 4th-order polynomial. Overall, more consistent results were achieved by extracting one average fitting function, which is shown in black. To adapt the averaged fitting function to each pixel, a scaling factor was introduced. This calibration function is later used to convert the ADC values to temperature values.

cooler plate. The two heating probes and the reference temperature sensor were embedded into the cooling plate and connected to an external temperature control unit. It contained the heating controls and the readout electronics for the Pt100 temperature sensor. The external temperature control, the readout device, and the delidded CPU were controlled from an external PC. Images of the full measurement setup, as well as of the readout device, are presented in Figure S2 (Supporting Information). The readout device was specially developed for the purpose of reading the presented temperature sensor array. A detailed image is presented in Figure S3 (Supporting Information).

One overall drawback of passive matrices is the interdependence among all linked pixels. This cross-talk can be attributed to parasitic current pathways through the other non-addressed pixels. The zero-potential-scanning[40–42] method represents an effective way to overcome this problem. Therefore, a precise driving voltage on the selected row is required, which in our case was set to 1 V. All not-addressed rows and columns are set to the same virtual potential. Here, the column drivers create an adapted measurement voltage depending on the resulting pixel current. At the same time, they also have to decouple and scale the resulting voltage of the read pixel to fit the analog-digital-converters (ADCs) measurement range. Since all columns and, therefore, all not actively driven rows are set to the same virtual ground, no parasitic currents occur. The individual pixels can be addressed by selectively multiplexing the associated rows and columns. The measurement could be potentially influenced by the self-heating of each sensor pixel. The impact is defined by the resistance of the sensor pixel and the readout procedure. In a worst-case scenario, the power dissipation can be estimated to be ≈2 μW when read continuously. However, this is generally not the case. The heat dissipation of the sensor pixels is a minimum of four orders of magnitude smaller compared to the waste heat emission of the processor due to the small read currents and the small duty cycle. We consider the self-heating of the sensor pixels as negligible.

The sensor was operated at a voltage of 1 V, showing a non-linear resistance-temperature-behavior. The curves in Figure 2b clearly represent the NTC properties of the thermistor material. The sensor pixels have slightly different resistance values but exhibit a similar temperature dependence. One performance indicator commonly used to compare temperature sensors and their property-defining materials is the so-called temperature-coefficient-of-resistance (TCR) value. High TCR values come with a bigger change in resistance when undergoing a temperature change, resulting in a higher temperature reading precision and potentially lower requirements for the readout electronics. The TCR values are calculated according to $\mathrm{TCR}_{T_{\mathrm{rel}}=25^{\circ}\mathrm{C}} = \frac{1}{R}\frac{\mathrm{d}R}{\mathrm{d}T}$. This takes into account the use of a fourth-order polynomial to fit the measured data. The non-linear behavior of the material comes along with temperature-dependent TCR values. The

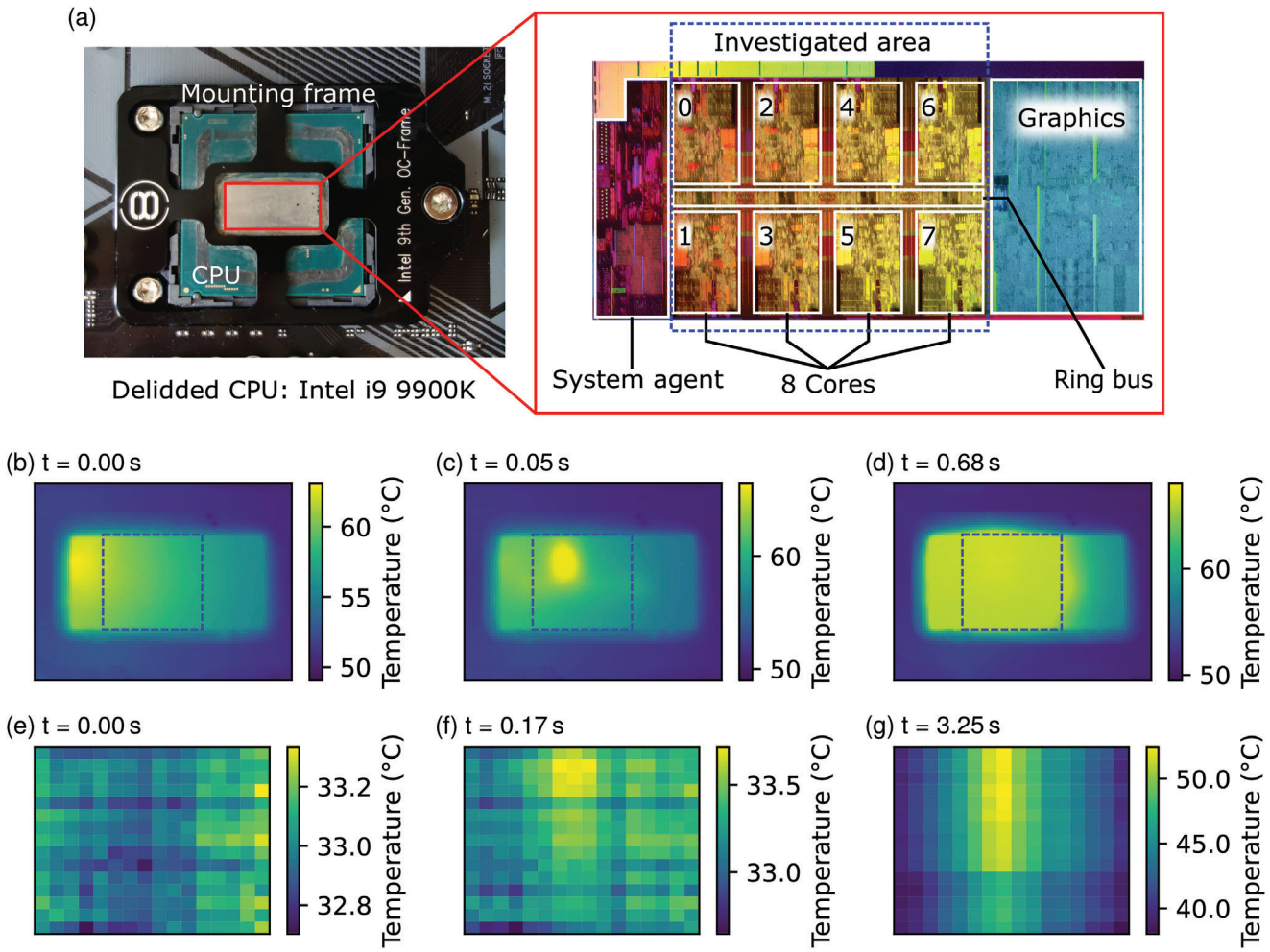

Figure 3. a) To have full access to the bare CPU die, the originally installed heat spreader was removed. The employed Intel Core i9 9900K facilitates eight cores, which are arranged in two opposing rows. For this study, only the cores were observed.[43] b–d) The Images show the thermal evolution of the CPU under stress. The images are taken without a CPU cooler. (b) shows the die in idle. (c) unveils a local hot spot right after stressing core two. (d) illustrates the heat distribution when core two is kept under persistent stress. The blue box marks the area containing the eight cores. e–g) For comparison, the images show the response of the printed temperature sensor array while stressing core two. A major difference is visible between (d) and (g). The heat distribution in (g) remains localized in one area.

presented sensor exhibits a TCR value of <-3.8 % $°C^{-1}$ at 20 °C and reaches down to <-2.2 % $°C^{-1}$ at 100 °C. This varies slightly from pixel to pixel.[34]

A calibration function is required to overcome the nonlinearity of the sensor and to achieve an appropriate temperature interpretation of the measured ADC values. This calibration function was determined by first heating the mounted cooler plate to 100 °C using the embedded heating probes and then reading all sensor pixels during the subsequent cooling phase. Data from these pixels were used to calculate temperature-dependent ADC mean values. By fitting these mean values with a polynomial of the fourth order, one generalized calibration function was generated, which is depicted in Figure 2c. This approach assumes a similar general temperature dependence of each pixel, only exhibiting variations in the absolute resistance values. To adjust the generalized calibration to the individual behavior of each pixel, a scaling factor was determined at the beginning of a measurement. This required an as evenly tempered cooling plate as possible. Therefore, the CPU was kept idle to record a short baseline and to determine the individual scaling factor. During this period, the current temperature was obtained from the external temperature sensor, and the associated ADC value was calculated from the generalized calibration function. This ADC value is then compared with the individual ADC values for each pixel at the given moment. Any disparity is offset by a distinct scaling factor specific to each sensor pixel. Afterward, this scaling factor is then applied across the hole temperature range without further rescaling. Figure S4 (Supporting Information) proves that this approach yields a strong correspondence between the generalized fit and the measured data. Moreover, it offers the advantage of effortless compensation for any occurring shifts due to system changes by establishing new scaling factors. We have experienced a smoother and more reliable overall temperature interpretation compared to individual calibration functions. This behavior is particularly desirable as it allows us to identify a distinct and discernible thermal fingerprint rather than solely

pursuing potentially higher accuracy in temperature interpretation. Furthermore, this approach leads to reduced computational requirements.

As described before, it was necessary to remove the originally installed heat spreader from the CPU, which would otherwise blur the thermal fingerprint in operation. Figure 3a shows the delidded CPU on the left side with the bare silicon CPU die in the middle. It was sufficient to press the CPU into position with the sensor array/CPU cooler mounted on top. Intel has published an official press release showing the architecture of the CPU (Figure 3a). The CPU is divided into several logical units: The System Agent organizes memory/cache, pipelines, and connectivity, among other things. The CPU features an integrated graphics unit occupying roughly a quarter of the CPU die. In this study, we only focus on the middle part, comprising the eight cores. The cores and the CPU sectors are connected via the ring bus positioned between the two rows of cores.

In the first set of experiments, the CPU behavior was analyzed with an infrared thermal camera. To conduct such measurement, the CPU cooler was disassembled, bearing the risk of overheating and shutting down the system. This problem was overcome by only stressing the core for a very limited time and applying a cooling spray right before and after the measurement. The thermal development over time is illustrated in Figure 3b,d. The blue box marks the area containing the eight CPU cores. Figure 3b shows the CPU idle, revealing a hotspot located in the system agent unit. Once one core is put under load, the thermal image shows a strongly localized hotspot within 50 ms (Figure 3b), which pinpoints the position of the assigned core. Over time, the heat spreads out over the entire CPU die (Figure 3d). This effect is presumably amplified due to the missing CPU cooler. Interestingly, the graphics unit seems to be separated within the die, leading to decreased heat conduction to the right side. After the CPU load is released, the temperature of the die decreases and returns to the idle state.

Next, the thermal fingerprints are investigated with the printed temperature sensor array attached to the CPU. 240 pixels of the sensor array, covering the area of interest, were used to map the temperature distribution in the area containing the cores. Figure 3e–g show the thermal development recorded with the sensor array. Following a similar procedure as before with a thermal camera, Figure 3e illustrates the idle state of the CPU. All cores share a uniform temperature behavior with a temperature variation of less than 1 °C. The core temperatures are about 20 °C lower due to the present CPU cooler containing the embedded sensor array. When the load is subjected to the same core as before, the sensor array detects a temperature rise within 170 ms. Despite the small observed temperature gradient, the hotspot is clearly confined to a specific area and located in a similar region as observed with the thermal camera. Upon further examination of the hotspot's development, its position can already be discerned within 50 ms but is not yet distinctive. With a reading speed of 20 frames per second (FPS), this corresponds to a response within one frame. Figure 3g shows the sensor after 3.25 s proving that the heat dissipation remains localized. This phenomenon is caused by the cooler attached to the system, which effectively directs the heat away from the CPU. With the cooler attached, the temperature of the core under load does not exceed a critical limit, causing system failure. Furthermore, the outer regions of the die remain at a temperature below 40 °C in agreement with the external reference temperature sensor implemented in the cooling plate measuring 33.1 °C in this state. **Figure 4** illustrates the relationship between the time and temperature of the stressed core. In Figure 4a, the row comprising the hotspot is marked with a red box. In the subsequent image (Figure 4b), the temperature distribution within the respective rows is plotted over time, providing a detailed view of the temporal temperature evolution. During idle, the entire row stays in equilibrium, and a uniform temperature distribution is detected. However, upon applying the load to the core, the temperature in the core region reaches values of more than 50 °C. The temperature gradually increases over time due to the slowly rising temperature of the cooler. The plot also nicely depicts that the heat generation is concentrated on the upper side of the CPU die. After releasing the load, the heated area quickly returns to its former state and temperature.

The proposed method for detecting the presence of malicious code on a computer relies on the concept of identifying unusual or unexpected thermal fingerprints. Besides analyzing the time-dependency of the thermal evolution, it is more important to monitor the behavior of the available cores. The operating system allocates the load induced by an executed program to the different cores of the CPU. Therefore, it is crucial to distinguish the single cores with the temperature sensor array and to discern their location. **Figure 5**a–h illustrates the measured temperature distribution corresponding to the stressed cores. Again, the red boxes mark the columns comprising the sensor pixel with the highest temperature. The adjacent plots present the temperature distribution of the highlighted column in the y-direction. As presented in Figure 3a, the CPU architecture comprises eight cores arranged in a grid pattern, with two rows and four columns. Therefore, each column contains a pair of two cores. The columns are clearly separated and defined by a strong temperature gradient in the x-direction. Interestingly, the cores arranged in pairs in each column have a slight variation in their x-position of the hotspot. Cores located on the upper row tend to the right, while the cores on the lower row are orientated to the left. Additionally, the position is reflected in the temperature distribution in the y-direction. Even though the temperature gradient is small, the location in the y-direction is clearly discernible. It has to be noted that in our formerly developed temperature sensor array,[34] we observed minor heat conduction along the silver electrodes. Here, the small temperature gradient along the y-direction can potentially also be attributed to this effect. In the x-direction, the bigger pitch of 1 mm probably helps mitigate this influence and explains the stronger temperature gradient in the x-direction. The manifestation of the hotspot clearly indicates the position of the CPU core, enabling precise identification of the cores under load, which is required for analyzing the temperature fingerprint. Additionally, the sensor demonstrates a fast response of only several milliseconds, making it crucial for detecting brief load spikes and/or load redistribution across all cores, adding time-dependent information to the data.

4. Conclusion

We presented a fully printed first-of-its-kind temperature sensor array that is completely integrated into the heat sink of a

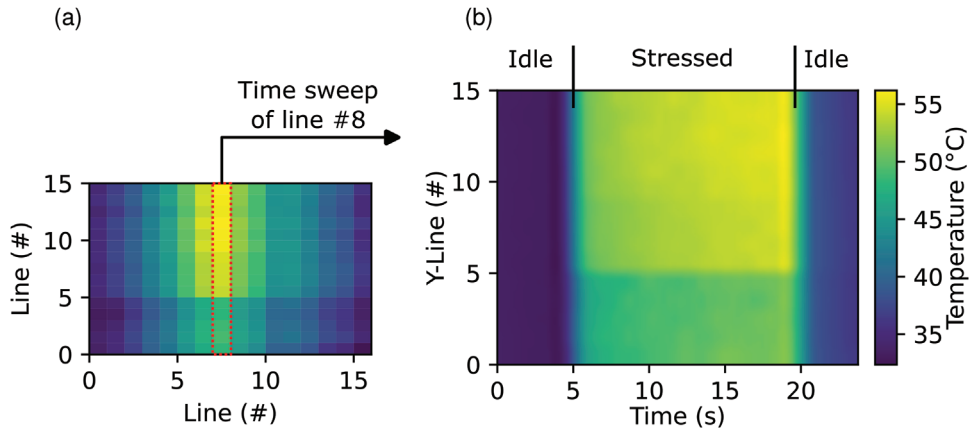

Figure 4. a) According to the heat map, core two is localized in line #8, which is marked with a red box. b) The image illustrates the temperature development of line #8 as a function over time. The measurement starts with core two in idle, showing a uniform temperature among all pixels of line #8. Applying stress to core two instantly increases the temperature with a focus on the top and location of the stressed core. The temperature continues to increase while the cooler starts to heat up. Finally, the core returns to idle, going hand in hand with decreasing temperature and reaching a similar temperature as before.

microprocessor cooling system. To accommodate the temperature sensor array, the surface of the heat sink was coated with an ultra-thin polyimide layer for electrical insulation. Utilizing aerosol jet printing, the temperature sensor stack was fabricated in a four-step process. The sensor array comprises 396 sensor pixels condensed into an area of 22x9 mm^2. The sensing concept is based on measuring the resistance change, which is mainly defined by the deposited thermistor layer. The material exhibits a non-linear NTC behavior and provides a high TCR value of up to <-3.8 % $°C^{-1}$. To overcome the disadvantages of the present passive matrix design, a special readout electronics was developed incorporating the zero-potential-scanning principle. The readout device combines accurate reading with a high frequency of 20 Hz. Before conducting a measurement, the sensor array was calibrated by introducing an average fitting function, which was adapted to each pixel by individual scaling factors. To prove the sensor's capabilities and demonstrate possible application cases for IT security, the sensor array was applied to a commercial 8-core CPU (Intel Core i9 9900k). With the integration of the sensor array into the heat sink, the effect on the CPU cooling performance was mitigated while offering ease of use and keeping the necessary adjustments on the CPU setup to a minimum. For comparison, the thermal fingerprint without the heat sink mounted was also observed by a thermal camera. To demonstrate the spatial resolution of the sensor, the individual CPU cores were stressed separately. Within 50 ms, the sensor senses clearly an initial temperature change. The thermal signature of the observed core remains distinct even after a few seconds. The sensor array could clearly distinguish the location and thermal fingerprint. After releasing the load from the core, the temperature quickly returns to idle again, and the array is ready to detect the next temperature spike. Taking these results, the developed fully integrated temperature sensor array has the potential to pave the way for new strategies in IT security and performance optimization. The utilization of additive manufacturing processes can offer many degrees of freedom concerning substrate, materials, and design. The measurement method provides a slick way to access the heat distribution of a CPU during run-time and supplies a detailed thermal map. Meanwhile, the high degree of integration eliminates the necessity for extensive alterations to the computer infrastructure.

5. Experimental Section

Sensor Array Fabrication: The fabrication of the sensor array is shown in Figure 1a and required a combination of a digital printing process and a spin coating step. First of all, the customized heat sink was designed to fit the liquid cooling system but also to accommodate an external reference temperature sensor as well as two heating elements. The heat sink was manufactured from aluminum, providing good thermal conductivity. The side of the aluminum pointing toward the CPU was polished in a lapping process to avoid any piercing or distorting of the layers on top. A layer made from polyimide was deposited first to introduce electrical insulation between the heat sink and the sensor array. It was crucial to keep the layer as thin as possible to minimize the additional thermal resistance. The polyimide layer was fabricated from a polyimide precursor (PI2611, HD MicroSystems GmbH). First, the aluminum was thoroughly cleaned with 2-propanol and acetone. The precursor required an adhesion promotor (VM-651, HD MicroSystems GmbH), which was diluted to a concentration of 0.1 % with deionized water. 1 ml of the solution was dispensed on the heat sink, and kept there for 20 s, followed by a dry spin with 500 rpm for 90 s, and 1500 rpm for 20 s, respectively. Right after, the precursor PI2611 was applied to the surface and sequentially spun at 500 rpm for 10 s, and 3500 rpm for 30 s, respectively. The deposition was succeeded by a soft bake on a hotplate at 90 °C for 90 s and 150 °C for 90 s, respectively. For final curing, the samples were placed in an oven (LT 15/14, Nabertherm GmbH) and heated to 350 °C with a ramp rate of 4 °C min^{-1}. The temperature was kept constant for 30 min. The samples were removed after the oven reached ambient temperature again. The polyimide layer thickness was approximately 5 µm and exhibited a roughness of <500 nm.

As the next step, the temperature sensor array was printed using an aerosol jet printer (Aerosol Jet 5X System, Optomec, Inc.). This was conducted in four successive steps, each comprising a printing and a curing process: 1) Connection lines between flat cable and sensor array 2) Bottom electrode 3) Thermistor material 4) Top electrode. All printed conductive lines were fabricated from nanoparticle/water-based silver ink (JS-A221AE, NovaCentrix).[44] The ink was loaded into the ultrasonic atomizer (UA) cassette of the printer, requiring 3 ml of solution. The printer was equipped with an additional solvent add-back system, which was filled with deionized water and heated to 28 °C. The printing platform was held constant

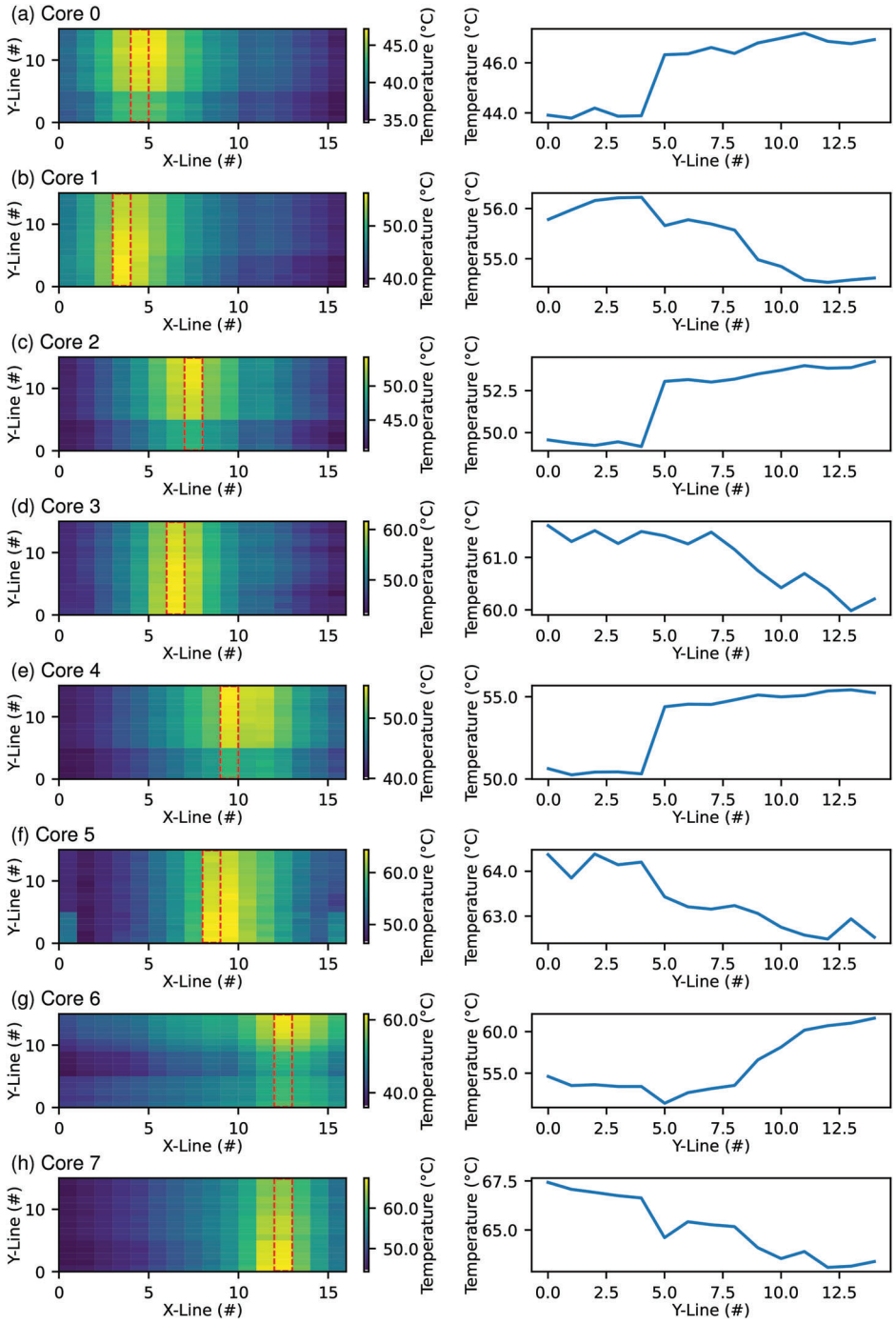

Figure 5. a–h) The images show the temperature response of the printed sensor array to the individually stressed cores of the CPU. The plot on the right side illustrates the temperature profile of the sensor pixels marked with the red box. Overall, the measured temperature fingerprint stands in great agreement with the position of the cores shown in the official CPU design depicted in Figure 3a. The x and y position of the hotspot can clearly distinguish each core position.

at 30 °C. First, the connection lines (1) were printed with a 600 µm nozzle and a printing speed of 15 mm s^{-1}. The sonication power of the ink tank was set to 500 mA and 27 °C. The atomizer flow rate was set to 50 sccm with a sheath flow rate of 220 sccm. Directly after deposition, the silver lines were photonically sintered (Pulseforge 1200, NovaCentrix) using 60 multi-pulse clusters with a frequency of 1 Hz at 400 V. Each cluster consists of 20 pulses with a length of 10 ms and exhibited a duty cycle of 50 %. The finished lines had a thickness of about 4 µm and a width of 230 µm (see Figure S5, Supporting Information) (Profilometer, DektakXT, Bruker). Second, we printed the bottom electrode (2) with a 200 µm nozzle at a speed of 10 mm s^{-1}. The atomizer flow rate was altered to 21 sccm with a sheath flow rate of 65 sccm. The printing was followed by the same

sintering process as described before. The bottom electrodes had a thickness of about 3 µm and a width of about 60–80 µm (see Figure S5, Supporting Information). Third, the thermistor lines (3) were printed at 90 ° with respect to the bottom electrodes. The uniformity of the thermistor lines significantly impacts the resistance values measured at each sensor pixel. It was discovered that operating the printing shutter caused slight pressure variations in the system, which had a minor effect on the atomizer flow rates, causing variations in the material deposition. To address this issue, a foil-based shadow mask on the sensor was employed, featuring a square opening with the size of the sensor and positioned where the thermistor lines were to be deposited. A generous tolerance was taken into account to keep the fabrication process simple. This enabled us to print the individual thermistor lines in a continuous meandering structure with high quality. Any structures outside the designated area could be easily removed by lifting off the mask, which is illustrated in Figure S1 (Supporting Information). For the printing process, a commercially available dielectric screen printing ink (LOCTITE EDAG PM 404 E&C, Henkel AG & Co. KGaA)[45] was modified to suit the requirements of the aerosol jet printer. To do so, 9 g of LOCTITE EDAG PM 404 E&C was diluted with 4.5 ml of triethylene glycol monomethyl ether (TGME) and thoroughly mixed using a vortex mixer. The properties of the resulting ink required the use of the pneumatic atomizer (PA) cassette (instead of the UA cassette) and an ink volume of 10 ml. The ink tends to agglomerate quickly and clog the orifice; therefore, the stirrer in the ink tank was set to 5 V and heated to 28 °C. The solvent add-back for both the atomizer and the virtual impactor stream was filled with 2-propanol and heated to 25 °C. To further improve the layer consistency, the 600 µm nozzle was chosen with a printing speed of 10 mm s^{-1}. The wider lines feature a more homogeneous layer thickness in the center of the line. For the pneumatic atomizer, the following parameters were used: the atomizer & virtual impactor flow rate was set to 1300 sccm, the virtual impactor exhaust pressure was set to 0.12 psi, the divert & boost flow rate was set to 300 sccm and the sheath gas flow rate was set to 200 sccm. In this case, the heat sink to be printed on was heated to 70 °C. To diminish print variations, 12 layers were deposited successively. After printing, the samples were placed in an oven (UF55plus, Memmert GmbH + Co. KG) at 120 °C for at least 6 h. The thermistor layer had a thickness of about 8 µ m and a width of 500 µm (see Figure S5, Supporting Information). The final and fourth step was the deposition of the top electrode (4). Although the printing was similar to the bottom electrode process, some printing and sintering parameters had to be adapted. Due to the underlying layers, the top electrodes were more susceptible to crack formation during the sintering process. Compared to the print parameters of the bottom electrode, the atomizer flow rate was decreased to 60 sccm. Additionally, the photonic sintering process was modified using only 20 multi-pulse clusters and a lower voltage of 340 V. The sintered top electrode line had similar properties to the bottom electrode, exhibiting a thickness of 2–3 µm and a width of <80 µm (see Figure S5, Supporting Information). Finally, the samples were placed in an oven for at least 24 h at 120 °C. We used an Intel Core i9 9900K processor, which was mounted on an ASUS Prime H310M-D Mainboard. Before use, the processor was delidded, releasing the bare CPU die. The remaining thermal paste was removed with 2-propanol. Due to space constraints and better accessibility of the components, a liquid cooling system (LQ240, Xilence GmbH) was chosen. The modified aluminum heat sink exhibiting the temperature sensor array was attached to the liquid cooling system. Fresh thermal paste was applied to the bare CPU die and covered with an ultra-thin 1.4 µ m Polyethylennaphthalat (PEN) plastic foil (Theonex Q72, DuPont Teijin Films) to ensure electrical insulation. The heat sink, including the sensor array, was mounted onto the CPU using the existing socket mounts of the mainboard. For operation, the PC was running the freely available CentOS 7 Linux distribution. To conduct a CPU stress test, Hyper-Threading in the UEFI settings while keeping Turbo Boost enabled was disabled. The PC was controlled over SSH from an external PC. To select and stress the CPU cores in a controlled manner, the shell commands were used: *stress-ng –matrix -l -t [time in seconds] –taskset [selected core(s)]*.[46]

The sensor array was connected to the readout electronics with a flat flexible cable (FFC) (WR-FFC 0.50 mm, Würth Elektronik eiSos GmbH & Co. KG), which was kept in place by pressing it downside-up onto the printed connection lines. The readout electronics were developed specifically for the requirements of the passive matrix sensor and are depicted in Figure S3 (Supporting Information). The experiments required at least a readout frequency of >10 Hz while suppressing as much noise as possible. The PCB was designed according to the zero-potential-scanning method.[40–42] The readout electronics were connected to an external PC to control the measurement and data acquisition.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Author Contributions

R.H., T.B., H.A., and U.L. designed and conceptualized the scope of this study while supervising the progress during execution. R.H. developed and printed the temperature sensor. The readout electronics were designed by D.B. Measurements performed on the CPU were conducted by R.H., T.B. and D.B. For reference, R.H. and L.F. modified the test setup and took thermal images. Finally, R.H. evaluated the data and prepared the first draft of the manuscript. All authors contributed to the discussing of the results and in writing the manuscript.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

aerosol jet, CPU monitoring, cyber security, fully printed, temperature measurement

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