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A high time resolution and high dynamic range ASIC for the micro-vertex detector in the PANDA experiment

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Abstract: A monolithic pixel sensor test chip for the PANDA micro-vertex detector has been implemented in a 180 nm HVCMOS technology on a high resistivity substrate. The sensor should have very high time resolution (1 ns sigma) and high dynamic range (up to 1000). The pixel electronics contains a charge sensitive amplifier, a feedback circuit and two comparators. One comparator receives the fast signal and enables accurate time measurement. The other comparator receives the low pass filtered signal and is used for precise amplitude measurement. This publication presents several novel features of the PANDA ASIC, its characterization and several measurement results.

Keywords: Analogue electronic circuits; Solid state detectors

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Contents

1 Introduction

The PANDA experiment will be one of the key experiments at the Facility for Antiproton and Ion Research (FAIR) [1]. A pixel detector is highly demanded for detection of ionizing particles and measurement of their trajectories. The specifications of such ASIC are summarized in table 1. Among them, high time resolution and large dynamic range are the most important specifications for a Micro-Vertex Detector for the PANDA experiment [1]. A hightime resolution is important for reconstruction because it will allow one sensor to precisely assign the particle signals to one track. A high dynamic range is important for particle identification because different particles have different average energy loss.

Table 1. Specifications for a Micro-Vertex Detector for the PANDA experiment.

Pixel size (prototype)	50 µm × 165 µm
Pixel size	80 µm × 80 µm
Detected particles	Charged particles
Charge measurement	12 bits and linear over 7 bits
Time resolution	1 ns
Dynamic range	1–100 MIP (i.e. 1 ke–100 ke for this chip)

To meet these requirements, a prototype pixel sensor, named PANDA ASIC, for the PANDA Micro-Vertex Detector has been designed and implemented in 180 nm HVCMOS technology on two high resistivity substrates (370 Ω cm and 5 kΩ cm) [2–4]. The PANDA ASIC contains a pixel matrix with 29 × 64 pixels of 50 µm × 165 µm size and digital readout circuits. The pixel electronics contains a charge sensitive amplifier (CSA), a feedback circuit and two comparators. One comparator receives the fast signal and enables accurate time measurement. The other comparator receives the low pass filtered signal and is used for precise amplitude measurement. Furthermore, several novel features have been implemented such as variable gain amplifier and a time to digital converter (TDC). The

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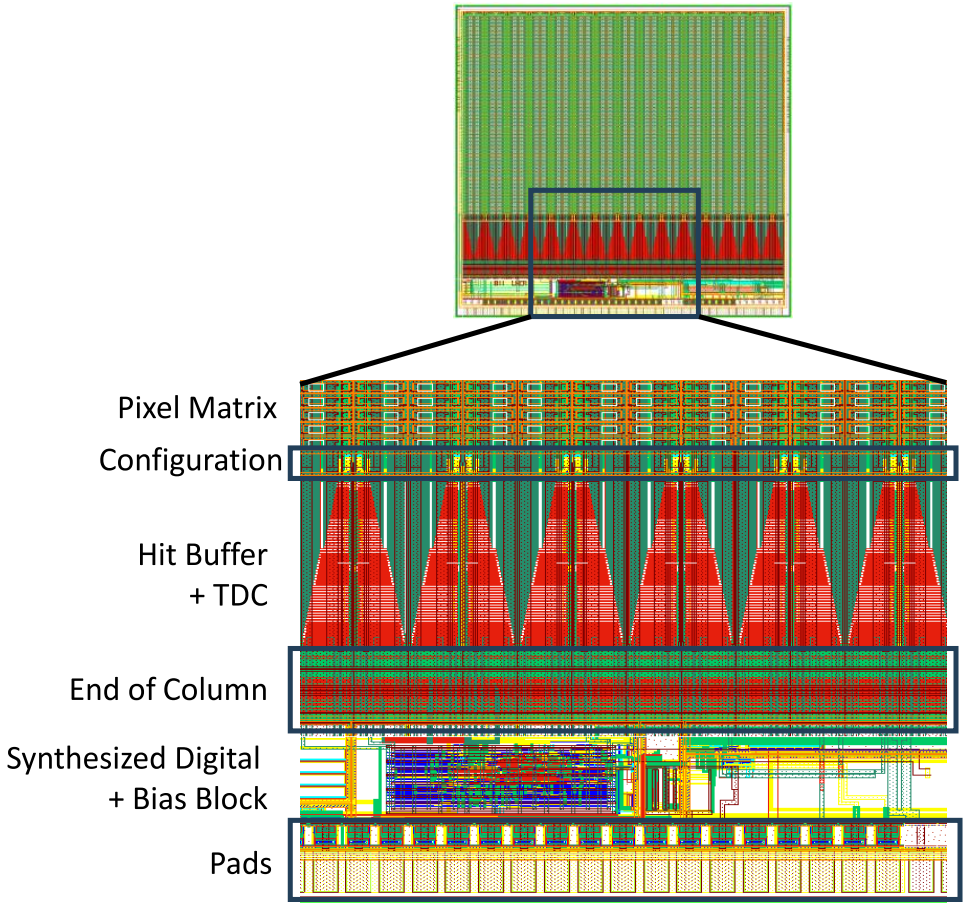

Figure 1. Chip architecture of the PANDA ASIC.

high time resolution can be achieved using the two comparators, the TDC and by correction of time walk. The high dynamic range can be achieved with the variable gain amplifier.

2 Pixel electronics of the PANDA ASIC

The architecture of the PANDA ASIC is presented in figure 1. The chip area is around 5 $mm \times 4.8$ mm. It consists of a pixel matrix of 29 columns and 62 rows, configuration bits, hit buffers, end of column (EoC) logic, bias DACs and pads.

The schematic of pixel electronics of the PANDA ASIC is shown in figure 2. It uses a standard folded cascode amplifier, which is a common choice for low voltage and high gain amplification. A PMOS transistor (TP6) is used as input, due to its low flicker noise and high radiation tolerance. A dedicated power supply VSSA is used for the amplifier. A typical value of VSSA is 1.2 V.

Furthermore, a current mirror in the bias block at the chip periphery provides the voltages for VN and VPLoad. To ensure a large amplification, a big transconductance and output resistance are needed. Since the transconductance is proportional to the bias current while the output resistance is inversely proportional to the load current, the bias current of TN5 is about 10 times larger than of TP4.

The second stage is a double source follower. It provides fast time constant and voltage level shifting. The bias current of the second source follower (VNFoll2) is smaller than that of the first source

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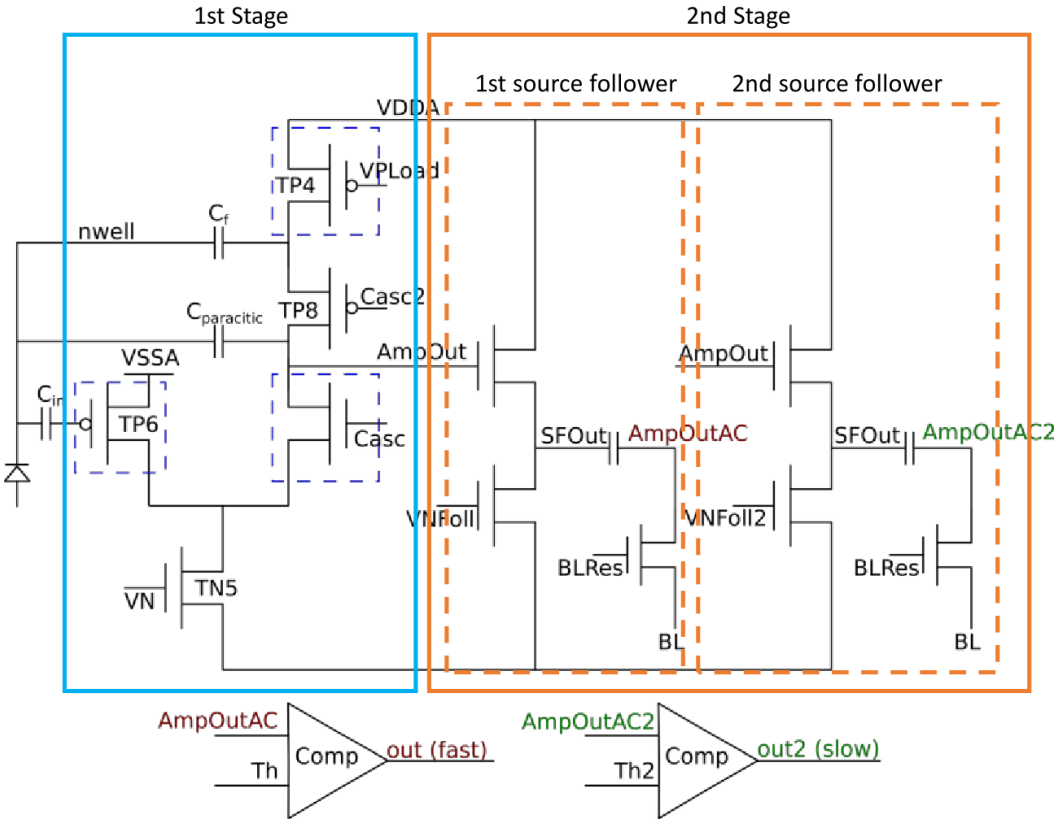

Figure 2. Pixel electronics of the PANDA ASIC.

follower (VNFoll). The second source follower acts as a low pass filter. The falling edge of its output (AmpOutAC2) is long, which reduces noise and improves SNR when the pulse width is measured.

One PMOS transistor TP8 is added to enlarge the amplification compared to the standard CSA and to implement variable gain. The CSA is designed to have larger gain when the signals are low and smaller gain when signals are high. For low signals the source voltage of TP8 is nearly constant and the capacitance C_f does not introduce feedback. Thus the gain is $1/C_{\text{parasitic}}$. For signals larger than the sum of the Casc2 voltage and the threshold voltage (Th), the source voltage of TP8 follows the AmpOut and the gain is $1/(C_f + C_{\text{parasitics}})$.

Furthermore, each pixel has two comparators and readout channels. In the fast channel, the first source follower is connected to the comparator. In the slow channel, the comparator is connected to the second source follower that acts as a low pass filter.

The two outputs of each pixel are connected to hit buffers. Slow and fast comparators have separated hit buffers. Each hit buffer contains a receiver, a 4-bit tune DAC, a fine time stamp circuit (time to digital converter), a row address generator and a hit buffer logic. The purpose of the hit buffer is to measure time and amplitude, generate the address and the hit bus signal, and to temporary store the hit information. There is a total of 47 bits of information per hit: 20 bits for the coarse time stamp measurement (TS1), 10 bits for energy measurement (TS2), 7 bits for fine time stamp measurement (TS3) and 10 bits for the row address. The time stamp frequency is typically 100MHz. TS1 uses two 10-bit counters, one clocked with positive edge and the other with the negative edge. The EoC block stores temporarily the hit information and adds the column address.

3 Time to digital converter

The hit time is measured by storing two time stamp values. One time stamp (coarse time stamp) indicates the hit time in input clock periods (clk). Another time stamp (fine time stamp) indicates the time position of the hit within the clock period, i.e. the time distance between the hit and the next rising clock edge. These two time stamp counters run with the same period of 10 ns and could be reset synchronously.

The schematic of the TDC is shown in figure 3. The output of the pixel comparator (hit) is connected to a flipflop FF to produce the hitSync at next rising clock edge. When the hit is received, a coarse time stamp is stored. The current sources Ibig and Ismall start to charge the capacitor. When hitSync is generated, the charging current changes to the lower current Ismall. The capacitor voltage is compared with a threshold Vth. The comparator output stores the fine time stamp. What matters here is the fine time stamp versus coarse time stamp difference, which is the duration between hit and the threshold crossing.

The circuit works as a time stretching TDC. The stretched (amplified) time is linearly proportional to the time distance between the hit and the next rising clock edge i.e. to the hit to hitSync time difference. The stretched time is calculated by subtracting two stored time stamps and multiplying by the input clock period clk:

$$\text{Stretched time} = (\text{TDC}_{\text{fine}} - \text{TDC}_{\text{coarse}}) \times T_{\text{clk}} \tag{3.1}$$

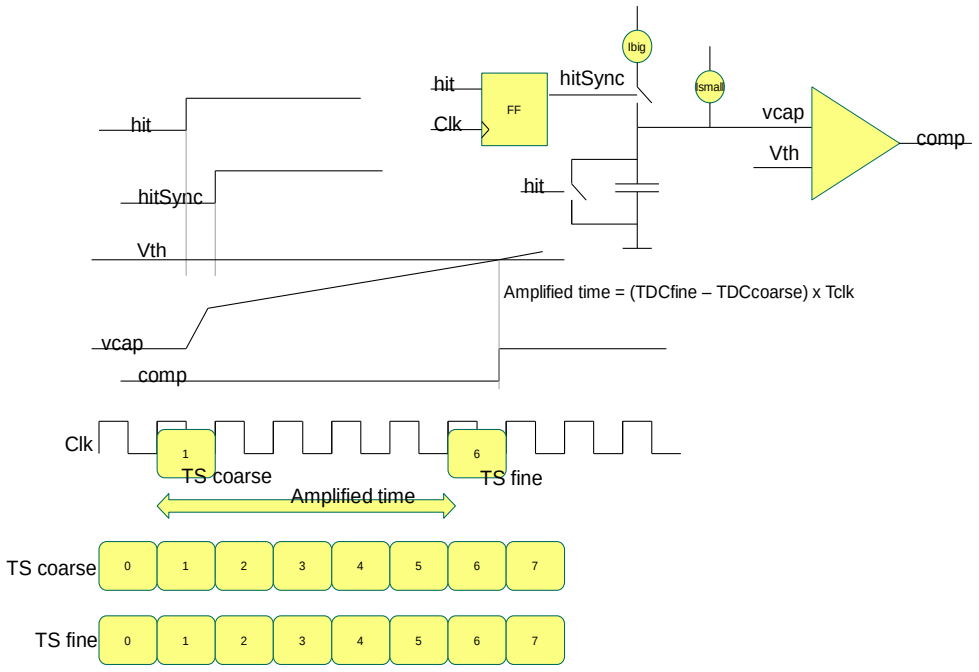

Figure 3. Description diagram of the TDC.

4 Experimental results

In order to test the performance of the test chip, a test system has been developed in our group. We use Nexys Video Artix-7 FPGA board to configure the chip and readout the digital data. The ASIC is wire

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bonded on a carrier board. A GECCO board is applied as interface [5, 6]. The GECCO board provides all necessary supply voltages as well as test signals and routes data lines from and to the FPGA.

The following measurements have been performed on the PANDA ASIC: pulse width calibration, time walk measurement, time and corrected time measurement versus pulse width, ToT and TDAC calibration.

4.1 Pulse width measurement

A measurement of the pulse width has been performed using an external injection circuit to test the high dynamic range. A charge injection circuit can be used to generate input signals for the amplifier. It is implemented on the carrier PCB and creates steep negative voltage steps with defined amplitude. The amplitude is defined by a DAC which can be programmed via the FPGA. The amplifier output can be measured directly via a test pad and the waveform captured with an oscilloscope. In the case of digital measurements, the time over threshold is digitized in the hit buffer and is readout using the digital part.

As mentioned, there are two channels inside each pixel. The pulse widths are different. The fast channel uses the source follower with the larger bias current, the slow channel uses the source follower with the smaller bias current. Therefore, the pulse width of the fast signal (red in figure 4) is shorter than the pulse width of the slow signal (black in figure 4). Figure 4 (right) shows the sigma values (RMS) of the pulse width. The sigma value for the slow channel is smaller, leading to significantly larger SNR.

The average ToT noise is about 48 ns ± 2.3 ns for the slow comparator. The gain for the small signals can be obtained fitting the ToT versus injection charge plot (figure 4 left), and it is 0.413 ns/e ± 0.02 ns. The noise in electrons is obtained dividing the noise by the gain and it is 116 e ± 6 e. The injection circuit is only linear up to 1 V, corresponding to 35 ke. The ratio of maximum measured signal (35000 e) and noise is about 302.

This is a promising result and shows that particle signals in the specified range 1–100 MIPs can be measured: we can vary the signal that a MIP will produce by adjusting the depletion voltage. We can set MIP to be ten times the noise, thus roughly above 1 ke. One should mention here that the amplifier could also measure stronger signals, the maximum signal was limited by the injection circuit.

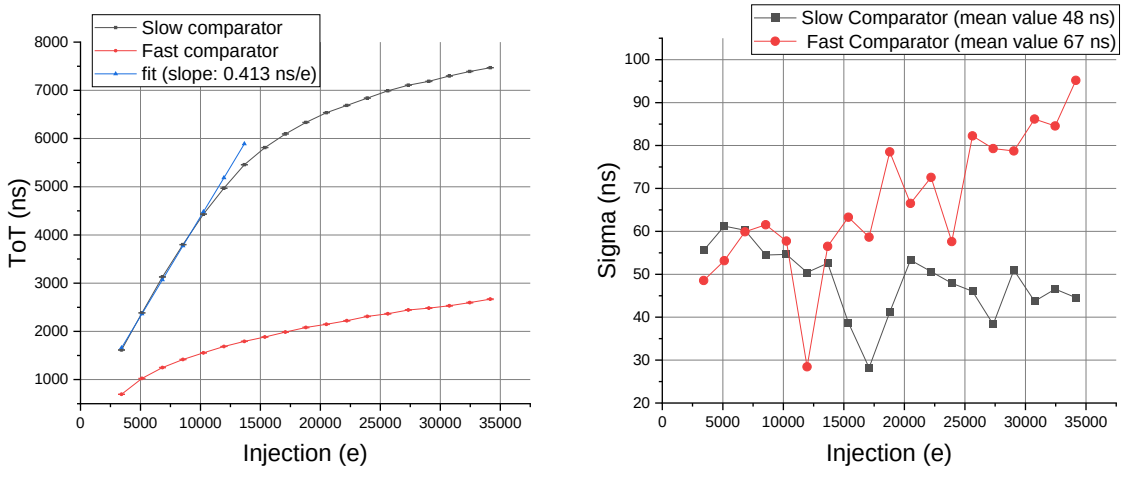

Figure 4. Pulse width of the slow and fast comparator versus injected charge (left). Sigma of the measured pulse width versus injected charge (right).

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4.2 The time walk measurement

A time resolution of 1 ns is specified for the PANDA micro-vertex detector. Time resolution is normally limited by the time walk effect caused by the variation of the signal size. The bigger the signal, the earlier the comparator fires. Because of the time constants of the amplifier and comparator, signals with larger amplitudes cause faster response. Signals that are just above threshold lead to excessive delay. The time walk value can be estimated by measuring the relation of the injection pulse delay and the generated time stamp value for different injection amplitudes.

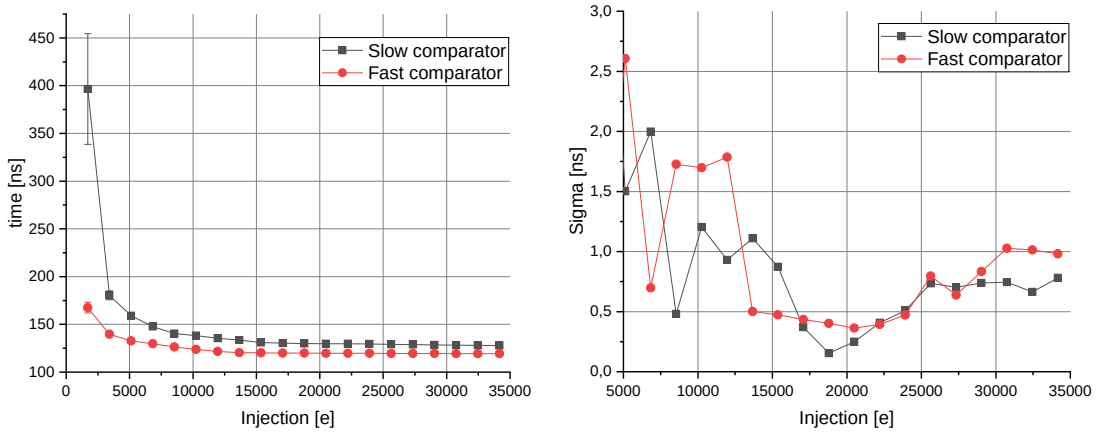

Figure 5. Measured comparator response time versus injected charge (left). Sigma of the measured time versus injected charge (right).

Figure 5 (left) shows the measured response time. The analogue signal is measured through the analog pads with an oscilloscope. The phase of the injection is always the same with respect to the system clock. The time walk of the fast comparator (red) is smaller than the time walk of the slow comparator (black) since its rising time is shorter. For small signals, the time walk for both fast and slow comparators are large. After repeating the measurement multiple times, the sigma is calculated and plotted in figure 5 (right). The signal slope at the threshold crossing is small for small signals, leading to large sigma.

4.3 Corrected time resolution

The relationship between the comparator response time and the pulse width is presented in figure 6 (top left). The x coordinate is the ToT of the slow comparator, and the y coordinate the measured time. Each point is the result of one injection. The injections have been varied from 150 mV to 800 mV with 50 mV step.

The time at which the signal crosses the threshold is smaller when the ToT is larger. An exponential function has been fitted to the data, which can be used for the time walk correction.

$$y = 33.52 + 35.06e^{(-(x-17.88)/28.08)} \tag{4.1}$$

The corrected time versus measured ToT and its histogram are shown in figure 6 (top right and bottom respectively). The time resolution is 1.28 ns ± 0.17 ns (RMS). The specification is almost fulfilled.

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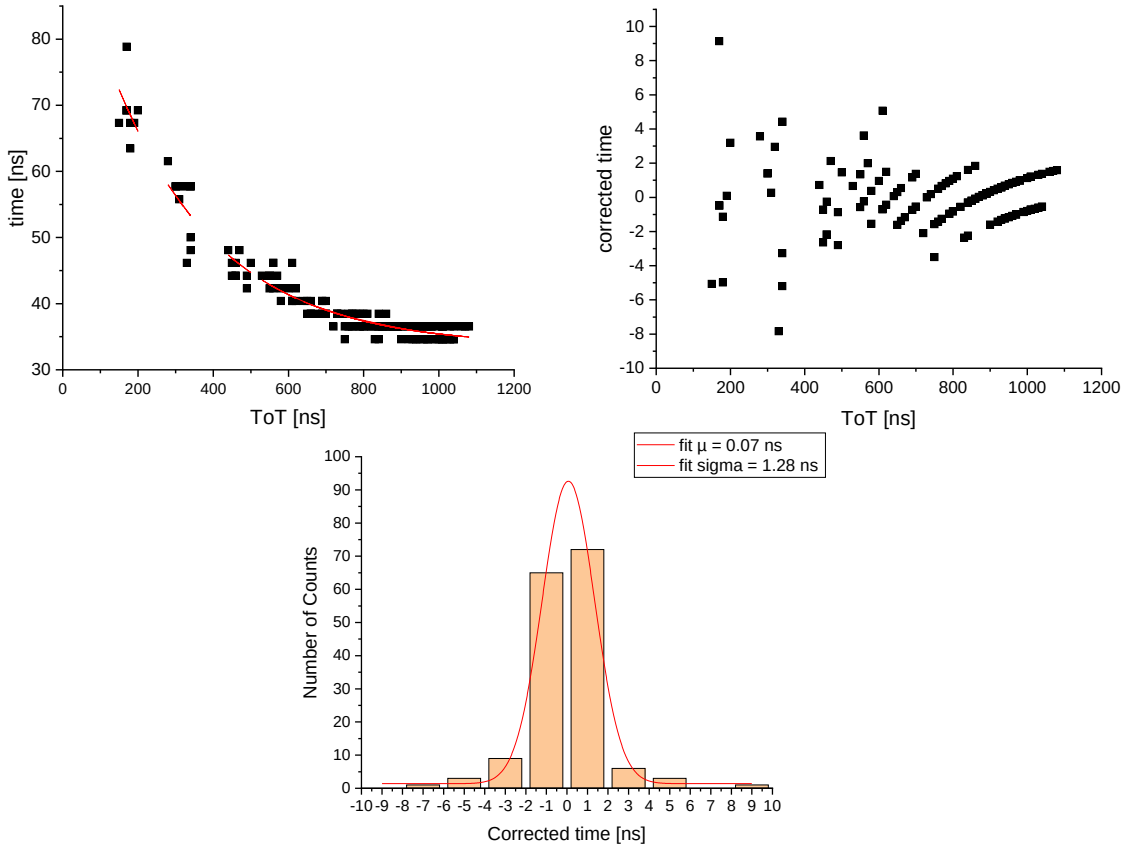

Figure 6. Comparator response time versus different pulse widths (top left). The x coordinate of each point is ToT measured with the slow comparator and the y coordinate is the response time measured with the fast comparator. Each point is the result of one injection. The injections have been varied from 150 mV to 800 mV with 50 mV step. The corrected time versus measured ToT and the corrected time histogram are also shown (top right and bottom respectively).

5 Conclusion

We are developing a monolithic pixel sensor for the PANDA micro-vertex detector. To evaluate the design a test chip has been designed, produced and tested. The test chip contains a pixel matrix with 29×64 pixels of 165 µm $\times$ 50 µm size and digital readout circuits. The chip has been implemented in a 180 nm HVCMOS technology.

The pixel electronics contains a CSA, a feedback circuit and two comparators. One comparator receives the fast signal and enables accurate time measurement. The other comparator receives the low pass filtered signal and is used for precise amplitude measurement. Several novel features have been implemented such as variable gain amplifier and time to digital converter with time-stretching (time-amplification). The design goal is to achieve a time resolution of 1 ns sigma and a high dynamic range of 1000. The high time resolution can be achieved using two comparators, a TDC and by correction of the time walk. A high dynamic range can be achieved by the adaptive gain amplifier.

The time walk corrected time resolution from measurements is 1.28 ns $\pm$ 0.17 ns. For comparison, the value obtained in simulation is around 0.7 ns. The experimental result presented in this paper is taken from a single pixel. The spread in the reported value obtained from measuring a number of pixels is only

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0.17 ns. A dynamic range of about 300 has been measured using an external charge injection circuit. Planned design improvements to reach the specified values for time resolution and dynamic range include reduction of detector capacitance, and thus noise, through optimisations in the circuit layout.

The design of the next prototype, named MiniPANDA, with the final pixel size pixel pitch of 80 µm has been completed. Small pixel size is required for spatial resolution. The layout routing is more complex due to the restricted area. Following submission and testing of the MiniPANDA ASIC, the full size sensor will be designed.

Acknowledgments

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