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Evaluating the RFSoC as a Software-Defined Radio readout system for Magnetic Microcalorimeters

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Abstract: Arrays of superconducting sensors enable particle spectrum analysis with superior energy resolution. To efficiently acquire data from frequency multiplexed sensors, the readout electronics operating at room temperature must perform multiple tasks, such as low-noise probe tone generation, frequency demodulation, and data decimation. We designed a Software-Defined Radio (SDR) system composed of an MPSoC board, an analogue-digital conversion stage, and a radio frequency front-end mixing stage to meet the system requirements of 4 GHz instantaneous bandwidth and real-time data analysis. Nevertheless, utilising a Radio Frequency System-on-Chip (RFSoC) could simplify the overall system by integrating the conversion stage. This work investigates the applicability of RFSoCs for the aforementioned use case.

Keywords: Data acquisition concepts; Modular electronics; Cryogenic detectors; Calorimeters

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Contents

1 Introduction

Software-defined radio (SDR) systems rely on digital signal processing (DSP) for their flexibility in signal modulation and data decimation. The accuracy and bit depth of any signal are not fixed and are rarely bound by computing limits. Consequently, the fidelity of any transmission is coupled to the quality of the analogue-to-digital (AD/DA) conversion stage. While a plethora of application-specific integrated circuits (ASICs) can be selected to form a custom system, the increasing data throughput for high sample rates complicates the link and board design from DSP to DA; a portion of logic is reserved for data transmission, some power is allocated to the transceivers, high-speed lanes require particular routing rules, and board space grows with the number of packages. AMD Xilinx has addressed this by creating the Zynq Ultrascale+ RFSoC family, integrating an FPGA MPSoC and some DA onto a single silicon substrate.

Frequency multiplexed cryogenic experiments are increasingly being read out by SDR systems [1–3]. In this work, we compare the RFSoC approach with a custom 4 GHz bandwidth DAQ system developed for the ECHo experiment [4, 5]. Since RFSoCs were not yet available when conceptualising the readout system, a holistic approach with dedicated converters was implemented: the digital back end contains the programmable logic and the processing system, while the data converters are on a separate board. Data transfer between the FPGA and the converters takes place via the high-speed transceivers. While the DAC used on the ECHo DAQ system is specifically configured to operate at $1\,\mathrm{GS\,s^{-1}}$, operation of the DACs on the RFSoC is more flexible. Therefore, part of the RFSoC characterisation is the evaluation of the signal quality with higher DAC sampling rates. The RFSoC approach was evaluated with the ZCU216 evaluation board. It is based on the ZU49DR, a third-generation device that provides 16 14-bit DACs with sampling rates up to $9.85\,\mathrm{GS\,s^{-1}}$ and 16 14-bit ADCs with sampling rates up to $2.5\,\mathrm{GS\,s^{-1}}$.

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Any ADC or DAC is reliant on its reference signals for its noise and spurious performance, with any reference voltage noise directly affecting the output level and jitter decreasing the spectral purity of every tone. The advantages of combining digital logic and AD into one package, as in an RFSoC, are thus counteracted by increasing the proximity of crosstalk sources. This effect, if appreciable, is of interest to this study. Nevertheless, both approaches operate at room temperature and can interface a plethora of frequency multiplexed cryogenic circuits through their programmable nature. Current applications within our group include the readout of Metallic Microcalorimeters (MMCs) [6], superconducting qubits [7], and more recently, Magnetic Microbolometers (MMBs) [8].

2 Hardware setup

Both of the architectures under evaluation here can interface the radio frequency front-end electronics in development for ECHo [5]. This means interfacing a complex analogue pair of baseband signal lines, both for the transmission direction through DACs and in reception for the ADCs. The platforms are compared in the DC to 400 MHz domain by analysing the output on a spectrum analyser and feeding in a low-distortion sinusoidal carrier from a radio frequency synthesiser. As the platforms feature high-density connectors, the measurements are performed through BalUn conversion cards, providing SMA connectors.

The ZCU216 evaluation kit is shipped with a BalUn board that offers various frequency ranges. However, for the aforementioned application in the ECHo experiment, this is not usable since it provides only two ports in the relevant frequency band below 1 GHz. The radio frequency front-end electronics are able to convert the 4 GHz bandwidth frequency comb into five baseband signals with I and Q components each. In total, 10 BalUn ports with transformers designed for frequencies below 1 GHz are required. Therefore, a custom board fulfilling this requirement has been developed.

While the ECHo SDR system has a central clocking unit containing a dual loop jitter cleaning PLL (Analog Devices HMC7044) with which all circuit constituents are provided their reference, the ZCU216 comes with an add-on clock card (CLK104) and will be measured with clocks from either source. All clocking configuration is performed through manufacturer-recommended register sets extracted from simulation software.

3 Firmware components and differences

One of the main challenges in developing the firmware for the MPSoC-based readout system for the ECHo experiment was the correct communication between the FPGA and the data converters. The converters need to be configured via SPI, which requires custom Linux kernel drivers and modifications in the device-tree for the processing system. Data transfer is implemented via the JESD204B protocol. Within the programmable logic, several IP cores are required for ensuring device synchronisation, data validity, and error correction. Implementation of these IP cores, including the necessary handling of control signals and status information, consumes precious resources, increases the build time and complicates the overall system.

On the RFSoC, however, the AD and DA converters are on the same die as the programmable logic, so the complex JESD interface is not needed. Instead, communication with the converters is controlled via the Radio Frequency Data Converter (RFDC) IP core provided by the manufacturer. Though there is no exact information on what the silicon contains, there is no need for the calibration of

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serial link lines or a specific deterministic latency procedure. The RFDC offers various configuration capabilities, such as the sampling rates of individual converters and the number of parallel samples in the digital domain. Additionally, internal mixing in the ADCs is available so they can be configured to operate exactly as the external devices in the ECHo readout electronics.

The digital interface on the RFSoC is kept identical to the ECHo system. Therefore, the digital signal generation and the full digital readout chain containing frequency demultiplexing, sample decimation, and data transfer can be retained. Evaluation of the effect of higher DAC sampling rates on the signal quality requires the transmission of more digital samples to the RFDC. To keep the system as flexible as possible, the bit-width of the vector containing parallel digital samples was kept identical, while the clock rate of the signal generation module increased for higher sampling rates of the DAC. To ensure a sufficiently small step size of the generated tones even for higher frequencies, the size of the BRAM containing the digital samples was increased.

FPGA resource consumption, as given in table 1, is slightly (10% FF and LUT) reduced for the RFSoC approach. This is achieved by omitting the IP cores for the JESD interface and only contrasted through increased BRAM usage for the aforementioned higher sample rate.

Table 1. FPGA resource usage comparison between the ECHo DAQ system and the Xilinx RFSoC evaluation card ZCU216.

Type \ Device	**MPSoC (ZU19EG)**	**RFSoC (ZU49DR)**
LUT	86754 (16.6 %)	74833 (17.6 %)
FF	126697 (12.1 %)	110887 (13 %)
BRAM	328.5 (34.2 %)	348.5 (33 %)
DSP	253 (12.9 %)	256 (6 %)

4 Output characterisation

In the first step, the output frequency response is determined. A tone generation module sweeps through various continuous wave (CW) stimuli. The output amplitude is determined with a spectrum analyser (Rohde & Schwarz FSWP50), which also enables scrutiny of spurious contributions beneath the intended carrier. The phase is not determined for evaluation, as it requires a well-defined reference plane that depends on the experimental setup and can be adjusted at will in the digital domain. Both platforms show very similar total output power and slope (see figure 1 left). This is based on the output matching networks for each respective current steering DAC and differences in PCB trace length amounting to variance in loss. Either transmission channel includes a 400 MHz anti-alias filter to prevent ambiguous signal output, which is easily identified by the sharp level drop off in the diagram. The spurious free dynamic range (SFDR) was evaluated over a 1 GHz bandwidth to test the full output band up to 600 MHz, including the stop-band of the alias filter. The resulting curves are very similar again, with an exception when the data and sample rate on the RFSoC are doubled, expanding the first Nyquist zone and therefore providing better image rejection (see figure 1 right).

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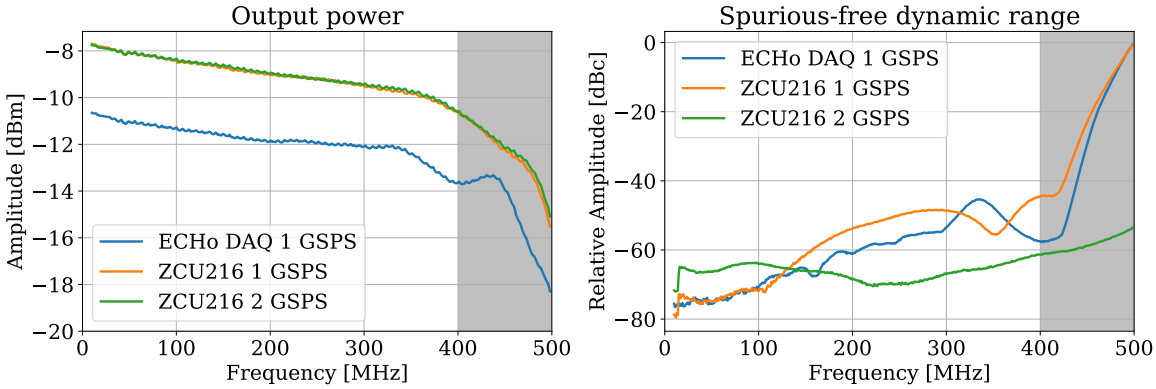

Figure 1. DAC output characteristics for both platforms. The gray region covers the roll-off and Nyquist image guard band.

5 Input characterization

The AD side is not just fed with a single carrier but a quadrature signal from the DACs and an arbitrary waveform generator (AWG, Active-Technologies AWG5064). The data streams are then extracted as raw samples, converted to a voltage, and subsequently transformed into a power spectral density (see figure 2 left). The carrier power shows similar behaviour as the DA side when driven in loopback, with a slope of around 4 dB and minimal ripple. The spurious free dynamic range shows broadly similar frequency dependence, except in some regions where the ZCU216 drastically improves in very narrow frequency regions (see figure 2 right). In contrast, the AWG signal source enables an improvement in ADC SFDR of up to 20 dB.

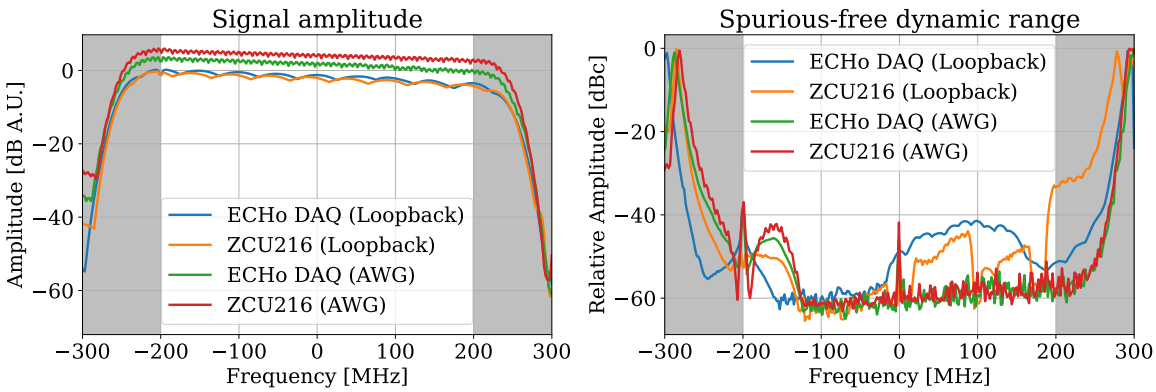

Figure 2. ADC input characteristics for both platforms. The Frequency on the X axis is complex as the ADCs output data after internal digital downconversion (see section 2). SFDR is limited by DAC performance in direct loopback and improves with an external signal source.

6 Phase noise

The clocking subsystem of the ECHo DAQ board as explained in [5] can provide reference clocks up to 3 GHz, while the AMD Xilinx evaluation board contains clocking devices capable of up to 15 GHz.

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The latter shows slightly increased integrated jitter due to a different phase-locked loop (PLL) circuit (see figure 3 left). A major motivation for this is coverage of the increased maximum sample rate from 2.8 GS s^{-1} on the ECHo system to 10 GS s^{-1} on the RFSoC. Though this exact ASIC is not used for AD clocking in the custom stack, it is used as a frequency reference for radio frequency mixing; its characteristics are also seen there and are again virtually identical. As the ZCU216 allows for fully external clocking, the ECHo DAQ stack can also be used to provide the clock reference. This closes the gap in jitter performance (see figure 3 right).

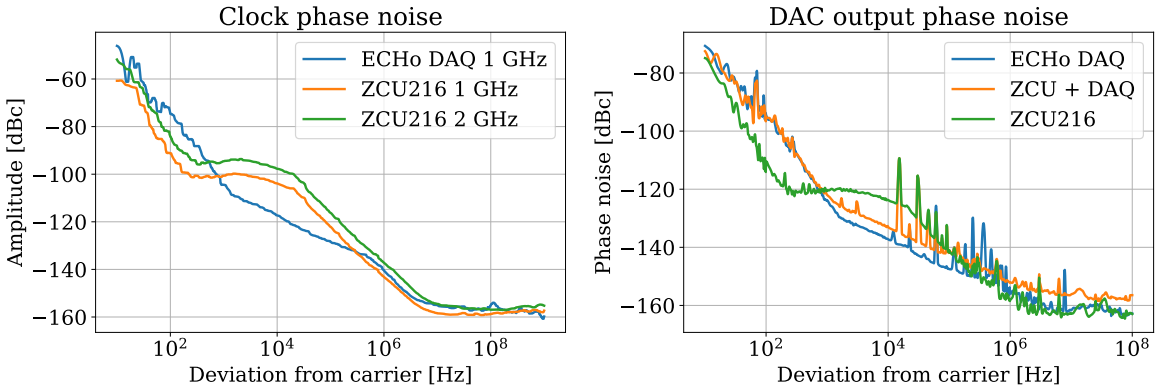

Figure 3. Phase noise of the clock reference and DAC output. The characteristic of the ECHo electronics are apparent when sourcing the clock to the ZCU216. The vertical offset is caused by a lower clock amplitude.

7 Conclusion

Due to wider Nyquist zones and far-off image frequencies that can be low-pass filtered, a better SFDR of the RFSoC is apparent, in particular at high frequencies. While care must be taken when providing the clock reference, the spectral purity is on par with custom-built systems. Furthermore, spatial channel density is increased when using the RFSoC, therefore simplifying the board design. Similarly, firmware complexity decreases significantly when using the more integrated approach of the RFSoC, while simultaneously increasing the possible operation modes of the converters. Overall, the custom ECHo DAQ and the ZCU216 show very similar performance in our tests, which makes them a suitable choice for further integration of SDR systems.

Acknowledgments

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