ADVANCED MATERIALS INTERFACES
Open Access
www.advmatinterfaces.de

Check for updates

α-TeO_2 Oxide as Transparent *p*-Type Semiconductor for Low Temperature Processed Thin Film Transistor Devices

*Nehru Devabharathi, Sandeep Yadav, Vanessa Trouillet, and Jörg J. Schneider**

In comparison to reports on *n*-type semiconducting oxides, *p*-type oxide semiconducting materials are still rare. Scarcely reported *p*-type oxide transistors demonstrated unsatisfactory environmental stability which still hinders their implementation for all oxide transistors and circuit applications. In this study, for the first time on α-TeO_2 as an active channel material with *p*-type characteristics accessible by direct evaporation technique. Notably, the fabricated 5 nm α-TeO_2 thin film in connection with an equally thin passivation layer exhibits a remarkable low processing temperature of 50 °C generating a hole mobility of 3.8 $cm^2\ V^{-1}\ s^{-1}$, an on-state current of 966 µA, and an on/off ratio of 3.8×10^3. Additionally, the reproducibility of these devices confirmed a narrow variation in the TFT metrics, yielding an average hole mobility, on-current, and on/off ratio of 3.59 $cm^2\ V^{-1}\ s^{-1}$, 914 µA, and 3.3×10^3, respectively. Furthermore, the devices are subjected to extensive stability testing under ambient atmospheric conditions that exhibits a marginal mobility reduction while maintaining a stable on/off ratio over 125-day period, highlighting their robust environmental stability. Notably, the low processing temperatures with both exceptional transistor performance and environmental endurance makes them suitable for the integration onto flexible substrates, particularly bendable/stretchable displays.

1. Introduction

Decades of research work have been devoted in oxide semiconducting materials for the realization of next-generation transparent/flexible electronic devices in a wide range of application areas including wearable/implantable, healthcare, high end displays and smart textiles.[1–6] Notably, their remarkable electronic properties, superior thermal/environmental stability, high transparency, and low processing cost have enabled them to realize in potential commercialization of high speed/high-definition displays and energy efficient transparent electronic devices. As an outcome of these efforts oxygen deficient *n*-type oxide semiconductors have shown nearly equivalent transistor performance with polycrystalline silicon.[5,7–9] However, on the downside, the *p*-type oxide semiconductors still demonstrate inferior/poor transistor performance compared to their *n*-type oxides owing to their highly localized oxygen 2p orbitals in the valence band maxima (VBM) resulting in high hole effective mass. As a result, they demonstrate unsatisfactory carrier transport properties. In fact, the available *p*-type oxide semiconducting materials itself are still scarce. Moreover, they require stringent environmental and fabrication conditions. Such drawbacks in obtaining a good performing high mobility *p*-type metal oxide semiconducting (PMOS) field effect transistors have limited many crucial applications such as all oxide complementary metal oxide semiconductor (CMOS) logic circuits, bipolar transistors, *p-n* junction devices and solar cells.[10,11]

Thus, until now, oxide semiconductors with *p*-type characteristics are limited to Cu_xO, NiO, SnO and delafossite-type $CuMO_2$ where M = Al, Cr, In etc.,[12–16] Among these, Cu_xO and delafossite materials display a very low device mobility of <1 $cm^2\ V^{-1}\ s^{-1}$ with the lowest reported processing temperature of 250 °C.[17,18] Especially delafossite *p*-type materials require much higher temperature to deliver a meaningful electronic performance. In contrast, SnO and NiO semiconductors demonstrate comparatively better mobility values;[19–21] However, they lack environmental stability issues as well as sufficient transparency in the visible, which altogether is a major drawback in applications. In this regard, recently tellurium oxide (TeO_2) has been identified as a promising and emerging *p*-type semiconducting material. TeO_2 is an interesting wide bandgap (3.5 eV) *p*-type oxide semiconducting material[22] present both in crystalline and amorphous form with excellent functional properties that makes it suitable for

N. Devabharathi, S. Yadav, J. J. Schneider
Department of Chemistry
Eduard-Zintl-Institute
Inorganic Chemistry
Technical University Darmstadt
Peter-Grünberg-Str. 12, 64287 Darmstadt, Germany
E-mail: joerg.schneider@tu-darmstadt.de

V. Trouillet
Institute for Applied Materials (IAM-ESS), and Karlsruhe Nano Micro Facility (KNMFi)
Karlsruhe Institute of Technology (KIT)
Hermann-von-Helmholtz-Platz 1, B 321, 76344 Eggenstein-Leopoldshafen, Germany

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/admi.202301082

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH. This is an open access article under the terms of the Creative Commons Attribution License, which permits use, distribution and reproduction in any medium, provided the original work is properly cited.

DOI: 10.1002/admi.202301082

technological applications including modulator,[23] deflectors,[24] optical storage materials,[25] phototransistors,[26] laser devices,[27] and gas sensors.[29] It exists in three polymorphs α, β and γ; wherein β-TeO_2 is a 2D layered material which has recently demonstrated a very high room temperature average hole mobility of 146 $cm^2\ V^{-1}\ s^{-1}$. However, it is currently only accessible by a surface oxidation route using molten metallic tellurium.[30] In addition, the process needs the handling of selenium alongside a molten liquid printing method. Altogether this is not an ideal situation for an incorporation into fabrication processes of electronic devices. Nevertheless, TeO_2 has three known polymorphs, tetragonal α-TeO_2 ($P4_12_12$), orthorhombic β TeO_2 ($Pcba$) and γ TeO_2 ($P2_12_12_1$) possessing different arrangements of corner sharing TeO_4 as basic structural units.[28,30,22] Among these three polymorphs, α-TeO_2 has been previously investigated primarily for their optoelectronic properties. To the best of our knowledge there have been no reports demonstrating its *p*-type hole mobility characteristics. Furthermore, attractive low temperature fabrication procedures of oxide-based *p*-type TFTs using *p*-type oxide semiconductors are rare and therefore, the present study mainly aims to show a better *p*-type TFT device characteristics when compared to the scarcely existing unsatisfactorily performing *p*-type oxide semiconductors with minimal fabrication steps. In addition, we introduce an emerging α-TeO_2 material for the first time to exploit its *p*-type device characteristics majorly by concentrating to lower the oxide TFT processing temperature close to the room temperature.

Herein, we report on a gas phase approach to exploit the electronic properties of α-TeO_2 oxide as a *p*-type semiconducting material for TFT fabrication. The *p*-type α-TeO_2 is deposited as active thin film alongside with a passivation layer achieving a hole mobility value of 3.8 $cm^2\ V^{-1}\ s^{-1}$, an on-state current and on/off ratio of 966 µA and 3.8×10^3 respectively, at a remarkable low processing temperature of only 50 °C. The fabricated devices have shown an excellent reproducibility with the average hole mobility, on-current and on/off of 3.59 $cm^2\ V^{-1}\ s^{-1}$, 914 µA and 3.3×10^3 considering two different batches of eight devices each. Importantly, the devices have been passivated with a thin layer of Al_xO_y (5 nm) and tested for their stability while storing at ambient atmospheric conditions over a period of >4 months. The stored devices have exhibited only a slight decrease in the mobility value from 3.8 to 2.5 $cm^2\ V^{-1}\ s^{-1}$, and almost a stable on/off ratio from 3.3×10^3 to $3.8 \times 10,^3$ demonstrating that the devices show a good environmental stability. The passivation of ultrathin Al_xO_y layer on active semiconducting film of α-TeO_2 showed a significant effect on improving the mobility, reducing the off state current and a substantial improvement on the device stability. The unique low temperature processing of these devices allows a fabrication on any kind of flexible substrate and thus opens the door for application, e.g., in bendable/stretchable displays.

2. Results and Discussion

2.1. Characterization of the p-Type Semiconductor Thin Film

α-TeO_2 thin film samples have been prepared on a 1×1 cm^2 SiO_2 substrate from α-TeO_2 powder by thermal evaporation (see Figures S1 and S2, Supporting Information). Prior to deposition of a 5 or 10 nm α-TeO_2 films, the substrates have been washed with acetone and isopropanol followed by subsequent treatment with UV light (254 nm). Morphological analysis of the 5 nm α-TeO_2 deposited thin film reveals a homogeneous, smooth and featureless characteristics of the film (**Figure 1a**).[32,33] Raman peaks of the 5 nm TeO_2 film observed at 230 and 647 cm^{-1} corresponds to the B_1 (5) and A_1 (4) vibrational modes which are characteristic for α-TeO_2; Notably, the two peaks at 647 cm^{-1}, and 230 cm^{-1} are mainly attributed to the symmetry and asymmetric stretching modes (Figure 1b). **Figure 2a** presents surface topography as determined by AFM of the as deposited 5 nm α-TeO_2 thin film (rms 0.14 nm). The additionally deposited 5 nm passivation layer (Figure 2b) shows an ultra-smooth surface (rms 0.11 nm). The remarkable smoothness of the Al_xO_y passivation layer is highly beneficial in forming a conformal interface without pinholes and voids in the active semiconducting surface layer of α-TeO_2. A topography for 10 nm and 30 nm deposited α-TeO_2 films demonstrates a comparable smooth surface (Figure S3a,b, Supporting Information) with respect to an increase in film thickness. Interestingly, the cross-section AFM micrographs (Figure 2c,d) of the as deposited α-TeO_2 film reveals an even lower height profile of 3.8 nm contrasting with a slightly larger profile height of 5 nm obtained by quartz crystal microbalance determination during evaporation (±0.37 Å).

The cross-sectional HRTEM analysis (Figure S4a,b, Supporting Information) of the deposited Al_xO_y -TeO_2 bi-layer film composite consisting of individual 5 nm α-TeO_2 and 5 nm Al_xO_y reveals a crystalline α-TeO_2 film with an interlayer distance of 0.326 nm which is in sound agreement to 0.340 nm reported for the [110] reflection of bulk α-TeO_2 (JCPDS 42–1365). In comparison and in contrast, the [102] reflection for β-TeO_2 is at a distance of 0.41 nm.[29] The deposited amorphous Al_xO_y film is of comparable thickness compared to the α-TeO_2 which can be clearly seen in Figure S4b (Supporting Information). A chemical surface analysis of the deposited TeO_2 thin films, with and without Al_xO_y passivation layer by X-ray photoelectron spectroscopy (XPS, for survey spectra see Figure S5a–c, Supporting Information) reveals the Te $3d_{5/2}$ and O 1s core levels of the deposited α-TeO_2 thin films (5 and 10 nm) together with a α-TeO_2 powder sample for comparison, respectively (**Figure 3a,b**). The main peak at a binding energy of 576.6 eV for Te $3d_{5/2}$ can be assigned to α-TeO_2 paratellurite for both film and powder materials. (Figure 3a). The corresponding O 1s peak is found at a binding energy of 530.9 eV[31] with a ratio oxygen to tellurium of nearly 2:1 which attests the presence of stoichiometric TeO_2. Apart from this major peak, a species with minor intensity is observed at a binding energy of 573.4 eV, reflecting the presence of elemental tellurium in the film.

The tellurium contribution increases with the thickness of the film and the time of deposition, however, is very minor for the 5 nm TeO_2/Al_xO_y composite film. It can be explained by a reduction process occurring during the TeO_2 deposition or by decomposition of TeO_2 under the chosen experimental conditions. Indeed, TeO_2 at temperatures above 550 °C decomposes into TeO which is unstable against Te(0) and O_2.[32–34] Nevertheless, the presence of such trace amounts of elemental Te^0 might have an impact on improving the transistor characteristics as it is one of the well-known *p*-type semiconducting material reported recently demonstrating good device characteristics.[35] Similarly, the final device architecture consisting of a bi-layer of α-TeO_2 and alumina passivation layer processed at 50 °C has also been studied with

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH

21967350, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/admi.202301082 by Karlsruher Institut F., Wiley Online Library on [25/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

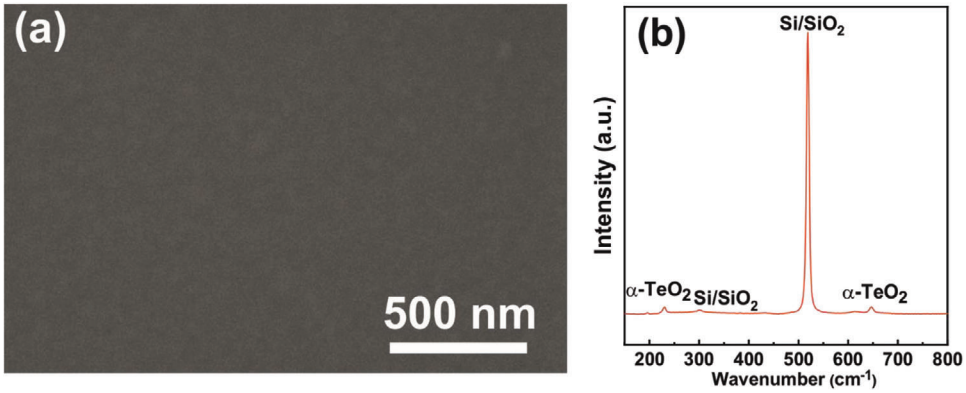

Figure 1. a) Scanning electron microscopy of the evaporated 5 nm α-TeO_2 film demonstrating deposition of a dense, homogeneous and void free thin film. b) Raman spectroscopy of the deposited 5 nm α-TeO_2 film on a SiO_2 substrate.

XPS (Figure 3c–e). Not unexpected, the deposited metallic aluminium layer in the bi-layer film has been oxidized into amorphous Al_xO_y to which the Al $2p_{3/2}$ binding energy at 74.8 eV corresponds well. In that regard it is interesting to note that in the bi-layer film, the Te $3d_{5/2}$ signal for Te(0) is slightly increasing compared to the bare TeO_2 5 nm film. This is probably due to the reaction of the deposited Al metal film on top of the TeO_2 layer creating the Al_xO_y passivation layer and elemental Te(0) even under slightly elevated temperature. Finally, the O 1s peak is deconvoluted into two peaks which can be assigned to the different oxide contributions of α-TeO_2 and Al_xO_y (531.5 eV). The O 1s peak at 532.6 eV is assignable to $Al(OH)_3$ and SiO_2.[36]

2.2. Electrical Characterization of p-Type Channel Behaviour of α-TeO_2 Thin Film

Our reported direct gas phase deposition of α-TeO_2 thin film allows for a wafer scalable route for the fabrication of a high mobility *p*-type semiconductors.[37,38] Therefore we assessed the

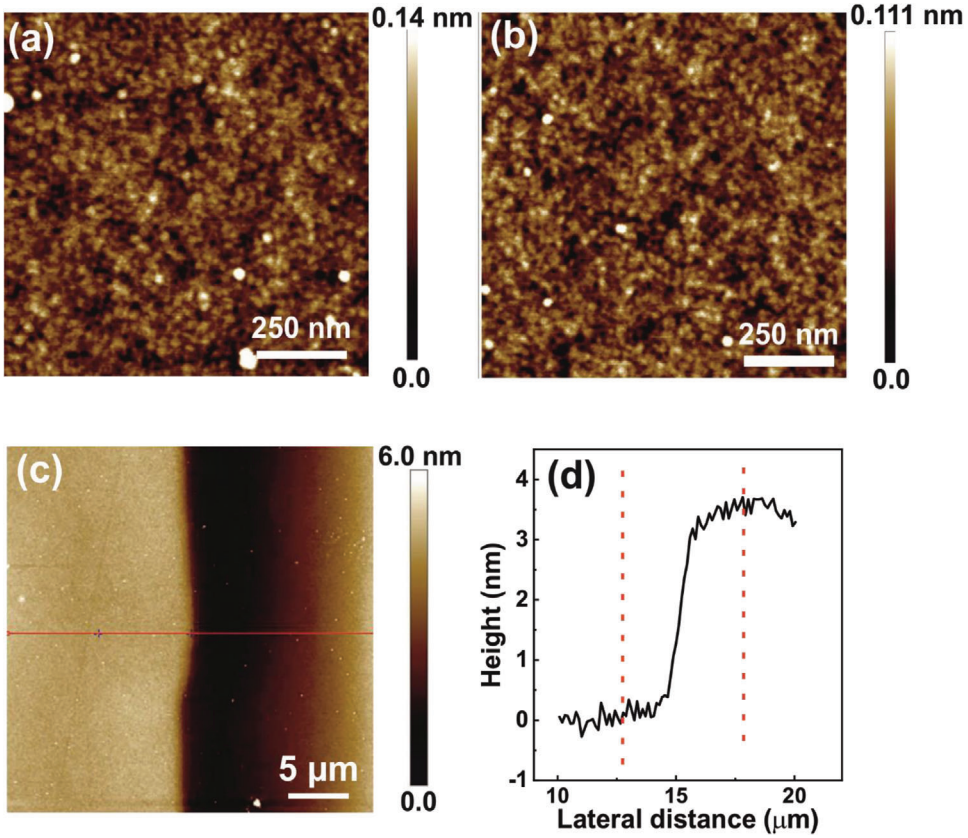

Figure 2. Atomic force micrographs of the deposited 5 nm α-TeO_2 film a,b) amorphous Al_xO_y thin film (5 nm) exhibiting excellent surface smoothness with very low roughness values. c,d) Cross-section atomic force micrograph showing the thickness profile of the deposited 5 nm α-TeO_2 thin film.

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH

21967350, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/admi.202301082 by Karlsruher Institut F., Wiley Online Library on [25/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

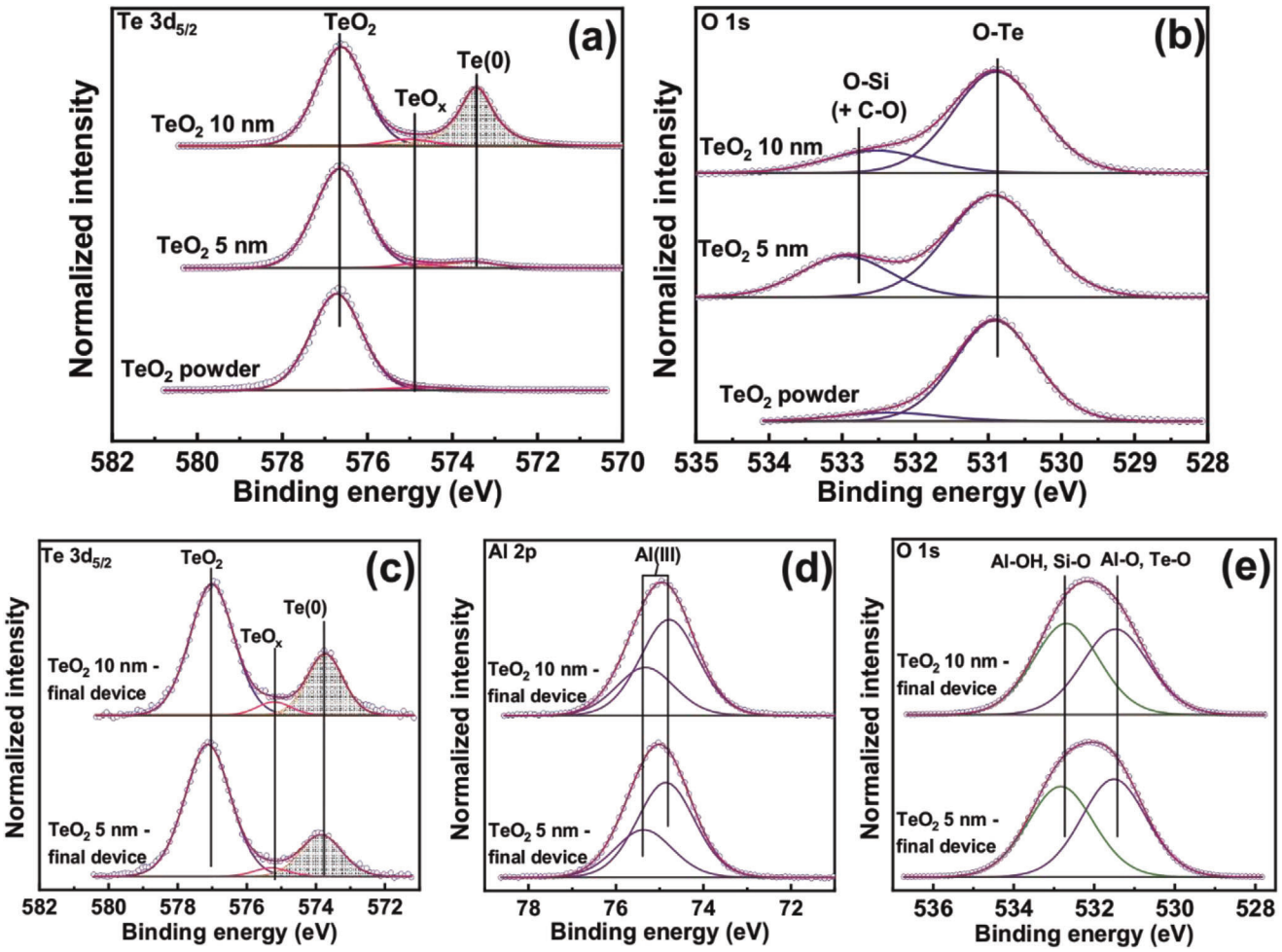

Figure 3. a,b) X-ray photoelectron spectra comparison of deposited (5 nm and 10 nm) α-TeO_2 thin film on a SiO_2 substrate with respect to the standard powder sample. Te $3d_{5/2}$ and O 1s photoelectron lines correspond mainly to Te (IV) and O^{2-} binding energies in TeO_2 tellurium oxide accompanied by a sub-stoichiometric oxide and a metal peak for the 10 nm thick film. c,d) XPS core level spectra of bi-layer final TFTs showing (c) Te $3d_{5/2}$ (d) Al 2p (e) O 1s spectra.

thin film device characteristics of the as deposited and passivated films. To start with, a 5 nm α-TeO_2 film is thermally evaporated on an interdigitated TFT substrate as shown in the schematic in **Figure** 4a. Therein the electrodes are made up of gold contacts and a 230 nm SiO_2 as dielectric layer is employed. The top and cross-sectional view of the device structure is shown in Figure 4a,b. The device deposited with an active layer of 5 nm (without passivation) has been characterized at first under ambient conditions (Figure S6a,b, Supporting Information) demonstrating transfer and output characteristics at room temperature. The device exhibits a decent *p*-type characteristics at room temperature demonstrating a nominal hysteresis, a hole mobility of 0.92 $cm^2\ V^{-1}\ s^{-1}$, and a low on/off ratio of $1.8 \times 10.^2$ Typically, the *p*-type conductivity in α-TeO_2 originates from tellurium vacancies which forms an acceptor level above the valence band depending on the film thickness, it varies from 1.29 to 0.69 eV as described elsewhere.[40]

To improve the fabricated TFTs device performance and their environmental stability, a thin passivation layer of 5 nm Al metal has been deposited on top of the semiconductor film at RT, followed by a single heating step of 50 °C for ≈30 min giving rise to the formation of Al_xO_y (Figure 3). Thus, a bi-layer consisting of active 5 nm α-TeO_2 thin film and a passivation layer (5 nm) of Al_xO_y has been formed (Figure 4a,b). The latter is crucial in modifying the charge carrier movement in the FET device. The so formed bi-layer devices demonstrate a significant improvement in the device characteristics by exhibiting a good hole mobility value of 3.8 $cm^2\ V^{-1}\ s^{-1}$, excellent *p*-type on-state current value near to ≈1 mA with a threshold voltage of 1 V and a good on/off ratio of 3.38×10^3 at a source-drain voltage of 30 V. The field-effect mobility was estimated using the following equation 1:

$$\mu_p = \frac{dI_D}{dV_G} \frac{L}{WV_{DS}C_{OX}} \quad (1)$$

where, g_m is the transconductance ($g_m = \frac{dI_D}{dV_G}$), V_{DS} is the drain voltage, W is the channel width (2000 µm), L is the channel length (80 µm) and C_{OX} represents the gate-oxide capacitance (1.42×10^{-8} F cm^{-2}) used in this study. The observed key

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH

21967350, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/admi.202301082 by Karlsruher Institut F., Wiley Online Library on [25/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

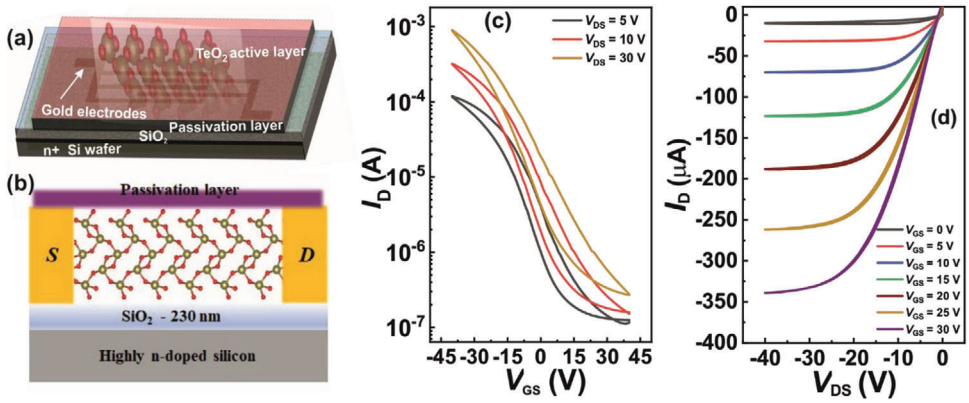

Figure 4. a,b) Schematic (top and cross-sectional view) showing the active semiconducting layer with the additional passivation layer on top. c) Transfer characteristics of the devices composed of 5 nm α-TeO_2 active layer with the additional Al_xO_y passivation layer fabricated at 50 °C. d) The corresponding output characteristics of the same device showing proper linear and saturation regime where the drain voltage has been varied from -40 to 40 V with a step of 5 V V_{GS}.

parameters of the fabricated bi-layer devices have been compared with the existing reports on the *p*-type oxide semiconductors and summarized in Table S1 (Supporting Information). The presented table clearly shows that the existing reports on *p*-type oxide semiconductors demonstrating poor device performance with exceptionally few studies reporting fair mobility values. However, almost all these reported oxides are formed at a high processing temperature. In this regard, the mobility value achieved in the present work at such a low processing temperature (50 °C) has not been reported earlier to the best of our knowledge. Additionally, these devices found to have a very low and negligible hysteresis in both the transfer and output characteristics, respectively (Figure 4c,d), denoting a reduced trap state situation at the interface of the fabricated devices. This may be attributed to the fact that the deposited thin passivation layer forms a low defect density interface with the α-TeO_2 films. The corresponding output characteristics (Figure 4d) shows current linearity at low source-drain voltages, indicating Ohmic contact between the α-TeO_2 and the Au electrodes. Overall, the important metrics of α-TeO_2-based transistors, such as on/off ratio, mobility and on-state current level, are superior when compared to the existing literature of thin film materials derived from *p*-type oxide FETs.[29] The observed improvement in the device performance can be attributed to the fact that adding a thin passivation layer on the active channel material may induce high charge carrier movement along the in-plane direction of the channel layer with the carrier confinement in a potential well,[39,40] which improves carrier mobility and device on-state current due to the two-dimensional carrier transfer formed in the bulk of α-TeO_2, which further avoids scattering and charge trapping by the defects from the back channel surface of the active material. Clearly, the added advantage of these devices is their high scalability and low temperature processability (50 °C) due to which they can be easily adopted onto low-cost flexible substrates.

Next, we studied the dependency of the channel thickness on the key TFT parameters (10 nm film TFT device characteristic given in Figure S7a,b, Supporting Information). Here a monotonous increase in mobility (3.8 to 13.3 $cm^2\ V^{-1}\ s^{-1}$) and a downward trend in the respective on/off ratios (3.3×10^3 to 3.6×10^2) has been observed (**Figure 5**a,b) for the devices fabricated at 50 °C processing temperature with the thickness of 10 nm. This observation can be correlated with the increasing presence of elemental tellurium in the 10 nm film compared to the 5 nm film.

This is responsible for the higher charge carrier concentration resulting in improved mobility and reduced on/off ratio. This observation is supported by the fact of a reduced electrostatic control for TFTs having thicker channel layers which is commonly observed for other material systems, too.[41–43] To examine the reproducibility of the fabricated TFTs based on the evaporated α-TeO_2 semiconductor thin films, two batches of devices (5 nm α-TeO_2/5 nm Al_xO_y) consisting in total of 8 TFTs and their performance parameter average value such as mobility (3.6 $cm^2\ V^{-1}\ s^{-1}$), on/off ratio (2.3×10^3), and on-state current value (916 μA) with standard deviations for 10 and 30 V V_{DS} are summarized in **Figure 6**a–c. The data depicts a narrow performance variation with a small standard deviation.

Finally, we investigate the air stability of the PMOS devices (5 nm α-TeO_2/5 nm Al_xO_y) by storing it for longer times (>4 months/125 days) under ambient atmospheric conditions with a humidity of 60–77%. **Figure 7**a–d presents the transfer and output characteristics of the PMOS devices with different source-drain voltages (10 and 30 V V_{DS}) for a set of TFTs fabricated at 50 °C as a function of storage time. After storing the devices for one month, a slight decrease in mobility from 3.8 to 2.4 $cm^2\ V^{-1}\ s^{-1}$, a stable on/off ratio from 3.2 to $3.3 \times 10,^3$ and a slight increase in hysteresis has been observed. The slight device degradation for the *p*-type oxide TFTs under ambient environment conditions can be attributed i) to the absorbed humidity content which creates an increased energy barrier for the hole transport at the semiconductor grain boundaries as well to humidity related hole traps near the VB edge which might also be reactive towards polar H_2O molecules.[2,44] In contrast, after 30 days and up to day 125 all devices are stable without any detectable degradation in the mobility and on/off ratio (**Figure 8**a,b) meeting the requirements for signal switching units in electric circuits. The observed stable performance over 125 days, indicates the superior ambient durability of the fabricated PMOS devices. Such durability with good mobility values alongside the low processing temperature

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH

21967350, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/admi.202301082 by Karlsruher Institut F., Wiley Online Library on [25/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

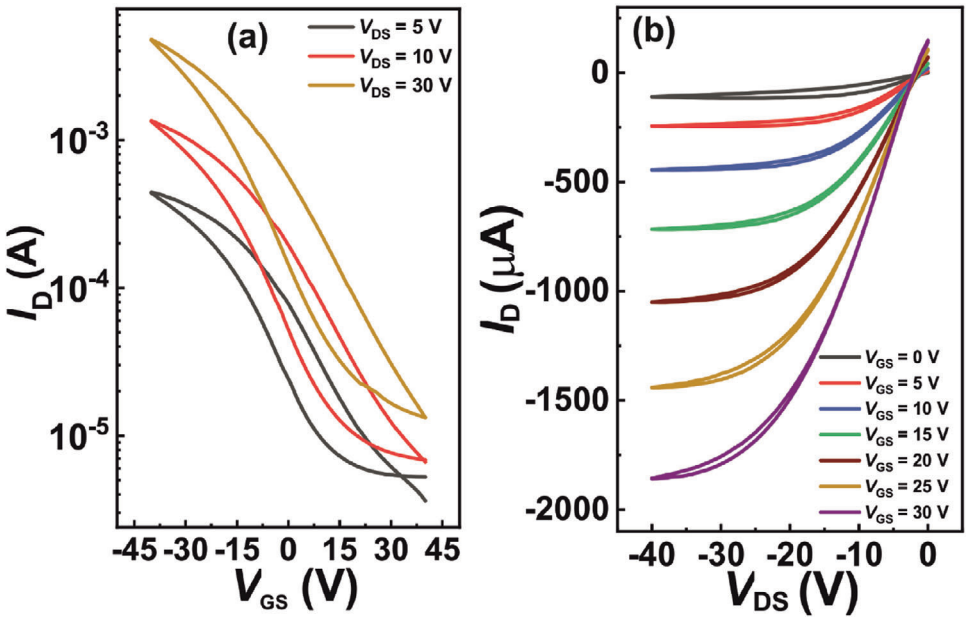

Figure 5. a,b) Transfer and output characteristics of the FETs fabricated with a 10 nm α-TeO_2 and a 5 nm Al_xO_y passivation layer depicting a decent *p*-type device characteristics with an on-state current of near to 4 mA at 30 V V_{DS}.

may qualify them for the implementation in flexible all-oxide electronics.

3. Conclusion

In summary, our study explores α-TeO_2 oxide as an active thin film *p*-type semiconductor while employing a highly scalable direct gas phase deposition method. Significantly, the engineered nanometric passivated α-TeO_2 thin film shows a superior hole mobility of 3.8 $cm^2\ V^{-1}\ s^{-1}$, an on-state current of 966 μA, and an on/off ratio of 3.8×10^3, all achieved at an exceptionally low processing temperature of 50 °C. Noteworthy is the consistent reproducibility of the devices, with minimal variance in the TFT metrics, yielding an average hole mobility, on-current, and on/off ratio of 3.59 $cm^2\ V^{-1}\ s^{-1}$, 914 μA, and $3.3 \times 10,^3$ respectively. Furthermore, the devices have undergone stability testing under ambient atmospheric conditions for an extended period exceeding of four months. The devices have exhibited marginal reduction in mobility, while maintaining a steadfast on/off ratio within the range of 3.8×10^3 to 3.3×10^3 throughout a 125-day duration, underscoring their robust environmental endurance. The observed transistor characteristics alongside their low processing temperature make them interesting candidates for integration onto flexible substrates, especially applications requiring large area implementations such as bendable and stretchable electronics.

4. Experimental Section

Thin Film Fabrication and Characterization: α-TeO_2 powder was obtained from Sigma–Aldrich (99.9995%) and used directly as thermal evaporation source for the thin film deposition of the active semiconducting layer. Aluminium wire (diameter 1.5 mm, purity of 99.999%, Umicore) was used as a source material for the passivation layer deposition of Al_xO_y by physical vapor deposition. For all-thin film depositions, thermal evaporation was carried out using Auto 306 FL400 thermal vacuum evaporator

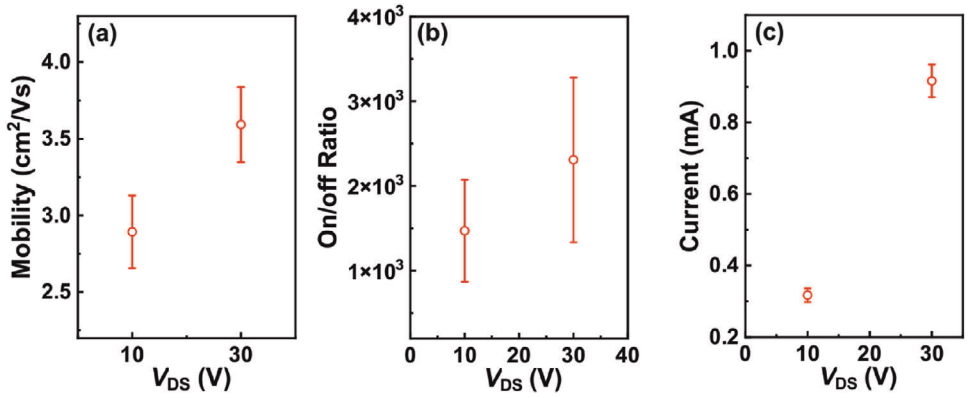

Figure 6. a–c) The performance parameters (mobility, on/off ratio, and on-current) extracted from the fabricated FETs considering at least eight devices obtained from two different batches, and their average values with standard deviation showing less variability in the devices.

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH

21967350, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/admi.202301082 by Karlsruher Institut F., Wiley Online Library on [25/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

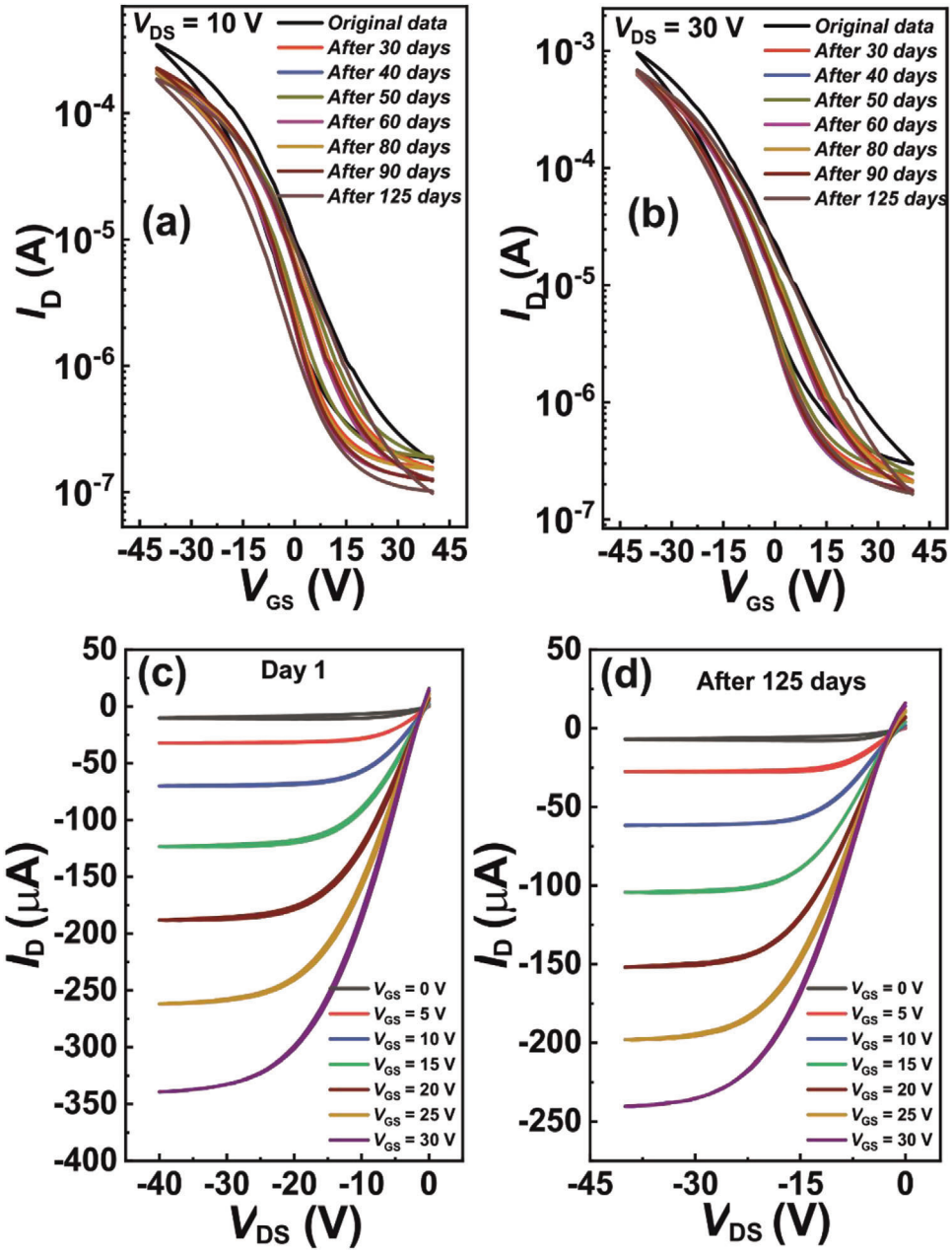

Figure 7. a,b) Plot showing FETs transfer characteristics of 10 V, and 30 V V_{DS} as a function of time under ambient conditions fabricated at 50 °C (5 nm α-TeO_2/5 nm Al_xO_y).

from HHV-Limited; where the substrate temperature was maintained at room temperature with a maintained vacuum pressure (5.5×10^{-5} Torr). An alumina coated tungsten basket was used as an evaporation source. The distance between the substrate and the alumina crucible was ≈25 cm and the thickness of the deposited films were monitored using a Sigma SQM160 quartz crystal balance. Scanning electron microscopy of the deposited films were performed on a Philips XL-30 FEI with an acceleration voltage of 15–20 kV. α-TeO_2 thickness analysis and surface roughness was carried out using atomic force microscopy (AFM) of Bruker Dimension Icon standard tapping mode procedure. X-ray diffraction (XRD) analysis was carried out on α-TeO_2 powder using a Rigaku Miniflex 600 (40 kV, 15 mA) equipped with Cu Kα radiation. Raman spectroscopy was performed using a DXR3 Raman spectrometer with 532 nm wavelength (Thermo Scientific). Transmission electron microscopy (TEM) was performed using a FEI Tecnai G2 with accelerating voltage of 200 keV. The cross-section samples were prepared via focused ion beam (FIB) equipment of FEI Helios NanoLab 460F1 FIB-SEM with a platinum layer deposition. The X-ray photo electron spectroscopy (XPS) measurements were performed using a K-Alpha+ XPS spectrometer (ThermoFisher Scientific). Thermo Avantage software was used for data acquisition and processing. All films and powder samples were analyzed using a micro focused, mono-chromated Al Kα X-ray source (400 μm spot size). The K-Alpha+ charge compensation system was employed during analysis, using electrons of 8 eV energy, and low-energy argon ions to prevent any localized

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH

21967350, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/admi.202301082 by Karlsruher Institut F. , Wiley Online Library on [25/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

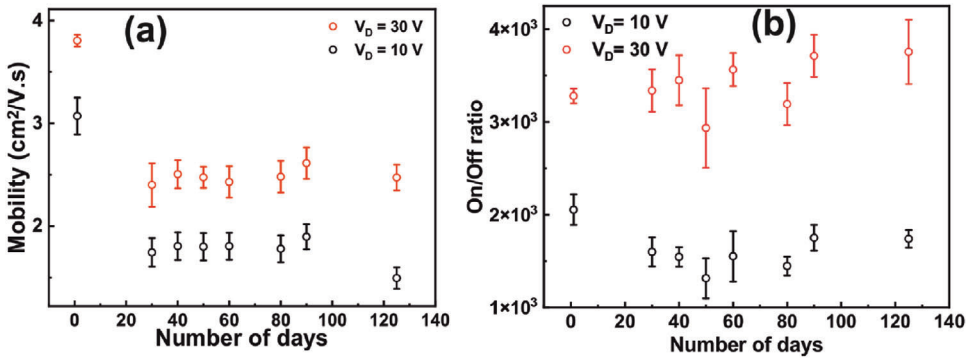

Figure 8. a) Performance parameters mobility and on/off ratio obtained of the stored FET devices (5 nm α-TeO_2/5 nm Al_xO_y) at 50 °C demonstrating their average values with respect to different drain voltages. The mobility values have slightly degraded with the number of stored days. b) On the other hand, the on/off has shown a highly stable performance as a function of number of stored days under ambient conditions.

charge build-up. The spectra were fitted with one or more Voigt profiles (BE uncertainty: ±0.2 eV) and Scofield sensitivity factors were applied for quantification.[45] All spectra were referenced to the C 1s peak (C—C, C—H) at 285.0 eV binding energy controlled by means of the well-known photoelectron peaks of metallic Cu, Ag, and Au, respectively.

Thin Film Transistor (TFT) Fabrication and Characterization: The PMOS TFTs were fabricated on commercially available substrate of highly *n*-doped silicon ($n = 3 \times 10^{16}$ cm^{-3}) with 230 nm silicon dioxide as a dielectric layer, source-drain electrodes were located on an interdigitated architecture comprising of 30 nm gold with a 10 nm indium tin oxide (ITO) adhesion layer (Fraunhofer IPMS, Dresden). The interdigitated structures consist of prefabricated passive source and drain electrodes in a bottom-gate-bottom-contact configuration. The electrodes were designed to have a *W*/*L* ratio of 25; where the channel length (*L*) and width (*W*) of 80 and 2000 µm respectively. Prior to PMOS TFT fabrication, the substrates were cleaned with acetone, and isopropanol (both HPLC-Grade, Carl Roth GmbH & Co. KG) via ultrasonication for 10 min each and dried under an intense argon stream followed by treating them with the UV light (wavelength of 254 nm, optical power of 4 W) for 10 min, using a modified UV Ozone Cleaner UVC-1014 (NanoBioAnalytics). Once the cleaning procedure was done, the required thin films were deposited using a thermal evaporator. Finally, the fabricated transistor transfer and output characteristics were performed in an inert gas atmosphere (argon) inside a glovebox, using a B1500A Semiconductor Device Analyzer (Agilent Technologies). The pressure inside the glovebox was maintained constant at 2.7 mbar with a water content of <0.5 ppm and an oxygen content of <0.5 ppm.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

The authors thank Silvio Heinschke, Jörg Engstler for X-ray and TEM measurements and Inga Dönges for technical assistance in thermal evaporation. The authors gratefully acknowledge Christian Dietz from the Department of Materials Science (TUDa, Physics of Surfaces) for AFM measurements. FIB/TEM sample preparation and measurements were done at the Ernst-Ruska Center (ERC) Jülich. We thank George Mathew (PhD student, KIT, Germany) for helping to create TOC schematic.

Open access funding enabled and organized by Projekt DEAL.

Conflict of Interest

There are no conflicts to declare.

Data Availability Statement

The data that support the findings of this study are available in the supplementary material of this article.

Keywords

oxide electronics, p-type semiconductor, tellurium oxide, thermal evaporation, thin film transistor

Received: December 20, 2023
Revised: February 12, 2024
Published online:

[1] P. Pattanasattayavong, S. Thomas, G. Adamopoulos, M. A. Mclachlan, D. Thomas, M. A. Mclachlan, T. D. Anthopoulos, *Appl. Phys. Lett.* **2013**, *102*, 163505.
[2] A. Liu, H. Zhu, Y. Y. Noh, *ACS Appl. Mater. Interfaces* **2019**, *11*, 33157.
[3] A. Liu, S. Nie, G. Liu, H. Zhu, C. Zhu, B. Shin, E. Fortunato, R. Martins, F. Shan, *J. Mater. Chem. C Mater.* **2017**, *5*, 2524.
[4] N. Devabharathi, J. R. Pradhan, S. S. Priyadarsini, T. Brezesinski, S. Dasgupta, *Adv. Mater. Interfaces* **2022**, *9*, 2200949.
[5] E. Fortunato, P. Barquinha, R. Martins, *Adv. Mater.* **2012**, *24*, 2945.
[6] P. Pattanasattayavong, S. Thomas, G. Adamopoulos, M. A. McLachlan, T. D. Anthopoulos, *Appl. Phys. Lett.* **2013**, *102*, 425.
[7] N. Devabharathi, S. K. Mondal, S. Dasgupta, *Nanoscale* **2019**, *11*, 13731.
[8] S. J. Kim, S. Yoon, H. J. Kim, *Jpn. J. Appl. Phys.* **2014**, *53*, 215.
[9] N. Devabharathi, J. R. Pradhan, S. Dasgupta, presented at 2022 IEEE Int. Conf. on Emerging Electronics, Bangalore, India, December **2022**, 52.
[10] S. K. Garlapati, T. T. Baby, S. Dehm, M. Hammad, V. S. K. Chakravadhanula, R. Kruk, H. Hahn, S. Dasgupta, *Small* **2015**, *11*, 3591.
[11] J. Yu, G. Liu, A. Liu, Y. Meng, B. Shin, F. Shan, *J Mater. Chem. C Mater.* **2015**, *3*, 9509.
[12] A. Liu, H. Zhu, Y. Noh, *Adv. Funct. Mater.* **2020**, *30*, 2002625.
[13] S. Y. Kim, C. H. Ahn, J. H. Lee, Y. H. Kwon, S. Hwang, J. Y. Lee, H. K. Cho, *ACS Appl. Mater. Interfaces* **2013**, *5*, 2417.
[14] J. Jang, S. Chung, H. Kang, V. Subramanian, *Thin Solid Films* **2016**, *600*, 157.
[15] C. Wang, H. Zhu, Y. Meng, S. Nie, Y. Zhao, B. Shin, E. Fortunato, R. Martins, F. Shan, G. Liu, *IEEE Trans. Electron Devices* **2019**, *66*, 1458.

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH

21967350, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/admi.202301082 by Karlsruher Institut F., Wiley Online Library on [25/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License

[16] S. Nie, A. Liu, Y. Meng, B. Shin, G. Liu, F. Shan, *J. Mater. Chem. C Mater.* **2018**, *6*, 1393.
[17] J. D. Lenef, J. Jo, O. Trejo, D. J. Mandia, R. L. Peterson, N. P. Dasgupta, *J. Phys. Chem. C* **2021**, *125*, 9383.
[18] H. A. Al-Jawhari, *Adv. Electron. Mater.* **2022**, *8*, 893.
[19] Y. Ogo, H. Hiramatsu, K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* **2008**, *93*, 197.
[20] R. Barros, K. J. Saji, J. C. Waerenborgh, P. Barquinha, L. Pereira, E. Carlos, R. Martins, E. Fortunato, *Nanomaterials* **2019**, *20*.
[21] J. A. Caraveo-Frescas, P. K. Nayak, H. A. Al-Jawhari, D. B. Granato, U. Schwingenschlögl, H. N. Alshareef, *ACS Nano* **2013**, *7*, 5160.
[22] C. Z. Yan, D. J. Kang, *Cryst. Res. Technol.* **2014**, *49*, 400.
[23] S. N. Antonov, *Tech. Phys.* **2004**, *49*, 84.
[24] A. W. Warner, D. L. White, W. A. Bonner, *J. Appl. Phys.* **1972**, *43*, 4489.
[25] S. N. B. Hodgson, L. Weng, Sol-Gel Processing of Tellurium Oxide and Suboxide Thin Films with Potential for Optical Data Storage Application, **2000**.
[26] H. Xu, T. Kim, H. S. Han, M. J. Kim, J. S. Hur, C. H. Choi, J. H. Chang, J. K. Jeong, *ACS Appl. Mater. Interfaces* **2022**, *14*, 3008.
[27] S. N. B. Hodgson, L. Weng, *J. Mater. Sci.: Mater. Electron.* **2006**, *17*, 723.
[28] Z. Liu, T. Yamazaki, Y. Shen, T. Kikuta, N. Nakatani, T. Kawabata, *Appl. Phys. Lett.* **2007**, *90*, 8.
[29] A. Zavabeti, P. Aukarasereenont, H. Tuohey, N. Syed, A. Jannat, A. Elbourne, K. A. Messalea, B. Y. Zhang, B. J. Murdoch, J. G. Partridge, M. Wurdack, D. L. Creedon, J. van Embden, K. Kalantar-Zadeh, S. P. Russo, C. F. McConville, T. Daeneke, *Nat. Electron.* **2021**, *4*, 277.
[30] S. Moufok, L. Kadi, B. Amrani, K. D. Khodja, *Results Phys* **2019**, *13*, 102315.
[31] P. Charton, L. Gengembre, P. Armand, *J. Solid State Chem.* **2002**, *168*, 175.
[32] K. J. Klabunde, *Chemistry of Free Atoms and Particles*, Academic Press, Cambridge, Massachusetts **1980**.
[33] J. R. Soulen, P. Sthapitanonda, J. L. Margrave, V. 59, J. R. Soulen, P. Sthapitanonda, J. L. Margrave, *J. Chem. Soc.* **1954**, *62*, 6372.
[34] H. G. Staley, *J. Chem. Phys.* **1970**, *52*, 4311.
[35] A. Liu, H. Zhu, T. Zou, Y. Reo, G. S. Ryu, Y. Y. Noh, *Nat. Commun.* **2022**, *13*, 6372.
[36] N. Koslowski, V. Trouillet, J. J. Schneider, *J. Mater. Chem. C Mater.* **2020**, *8*, 8521.
[37] A. Liu, H. Zhu, S. Bai, Y. Reo, T. Zou, M. G. Kim, Y. Y. Noh, *Nat. Electron.* **2022**, *5*, 78.
[38] E. Habtmann, L. Kovacs, *Phys. Stat. Sol.* **1982**, *59*, 59.
[39] C. H. Ahn, H. K. Cho, H. Kim, *J. Mater. Chem. C Mater.* **2015**, *4*, 727.
[40] Z. Zheng, Y. Zeng, R. Yao, Z. Fang, H. Zhang, S. Hu, X. Li, H. Ning, J. Peng, W. Xie, X. Lu, *J. Mater. Chem. C. Mater.* **2017**, *5*, 7043.
[41] C. Zhao, C. Tan, D. H. Lien, X. Song, M. Amani, M. Hettick, H. Y. Y. Nyein, Z. Yuan, L. Li, M. C. Scott, A. Javey, *Nat. Nanotechnol.* **2020**, *15*, 53.
[42] Z. Wu, Y. Lyu, Y. Zhang, R. Ding, B. Zheng, Z. Yang, S. P. Lau, X. H. Chen, J. Hao, *Nat. Mater.* **2021**, *20*, 1203.
[43] J. Wu, H. Yuan, M. Meng, C. Chen, Y. Sun, Z. Chen, W. Dang, C. Tan, Y. Liu, J. Yin, Y. Zhou, S. Huang, H. Q. Xu, Y. Cui, H. Y. Hwang, Z. Liu, Y. Chen, B. Yan, H. Peng, *Nat. Nanotechnol.* **2017**, *12*, 530.
[44] Y. J. Han, Y. J. Choi, C. Y. Jeong, D. Lee, S. H. Song, H. I. Kwon, *IEEE Electron Device Lett.* **2015**, *36*, 466.
[45] G. W. Coulston, E. A. Thompson, N. Herron, Characterization of VPO Catalysts by X-Ray Photoelectron Spectroscopy, **1996**.

© 2024 The Authors. Advanced Materials Interfaces published by Wiley-VCH GmbH

21967350, 0, Downloaded from https://onlinelibrary.wiley.com/doi/10.1002/admi.202301082 by Karlsruher Institut F., Wiley Online Library on [25/03/2024]. See the Terms and Conditions (https://onlinelibrary.wiley.com/terms-and-conditions) on Wiley Online Library for rules of use; OA articles are governed by the applicable Creative Commons License