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Characteristics and ultra-high total ionizing dose response of 22 nm fully depleted silicon-on-insulator

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ABSTRACT: The radiation response of MOS transistors in a 22 nm Fully Depleted Silicon-On-Insulator (FDSOI) technology exposed to ultra-high total ionizing dose (TID) was investigated. Custom structures including n- and p-channel devices with different sizes and threshold voltage flavours were irradiated with X-rays up to a TID of $100\,\mathrm{Mrad}(SiO_2)$ with different back-gate bias configurations, from $-8\,\mathrm{V}$ to $2\,\mathrm{V}$. The investigation revealed that the performance is significantly affected by TID, with the radiation response being dominated by the charge trapped in the buried oxide.

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Contents

1 Introduction

Single Event Effects (SEEs) are a major cause of failure for Application-Specific Integrated Circuits (ASICs) operating in harsh radiation environments, such as space or particle accelerators [1]. A particle with high Linear Energy Transfer (LET), like an energetic ion, generates an ionization tail of electron-hole pairs as it passes through the substrate of a semiconductor device. In a bulk technology, this charge can be collected relatively deep in the substrate and is responsible for current pulses at active nodes of the circuit, giving origin to SEU (upsets), SET (transient) or SEL (latchup) [2–4].

In Silicon-On-Insulator (SOI) technologies, the thin silicon channel layer overlays a thick Buried OXide (BOX) that isolates the channel from the bulk substrate. The presence of the BOX limits the extension of the charge collection region and makes these technologies intrinsically more tolerant to SEE [5, 6]. Furthermore, the electrical coupling between the front and back channel interfaces in a Fully Depleted SOI (FDSOI) transistor enables the tuning of its electrical characteristics via back-gate biasing [7]. However, the BOX is typically tens of nanometers thick and therefore trapping significant amounts of charge when exposed to ionizing dose [8]. Total Ionizing Dose (TID) susceptibility of FDSOI devices results mainly from the coupling between the back gate and the front gate, meaning that charges trapped in the BOX modify the electrical characteristics of the transistor [9–13]. Thus, although SOI technologies are appealing in reducing SEE, they may exhibit a greater sensitivity to TID compared to bulk technologies. In view of possible application in HEP, where doses can be orders of magnitude higher than those typically reached in space applications [14], it is interesting to study the TID response of commercial SOI technologies and if/how it can be improved by dedicated biasing techniques. In this work, the characteristics of n- and p-channel transistors with different sizes and threshold voltage in a 22 nm FDSOI technology were evaluated before irradiation and after exposure to X-rays up to a TID of 100 Mrad(SiO_2). High-temperature annealing and compensation of TID-induced effects using back-biasing were also studied.

2 Test structures

The irradiated samples were custom test structures containing several isolated n- and p-channel transistors as schematically depicted in figure 1. Note that both pMOS and nMOS can be built on top of a p- or n-well doped substrate region, and that p-wells have to be biased at voltages lower than n-wells. The chips were designed at Karlsruhe Institute of Technology (KIT) and fabricated in a commercial-grade 22 nm FDSOI technology. In the technology studied, the thin silicon film
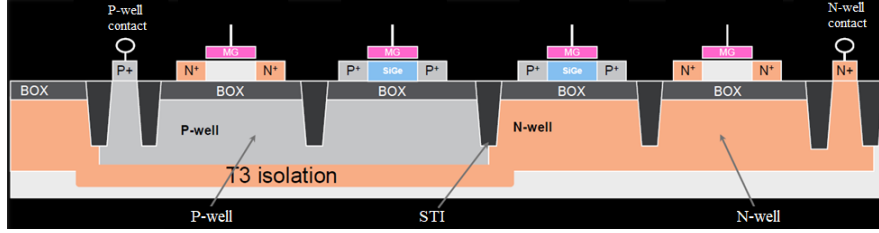
Figure 1. Schematic of the irradiated transistors in 22 nm FDSOI. The p-well and n-well contact are used to tune the threshold voltage of the device.

that forms the channel is undoped and the devices are equipped with an external pad to provide back-gate biasing via p-well/n-well contacts in order to tune the threshold voltage (V_{th}) of the device. Applying a negative bias to the p-well reduces the V_{th} of the pMOS (forward body biasing, FBB) and increases it for the nMOS (reverse body biasing, RBB). Similarly, applying a positive bias to the n-well increases the V_{th} of the pMOS and reduces it for the nMOS.

3 Results

3.1 TID response

In this section the radiation response of 22 nm FDSOI technology is discussed referring only to the devices that are in the p-well, i.e., FBB pMOS and RBB NMOS (left structure in figure 1). The same phenomena were observed in the devices in the n-well.

In a fully depleted SOI technology the silicon film of the SOI structure is thin enough that completely depletion can occur, thereby coupling the two gates, hereafter front-gate (FG) and back-gate (BG), and rendering the threshold voltage of each gate dependent on the conditions of the other [9]. Once the two gates are coupled, applying a bias to the BG influences the front channel threshold voltage V_{th}. Low, high and standard threshold voltage transistors were investigated, hereafter denoted as lvt, hvt and svt respectively. Figure 2 shows the ΔV_{th}^{sat} of the FG V_{th} induced by changing the BG bias from 0 to -2 V in pMOS and nMOS transistors with $W = 3\,\mu$m and L ranging from 20 nm to 360 nm built on p-well. As the bias applied to the BG decreases, V_{th} linearly decreases for p-type transistors whereas it linearly increases for n-type devices. In this V_{BG} range, the threshold variation induced by the back-gate voltage is only slightly dependent on device size.

Figure 3 reports the ΔV_{th}^{sat} measured at $V_{BG} = 0$ V of p- and n-type transistors with $W = 3\,\mu$m and L ranging from 20 nm to 360 nm irradiated up to 100 Mrad(SiO$_2$) with X-ray at T = 25 °C. During exposure, the devices were biased with $V_{FG} = \pm 0.8$ V, $V_S = V_D = 0$ V, $V_{BG} = -2$ V. Both types of transistors are severely affected by TID; the relatively small dose of 1 Mrad(SiO$_2$) is already sufficient to increase the $|V_{th}|$ by ~ 110 mV for pMOS and a reduction of about the same amount for nMOS transistors, exception made for the shortest one which exhibit a decrease of about 150 mV. After 2 Mrad(SiO$_2$), nMOS transistors show a rebound caused by the different build-up time of positive charge in the oxides and negative charge at the interface [15–18]. In pMOS devices, the charge in the oxide and at the interface has the same sign, causing the monotonic behavior of the radiation response. The radiation response of the V_{th} is caused by the charge in the buried oxide which being coupled to the front-gate causes a change in the threshold voltage of the front channel [9–13]. The observed response depends on transistor length, with shorter devices exhibiting a greater variation. This is
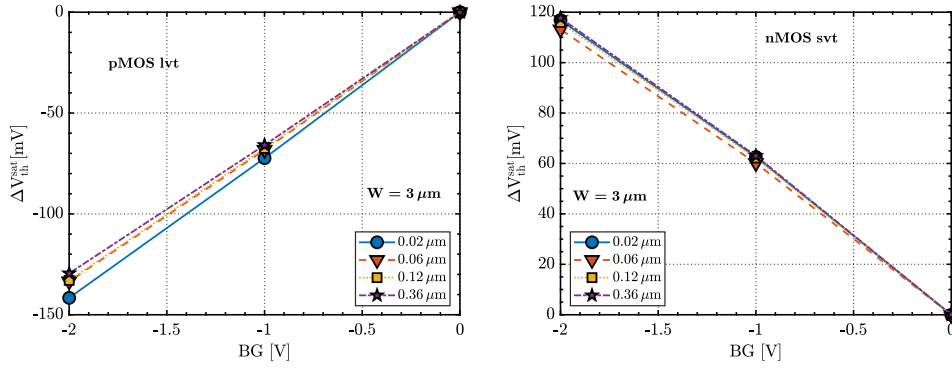
Figure 2. Front-gate threshold voltage as a function of back-gate bias of pristine $W = 3\,\mu\text{m}$ and L ranging from 20 nm to 360 nm pMOS(left) and nMOS(right) built on p-well.
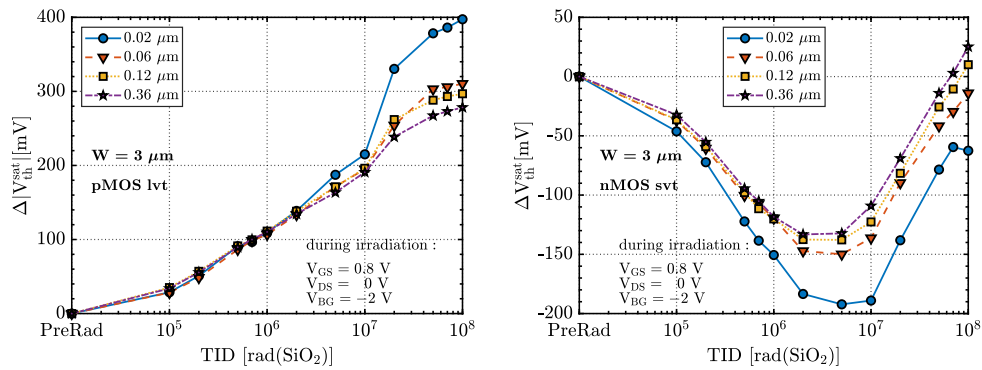

Figure 3. $\Delta V_{\text{th}}^{\text{sat}}(\text{TID})$ of p- and n-type transistors with $W = 3\,\mu\text{m}$ and L ranging from 20 nm to 360 nm exposed to $10\,\text{Mrad}(\text{SiO}_2)$.

especially evident in the minimum size device, but it is also visible in the other transistors. The reason for the dependence of this technology on channel length is not yet fully understood. Some authors have observed greater degradation in the short transistors of certain FDSOI technologies [13, 19], but these studies investigate devices with doped channels, thus different from the undoped FDSOI studied in this paper. The TID response of some bulk technologies is dependent on the L due to the presence of the spacer oxides [15, 20] or the presence of the halo implants in the channel [21]. However, because the channel is undoped, in this technology there are no halo implants, low-doped drain, or spacer oxides used in creating the latter.

Figure 4 shows the percentage degradation of the on current of $[80, 300] \times 20\,\text{nm}$ lvt pMOS and $[80, 300] \times 20\,\text{nm}$ hvt nMOS transistors measured at room temperature with $V_{\text{BG}} = 0\,\text{V}$ after irradiation to $100\,\text{Mrad}(\text{SiO}_2)$ and then annealed at different temperature up to T = $100\,°\text{C}$. During irradiation, the devices were biased at $V_{\text{GS}} = \pm 0.8\,\text{V}$ and $V_{\text{DS}} = V_{\text{BG}} = 0\,\text{V}$. The same bias was kept during annealing with exception of the back-gate where V_{BG} was set to = $-4\,\text{V}$. In the last $\sim 50\,\text{h}$ of annealing, V_{BG} was set to = $-8\,\text{V}$ to enhance the recovery of the devices. The performance of both types of transistors is severely degraded by TID, with pMOS devices most affected (figure 4, left). In pMOS, a total dose of $1\,\text{Mrad}(\text{SiO}_2)$ results in $\sim 50\%$ degradation of the turn-on current. Unlike what observed in bulk technology [15], the radiation response is independent of the transistor width. The performance of the devices did not recover after several hours of annealing at T = $25, 40, 60, 100°\text{C}$, indicating that the
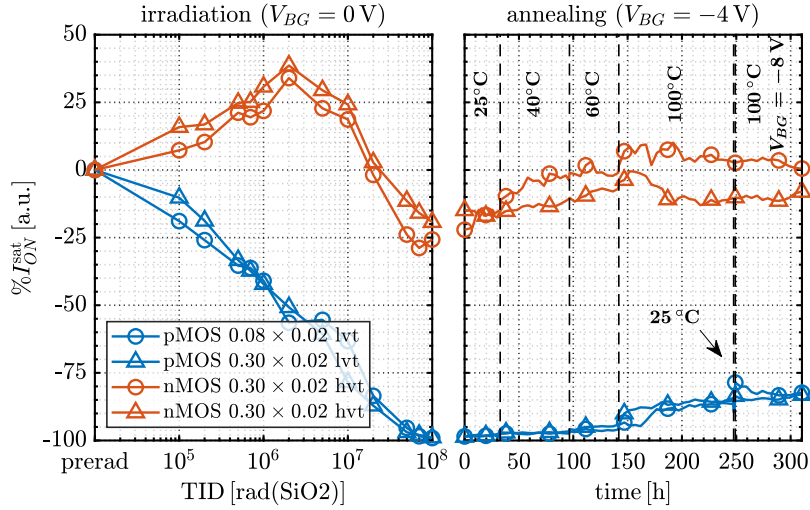
Figure 4. $\%I_{\mathrm{ON}}^{\mathrm{sat}}(\mathrm{TID})$ of $[80, 300] \times 20\,\mathrm{nm}$ lvt pMOS and $[80, 300] \times 20\,\mathrm{nm}$ hvt nMOS irradiated to $100\,\mathrm{Mrad}(\mathrm{SiO}_2)$ and annealed at different temperatures T = 25–100°C. The last measurement after annealing was performed at room temperature.

irradiation produced deep-level defects whose removal process requires more energy than that provided during annealing at this temperature. Switching to $V_{\mathrm{BG}} = -8\,\mathrm{V}$ did not significantly enhance recovery.

3.2 Compensation of TID effects

The most significant effect induced by TID in 22 nm FDSOI is the threshold voltage shift (figure 3). Since the back-bias provides designer with an additional degree of freedom for tuning the threshold voltage, it might be possible to compensate for TID induced threshold voltage shift by varying the back-gate bias accordingly. Figure 5 shows the BG voltage that should be applied in order to compensate for the V_{th} shift induced by different levels of TID as a function of the length of the transistor for both pMOS and nMOS devices. To obtain compensation voltage values, the $I_D(V_G)$ characteristics of the devices were measured at varying back-gate voltages. The V_{BG} used ranged from $-8\,\mathrm{V}$ to $0\,\mathrm{V}$ with a step size of 1 V. The compensation value was then obtained by finding the intersection point between the $\Delta V_{\mathrm{th}}(V_{\mathrm{BG}})$ curve and $0\,\mathrm{V}$.
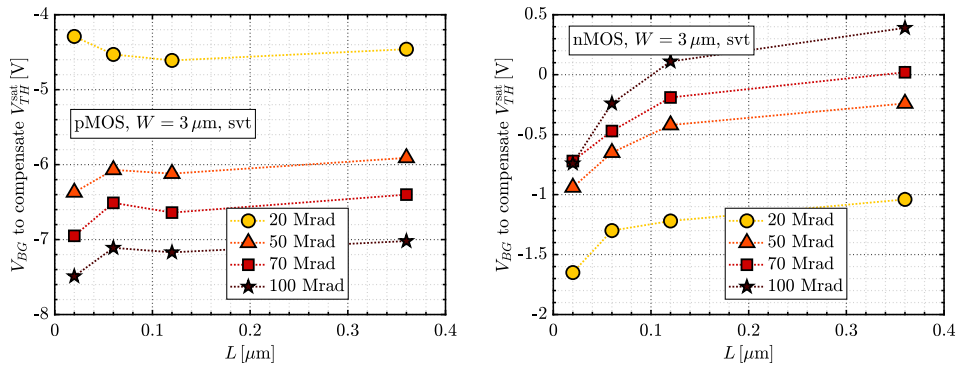

Figure 5. Compensation of the threshold voltage shift caused by different levels of TID by applying a different back-gate bias in pMOS (left) and nMOS (right) with same width and different lengths.

Although it is possible to compensate the shift caused by a certain level of TID by applying a specific BG bias, the voltage to be applied depends on the size of the transistors. For each level of TID considered there is a difference of about 0.5 V in the bias to be applied between the shortest and the longest transistor for pMOS transistors and about 1 V for nMOS devices.

4 Conclusions

The radiation response of 22 nm FDSOI transistors was evaluated by X-ray irradiation at ultra-high levels of TID. The study revealed that the coupling between the front and back gates allows the charge trapped in the buried oxide to severely shift the front gate threshold voltage, which is the main TID-induced effect observed in this technology. The observed degradation is not recovered when the devices are annealed at high temperature. The possibility to compensate TID-induced effects by varying the back-gate bias has been explored, showing that the V_{BG} needed to compensate for the TID-induced V_{th} shift depends on the channel length of the device. From a practical standpoint, this study underscores two noteworthy issues in implementing a compensation method in a real chip where hundreds of thousands of transistors with different sizes are involved. Firstly, it is necessary to actively monitor the degradation of the device to apply the appropriate bias. Secondly, the bias to be applied at each TID level is different for devices of different sizes, posing a significant challenge in the actual application of the compensation method.

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