A 223-276 GHz Cascadable FMCW Transceiver for Scalable MIMO Radar Arrays

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Abstract

The design, implementation, and characterization of an ultra-high resolution 223-276 GHz radar transceiver chip have been presented. It was implemented in IHP's 130-nm silicon-germanium (SiGe) bipolar-complementary-metal-oxide-semiconductor (BiCMOS) technology, SG13G2, with a unity current gain cut-off frequency (f_T) of 300 GHz and a maximum oscillation frequency (f_{max}) of 500 GHz, offering high yield and very-large-scale of integration with moderate mask costs. The mainly targeted application for the developed radar front-end chip is the non-destructive inspection and characterization of materials. In this dissertation, it has been aimed to develop a transceiver chip that operates in a broad frequency range to provide high range resolution and is suitable for building massive multiple-input multiple-out (MIMO) radar arrays to achieve high angular resolution. The designed transceiver chip is suitable to build massive MIMO radar arrays in the daisy-chain architecture thanks to its cascadable feature based on the injection-locked local oscillator (ILO) feedthrough synchronization technique. In this way, the drawbacks of the central local oscillator (LO) signal distribution network in the conceptual massive MIMO radar studies can be avoided. In addition, the designed radar front-end chip has an external voltage-controlled oscillator (VCO) input, making it also suitable for use in MIMO radar arrays based on the conventional central LO signal distribution architecture.

The designed transceiver chip with the on-chip antenna occupies an area of 2.72 mm^2 (2.16 mm × 1.26 mm). In addition, the transceiver test chip derived by placing the Marchand balun instead of the on-chip antenna was also manufactured. The Marchand balun was placed for on-wafer probing and de-embedded from the measurement results using the measured insertion loss data of the back-to-

back connected Marchand baluns. When the internal VCO is de-activated and the input amplifier for the external LO input is activated, the circuit draws a quiescent direct current (DC) current of 138.1 mA, 151.6 mA, and 208 mA from a single supply of 3.3 V, respectively, for the transmitter, receiver, and transceiver operation modes. In the transmitter mode, the transceiver circuit achieves a peak output power value of 3.6 dBm at 240 GHz, and its 3-dB frequency bandwidth is about 41 GHz, from 220 GHz to 261 GHz. On the other hand, its peak output power is around 3.1 dBm at 240 GHz with a 3-dB bandwidth of about 45 GHz in the transceiver mode. In the receiver mode, the peak value of the down-conversion power gain was measured to be about 16.24 dB at 240 GHz, and the circuit achieves a measured 3-dB bandwidth of 41 GHz from 220 GHz to 261 GHz. The difference between the measured down-conversion power gain results of the receiver and transceiver operating modes is lower than 0.7 dB across 220 GHz to 280 GHz. In the transceiver mode, the circuit exhibits a measured single sideband (SSB) noise figure of 18.73 dB at 255 GHz, and better than 21 dB across the 3-dB bandwidth. The measured input referred 1-dB compression point of the receiving path was found to be –16 dBm at 220 GHz, -16.5 dBm at 240 GHz, and –13.5 dBm at 260 GHz. When the internal VCO is activated, the transceiver circuit consumes a DC current of 197 mA, 213.2 mA, and 270.1 mA from a single supply voltage of 3.3 V, respectively, for the transmitter, receiver, and transceiver operation modes. The measured operating frequency range is from 222.7 GHz to 275.6 GHz, resulting in a frequency tuning range of about 52.9 GHz. In the transmitter mode, the circuit achieves a peak output power of 3.3 dBm at 241 GHz, and its 3-dB bandwidth is around 43 GHz, from 220 GHz to 263 GHz. On the other hand, the transceiver test circuit has a peak output power value of 3 dBm at 241 GHz, and the 3-dB bandwidth extends from 220 GHz to 265 GHz in the transceiver mode. The receiver channel in the transceiver test circuit achieves a measured peak down-conversion power gain of 16.5 dB at 240.5 GHz and has a 3-dB frequency bandwidth of about 40 GHz, from 220 GHz to 260 GHz. The minimum value of the noise figure was measured to be 18.7 dB at 255 GHz. The measured noise figure is better than approximately 20.6 dB across the 3-dB frequency bandwidth. The measured input referred 1-dB compression point of the receiver channel is -15 dBm at 230 GHz, -16.4 dBm at 240 GHz, and -14 dBm at 260 GHz. The circuit

achieves an amplitude imbalance of lower than 1 dB and a phase error of less than approximately 4° along the frequency tuning range from 222.7 GHz to 275.6 GHz. These values ensure that the in-phase and quadrature (I/Q) receiver channel has an image rejection ratio of higher than 23.5 dBc over the frequency tuning range.

Zusammenfassung

Design, Implementierung und Charakterisierung eines ultra-hohen Auflösungs-Radar-Transceiver-Chips im Frequenzbereich von 223-276 GHz wurden vorgestellt. Er wurde in der 130-nm-SiGe-BiCMOS-Technologie von IHP, SG13G2, mit f_T/f_{max} von 300/500 GHz implementiert und bietet hohe Ausbeute und sehr große Integrationsmöglichkeiten bei moderaten Maskenkosten. Die hauptsächlich anvisierte Anwendung für den entwickelten Radarfrontend-Chip ist die zerstörungsfreie Inspektion und Charakterisierung von Materialien. In dieser Dissertation wurde angestrebt, einen Transceiver-Chip zu entwickeln, der in einem breiten Frequenzbereich arbeitet, um eine hohe Reichweitenauflösung zu bieten und für den Aufbau von massiven MIMO-Radar-Arrays geeignet ist, um eine hohe Winkelauflösung zu erreichen. Der entworfene Transceiver-Chip eignet sich zum Aufbau von massiven MIMO-Radar-Arrays in der Daisy-Chain-Architektur dank seiner kaskadierbaren Funktion aufgrund der ILO-Feedthrough-Synchronisierungstechnik. Auf diese Weise können die Nachteile des zentralen LO-Signalverteilungsnetzes in den konzeptionellen massiven MIMO-Radarstudien vermieden werden. Darüber hinaus verfügt der entworfene Radarfrontend-Chip über einen externen VCO-Eingang und ist daher auch für den Einsatz in MIMO-Radar-Arrays auf der Grundlage der herkömmlichen zentralen LO-Signalverteilungsarchitektur geeignet.

Der entworfene Transceiver-Chip mit der On-Chip-Antenne nimmt eine Fläche von 2,72 mm^2 (2,16 mm × 1,26 mm) ein. Außerdem wurde auch der Transceiver-Testchip hergestellt, der durch Platzieren des Marchand-Baluns anstelle der On-Chip-Antenne entstanden ist. Der Marchand-Balun wurde für die On-Wafer-Probing platziert und aus den Messergebnissen entfernt, indem die gemessenen Einfügedämpfungsdaten der rückwärts verbundenen Marchand-Baluns verwen-

det wurden. Wenn der interne VCO deaktiviert und der Eingangsverstärker für den externen LO-Eingang aktiviert wird, zieht das Schaltkreis einen Ruhestrom von 138,1 mA, 151,6 mA und 208 mA aus einer einzigen Spannungsversorgung von 3,3 V bei den Betriebsarten Sender, Empfänger und Transceiver. Im Sendermodus erreicht der Transceiver-Schaltkreis einen Spitzenwert von 3,6 dBm bei 240 GHz und eine 3-dB-Bandbreite von etwa 41 GHz von 220 GHz bis 261 GHz. Auf der anderen Seite beträgt seine Spitzenleistung etwa 3,1 dBm bei 240 GHz mit einer 3-dB-Bandbreite von etwa 45 GHz im Transceiver-Modus. Im Empfängermodus wurde der Spitzenwert des Leistungsabfall-Verstärkungsfakts bei 240 GHz auf etwa 16,24 dB gemessen, und der Schaltkreis erreicht eine gemessene 3-dB-Bandbreite von 41 GHz von 220 GHz bis 261 GHz. Der Unterschied zwischen den gemessenen Leistungsabfall-Verstärkungsergebnissen der Empfänger- und Transceiver-Betriebsarten ist niedriger als 0,7 dB über 220 GHz bis 280 GHz. Im Transceiver-Modus weist der Schaltkreis eine gemessene SSB-Rauschzahl von 18,73 dB bei 255 GHz und besser als 21 dB über die 3-dB-Bandbreite auf. Der gemessene Eingangsreferenz-1-dB-Kompressionspunkt des Empfangswegs wurde bei -16 dBm bei 220 GHz, -16,5 dBm bei 240 GHz und -13,5 dBm bei 260 GHz. Wenn der interne VCO aktiviert ist, verbraucht der Transceiver-Schaltkreis einen Gleichstrom von 197 mA, 213,2 mA und 270,1 mA aus einer einzigen Spannungsversorgung von 3,3 V bei den Betriebsarten Sender, Empfänger und Transceiver. Der gemessene Betriebsfrequenzbereich liegt zwischen 222,7 GHz und 275,6 GHz, was einen Frequenzeinstellbereich von ca. 52,9 GHz ergibt. Im Sendermodus erreicht der Schaltkreis eine Spitzenleistung von 3,3 dBm bei 241 GHz und eine 3-dB-Bandbreite von ca. 43 GHz von 220 GHz bis 263 GHz. Auf der anderen Seite hat der Transceiver-Test-Schaltkreis eine Spitzenleistung von 3 dBm bei 241 GHz und eine 3-dB-Bandbreite reicht von 220 GHz bis 265 GHz im Transceiver-Modus. Der Empfängerkanal im Transceiver-Test-Schaltkreis erreicht eine gemessene Spitzenleistungsabfall-Verstärkung von 16,5 dB bei 240,5 GHz und hat eine 3-dB-Frequenzbandbreite von ca. 40 GHz von 220 GHz bis 260 GHz. Der niedrigste Wert der Rauschzahl wurde bei 255 GHz auf 18,7 dB gemessen. Die gemessene Rauschzahl ist besser als ca. 20,6 dB über die 3-dB-Frequenzbandbreite. Der gemessene Eingangsreferenz-1-dB-Kompressionspunkt des Empfängerkanals beträgt -15 dBm bei 230 GHz, -16,4

dBm bei 240 GHz und -14 dBm bei 260 GHz. Der Schaltkreis erreicht eine Amplitudenimbalanz von weniger als 1 dB und einen Phasenfehler von weniger als ca. 4° entlang des Frequenzeinstellbereichs von 222,7 GHz bis 275,6 GHz. Diese Werte gewährleisten, dass der I / Q-Empfängerkanal eine Bildablehnungsrate von mehr als 23,5 dBc über den Frequenzeinstellbereich aufweist.

Vorwort

I extend my deepest gratitude to the individuals who have played pivotal roles in the completion of this doctoral work:

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Contents

List of Abbreviations and Symbols

List of abbreviations

AAF	Anti-aliasing filter
AC	Alternating current
ADC	Analog-to-digital converter
BEOL	Back-end-of-line
BiCMOS	Bipolar-complementary-metal-oxide-semiconductor
BJT	Bipolar junction transistor
BPF	Band-pass filter
CDM	Code-division multiplexing
CMOS	Complementary-metal-oxide-semiconductor
CMRR	Common-mode rejection ratio
CW	Continuous-wave
DAC	Digital-to-analog converter
DAQ	Data acquisition
DC	Direct current
DDS	Direct digital synthesis

DSB	Double sideband
DSP	Digital signal processor
ECL	Emitter coupled logic
EIRP	Equivalent isotropic radiated power
EM	Electromagnetic
ESD	Electro-static discharge
ETSI	European Telecommunications Standards Institute
FDM	Frequency-division multiplexing
FGL	First grating lobe
FMCW	Frequency-modulated continuous-wave
FoV	Field of view
GFRT	Glass fiber-reinforced thermoplastic
HBT	Heterojunction bipolar transistors
HEMT	High-electron-mobility transistor
HPBW	Half-power beam-width
I/Q	In-phase and quadrature
IF	Intermediate frequency
ILO	Injection-locked local-oscillator
IL-VCO	Injection-locked voltage-controlled oscillator
ISM	Industrial, scientific and medical
ITU	International Telecommunication Union

LNA	Low noise amplifier
LO	Local oscillator
LPF	Low-pass filter
MESFET	Metal-semiconductor field-effect transistor
MIMO	Multiple-input multiple-output
NMOS	N-channel metal-oxide semiconductor
NSLA	Non-uniformly spaced linear array
NSPA	Non-uniformly spaced planar array
PLL	Phase-locked loop
PMCW	Phase-modulated continuous-wave
PMOS	P-channel metal-oxide semiconductor
PVT	Process, voltage, and temperature
RCS	Radar cross section
RF	Radio frequency
Si	Silicon
SiGe	Silicon-germanium
SIMO	Single-input multiple-output
SNR	Signal-to-noise ratio
SPDT	Single-pole double-throw
SSB	Single sideband
SSL	Sidelobe suppression level

TDM	Time-division multiplexing
USLA	Uniformly spaced linear array
USPA	Uniformly spaced planar array
VCO	Voltage-controlled oscillator
3D	Three dimensional

Frequently used symbols

$\Delta\theta$	Phase change
Δf_{Bmin}	Rayleigh frequency
ΔR_{min}	Range resolution
ΔT	Propagation time delay
$\Delta\varphi$	Angular resolution
λ	Wavelength
σ	Radar cross section
φ_{FGL}	Positions of first grating lobes
A_R	Effective area of the receiving antenna
B	Frequency bandwidth
c	Speed of electromagnetic waves in air
D	Size of the virtual array aperture
d_e	Inter-virtual element spacing
f	Frequency
f_0	Free-running frequency
f_B	Beat frequency

f_{IFmax}	Maximum IF frequency
f_{max}	Maximum oscillation frequency
f_S	Sampling rate
f_T	Unity current gain cut-off frequency
G_T	Gain of the transmitter antenna
m_C	Slope of the chirp
P_R	Received power
P_{RT}	Power of the reflected signal
P_T	Peak power of the transmitter
Q	Quality factor
R	Range of a target
S_r	Power density of the reflected signal
S_t	Power density of the transmitted signal
T_C	Chirp duration

1 Introduction

1.1 High Resolution Millimeter-wave Radars

Nowadays, radars are gradually increasingly used in a wide variety of applications with very diverse requirements, owing to their capability of providing information on the range, velocity and angular direction of targets and operating robustly under different weather, temperature, and light conditions. Specific portions of the available radio frequency (RF) spectrum have been allocated worldwide by the International Telecommunication Union (ITU) for industrial, scientific, and medical (ISM) applications, and they are also known as the ISM frequency bands. The center frequency points of the ISM frequency bands of interest for radar-based sensor systems in the literature are listed as follows: 5.8 GHz [LYL+10, LL18, WGIL13, ML19, GAPV22], 24.125 GHz [PJL+19, KKH07, KKBH09, WKL15, WVCS19, WDGK12, BPJ+12], 61.25 GHz [LDVG20, KPR+21, FKH+20, RCS+20, Y+17, KLY+16, BNA+16, KYS+13], 122.5 GHz [NKAK17, NK18, Y+18, SMF+13, GBH+13, JHTS11, SGA+15], and 245 GHz [MMW+19, BDCS13, TBP19, YWC+21a, JBP13, RMB16, JBP14, MRB16, GSS+16, BPJ+13, KMA+20, AFAS21]. In addition, the frequency band of 76 GHz to 81 GHz has been reserved for radars to be used in advanced driver-assistance systems and autonomous driving [HTS+12, NKG+06, JTZH09, FTW+17, LLHH10, KSI+14, GJB+01, JKZ+16, NYP+08, UMU+20, GSD+17a]. Furthermore, a substantial number of studies have been reported on radar-based active imaging systems operating at around 94 GHz [ACK+13, PCK+15, PGL+19, TST+17, JFW+12, LD91, WHB+20, NCSV08] and 140 GHz [MCA17, DSH+19, CJW+13, AIW20, KMK+14]. For some applications such as high-resolution imaging [RMB16, JBP14, MRB16, NPK+14, GRCB+17], non-destructive inspection and characterization of materials [MMW+19, BZR18,

NKFG22, AS15, NSS12, JBWR19, JBR18, BCV+12, SKW+22, KWH+22], high presicion distance measurements [JBKP14, WWG08], tank level gauging systems [VG17], and autonomous navigation in robotic platforms [MS14], it is extremely crucial to be able to accurately distinguish two different targets which are at close proximity to each other. The ability to distinguish closely spaced targets depends on the range and angular resolution of radar-based sensor systems.

Signal waveforms employed in radar systems can be classified into two main categories: pulse signal and continuous signal. An unmodulated continuous-wave (CW) radar is not capable of measuring the range of targets; thus, it is necessary to apply either frequency- or phase- modulation, or a combination of both, to measure the distance between the radar and targets. The most commonly used modulated CW waveforms in the literature are listed as follow: frequency-modulated continuous-wave (FMCW) and phase-modulated continuous-wave (PMCW). The FMCW modulation tecnique requires high-speed fast-settling frequency synthesizers providing a very linear frequency slope [WBSL13]. The design complexity and precision requirements of the frequency synthesizers can be alleviated in PMCW radar architectures [GGE+19]. However, the frequency bandwidth of the intermediate frequency (IF) outputs of PMCW radars is equal to the RF bandwidth of the front-end circuit, resulting in the need for very high-speed analog-to-digital converters (ADCs) [GGS+14]. But on the other hand, the baseband frequency bandwidth of FMCW radars can be determined by changing the slope of the frequency ramp, and even very low-speed ADCs are sufficient for the high range resolution applications mentioned above. Pulse radars measure the time difference between the transmitted and received signals to calculate the distance between the radar and targets. Likewise, the time difference between echoes reflected from multiple targets has to be measured to distinguish targets from each other. To achieve a range resolution of better than 10-mm, a time resolution on the order of a few tens of picoseconds is required in the signal processing side. This requires the use of high-sampling rate ADCs in the receiver baseband. In addition, the pulse length (or pulse width) must be short enough to allow the radar to distinguish echoes separately. There are various pulse compression techniques that can be used to shorten the pulse length [SKM05]. The pulse length is inversely proportional to the

modulation frequency bandwidth, which requires a wide frequency bandwidth in the transmitter and receiver channels [LPM+15]. This, in turn, requires the use of complex, high-speed pulse generator circuits in the transmitter channel to generate ultra-short pulses [ACK+10, OJKH15, TLCH15]. As discussed above on different signal waveforms employed in radar systems, the FMCW waveform is more suitable to build a radar with a high range resolution of better than 10-mm, as it significantly alleviates the speed requirements and complexity of the baseband circuitries in the transmitter and receiver channels without introducing any critical technical constraints on radar performance metrics. This conclusion is justified by the fact that all reported radars with a range resolution of better than 10-mm in the literature are based on FMCW waveforms [RMB16, JBP14, MRB16, GRCB+17, MMW+19, BZR18, NKFG22, JBWR19, JBR18, BCV+12, SKW+22, KWH+22, JBKP14].

In FMCW radars, the range resolution is inversely proportional to the modulation frequency bandwidth of radar front-end circuits [Sko03]. The need for circuits with high quality-factor to provide sufficient performance metrics inevitably limits the realizable fractional bandwidth of radar front-end building blocks. Although there are some circuit techniques to enhance the fractional frequency bandwidth of amplifiers, such as stagger-tuning amplification [LL09, JJK+20] and travelling-wave amplification (also known as distributed amplification) [GHJN48, AMV+82], these circuit techniques do not address the limited frequency tuning range of signal generator circuits. As presented in [RUFC16] and [SKH09], an ultra-broadband frequency tuning range can be achieved by utilizing switched capacitor/varactor/inductor banks. However, the discrete nature of the tuning range obtained as a result of employing switching techniques is not suitable for a radar system requiring continuous frequency change over time. Another approach is the frequency comb architecture based on multiple frequency sub-bandwidths [NMMZ20, YWC+21b]. Even though this approach is applicable to generate a broadband continuous synthetic frequency tuning range for radar front-end circuits, it is not able to solve the problem of limited operating frequency bandwidth of antennas. Therefore, it is required to implement multiple antennas for each frequency sub-bandwidth [YWC+21b], resulting in a significantly reduced capability to

build a phased-array or multiple-input multiple-output (MIMO) radar. In addition, two different wideband frequency synthesizer architectures based on voltage-controlled oscillator (VCO) arrays are proposed to achieve wide continuous frequency tuning range in [ALESS11] and [DJE17]. Moreover, a similar approach was employed in [WBP20] to build a radar front-end with over 40 GHz bandwidth below 60 GHz. However, as in the frequency comb architecture, the operating frequency bandwidth of antennas is still a limiting factor. Beyond these aforementioned technical limits, international agreements on frequency regulation prohibit emission over such a wide frequency bandwidth below 100 GHz to effectively use the frequency spectrum which is an already limited resource [Uni22]. Consequently, it becomes more realizable to provide a wider absolute continuous frequency bandwidth by operating at a higher frequency. Furthermore, the European Telecommunications Standards Institute (ETSI) is considering to open a wide frequency range where ultra-wide-band short range devices can operate for radio-determination applications [ETS19]. In addition, operating at higher frequencies enable the implementation of smaller size antennas hence more compact size radar based sensor systems. Considering all the points mentioned, the wideband frequency window around the 245 GHz ISM band makes this frequency spectrum part attractive for high resolution radar applications [MMW+19, BDCS13, TBP19, YWC+21a, JBP13, RMB16, JBP14, MRB16, GSS+16, BPJ+13, KMA+20, AFAS21].

A radar array with more than one element is utilized to estimate the angular position, direction-of-arrival (DoA), of targets relative to the radar. Radar array configurations can be classified into two main types, that is, phased-array radars [Sko03, Sim93] and MIMO radars [FHB+04, LS07, HBC08]. The angular resolution is dependent on the aperture size of a radar antenna array. In a MIMO system with M number of transmitters and N number of receiver antennas, a radar antenna array consisting of M×N elements can be virtually synthesized since the transmitters emit orthogonal signals [RCW+04]. However, the total number of elements in a phased-array radar is equal to M+N due to the non-orthogonality [Sko03], resulting in lower angular resolution compared to the MIMO array technique for the same number of physical elements. Therefore, the MIMO array architecture is better suited to applications that require high

angular resolution. In addition, it facilitates the building of miniaturized radar array based sensors, thanks to the virtual aperture concept. On the other hand, the phased-array concept improves the detection probability of targets with small radar cross section (RCS), and the maximum range of the radar since it provides the coherent processing gain at the transmitting side, hence higher effective isotropic radiated power (EIRP), which is not utilizable in MIMO radar arrays due to the waveform orthogonality of transmitted signals [DH09]. A new array architecture based on portioning the MIMO array into phased subarrays, which has recently been developed, enables the coherent processing gain and virtual aperture concept together, and it is called phased MIMO array (or hybrid MIMO phased-array) [HV10]. However, this hybrid solution requires advanced level signal processing algorithms [FBR10, MF16] and introduces implementation challenges [HH22]. Moreover, the virtual antenna array aperture size is smaller compared to that of a full MIMO radar array with the same number of physical transmitter and receiver antenna elements since the signal orthogonality between elements of phased subarrays is traded off with the coherent processing gain in a hybrid MIMO phased-array [HH22].

The waveform orthogonality in MIMO radars can be achieved using multiplexing schemes such as time-division multiplexing (TDM), frequency-division multiplexing (FDM) and code-division multiplexing (CDM). The CDM technique inherently requires the use of PMCW based waveforms that the bandwidth of the baseband signals to be processed is equal to the RF bandwidth of the front-end circuit, resulting in the need for very high-speed ADCs [GGS+14]. Therefore, the CDM is not suitable for use in radar-based sensor systems with a high range resolution such as better than 10-mm which means an RF bandwidth of more than 15 GHz. Another multiplexing method, the FDM scheme, is based on simultaneous transmission of signals with a frequency offset between each other. Therefore, it increases the design complexity of transmitter channels to be used in an FDM-based MIMO array since an up-converter has to be utilized to mix the RF signal and the low frequency offset signal generated by a direct digital synthesizers (DDS) [PFWS13]. Moreover, this up-conversion has to be performed by an image-rejection mixer based on in-phase and quadrature (I/Q) up-conversion architecture to avoid false target detection. Furthermore, the ADC

sampling rate requirements at the receiving side substantially increases as the number of array elements increases, which is the case in massive MIMO radar arrays to achieve high angular resolution. On the other hand, the TDM arrangement, in which transmitter array elements are operated sequentially, offers design simplicity with corresponding low cost. The drawbacks of the TDM scheme are linear increase in measurement time with increase in the number of transmitting array elements, and measurement errors in the range, angular position and velocity estimation of moving targets [ZZ15]. However, this is not a problem for most high resolution radar applications, such as non-destructive inspection and characterization of materials [MMW+19, BZR18, NKFG22, AS15, NSS12, JBWR19, JBR18, BCV+12, SKW+22, KWH+22], where scenes consisting of stationary targets are observed.

Each radar-based sensor system needs a specific number of array elements configured according to a specific MIMO array topology regarding performance metrics such as angular resolution, field of view (FoV) and power consumption. It is not feasible to design a MIMO radar chip that meets all the requirements of a large variety of applications. One solution is to design application-specific integrated MIMO radar array circuits [NK18, FWS+09, GSD+17b, LGM22], which is very costly due to the fabrication of a new mask set every time. A more reasonable and lower-cost solution to building a MIMO radar array is to assemble multiple radar chips which have either single and/or multiple channels on a board or in a package [PFS+12, KCP17]. In this case, how to generate the FMCW signal and how to distribute and synchronize this signal so that it can operate at the same frequency and, if necessary, with the same phase in every radar chips arise as a new set of technical questions. Main approaches addressing the signal distribution and synchronization related questions to build scalable massive MIMO radar arrays can be classified under two network topologies: centralized local oscillator (LO) signal distribution network [FKH+20, KCP17, KKS+20, CKHP20] and decentralized daisy-chain network, which is also called LO feedthrough, based on cascading multiple radar front-end chips [GGE+19, K+19, KEA+19, NHK19, AKE+21]. Moreover, a novel methodology called injection-locked LO (ILO) feedthrough, which relies on cascading radar front-end chips through injection-locked oscillators to

provide phase synchronization between array elements in the daisy-chain array topology, has been recently proposed in [MWK19].

1.2 Motivation

Ultra-high range resolution (better than 10-mm) radar front-end chips operating beyond 200 GHz were first implemented in III-V group semiconductor technologies [MMW+19, BDCS13, RMB16, GRCB+17]. There are significant disadvantages of developing a product in III-V group semiconductor technologies, such as low yield, small scale of integration, and high production cost, hence resulting in an inefficient and uneconomic solution for high-volume production. Thanks to the continuing progress in the field of silicon-based semiconductor technologies over the last decades, it has been enabled the development of ultra-high range resolution radar front-ends chips at high yield and very-large-scale of integration with moderate mask costs [TBP19, YWC+21a, JBP13, JBP14, GSS+16, BPJ+13]. Especially, silicon-germanium (SiGe) bipolar-complementary-metal-oxide-semiconductor (BiCMOS) technologies, offering extremely high-speed heterojunction bipolar transistors (HBTs) for excellent millimeter-wave circuit performance and complementary-metal-oxide-semiconductor (CMOS) transistors with very-high scale digital and analog integration capability together, pave the way to the commercialization of the use of ultra-high range resolution radar-based sensor systems in many different industrial applications. One of the promising industrial applications of ultra-high range resolution radars is non-destructive inspection and characterization of materials [MMW+19, BZR18, NKFG22, AS15, NSS12, JBWR19, JBR18, BCV+12, SKW+22, KWH+22].

In these days, one of the key goals of the automotive industry is to compensate for the weight increase due to bulky electric batteries by replacing heavy body parts with lighter counterparts. In this respect, glass fiber-reinforced thermoplastics (GFRTs) are considered as having a significant potential for minimizing the weight of body components in the automotive industry [Mal21]. Furthermore,

GFRTs can be manufactured using less energy than that of currently employed vehicle body components, and they can be recycled with a higher efficiency [Mal21]. In this regard, GFRTs have an enormous potential to contribute to more sustainable manufacturing of vehicle components. However, there are some issues arising during the mass production of GFRTs such as delamination, consolidation, fiber crack and fiber shift [SKW+22]. Therefore, it is very important to analyze the effects of damage on mechanical properties and forming properties of GFRT. Furthermore, thanks to either millimeter-wave/terahertz imaging or thermography-based non-destructive inspection techniques, defects inside manufactured laminates can be detected in-line in order to sort out manufactured laminates accordingly and to be able to intervene in the process. In [SKW+22], non-destructive characterization of GFRTs based composite materials was successfully performed using a single-element 499-733 GHz 3D THz-FMCW imaging system mounted on a mechanical scanner. Similarly, a non-contact surface inspection of a GFRT based component was carried out using a mechanically stepped single-element 514-640 GHz THz-FMCW module in [KBEB19]. Both of these studies present experimental demonstration of the non-destructive inspection using III-V semiconductor technologies based bulky active and passive waveguide components assembled in a laboratory setting to build a single-channel FMCW imaging radar mounted on a mechanical scanner. However, these studies do not address the real-time in-line inspection of GFRTs during production. A concept study based on system simulation results of a 220-260 GHz sparse MIMO imaging array consisting of 32 transmitters and 30 receivers has been reported to address the real-time in-line testing without affecting the production cycle time [WKFB17]. After that, the conceptual design of a 220-260 GHz sparse MIMO radar array, which is planned to consist of 12 transmitters to be implemented in III-V semiconductor technology and 64 receivers to be implemented in a SiGe BiCMOS process, has been presented [KWH+22]. These conceptual MIMO array designs are based on the centralized LO signal distribution network. Considering that the total number of physical array elements is more than 62, they will require an external LO signal source with high output power, a large area LO signal distribution network and possibly amplifiers on the distribution network depending on the output power of the LO signal source and the input power requirements of the

array channels in real implementation.

In this study, the design, implementation and characterization of a cascadable 223-276 GHz SiGe BiCMOS transceiver front-end chip for ultra-high resolution scalable massive MIMO radar arrays are presented to enable the realization of the conceptually reported massive MIMO radar arrays for non-destructive inspection and characterization of materials. Moreover, the designed transceiver chip is suitable to build massive MIMO radar arrays in the daisy-chain architecture thanks to its cascadable feature based on the ILO feedthrough synchronization technique. In this way, the above-mentioned drawbacks of the central LO signal distribution network in the conceptual massive MIMO radar studies can be avoided.

2 Radar Fundamentals and System Architecture

The primary objective of this chapter is to investigate the fundamental principles and techniques that facilitate the design and implementation of advanced radar systems. The chapter begins by introducing the radar range equation. It then delves into FMCW radar theory. The chapter also covers TDM MIMO array theory, which enables the use of multiple antennas to improve the angular resolution of the radar arrays. The architecture of the designed transceiver is also discussed, as this is the key component responsible for transmitting and receiving signals. Finally, the chapter concludes with a detailed examination of the ILO feedthrough technique that allows the cascading of multiple transceivers in a more compact manner.

2.1 Radar Range Equation

The range of a target is defined as the line of sight distance between the radar and the illuminated target object. To begin deriving the radar range equation, we first assume that the radar uses the same antenna for both transmitting and receiving, or that the distance between the transmitter and receiver antennas is negligibly short compared to the range of the target. Then, we assume that the transmitter antenna radiates electromagnetic waves out uniformly and equally in all directions as an omnidirectional antenna. If the peak power of the transmitter is denoted by P_T, the power density S_t at any distance R from the transmitter is equal to the peak transmitter power divided by the surface area of the sphere with a radius of R, as given in (2.1).

$$S_t = \frac{P_T}{4\pi R^2} \tag{2.1}$$

In practical radars, the transmitter antenna does not radiate in all directions. Instead, a directive antenna is employed to shape the beam, which radiates the energy preferentially in one direction. The antenna gain is the power radiation intensity of an antenna in a specific direction over that of an isotropic antenna. Then, the power density from a directive antenna at any R is equal to (2.1) multiplied by the gain of the transmitter antenna G_T, as shown in (2.2).

$$S_t = \frac{P_T G_T}{4\pi R^2} \tag{2.2}$$

The electromagnetic waves radiated by the transmitter antenna continues to propagate until they encounter a target. Then, the impinging radiated power is reflected by the target in the direction of the radar in proportion to the target's RCS. RCS, a measure of the energy emitted by the target back towards the radar, depends on shape, size, material, or orientation of target objects. It can be intuitively defined as the effective electromagnetic size of the target seen by the radar and is denoted with σ in equations. Assuming that the object is a point target whose physical size is small enough compared to the illuminated area at R by the radar, the power of reflected signal P_{RT} at the range of the target is then given by (2.3), which is equal to the power density at the range of the target multiplied by the RCS of the target object.

$$P_{RT} = S_t \times \sigma = \frac{P_T G_T}{4\pi R^2} \times \sigma \tag{2.3}$$

Afterwards, the power density of the reflected signal S_r at the radar is equal to the power of the reflected signal at the target divided by another factor of the surface area of the sphere with a radius of R, as expressed in (2.4).

$$S_r = \frac{P_{RT}}{4\pi R^2} = \frac{P_T G_T \sigma}{(4\pi R^2)^2} \tag{2.4}$$

As presented in (2.5), the received power P_R at the receiving antenna of the radar can be calculated by multiplying the power density of the reflected signal S_r at the radar with the effective area A_R of the receiving antenna. And, the effective area, also called the effective aperture, of the receiving antenna can be calculated using (2.6).

$$P_R = S_r A_R = \frac{P_T G_T \sigma A_R}{(4\pi R^2)^2} \tag{2.5}$$

$$A_R = \frac{G_R \lambda^2}{4\pi} \tag{2.6}$$

If the expression of the effective area of the receiving antenna (2.6) is substituted into the equation of the received power P_R at the receiving antenna of the radar (2.5), then the received power P_R can be expressed by (2.7).

$$P_R = P_T \frac{G_T G_R \lambda^2}{(4\pi)^3 R^4} \sigma \tag{2.7}$$

If the minimum detectable power by the receiver providing a certain signal-to-noise ratio (SNR) at the receiver output is denoted by P_{R-min}, the maximum detectable range can be calculated using (2.8). According to this equation, the transmit antenna gain, the receiver antenna gain, the wavelength of the operating signal, hence the operating frequency, the power of the transmitted signal, and the minimum detectable power by the receiver are important metrics determining the maximum range of a radar.

$$R_{max} = \sqrt[4]{(P_T \frac{G_T G_R \lambda^2}{(4\pi)^3 P_{R-min}} \sigma)} \tag{2.8}$$

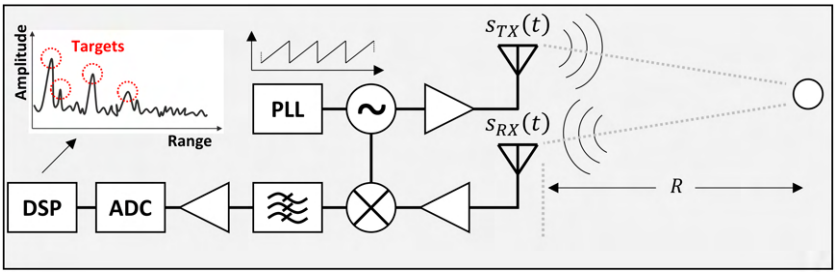


Figure 2.1: A typical simplified circuit block diagram of an FMCW radar.

2.2 FMCW Radar Theory

As mentioned in Section 1.1, the most suitable signal waveform employed for observing scenes consisting of stationary objects is FMCW for radars with ultra-high range resolution. In an FMCW radar, a chirp, whose frequency is linearly changing monotonically, usually in saw-tooth or triangular modulation forms, within a time frame T_C is radiated continuously across a given frequency bandwidth B. The slope of the chirp m_C defines the rate at which the chirp ramps up, and is expressed in (2.9).

$$m_C = \frac{B}{T_C} \tag{2.9}$$

A typical simplified circuit block diagram of an FMCW radar, consisting of a single transmitter and a single receiver channels, is presented in Figure 2.1. A frequency synthesizer, consisting of a phase-locked loop (PLL) and a VCO, generates a chirp, and then this chirp signal is amplified by a power amplifier and then transmitted through the transmit antenna. After that, the transmitted chirp signal is reflected from targets, and then captured by the receiving antenna with a round trip propagation time delay Δt corresponding to the distance, which is given in (2.10), where R is the distance between the radar and the target, c is the speed of electromagnetic waves in air.

$$\Delta t = \frac{2R}{c} \tag{2.10}$$

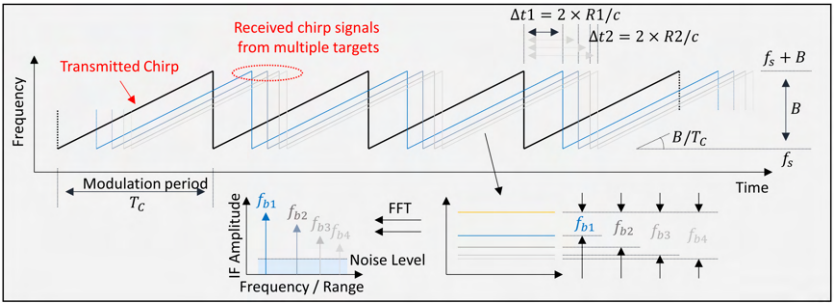


Figure 2.2: A basic detection operation of an FMCW radar with multiple target objects.

The received signal is then mixed with the chirp signal from the synthesizer by a down-converter mixer. The frequency of the IF signal produced by the mixer, called the beat frequency f_b, is equal to the frequency difference between the received chirp signal and transmitted chirp signal. It is also equal to the slope of the chirp m_C multiplied with the round trip propagation time delay Δt. Combining (2.9), (2.10), and the value of the beat frequency f_B, the range of the target can be calculated by (2.11).

$$R = \frac{\Delta t \times c}{2} = \frac{f_B \times c}{2 \times m_C} = \frac{f_B \times T_C \times c}{2 \times B} \tag{2.11}$$

Figure 2.2 demonstrates how an FMCW radar detects multiple target objects. As noted in Section 1.1, for applications that require ultra-high range resolution, it is extremely important to be able to accurately distinguish two different targets that are close to each other in the range domain. The range resolution depends on whether two beat frequencies that are close to each other can be resolved in the signal processing part. After the Fourier transform is performed within a finite observation time window of T, the minimum resolvable frequency, which is also known as the Rayleigh frequency, is equal to $1/T$ in the frequency spectrum. Assume that there are two objects which are at distance $R1$ and $R2$ ($R1 < R2$) from an FMCW radar. In order to detect these two objects separately, the range resolution of the radar has to be better than $\Delta R = R2 - R1$. If it is assumed that the distance between these two targets is equal to the theoretical range

resolution ΔR_{min} of the radar, then the range resolution of the radar can be expressed by (2.12), where f_{B1} and f_{B2} are the beat frequencies produced due to these targets, and Δf_{Bmin} is the Rayleigh frequency.

$$\Delta R_{min} = R2 - R1 = \frac{(f_{B2} - f_{B1}) \times T_C \times c}{2 \times B} = \frac{\Delta f_{Bmin} \times T_C \times c}{2 \times B} \tag{2.12}$$

In an FMCW radar, the chirp frequency is swept over a frequency modulation bandwidth of B during a time period of T_C. Therefore, the Fourier transformation is performed for a time window of T_C, and thus the Rayleigh frequency Δf_{Bmin} is equal to $1/T_C$. Then, the range resolution of an FMCW radar can be calculated using (2.13), by substituting $1/T_C$ instead of Δf_{Bmin}. As seen from the equation, the range resolution is only dependent on the frequency modulation bandwidth of the radar.

$$\Delta R_{min} = \frac{\frac{1}{T_C} \times T_C \times c}{2 \times B} = \frac{c}{2 \times B} \tag{2.13}$$

As illustrated in Figure 2.1, the IF signal is typically digitized for subsequent further processing on a digital signal processor (DSP). An analog low-pass filter (LPF) is employed to filter out high frequency components and noise in order to provide anti-aliasing filtration before the ADC. That is why this LPF is also known as anti-aliasing filter (AAF). While designing data acquisition (DAQ) circuit, one of the most important points is to determine the frequency bandwidth of the LPF and the sampling rate of the ADC. Because, these two parameters determines the maximum range of an FMCW radar while assuming the receiver power is higher than the minimum detectable level. As depicted in (2.14), (2.11) can be rewritten by leaving only the beat frequency on the left side and replacing the range term R by the maximum range R_{max}, and also replacing the beat frequency by the maximum IF frequency f_{IFmax}. It should be noted here that the maximum range R_{max}, which is limited by the frequency bandwidth of LPF and the sampling rate of ADC, is assumed to be smaller than the maximum unambiguous range. The maximum unambiguous range is

determined by the required temporal overlap of the delayed received chirp with the transmitted chirp.

$$f_{IFmax} = \frac{2 \times R_{max} \times m_C}{c} \tag{2.14}$$

According to the Nyquist sampling theorem, the sampling rate f_S of the ADC has to be greater or equal to twice the maximum IF frequency f_{IFmax}. However, if the baseband signal is complex, then an ADC with a sampling rate of $f_S = f_{IFmax}$ can be used.

2.3 TDM MIMO Array Theory

As explained in Section 1.1 presenting the literature review, the MIMO array concept is perfectly suited for estimating the DoA of targets at high angular resolution. In a MIMO radar array, the waveform orthogonality between transmitting elements must be achieved by utilizing a multiplexing technique to synthesize virtual antenna arrays [RCW+04]. The TDM is the most suitable multiplexing scheme to provide waveform diversity for massive MIMO radar arrays. Because unlike other multiplexing techniques such as FDM and CDM, it does not cause the need to increase the sampling rate of ADCs used in receiver channels as the number of array elements increases. Moreover, there is not any interference between transmitting antennas since transmitting elements are activated sequentially [FWS+09]. Although it may cause measurement errors in the range, angular position and velocity estimation of moving targets due to the low frame rate as a result of the sequential operation [ZZ15], these measurement errors do not occur when observing stationary targets, as in applications such as non-destructive inspection and characterization of materials. For accurate DoA estimation, there must be a phase correlation between array elements or the phase mismatch between array elements must be calibrated. In TDM-based MIMO radar arrays, the phase calibration can be easily performed in the digital domain after IF signals are digitized by ADCs in receiver channels [GKD13]. Therefore, it is sufficient to perform only frequency synchronization between the array elements in TDM MIMO radars. Methods of achieving frequency

synchronization will be discussed in detail later.

To evaluate key performance parameters of a MIMO radar array consisting of N_{RX} receiver and N_{TX} transmitter elements, such as angular resolution, unambiguous FoV and sidelobe suppression level (SSL), the MIMO radar array can be modelled as a single-input multiple-output (SIMO) radar consisting of a single transmitter and a number of receiver elements equal to the product of N_{RX} and N_{TX} [SPS+13]. This modelling approach is also termed the virtual array concept [RCW+04]. The analysis of the performances of different MIMO radar array geometries will start with dense uniformly spaced linear arrays (USLAs) with conventionally $\lambda/2$ spaced array elements, where λ denotes the wavelength at the operating frequency, and the evaluation will be extended to sparse non-uniformly spaced planar arrays (NSPAs). There are different equations in the literature mathematically expressing the angular resolution of a MIMO radar array [NK18, HTS+12, SPP20, APR+22, VRD+20]. However, it is widely accepted to use the Rayleigh criterion-related angular resolution definition. As given in [VRD+20], the angular resolution defined according to the Rayleigh criterion can be approximately calculated by (2.15), where D is the size of the virtual array aperture in the direction considered.

$$\Delta\varphi \cong \frac{180^\circ}{\pi} \times 1.22 \times \frac{\lambda}{D} \tag{2.15}$$

Another widely accepted definition of the angular resolution is the half-power (or 3-dB) beam-width (HPBW) of the main lobe of the array factor derived based on the virtual SIMO array model. This definition is very useful to evaluate the angular resolution of MIMO radar arrays in a very wide variety of array geometries. In addition, the calculated array factor can be used to find the unambiguous FoV and SSL values of MIMO radar arrays. The HPBW of a USLA can be approximately expressed by (2.16) [SPP20], where N is the number of virtual SIMO array elements and d_e is the inter-virtual-element spacing. For a uniformly spaced antenna array, the angular positions of first

grating lobes (FGLs) can be approximately calculated by (2.17) [APR+22] for a target at 0°.

$$\Delta\varphi_{3-dB} \cong 2\arcsin(\frac{1.4\lambda}{\pi \times N \times d_e}) \cong 2\arcsin(\frac{1.4\lambda}{\pi \times D}) \tag{2.16}$$

$$\varphi_{FGL} \cong \arcsin(\frac{\lambda}{2 \times d_e}) \tag{2.17}$$

It is clear that the angular resolution of a MIMO radar array can be further enhanced by increasing the effective antenna aperture size D, which is roughly equal to the term of $N \times d_e$ in both (2.15) and (2.16) for $N >> 1$. In order to have better angular resolution without increasing the total number of array elements, the inter-element spacing of array elements can be extended. However, it leads to a reduction in the ambiguous-free region in the FoV if the inter-element spacing is larger than $\lambda/2$, as can be seen from (2.17). The way to break this trade-off between the angular resolution and the unambiguous FoV of a MIMO radar array is to utilize the sparse non-uniformly spaced array technique [SPS+13, ASS11, BAM+17]. The key challenge for building sparse MIMO radar arrays is to determine the optimum locations of array elements so as not to result in high SSL and grating lobes limiting the unambiguous FoV [SPP20]. Unfortunately, there is no reported mathematical method yet to find out the optimum locations of array elements that achieve an ambiguous-free FoV with an improved SSL performance [FWS+09]. However, there are various algorithms used in the optimization of array configurations, such as the simulated annealing algorithm [BRK+17], particle-swarm algorithm [JRS07], brute-force approach [SFWS09], iterative convex optimization [FWS+09], deterministic synthesis procedure [BDI+10], global optimization algorithm [CRGG+14], and genetic algorithm [VBW17]. With the help of these optimization algorithms, the sparse array technique allows to increase the distance between array elements and thus enables the use of larger antenna structures, such as horn antennas and plastic or silicon lenses, which provides higher antenna gain and better SSL, as physically demonstrated in [BRK+17] and [CCL+18]. Figure 2.3(a) shows a dense USLA MIMO radar consisting of four receiver and four transmitter elements. Its equivalent virtual array is also illustrated in Figure 2.3(a). In order to meet the requirements of the Nyquist spatial sampling theorem [DSL14],

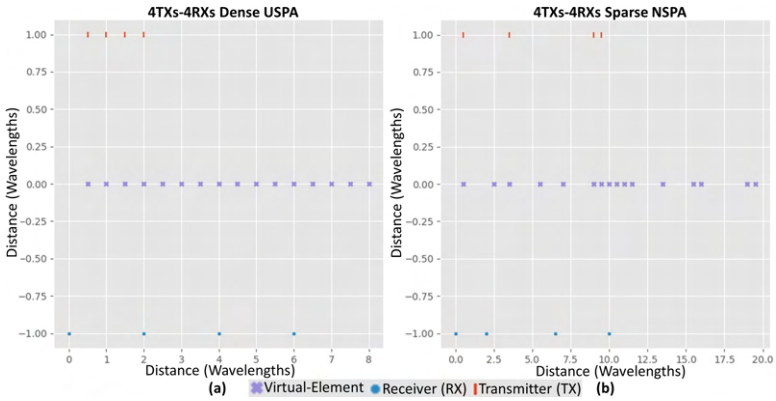


Figure 2.3: (a) Dense USLA MIMO radar array geometry showing positions of 4-TXs and 4-RXs (b) Sparse NSLA MIMO radar array geometry showing positions of 4-TXs and 4-RXs (red-bar:RX, blue-point:TX, cyan-star: virtual).

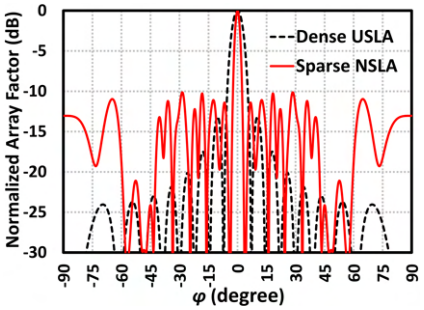


Figure 2.4: Simulated array-factors of the dense USLA and sparse NSLA configurations given in Figure 2.3

the spacing between neighboring receiving antennas was set to $\lambda/2$ and the transmit antennas were placed apart from each other by the product of the total number and inter-element distance of the receiving antennas. Figure 2.3(b) presents a sparse non-uniformly spaced linear array (NSLA) MIMO radar with the same number of array elements as the array of Figure 2.3(a). The distances between two consecutive array elements were optimized using the global optimization technique as in [CRGG+14]. The effective antenna aperture size

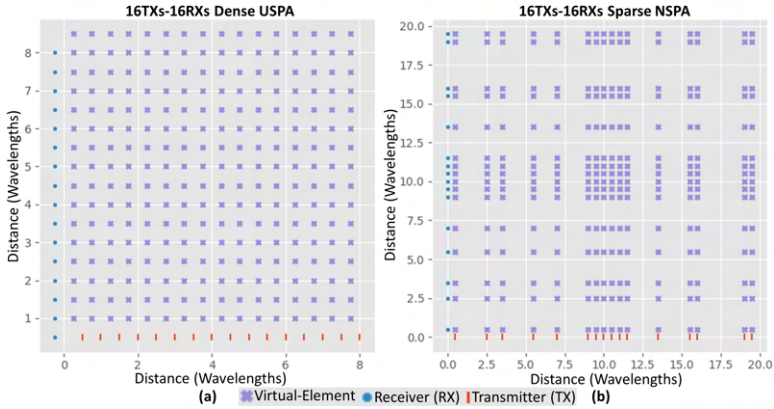


Figure 2.5: (a) Dense USPA MIMO radar array geometry showing positions of 8-TXs and 8-RXs (b) Sparse NSPA MIMO radar array geometry showing positions of 8-TXs and 8-RXs (red-bar:RX, blue-point:TX, cyan-star: virtual).

of the sparse array is 19λ, and it is considerably more than that 7.5λ of the dense array. Figure 2.4 depicts the normalized magnitude plots of the calculated array factors of the arrays in Figure 2.3. The HPBW values of the equivalent virtual SIMO arrays synthesized using the physical elements in Figure 2.3, are calculated to be 6.4° and 2.7° for the dense and sparse arrays, respectively. As can be seen from Figure 2.4, these calculated HPBW values are very close to the actual HPBW values which can be deduced from the main-lobe of the normalized array factors. Figure 2.4 also points that there is no grating lobe in the ±90° FoV for a target at 0° for both the dense and sparse linear arrays.

In order to estimate the DoA of targets in both the azimuth and elevation directions, a planar radar array should be employed. Figure 2.5(a) visualizes an example of a dense uniformly spaced planar array (USPA) MIMO radar geometry, consisting of four receiver and four transmitter elements placed on the x-y plane. The synthesized equivalent virtual SIMO array is also illustrated in Figure 2.5(a). As can be seen, the virtual elements are equally spaced with a distance of $\lambda/2$ so that the sampling theorem is fulfilled in the spatial domain to avoid ambiguities (grating lobes) in the ±90° FoV. In addition, a sparse NSPA with the same number of array elements as the dense USPA is designed,

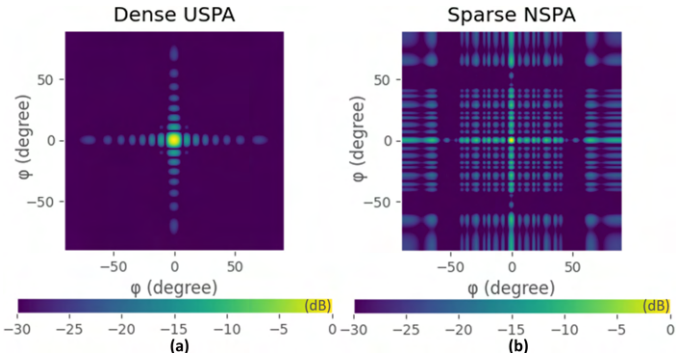


Figure 2.6: Simulated array-factors of the dense USPA and sparse NSPA configurations given in Figure 2.5.

and illustrated in Figure 2.5(b). As mentioned above, the distances between the physical elements were optimized using a global optimization technique to avoid grating lobes in the ±90° FoV while determining the geometry of the sparse NSPA MIMO radar. Thanks to the used optimization algorithm, the effective aperture size of the sparse array was enhanced to 19λ from 7.5λ in both the azimuth and elevation directions. The normalized antenna factors of the equivalent virtual SIMO arrays are presented in Figure 2.6(a) and Figure 2.6(b) on the 2D-plane, respectively, for both the dense and sparse planar arrays in response of a target at 0°. As can be seen from Figure 2.6, the angular resolution of the designed sparse NSPA MIMO radar, which is found as 2.7° in both the azimuth and elevation planes, is quite higher compared to that of the dense USPA configuration with the same number of the physical elements. As seen from Figure 2.6, no grating lobes, which may cause ambiguity, are observed in the ±90° FoV for a target at 0° for both the dense and sparse planar arrays.

As can be concluded from the comparison of the dense and sparse MIMO radar array configurations and their simulation results presented above, the sparse array technique enhances the angular resolution without increasing the number of physical receiver or transmitter elements. Thanks to the optimization

algorithms, an optimum array geometry can be designed such that it will not cause any ambiguities in the FoV range of interest.

2.4 Transceiver Architecture

For an FMCW radar transceiver, the first design step is to determine how to generate the chirp signal. There are two commonly preferred methods to generate the chirp signal. The first method, which is to employ a fundamental VCO, suffers from a narrow tuning range for the frequency range of interest [VTD+13]. It also poses a significant challenge to design a reliable frequency divider which is robust to process, voltage, and temperature (PVT) variations since the operating frequency is very close to the nominal unity current gain frequency (f_T) of the used semiconductor process [AEKL+15]. The second method is to utilize a frequency multiplication circuitry to move the frequency of the generated chirp signal into the operating frequency range. In [SBH+16], a VCO is followed by a frequency doubler, resulting in high phase noise and narrow tuning range caused by insufficient performance of varactors in the frequency range of the VCO. To overcome these problems, it is generally preferred to employ a frequency multiplier circuit with a higher multiplication factor [AYK+20, P11, BMAP20, SHP14, SRS+20, YCL+21]. Moreover, using a high multiplication factor allows the RF input and output pins required for synchronization between front-end chips in MIMO radar arrays to operate in a lower frequency range. In this way, this enables the use of low cost packaging solutions suitable for mass production. In addition, it allows to use low-cost laminates and low-resolution manufacturing processes for board implementation. However, using a high multiplication factor comes with the necessity to suppress a large number of unwanted harmonics falling into the operating frequency range in case of high bandwidth operation. Therefore, suppression of unwanted harmonics is very important to prevent false target detection in radar applications. Considering aforementioned points, it was decided that the total multiplication factor of the designed front-end transceiver chip is x18. As explained in [TAD+22b], a high degree rejection is required at the nodes between the multiplier sub-circuits in order to avoid the strong products of the mix of the

undesired and desired harmonics. Especially, the undesired signals at the node between the first and second triplers play an important role in the suppression levels of the in-band harmonics since their final products fall in the operating frequency range of the receiver input and transmitter output nodes of the designed transceiver. Therefore, a 3rd-order Chebyshev band-pass filter (BPF) was placed between the first and second triplers. As explained before, there are mainly two array topologies used in massive MIMO radar systems, which are centralized LO signal distribution and decentralized daisy-chain network. Since the transceiver chip designed within the scope of this study is aimed to be suitable for both types of array topologies, a single-pole double-throw (SPDT) switch that switches between the external LO input and the internal VCO was placed before the multiplication chain. Thanks to the external LO input and high multiplication factor, the use of off-the-shelf frequency synthesizers, providing better phase noise performance compared to on-chip silicon based VCOs, is also enabled for the centralized LO signal distribution configuration. On the other hand, an injection-locked VCO (IL-VCO) was placed as an internal signal generator for the ILO feedthrough based daisy-chain array topology for scalable massive MIMO radar configurations. Finally, a frequency divider chain with a total division factor of 4 was placed to divide the VCO frequency to enable the use of off-the-shelf PLLs in order to generate highly linear frequency ramps.

A receiver channel should have a sufficient down-conversion power gain to suppress the noise contribution from the following IF and digitalization stages and a low noise figure to provide good SNR on the IF spectrum. The IF output frequency of FMCW radar receivers is generally limited to a few tens of MHz and is a function of the chirp bandwidth, modulation period, and target range. The I/Q receiver architecture is highly preferred over the single-path receiver topology because it enables the suppression of noise contribution from the image band, potentially enhancing the SNR of the IF output signals by 3 dB at the cost of higher power consumption and larger chip area. Furthermore, the required sampling rate is halved thanks to enabled complex signal sampling. The most critical point of utilizing an I/Q receiver from building a MIMO array point of view is that the phase calibration techniques require complex signal processing [GKD13]. Consequently, it is decided to have an I/Q recei-

ver channel in the designed transceiver chip. One of the main challenges in designing an low noise amplifier (LNA) for the intended frequency range is achieving a noise figure that is lower than the total noise figure of the subsequent circuits, while also providing sufficient power gain to suppress noise from later stages. In [TKN15] and [ADS+20], the employment of the mixer-first RX architecture, without any pre-amplification, is indispensable as the cut-off frequencies of used technologies are only slightly above the frequency range of interest. Even though the used semiconductor process is convenient to design an LNA, the mixer-first architecture can be evaluated as a reasonable choice because of low power consumption, enhanced frequency range and linearity as discussed in [AM10] and as demonstrated in [EAK+17], [VGS+17]. However, the I/Q receiver architecture requires pre-amplification to compensate for the insertion loss that occurs when the RF signal is divided into I- and Q- channels. It is presented in [TAD+22a] that an I/Q receiver channel with LNA outperforms mixer-first topologies for the frequency range of interest. Therefore, an LNA-first I/Q receiver channel was employed to perform the down-conversion operation required for the radar signal processing.

Existing board manufacturing processes used in high-volume mass production do not allow the implementation of any antenna structures at 240 GHz with high precision. Even if this issue is somehow solved in the future, it is inherently not feasible to provide a signal path between the chip and the on-board antenna with an acceptable insertion loss over the frequency range of interest. Because pins made of a conductive material in any type of packaging concepts will introduce significant parasitic inductance and shunt capacitance, which cannot be compensated for a broad frequency bandwidth operation around 240 GHz. Therefore, it is inevitable to use one of the following antenna concepts: antenna-in-package (AiP) or antenna-on-chip (AoC). In [AFS18], an antenna at 240 GHz implemented in an embedded wafer level ball grid array (eWLB) package is demonstrated in accordance with the AiP concept. Although the implemented antenna in the eWLB package has a good directivity, it still suffers from the high chip-to-package transition loss for the frequency range of interest. Consequently, the AoC concept seems to be the most feasible method for radiation for this frequency range of interest, considering the limits

of today's packaging technologies. In a silicon-based semiconductor process, antenna structures without ground radiate out a significant amount of energy through the silicon substrate instead of upward into the air due to the high dielectric constant of the silicon substrate (ε_r = 11.7) [RNK83]. Therefore, it is a preferred rational approach to utilize an integrated antenna in such that it radiates out from the back side of the chip according to the numerical analysis in [RNK83]. Moreover, to have a more directive radiation pattern, a lens can be coupled on the back-side of the chip so that its focal plane is aligned with the radiation center of the on-chip antenna, as proposed by [Reb92] and demonstrated in [BGK+06]. One of the critical points to be decided while determining the architecture of a radar transceiver chip with an AoC concept is whether the transceiver chip will be in a monostatic or bistatic configuration. In the bistatic configuration, it is not possible to align the focal plane of the lens so that it passes through the radiation centers of both transmitting and receiving antennas. This causes the main radiation lobes of the two antennas to have angular offsets in opposite directions with respect to each other as depicted in Figure 2.7(a), thus having a limited maximum detectable range in a radar based sensor system. Therefore, it was decided that the transceiver front-end chip should have a single antenna used in both the transmitting and receiving directions simultaneously as illustrated in Figure 2.7(b). For this reason, a coupler providing high isolation between the receiver and transmitter channels was placed to create the signal paths of transmitter-to-antenna and antenna-to-receiver at the same time. The circuit block diagram of the transceiver front-end chip which was designed by considering the key design points discussed above is shown in Figure 2.8. It allows to use either internal VCO signal or external LO signal thanks to the digitally controlled SPDT switch. Furthermore, it enables to build massive MIMO radar arrays through the injection input and LO output ports of the designed IL-VCO. In addition, the designed front-end chip can be configured via the digital enable/disable control pins to operate in one of the following modes: transmitter, receiver, and transceiver.

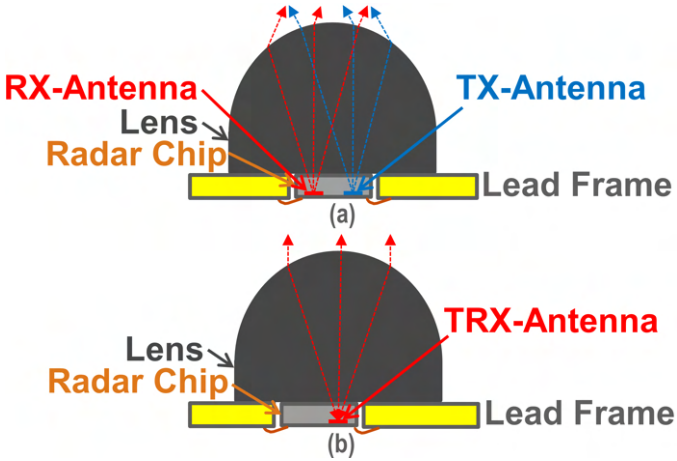


Figure 2.7: (a) On-chip antennas coupled with a lens in bistatic configuration (b) On-chip antenna coupled with a lens in monostatic configuration.

2.5 Cascadable Transceiver

As discussed earlier, the frequency synchronization between array elements is required in TDM MIMO radar systems. On the other hand, the phase mismatch between array elements can be easily calibrated in the digital domain after digitizing the IF signals [GKD13]. According to the literature review presented in Section 1.1, it has been stated that there are two commonly preferred array topologies used to build massive MIMO radar arrays, and these are centralized LO signal distribution network [FKH+20, KCP17, KKS+20, CKHP20] and decentralized daisy-chain network [GGE+19, K+19, KEA+19, NHK19, AKE+21]. There are two types of feedthrough techniques, which are also termed cascading methods, used in the building of decentralized daisy-chain MIMO radar arrays: the LO feedthrough cascading method [GGE+19, K+19, KEA+19, NHK19,AKE+21], and the ILO feedthrough synchronization technique recently proposed in [MWK19].

Key design parameters or requirements of MIMO radar arrays, such as angular resolution, unambiguous FoV, and SSL, differ from application to applicati-

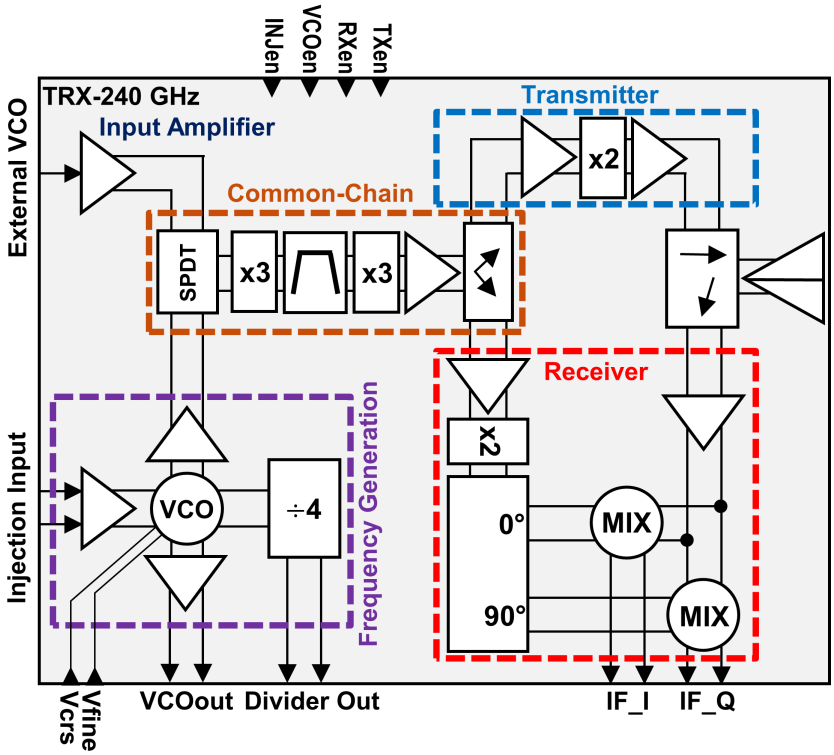


Figure 2.8: Circuit block diagram of the designed transceiver chip.

on. If the centralized LO signal distribution topology is employed, the power budget calculations and the design of the LO signal distribution network must be re-performed according to the number of physical array elements and the inter-element spacing requirements for each application. Additionally, as the number of physical array elements increases as like in massive MIMO radar arrays, the design complexity and area of the LO signal distribution network increase. Moreover, as the number of physical array elements increases, either the output power of the central oscillator must be enhanced or amplifiers must be placed on the appropriate branches in the LO signal distribution network, or even both in some cases, in order to provide the minimum required power

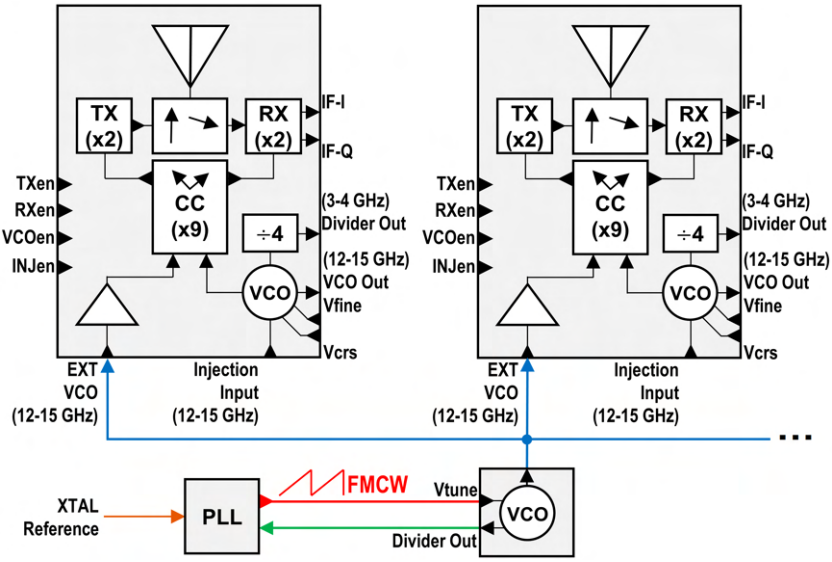


Figure 2.9: Simplified block diagram of a MIMO array in the centralized LO signal distribution configuration.

at the external LO input of array elements. All these are significant drawbacks of the centralized LO signal distribution configuration, which increase both the design time and overall costs of a radar-based sensor system. Figure 2.9 visualizes how a MIMO radar array can be built in the centralized LO signal distribution topology using the designed transceiver chip. On the other hand, in the daisy-chain method, the need for this bulky and costly LO signal distribution network is eliminated thanks to its scalable structure by cascading multiples of array elements. However, the conventional LO feedthrough cascading technique is not able to ensure wideband phase coherence between array elements when required for any reason. Although the centralized LO signal distribution configuration theoretically seems to provide a wideband phase-matched LO signal for the array elements, there will be phase differences from transceiver chip to transceiver chip due to fabrication tolerances of transmission lines, bondwires, and packages in practice. As proposed in [MWK19], the ILO feedthrough synchronization concept can provide phase-matched operation for

all array elements thanks to the phase-shifting feature of the injection-locking mechanism to eliminate the need for complex-signal processing required for the phase calibration in the digital domain. Figure 2.10 illustrates how a MIMO radar array can be built in the daisy-chained manner based on the ILO feedthrough technique using the designed transceiver chip. Each array element utilizes its own IL-VCO as an LO signal generator. Both the tuning control pins V_{COARSE} and V_{FINE} of the transceiver chip configured as the master array element are connected together to an external PLL driven by the frequency divider output of this chip in the closed-loop feedback to generate the FMCW signal. In order to keep the oscillation frequencies in close proximity to each other, the high-gain tuning control pins (V_{COARSE}) of all array elements are tied together and the consecutive transceiver chips are cascaded through their VCO Out and injection input ports. The low-gain tuning control pins (V_{FINE}) of each slave array element are controlled by a non-inverting op-amp based amplifier with a tunable resistor tuned by a high-resolution digital-to-analog converter (DAC). Thus, the low-gain tuning control pin of each element can be individually tuned to a voltage level to shift the phase of the signal generated by the internal IL-VCO without changing its frequency which is locked to that of the master element. The phase change with respect to the input injection signal $\Delta\theta$ can be analytically given by (2.18), as presented in [Raz04], where Q is the quality factor of the oscillator tank, f_0 is the free-running frequency of the IL-VCO, I_{osc} and I_{inj} are the oscillation and injection currents, respectively, f_{inj} is the frequency of the injection signal.

$$\Delta\theta = \frac{180^\circ}{\pi} \times \frac{2Q}{f_0} \times \frac{I_{osc}}{I_{inj}} \times (f_0 - f_{inj}) \tag{2.18}$$

As mathematically expressed by (2.18) and explained in [Raz04], an ILO can be utilized as a continuous analog phase shifter in the locking range. In [MWK19], it has been proposed to employ an ILO for simultaneous frequency and phase synchronization across array elements of a MIMO radar array as also described above. Later, it has been demonstrated that the phase noise of different ILOs is fully correlated in a daisy-chained MIMO radar array based on the ILO feedthrough technique [SMD+21]. Additionally, it can be proposed that the phase-shifting capability of the ILO feedthrough technique enables the analog

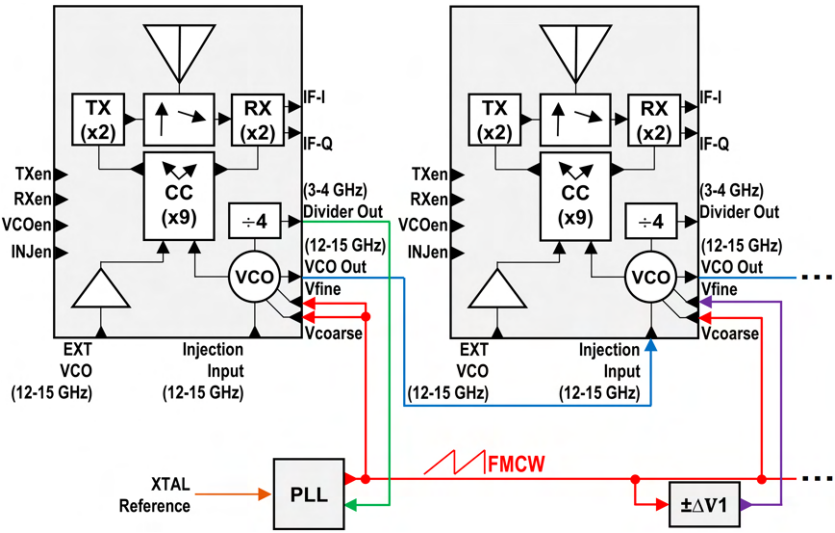


Figure 2.10: Simplified block diagram of a MIMO array in the daisy-chain configuration based on the ILO-feedthrough technique.

beamforming of the transmitter channels. In this way, a hybrid MIMO phased-array can be also built using the proposed transceiver architecture, thus it can benefit from the coherent processing gain [HV10].

3 Design and Implementation of the Transceiver Chip

Recent advances and continued developments in SiGe BiCMOS technologies have made it possible to manufacture low-cost, fully integrated single-chip millimeter wave systems with competitive performance compared to their III-V counterparts. Therefore, the transceiver chip was implemented using IHP's 0.13µm SiGe BiCMOS technology, SG13G2, featuring high-performance transistors with f_T/f_{max} of 300GHz/500GHz [HBB+10]. The all-aluminum back-end-of-line (BEOL) contains five thin metal layers and two thick metal layers for high quality on-chip inductor and transmission line designs. The BEOL also includes metal-insulator-metal (MIM) capacitors offering high-performance high-capacitance density.

As presented in Fig. 2.8 before, the designed transceiver circuit consists of seven different sub-parts: transmitter, receiver, common-chain, signal generation, input amplifier, rat-race coupler, and on-chip antenna. The full-layout of each sub-block was simulated using ADS Momentum, and the circuit simulations were performed using these electromagnetic (EM) models. In this chapter, the design, implementation and simulation results of the sub-blocks of the designed transceiver chip are given.

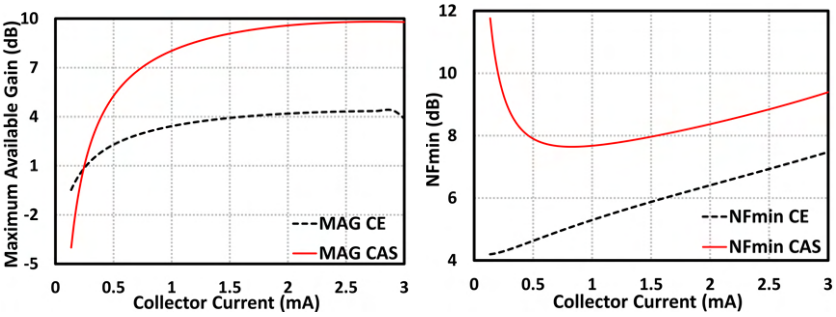
3.1 Receiver Channel

The designed I/Q receiver channel consists of a 240 GHz LNA, a 240 GHz Wilkinson power divider, two 240 GHz down-conversion mixers, a 240 GHz branch-line coupler, and a frequency doubler with its 120 GHz driver amplifier.

The branch-line coupler, generating the I/Q LO signals, was placed at the LO-path of the down-conversion mixers instead of the RF-path to mitigate the effect of its amplitude error on the IF outputs. Because the conversion gain performance of mixers becomes less sensitive to variations in LO power compared to variations in RF power if the available LO power is high enough to drive mixers into switching regime. In FMCW radar applications, the lower and higher limits of the IF frequency range can be adjusted by changing the sweeping slope of the chirp considering the intended target range. Therefore, the IF-outputs can be alternating current (AC) coupled to off-the-shelf low-frequency amplifiers, exhibiting very low flicker noise and promising high gain without being saturated, to get rid of DC offset voltage related limitations [Raz97]. The rejection of the noise from the image band can be done in the digital domain, using the quadrature IF signals of the I/Q receiver. Firstly, the design details of the LNA are discussed. Secondly, the design and simulation results of the down-conversion mixers are given. Thirdly, the design of passive structures, power divider and branch-line coupler, in the I/Q receiver channel are summarized. Finally, the designed frequency doubler circuit with its driver amplifier is presented. This section is based on my letter [TAD+22a] published during my PhD study.

3.1.1 Low Noise Amplifier

Figure 3.1 shows the performance comparison of cascode and common-emitter amplifier topologies at 240 GHz. The figure presents the maximum available gain and minimum achievable noise figure of these topologies versus the collector current for the minimum-size transistor. Although the common-emitter topology has a better minimum achievable noise figure, it has a very low maximum available gain. Additionally, its real gain is likely to be even lower due to the quality factor values of inductors, capacitors, or transmission lines at this frequency range, which may not be sufficient to suppress noise from later stages. As a result, the cascode amplifier topology was preferred over the common-emitter topology. Considering Figure 3.1, the DC operating points of the first and second stages were set to about 1.3 mA and 2 mA, respectively,



(a) Maximum available gain

(b) Minimum noise figure.

Figure 3.1: Comparison of the simulation results of the cascode and common-emitter topologies.

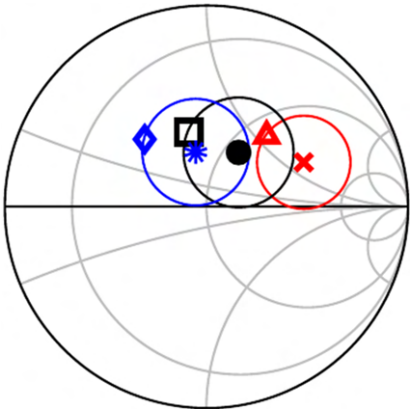


Figure 3.2: (a) Simulated maximum available gain and minimum noise figure at 240 GHz versus collector current. (b) Simulated Z_{in}^{*}, S_{opt} and related noise figure circles of about 0.37 dB of the first cascode core at 240 GHz for different N_E (blue-diamond:Z_{in}^{*} of N_E=3,blue-star:S_{opt} of N_E=3,black-square:Z_{in}^{*} of N_E=2,black-point:S_{opt} of N_E=2,red-triangle:Z_{in}^{*} of N_E=1,red-cross:S_{opt} of N_E=1).

for the unit-size transistor. Figure 3.2 displays the simulated conjugated input impedance Z_{in}^{*}, optimum noise source impedance S_{opt}, and related noise figure circles of approximately 0.37 dB of the first cascode core at 240 GHz for different number of emitters. As shown in Figure 3.2, this allows for simultaneous noise and power impedance matching, resulting in an increase of about 0.37

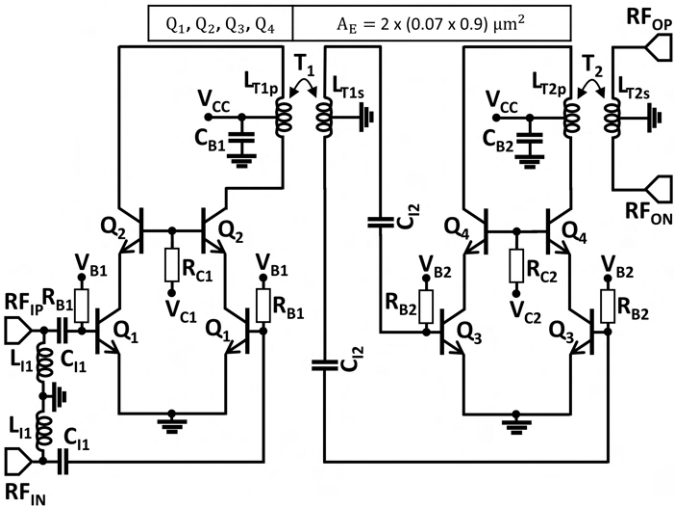


Figure 3.3: Circuit schematic of the designed low noise amplifier.

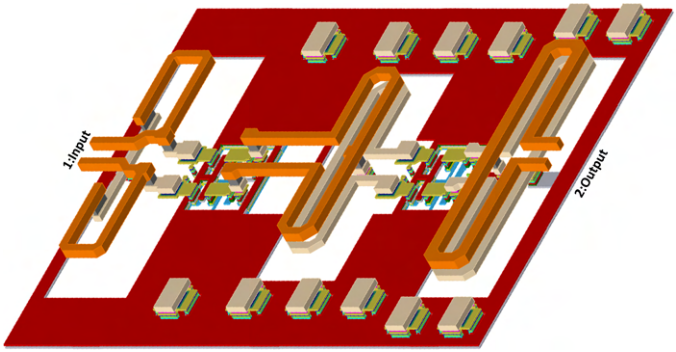


Figure 3.4: 3D layout view taken from EM simulation setup of the low noise amplifier.

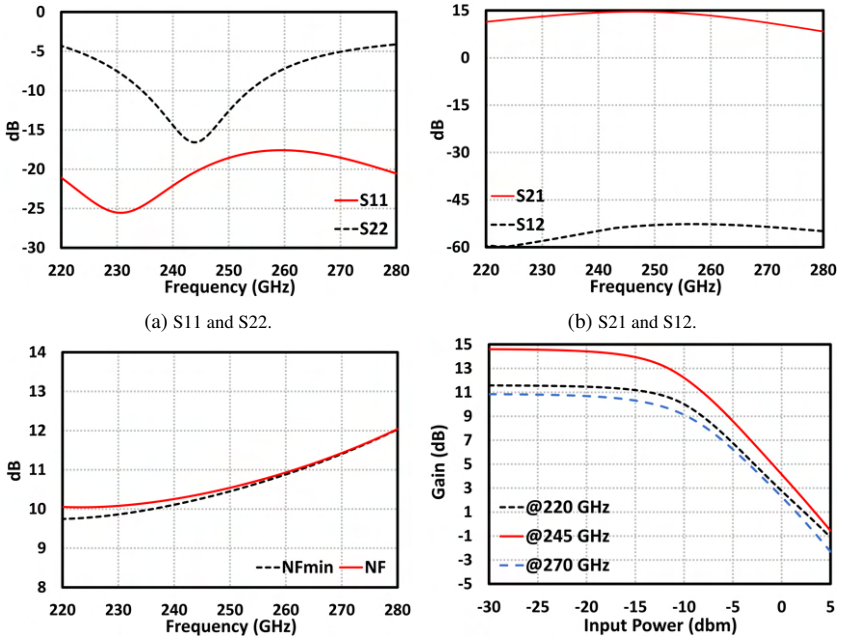
dB in the noise figure, without using an emitter degeneration inductor which would reduce the maximum available gain.

The circuit schematic of the designed fully-differential two-stage LNA is shown in Figure 3.3. The transistors were sized by compromising between the current

consumption, power linearity, and lower impedance transformation ratio. The input of the LNA was matched to the differential 100Ω using the shunt inductors L_{I1} and series capacitors C_{I1}. The interstage stage, consisting of the inductor based transformer T_1 and series capacitors C_{I2}, was implemented to match the output of the first stage to the input of the second stage. The output of the LNA was matched to the differential 100Ω by the inductor based transformer T_2. The bypass capacitors C_{B1} and C_{B2} were placed on the supply plane to provide AC ground and filter the noise coming from the supply source. Figure 3.4 shows the 3D-view of the full-layout of the designed LNA occupying an area of 0.02 mm^2 (0.167 mm × 0.122 mm). The circuit draws a DC current of 14.7 mA from a single supply voltage of 3.3V in quiescent operation. Figure 3.5(a) and Figure 3.5(b) present the simulated s-parameter results of the LNA. The input return loss is higher than 17.5 dB across from 220 GHz to 280 GHz. The circuit exhibits an output return loss of more than approximately 5 dB over a frequency range of 220 GHz to 270 GHz. The peak value of the small-signal gain is about 14.6 dB at 246 GHz, and its 3-dB frequency bandwidth is 47 GHz. The simulated noise figure and minimum noise figure results are shown in Figure 3.5(c). The simulated noise figure is better than 12 dB across from 220 GHz to 280 GHz, and it is 10.4 dB at 245 GHz. Figure 3.5(d) presents the power linearity simulation results of the circuit. The circuit achieves an input referred 1-dB compression point of -13.5 dBm at 245 GHz where it exhibits the peak-gain.

3.1.2 Down-conversion Mixer

In this design, the fundamental mixer configuration was chosen over sub-harmonic mixing because of its higher down-conversion power gain and lower noise figure performance [OHP12]. The Gilbert cell was used because it offers common-mode noise immunity and excellent port-to-port isolation. The mixer circuit schematic, consisting of a transconductance pair, a switching quad, load resistors, and emitter-follower buffer, is shown in Figure 3.6. As previously mentioned, the IF frequency of radar receivers is limited to a few tens of MHz, so a resistive load was used instead of an inductive load. However, this intro-



(a) S11 and S22.

(b) S21 and S12.

(c) Noise figure.

(d) Power linearity.

Figure 3.5: EM-assisted simulation results of the low noise amplifier.

duces a trade-off between power conversion gain and linearity due to the DC voltage drop across the load resistors. The transconductance stage was biased at the point that maximizes its f_T to provide a high gain from the transconductance stage. The transistor size of the switching quad was chosen to be as small as possible to minimize the power requirement of the LO. The RF input of the mixer was matched to the differential 100Ω using the shunt-inductors L_{R1} and series capacitors C_{R1}. The series capacitors also provide DC blocking for the base bias voltage V_{B1} of the transconductance stage, is applied through the high value resistors R_{B1} that behaves as an open circuit for the RF-signals. The LO input matching was performed by the impedance matching network consisting of the series capacitors C_{L1} and shunt inductors L_{L1}. The IF outputs were followed by the differential emitter-followed buffer to be able to drive subsequent stages and

Q_1	$A_E = 2 \times (0.07 \times 0.9)\ \mu m^2$
Q_2	$A_E = 1 \times (0.07 \times 0.9)\ \mu m^2$
Q_3	$A_E = 10 \times (0.07 \times 0.9)\ \mu m^2$

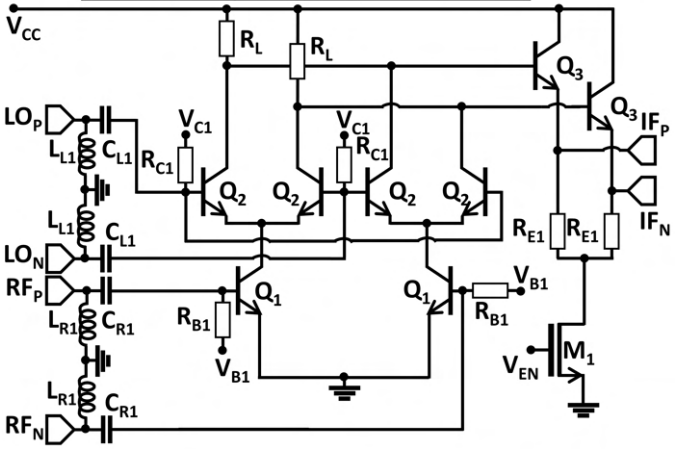
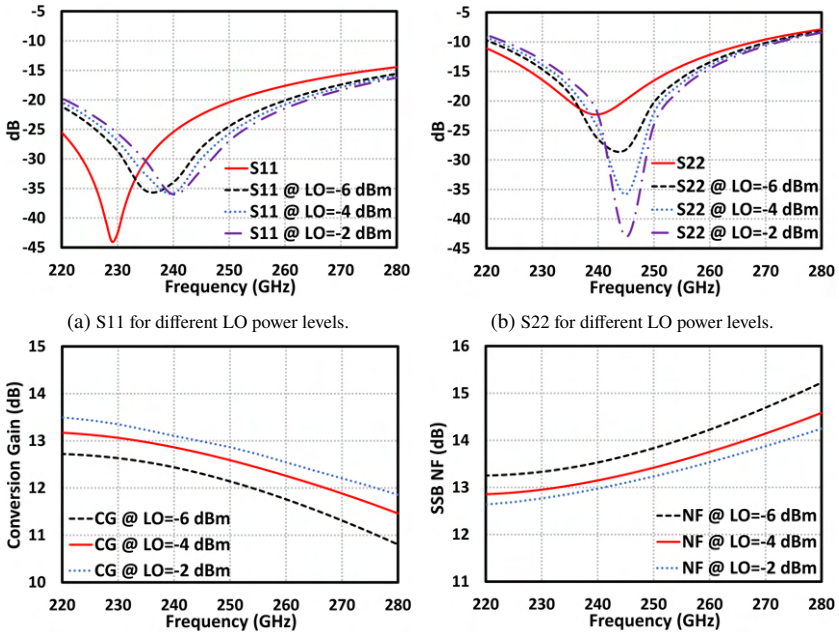


Figure 3.6: Circuit schematic of the designed down-conversion mixer.

Figure 3.7: 3D layout view taken from EM simulation setup of the down-conversion mixer.

were matched to differential 500Ω. An N-channel metal-oxide semiconductor



(a) S11 for different LO power levels.

(b) S22 for different LO power levels.

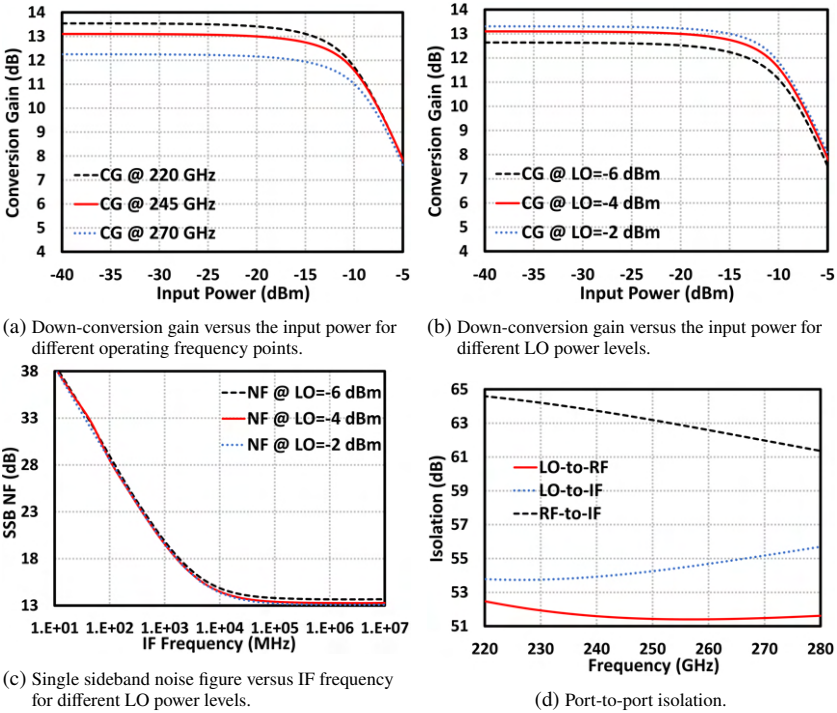
(c) Down-conversion power gain for different LO power levels.

(d) Single sideband noise figure for different LO power levels.

Figure 3.8: EM-assisted simulation results of the down-conversion mixer.

(NMOS) transistor based switch was placed at the tail of the emitter-follower buffer circuit to enable/disable its operation.

The 3D view of the designed down-conversion mixer is presented in Figure 3.7. The overall area of the circuit is about 0.01 mm^2 (0.106 mm $\times$ 0.1 mm). The EM simulations of the full-layout of the designed mixer was performed in ADS Momentum. And, the circuit simulations of the mixer were done using this EM-model. The designed mixer consumes a quiescent DC current of 9.75 mA at a supply voltage of 3.3V. Figure 3.8a shows the simulated s-parameter results of the RF-input of the mixer with respect to different LO power levels. It is better than -15 dB across from 220 GHz to 275 GHz. The simulated return loss results of the LO-input port for different LO power levels are presented in Figure



(a) Down-conversion gain versus the input power for different operating frequency points.

(b) Down-conversion gain versus the input power for different LO power levels.

(c) Single sideband noise figure versus IF frequency for different LO power levels.

(d) Port-to-port isolation.

Figure 3.9: EM-assisted simulation results of the down-conversion mixer.

3.8b. The return loss of the LO-port is approximately better than 10 dB over a frequency range of 222 GHz to 269 GHz for LO power levels up to -2 dBm. The IF frequency was set to be 1 MHz during the circuit simulations of the designed mixer. As shown in Figure 3.8c, the down-conversion mixer achieves a power conversion gain of about 13 dB at 245 GHz, and it is higher than 11.9 dB along from 220 GHz to 270 GHz for an LO power of -2 dBm. Figure 3.8d presents the single sideband (SSB) noise figure versus RF frequency. The circuit exhibits an SSB noise figure of less than 14 dB over a frequency range of 220 GHz to 273 GHz for an LO power level of -2 dBm. The power linearity performance of the designed mixer is depicted in Figure 3.9a and Figure 3.9b. The input referred 1-dB compression point is about -12 dBm, -11.5 dBm, and -10.5 dBm,

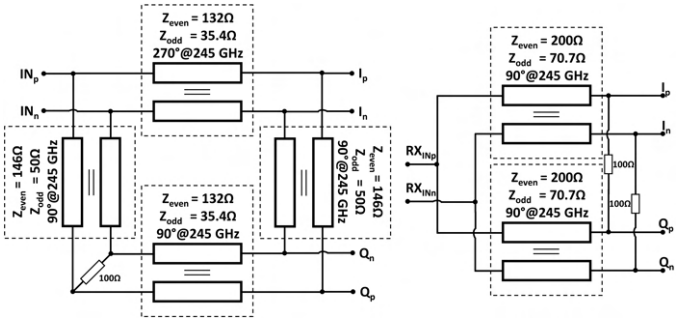


Figure 3.10: Circuit schematics of the designed branch-line coupler (left) and power divider (right).

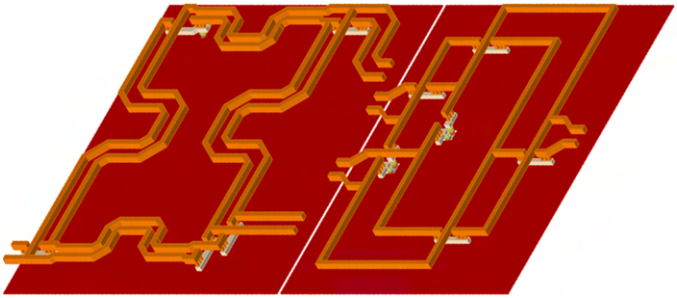
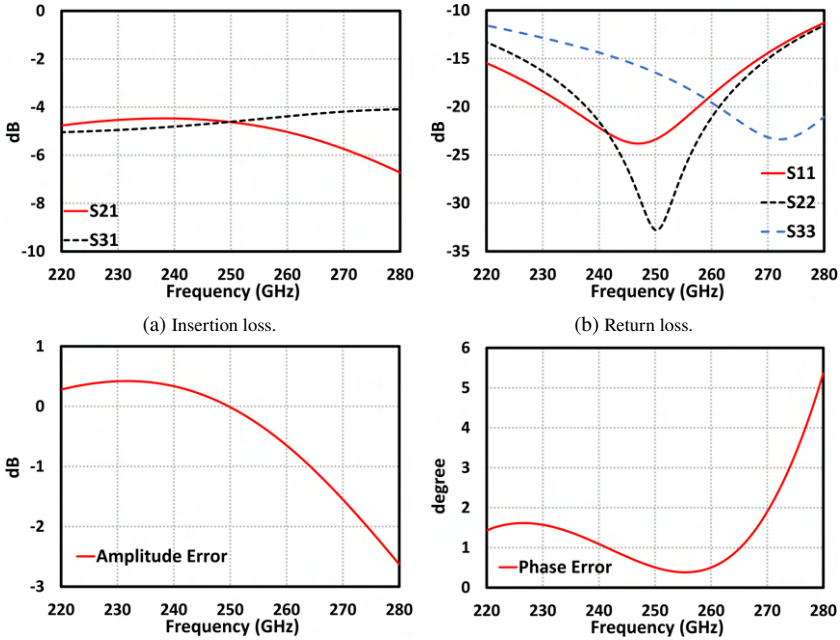


Figure 3.11: 3D layout view taken from EM simulation setups of the branch-line coupler (left) and power divider (right).

respectively, for the RF frequency points of 220 GHz, 245 GHz, and 270 GHz. Figure 3.9c shows the SSB noise figure of the mixer versus IF frequency points, with respect to different LO power levels. The 1/f noise corner frequency was found to be around 20 kHz. As presented in Figure 3.9d, the circuit achieves a port-to-port isolation of more than 51 dB over a frequency range from 220 GHz to 280 GHz.



(a) Insertion loss.

(b) Return loss.

(c) Amplitude error.

(d) Phase Error.

Figure 3.12: EM-assisted simulation results of the branch-line coupler.

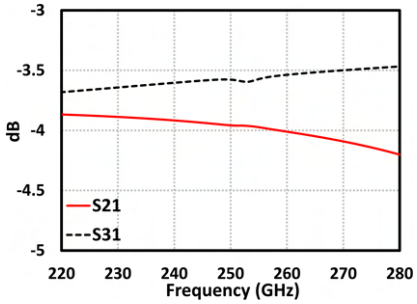
3.1.3 Branch-line Coupler and Power Divider

A branch-line coupler was designed to produce quadrature signals for the I/Q receiver. And, a Wilkinson power divider was implemented to split the RF signal into I- and –Q channels with equal phase and amplitude. The circuit schematics of the designed branch-line coupler and Wilkinson power divider are presented in Figure 3.10. The branch-line coupler was implemented using four quarter-wavelength differential transmission lines. The horizontal and vertical differential transmission lines were implemented using parallel coupled microstrip lines. The even-mode and odd-mode characteristic impedances of the horizontal transmission lines are 132Ω and 35.4Ω, respectively. The vertical transmission lines have even-mode and odd-mode characteristic impedances of

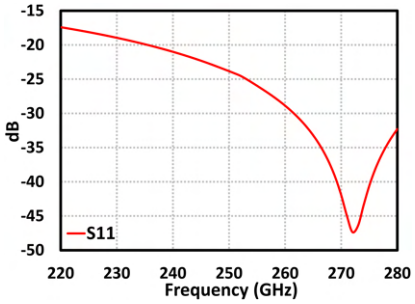
146Ω and 50Ω, respectively. The Wilkinson power divider was implemented using two differential-quarter wavelength transmission lines based on parallel coupled microstrip lines with even-mode and odd-mode characteristic impedance values of 200Ω and 70.7Ω, respectively. Figure 3.11 shows the 3D views of the full-layouts of the designed branch-line coupler and Wilkinson power divider. The S-parameter simulations were performed using the EM-models of the layouts. As seen in Figure 3.12a, the branch-line coupler achieves an insertion loss of less than 6 dB over a frequency range of 220 GHz to 270 GHz. Figure 3.12b shows the return loss values of the branch-line coupler. It exhibits a return loss value of better than approximately 12 dB across from 220 GHz to 270 GHz. As depicted in Figure 3.12c, the amplitude imbalance of the designed branch-line coupler is less than 1.6° over the frequency range of interest. Figure 3.12d presents the phase error between the outputs of the branch-line coupler. The simulated phase error is less than about 2° along from 220 GHz to 270 GHz. The implemented branch-line coupler occupies an area of 0.025 mm^2 (0.143 mm × 0.174 mm). The simulated insertion loss results of the power divider is given in Figure 3.13a. It achieves an insertion loss of less than 4.1 dB over the frequency range of interest. Figure 3.13b shows the return loss of the input of the power divider. The input return loss was found to be better than 17.5 dB across from 220 GHz to 280 GHz. The output return loss results of the designed Wilkinson power divider are presented in Figure 3.13c. It is better than 14 dB over the frequency range of interest. Figure 3.13d shows the isolation between the output ports of the power divider. The maximum value of the isolation was simulated to be almost 54 dB at 242 GHz, and it is better than approximately 22 dB along from 220 GHz to 280 GHz. The overall area of the implemented Wilkinson power divider is 0.023 mm^2 (0.119 mm × 0.197 mm).

3.1.4 Frequency Doubler with Driver Amplifier

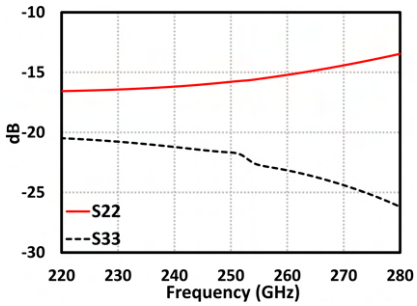
There are two common configurations to perform the frequency doubling: push-push topology [AYK+20] to combine the second harmonic components of the collector (or emitter) current of the balanced pair, and Gilbert-cell [BMAP20] to perform the self-mixing of the signal. The Gilbert-cell based frequency doubler



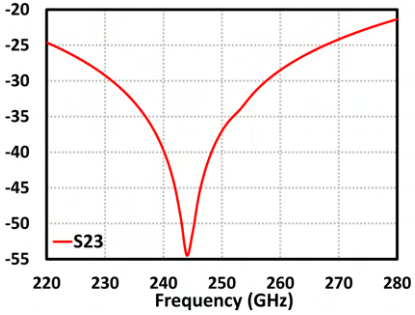
(a) Insertion loss.



(b) Return loss of the input port.



(c) Return loss of the output ports.



(d) Isolation.

Figure 3.13: EM-assisted simulation results of the power divider.

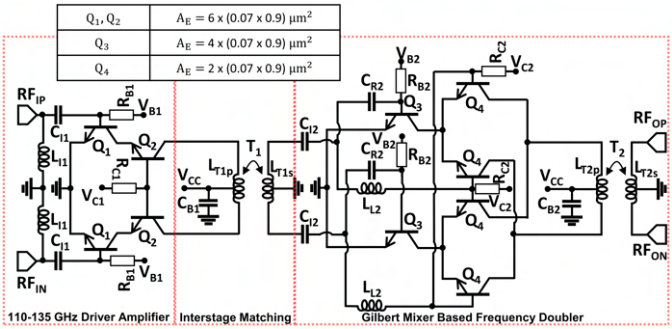


Figure 3.14: Circuit schematic of the designed frequency doubler with its driver amplifier.

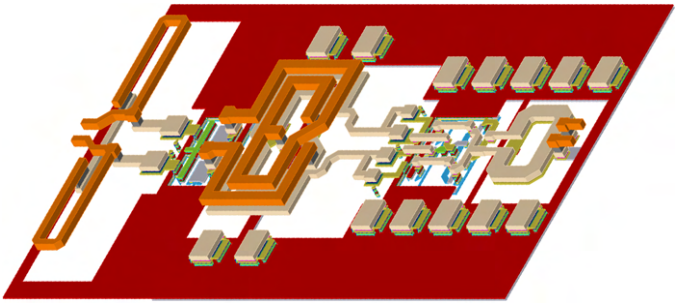
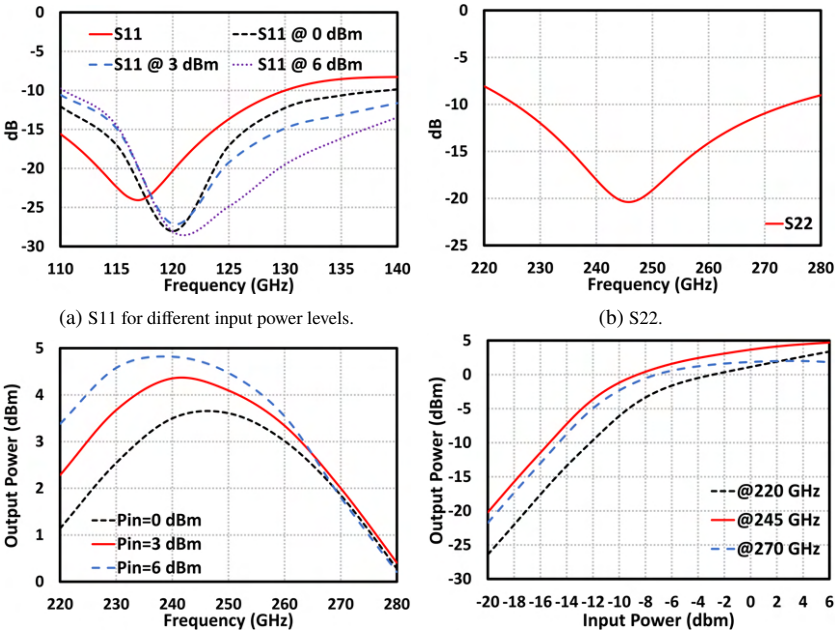


Figure 3.15: 3D layout view taken from EM simulation setup of the frequency doubler with its driver amplifier.

topology was preferred since it can be built as fully differential, and so that it allows higher voltage swing at the output. In addition, it provides common-mode noise immunity and excellent port-to-port isolation. Figure 3.14 presents the circuit schematic of the designed Gilbert-cell based frequency doubler and its driver amplifier.

The conversion-gain performance of the Gilbert-based frequency doubler strongly depends on the phase and amplitude ratio of the input signals of the transconductance pair and switching quad. In [FSF+10], a mathematical explanation is given for the need of a phase difference of 90° to acquire maximal conversion gain. For a similar SiGe process, it is reported that the power of the input signal of the switching quad should be larger about 5 dB than the input signal of the transconductance pair, using plot contours based on large-signal simulations [BMAP20]. There is a tendency to introduce 90° phase difference by either a transmission line [BMAP20, FSF+10] or a hybrid quadrature coupler [WCAW17], although they are not capable to provide optimum amplitude ratio and occupying large area. In this work, the Gilbert topology was modified by integrating a compact LC-circuit (L_{L2} and C_{R2}) into the cell to introduce required phase difference and amplitude ratio, as depicted in Figure 3.14. The transistors of the Gilbert-cell was biased at a base-emitter voltage value giving highest f_T, and scaled to provide sufficient power to drive the LO-ports of the down-conversion mixer in the receiver channel. The transistors of



(a) S11 for different input power levels.

(b) S22.

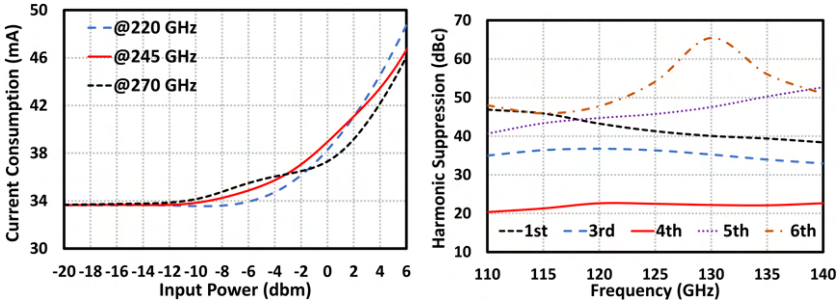
(c) Output power versus frequency.

(d) Output power versus input power.

Figure 3.16: EM-assisted simulation results of the frequency doubler with its driver amplifier.

the driver amplifier which is based on the fully-differential single-stage cascode topology was biased at maximum f_{max}, and their size was determined considering the input power requirement of the designed frequency doubler circuit. The input port of the whole circuit was matched to differential 100Ω using the shunt-inductors L_{I1} and series-capacitors C_{I1}. The inductor-based transformer T_1 was employed to perform the matching between the driver amplifier and frequency doubler circuit. The output of the frequency doubler circuit was matched to differential 100Ω using the inductor-based transformer T_2. The bypass capacitors C_{B1} and C_{B2} were placed on the supply-line to provide common-mode AC ground and filter the undesired signals coming from the supply source.

The circuit draws a quiescent DC current of 33.8 mA from a single supply voltage of 3.3V. Figure 3.15 shows the 3D view of the full-layout of the circuit



(a) Current consumption versus input power.

(b) Harmonic suppression levels.

Figure 3.17: EM-assisted simulation results of the frequency doubler with its driver amplifier.

consisting of the designed frequency doubler and driver amplifier. The circuit simulations were performed using the EM-model of the full-layout. The circuit occupies an area of 0.032 mm^2 (0.217 mm $\times$ 0.146 mm) in total. The input matching performance of the circuit is presented for various input power levels in Figure 3.16a. The input return loss is better than 10 dB along from 110 GHz to 140 GHz. Figure 3.16b shows the simulated S22 of the circuit. The simulated S22 is less than approximately -8 dB across from 220 GHz to 280 GHz. The simulated output power versus the operating frequency is presented in Figure 3.16c for the input power values from 0 dBm to 6 dBm with a step size of 3 dB. The 3-dB frequency bandwidth is more than 50 GHz for the output power levels. The circuit achieves a peak output power of about 4.3 dBm at 242 GHz for an input power of -3 dBm. Figure 3.16d shows the simulated output power versus the input power for the operating frequency points from 220 GHz to 270 GHz with a step size of 25 GHz. The output power was found to be more than 0 dBm for an input power of larger than -2 dBm over the 3-dB frequency bandwidth. The total current consumption versus input power levels from -20 dBm to 6 dBm is presented in Figure 3.17a. Figure 3.17b shows the simulated harmonic suppression levels versus the input frequency for an input power of 3 dBm. The circuit exhibits a harmonic rejection performance of better than 20 dB over an output frequency range of 220 GHz to 280 GHz.

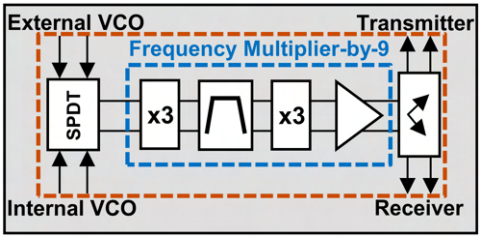


Figure 3.18: Block diagram of the designed common chain.

3.2 Common Chain

The circuit block diagram of the designed common chain is shown in Figure 3.18. It consists of an SPDT switch, a frequency multiplier-by-9 chain, and a Wilkinson power divider. First, the design and implementation of the SPDT switch are discussed. Then, the design, implementation, and simulation results of the frequency multiplier-by-9 chain, consisting of two frequency triplers, a Chebyshev-distribution based BPF, and a buffer amplifier, are given. Finally, the designed Wilkinson power divider is presented. This section is based on my letter [TAD+22b] published during my PhD study.

3.2.1 SPDT Switch

The NMOS transistor based shunt-series SPDT switch topology was employed to achieve good insertion loss and isolation while keeping the DC power consumption as minimum as possible. The circuit schematic of the designed SPDT switch is shown in Figure 3.19. In the switching core, NMOS transistors were preferred to P-channel metal-oxide semiconductor (PMOS) transistors as they promise lower on-state resistance and hence lower insertion loss. The size of the low-voltage (LV) NMOS transistors N_2 were determined considering the trade-off between the insertion loss and isolation of the SPDT switch. An isolated body technique was employed to reduce the losses due to the substrate conductivity [LZ10]. The gate terminals of all transistors were biased through

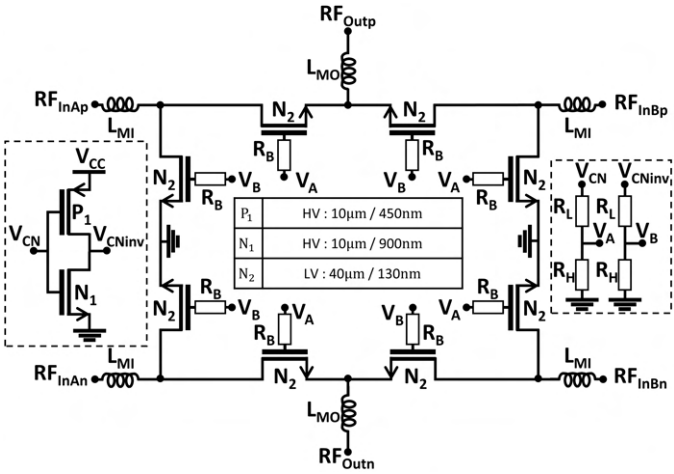


Figure 3.19: Circuit schematic of the designed SPDT switch.

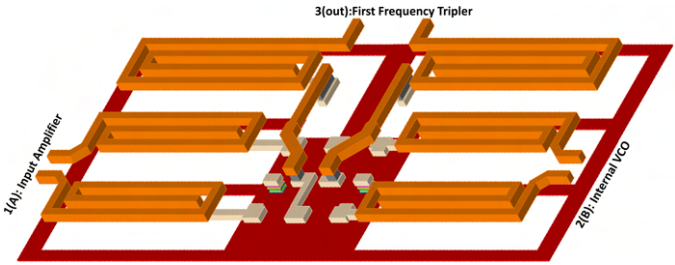
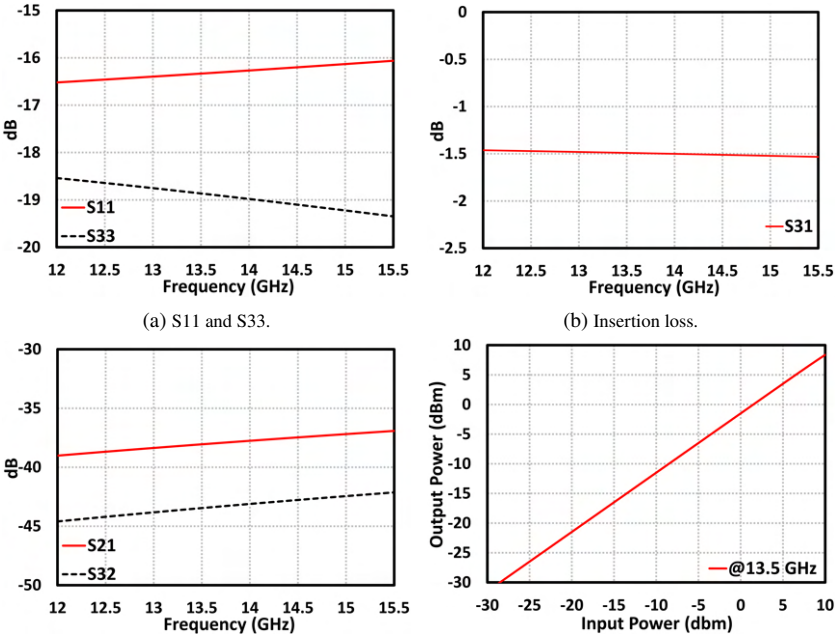


Figure 3.20: 3D layout view taken from EM simulation setup of the SPDT switch.

high-value resistors R_B providing open-circuit for AC signals. A CMOS inverter circuit (P_1, N_1) were implemented to enable the SPDT switch circuit to be operated using only a single digital control signal. A resistor voltage divider (R_L, R_H) was employed to reduce the digital control voltage of 3.3V to less than the breakdown voltage of the LV-NMOS transistors used in the switching core. The input and output ports of the SPDT switch was matched to differential 100Ω using the series inductors (L_{MI}, L_{MO}) which are cancelling the reactive



(a) S11 and S33.

(b) Insertion loss.

(c) Isolation.

(d) Power linearity.

Figure 3.21: EM-assisted simulation results of the SPDT switch.

impedance part due to the parasitic drain-to-source capacitances of the series transistors.

The 3D view of the full layout of the SPDT switch is presented in Figure 3.20. The circuit occupies an area of 0.017 mm^2 (0.19 mm $\times$ 0.089 mm). The EM simulation of the full layout was performed by an EM simulator, and the circuit simulations of the SPDT was done using the EM-model. The circuit draws a DC power of 0.169 mW in total. The simulated input S-parameters is shown in Figure 3.21a. They remain below -16 dB for a frequency range of 12 GHz to 15.5 GHz. Figure 3.21b presents the insertion loss of the SPDT switch. It is around 1.5 dB over the frequency range of interest. The simulated port-to-port isolation results of the circuit are given in Figure 3.21c. The switch circuit provides better than 37 dB isolation throughout the operating frequency range.

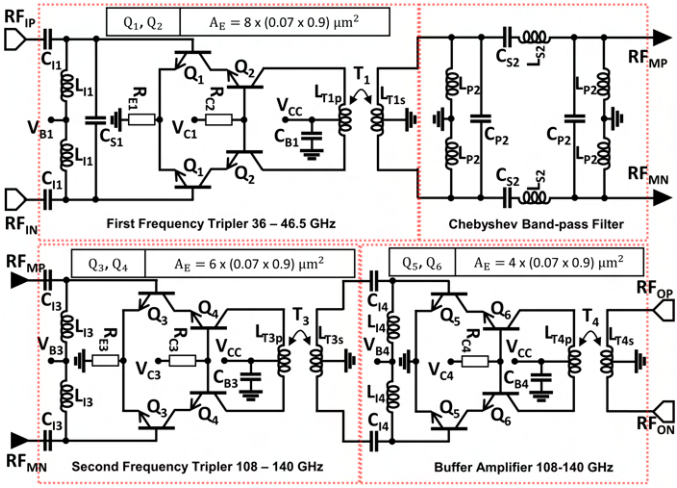


Figure 3.22: Circuit schematic of the designed frequency multiplier-by-9 chain.

The output power versus input power at 13.5 GHz is depicted in Figure 3.21d. The circuit achieves an excellent power linearity for an input power range of -30 dBm to 10 dBm.

3.2.2 Frequency Multiplier-by-9 Chain

The circuit block diagram of the designed frequency multiplier-by-9 chain is depicted in Figure 3.22. It consists of two frequency triplers, a Chebyshev BPF, and a buffer amplifier. It is common approach to utilize the nonlinearity of an amplifier to multiply the frequency by three. As reported in [WCH12], there are two harmonic-rich regions: biasing at turn-on point and overdriving to operate in the saturated regime. It is a power efficient approach to bias a transistor at its turn-on point to enhance the nonlinearity [WCH12]. However, the second approach, overdriving into the saturation, promises higher output power [WCH12], since odd-harmonics are enhanced because of the square-wave signal the output. Furthermore, the first approach is based on the conduction angle which is the function of the input power and base bias of the transistors. Therefore, it is

much more dependent on the process and temperature variations, and so that it comes with a need of more accurate large-signal models of the transistors in the millimeter-wave region [RCE19]. Considering the aforementioned advantages and disadvantages of the topologies, the cascode pair operating in the saturated regime were cascaded to perform the multiplication of the frequency by nine in this work. The common-mode degeneration resistors (R_{E1} and R_{E3}) were used to stabilize the DC current over the input power in order to push the circuits operating into the saturated regime with a lower voltage swing. Because, the common-emitter differential pair transistors (Q_1 and Q_3) start to draw higher DC collector current as the voltage swing at their base nodes increases. However, the common-mode degeneration resistors also cause an increase in the DC voltage levels of the emitter nodes, limiting the current and voltage swing at the output. This technique provides a square-wave signal at the output for a lower input power range, thus increasing the power levels of odd-harmonics. Furthermore, the fundamental output power is reduced thanks to this early power saturation mechanism, resulting in a better fundamental harmonic rejection. The input impedance of the first frequency tripler was matched to differential 100Ω using the shunt inductor L_{I1}, shunt capacitor C_{S1} and series capacitors C_{I1}. The optimum number of the transistors was found to be 8 considering the insertion loss of the bandpass filter and the input power requirement of the second frequency tripler circuit. The inductor-based transformer of T_1 was implemented to match the output to differential 100Ω. The second frequency tripler was designed in the same way as the first frequency tripler, yet the transistor size was optimized to transmit sufficient power to saturate the buffer amplifier. The 3D layout views of the first and second frequency triplers taken from the EM simulation setup are presented in Figure 3.23 and Figure 3.24, respectively.

A 3rd-order Chebyshev BPF was placed between the triplers to suppress the undesired fundamental and harmonic signals produced by the first tripler. It is quite important to significantly suppress the undesired harmonics here. Because these unwanted harmonic signals between the first and second triplers might mix with the carried and other harmonic signals later if they were not rejected well and produce strong undesired harmonics falling into the frequency range of interest. The targeted input frequency range of the designed frequen-

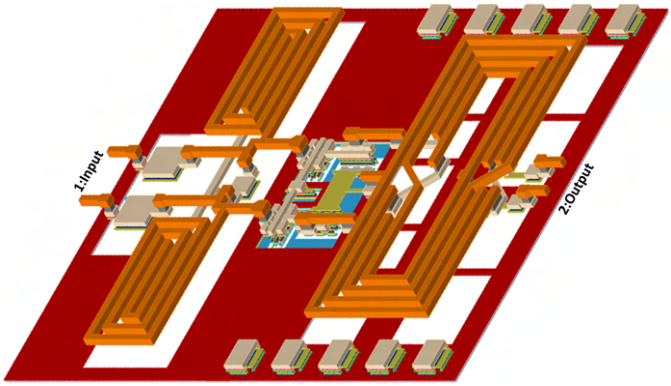


Figure 3.23: 3D layout view taken from EM simulation setup of the first frequency tripler.

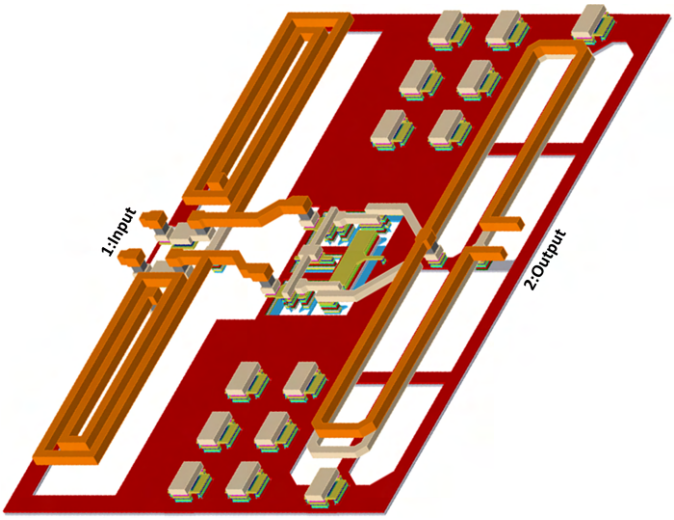


Figure 3.24: 3D layout view taken from EM simulation setup of the second frequency tripler.

cy multiplier-by-9 chain is from 12 GHz to 15 GHz. Therefore, the designed BPF, which was placed after the first tripler circuit, should pass signals over a frequency range 36 GHz to 45 GHz. The values of the MIM-capacitors provi-

ded by the PDK are considerably dependent on the process variation. For this reason, the pass-band was aimed to be from 32 GHz to 49 GHz in order to guarantee that it will always cover the frequency range of interest. The BPF was employed to suppress the fundamental and 5th harmonic signals produced by the first frequency tripler. The rejection ratio of the 1st or 2nd order BPF topologies are not sufficient to suppress the unwanted harmonic signals. The rejection ratio of the BPF topologies higher than 3rd-order is unrealistic in a silicon based process due to the signal leakage through the substrate. Therefore, it was decided to design a third-order BPF. Figure 3.25 shows the simulation results of various BPF topologies using ideal lumped components. As can be seen in Figure 3.25, 3rd-order Chebyshev and Elliptic BPF topologies provide the broadest input and output impedance matching. Elliptic BPFs require one more LC-resonator compared to Chebyshev BPF topologies. Accordingly, it was decided to employ a 3rd-order Chebyshev topology to implement the BPF. If the inductance value is higher than 600 pH, the self-resonance frequency of an inductor is less than the targeted operating frequency range of the BPF. For this reason, the Chebyshev BPF with the shunt-first LC network was chosen over the series-first network which is needing an inductance of 834 pH. The 3D view of the full layout of the designed Chebyshev BPF is presented in Figure 3.26. The simulated s-parameter results of the implemented filter is depicted in Figure 3.27.

A single-stage fully-differential cascode topology was utilized to amplify the 9th harmonic signal after the second frequency tripler. The buffer amplifier, whose circuit schematic is given in Figure 3.22, has a band-pass characteristic that suppresses unwanted harmonics outside the frequency range of interest. The input of the amplifier was matched to differential 100Ω using the shunt inductors L_{I4} and series capacitors C_{I4}. The base bias voltage of the transistors was set to obtain highest available f_{max}. The size of the transistors was chosen to be 4 considering the input power requirements of the transmitter and receiver channels and taking into account the insertion loss of the designed 120 GHz Wilkinson power divider splitting the output signal of the common chain into two output signals of equal power. The output matching was performed using the inductor-based transformer of T_4. A bypass capacitor array was placed on

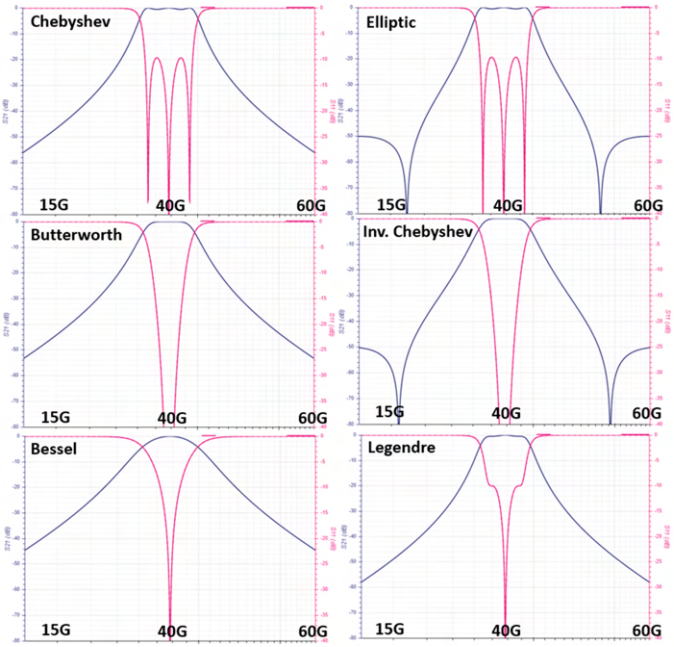


Figure 3.25: Simulation results of various BPF topologies using ideal lumped components.

the supply plane to provide AC ground and filter power supply noise. Figure 3.28 shows the 3D view of the full layout of the buffer amplifier.

The circuit simulations of the designed frequency multiplier-by-9 chain were done using the EM-models of each sub-block. The overall area of the frequency multiplier-by-9 chain is 0.089 mm^2 (0.47 mm $\times$ 0.19 mm). The circuit draws a quiescent DC current of 52.3 mA from a single supply voltage of 3.3V, and it consumes a DC current of 64 mA for an input power of 1 dBm. Figure 3.29a presents the simulated input return loss results of the chain. The input return loss was found to be better than approximately 10 dB over a frequency range of 12 GHz to 15.5 GHz for input power levels from -1 dBm to 3 dBm with a step size of 2 dB. As depicted in Figure 3.29b, the simulated S22 is less than about -3.5 dB over the frequency range of interest which is from 110 GHz to

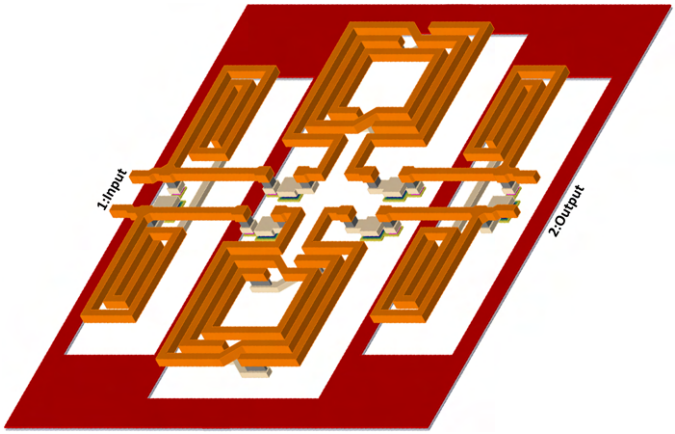


Figure 3.26: 3D layout view taken from EM simulation setup of the designed BPF.

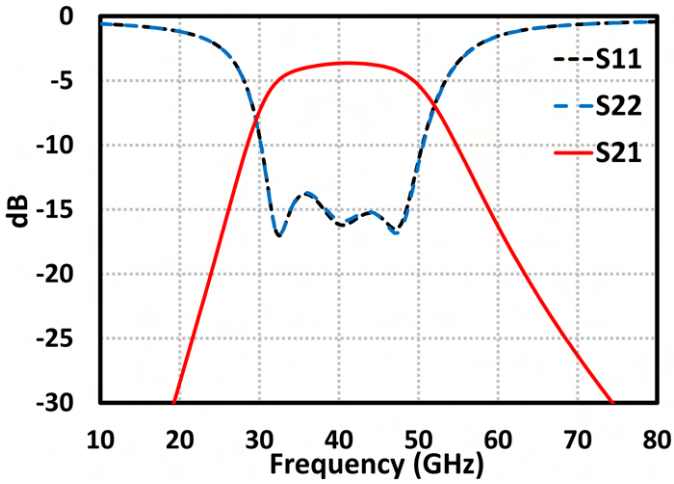


Figure 3.27: EM-assisted simulation result of the BPF.

135 GHz. Figure 3.29c presents the simulated output power versus the input power of the frequency multiplier-by-9 chain at the lower, center, and upper points of the frequency range of interest. The output power remains almost

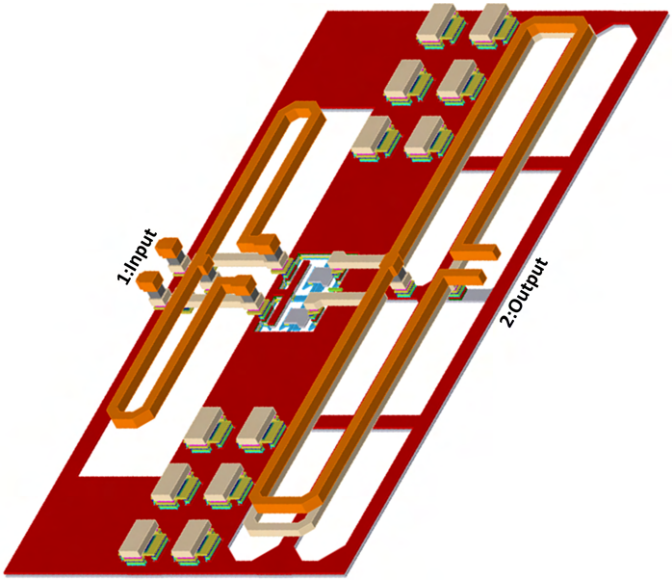
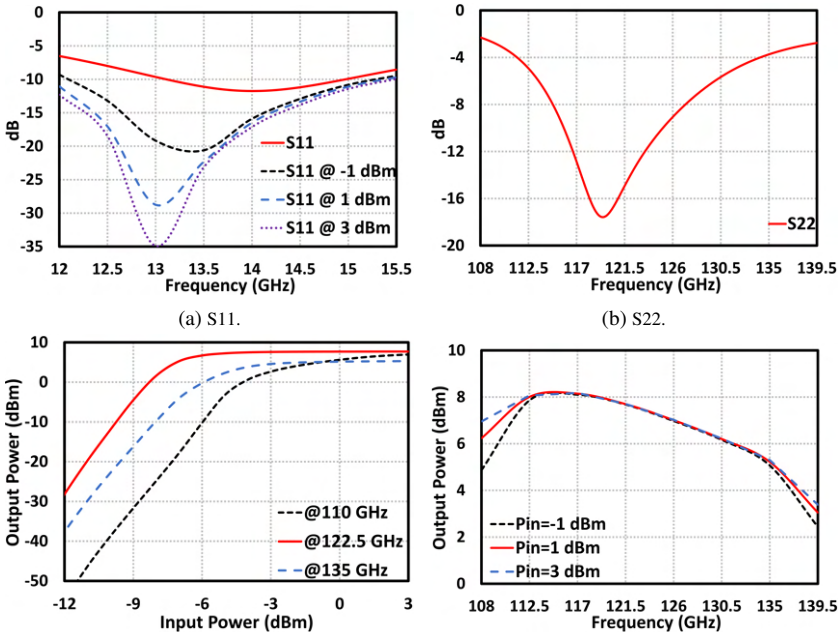


Figure 3.28: 3D layout view taken from EM simulation setup of the buffer amplifier.

constant for an input power of more than 1 dBm for all frequency points. The simulated output power across the output frequency range from 108 GHz to 139.5 GHz is shown in Figure 3.29d. The designed circuit has a peak output power of about 8.2 dBm at 115 GHz, and its 3-dB power bandwidth is about 26 GHz from 109 GHz to 135 GHz. Figure 3.30 presents the simulated harmonic suppression performance of the designed frequency multiplier-by-9 chain for an input power of 1 dBm. The circuit achieves a suppression of more than 30 dBc for all harmonics over the output frequency range of interest, which is corresponding to 12.2 GHz to 15 GHz for the input frequency range.

3.2.3 120-GHz Wilkinson Power Divider

As mentioned above, the output signal of the common-chain of the transceiver is split in half with equal power by an implemented Wilkinson power divider



(a) S11.

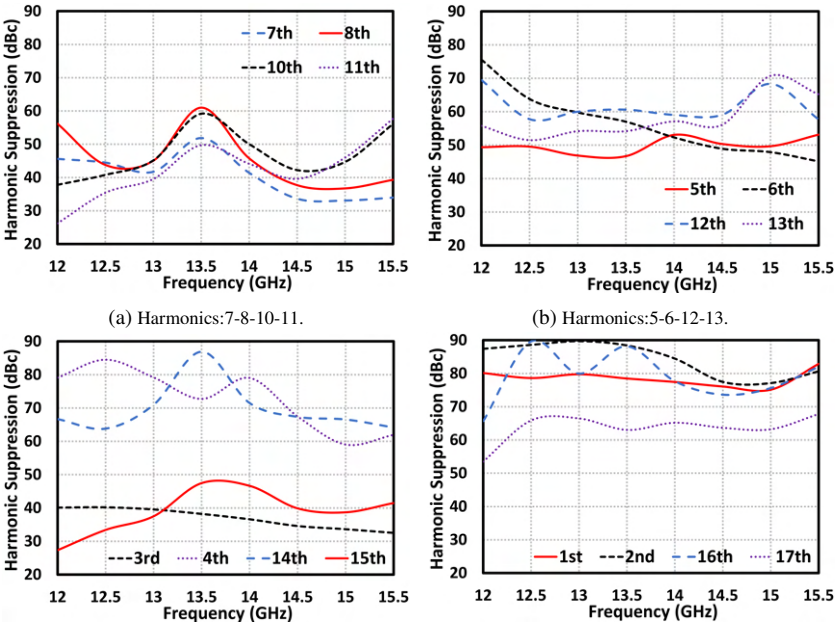
(b) S22.

(c) Output power versus input power.

(d) Output power versus output frequency.

Figure 3.29: EM-assisted simulation results of the frequency multiplier-by-9 chain.

operating across a frequency range from 110 GHz to 135 GHz. The circuit schematic and 3D EM model of the designed power divider are shown in Figure 3.31. The Wilkinson power divider was implemented using two differential quarter wavelength (at 122.5 GHz) transmission lines which are realized by the parallel coupled microstrip lines whose the even-mode and odd-mode characteristic impedances are 70.7Ω and 200Ω, respectively. The s-parameter simulations of the power divider were done using the EM-model presented in Figure 3.31. The implemented circuit occupies an overall area of 0.046 mm^2 (0.123 mm × 0.378 mm). Figure 3.32 presents the simulated s-parameter results of the implemented Wilkinson power divider. The input and output return loss levels are better than 20 dB over the frequency range of interest which is from 110 GHz to 135 GHz. The insertion loss varies between -3.8 dB and -3.7 dB over the frequency range



(a) Harmonics:7-8-10-11.

(b) Harmonics:5-6-12-13.

(c) Harmonics:3-4-14-15.

(d) Harmonics:1-2-16-17.

Figure 3.30: EM-assisted simulated harmonic suppression levels of the frequency multiplier-by-9 chain.

of interest. The maximum isolation value between the outputs of the circuit was found to be about 44 dB at 116 GHz, and it is higher than 20 dB over the entire operating frequency range.

3.3 Signal Generation Part

The circuit block diagram of the signal generation part is shown in Figure 3.33. The signal generation part consists of an IL-VCO, a frequency divider chain with a total division factor of 4, and buffer amplifiers. This section begins with a brief overview of the signal generation part. After the brief overview, first,

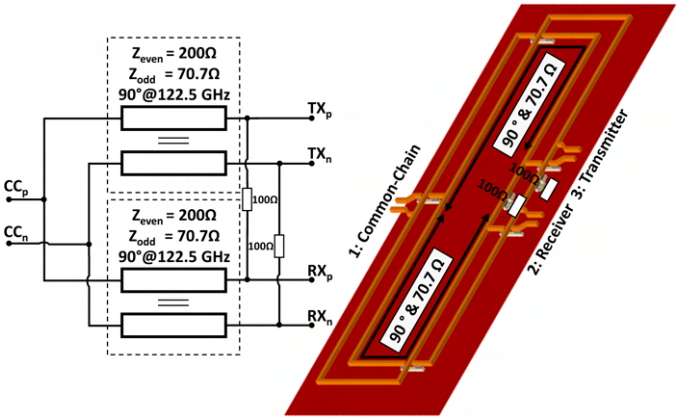
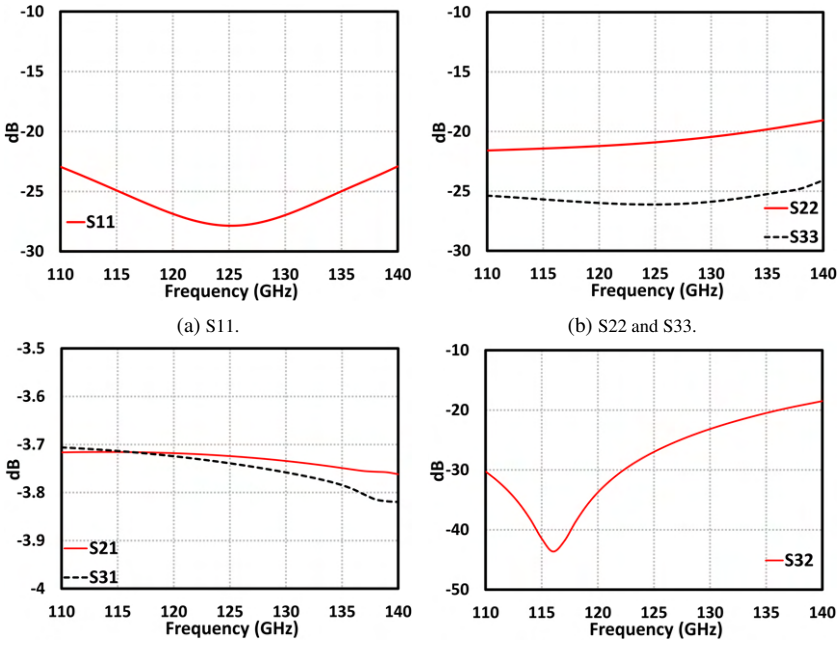


Figure 3.31: Circuit schematic and 3D layout view of the designed 120-GHz Wilkinson power divider.

the design of the frequency divider chain is given. Secondly, the design of the IL-VCO with its injection input amplifier is presented. The third sub-section gives information on the implementation of the buffer amplifiers. Finally, the simulation results of the signal generation part are presented.

In order to meet the frequency bandwidth requirement of 40 GHz within the scope of the project, and considering the total multiplication factor of 18, the fundamental frequency tuning range of the VCO must be higher than 2.25 GHz. On top of that, it was aimed for the VCO to have a tuning range of at least 3 GHz in order to cover frequency shifts due to PVT variations and a possible discrepancy between the simulation and measurement results due to inaccurate EM models of the passive structures. As seen in the block diagram of the LO signal generation part depicted in Figure-1, the VCO output is directly coupled to the buffer amplifiers and frequency divider chain. Therefore, the IL-VCO should provide sufficiently large output swing in order to drive the subsequent stages. Considering the requirement of providing a frequency tuning range of more than 3 GHz and the targeted center frequency of 245 GHz at the output of the transceiver circuit, the frequency tuning range of the designed LO signal



(a) S11.

(b) S22 and S33.

(c) S21 and S31.

(d) S32.

Figure 3.32: EM-assisted simulation results of the 120-GHz Wilkinson power divider.

generation part can be roughly determined to be from 12.5 GHz to 15.5 GHz. As mentioned earlier, the transceiver circuit has a total multiplication factor of 18 so that the output frequency is roughly between 225 GHz and 279 GHz when using the internal VCO. The injection signal is amplified by an amplifier, called the injection input amplifier, and electromagnetically coupled to the core of the designed VCO. The output of the VCO is connected to a frequency divider with a frequency division ratio of 4 and two buffer amplifiers: one amplifies the VCO signal for the common chain of the transceiver and the other one amplifies the VCO signal for the external VCO output port of the transceiver, which can be used to cascade the transceiver chips.

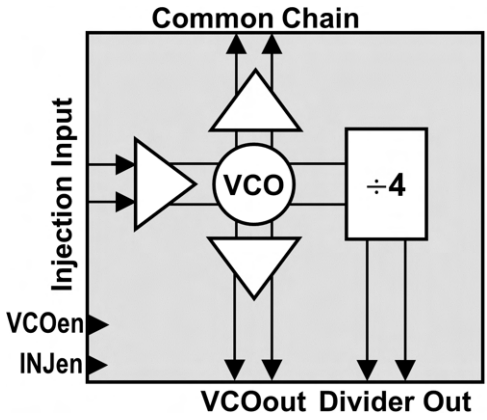


Figure 3.33: Circuit block diagram of the designed signal generation part.

3.3.1 Frequency Divider

Circuit topologies used in frequency divider circuits can be grouped under two main headings as static and dynamic frequency dividers. Although dynamic frequency divider topologies have very low power consumption, their maximum operating frequencies are lower than static frequency dividers [Tie04]. With the recent advancements in CMOS technology, dynamic frequency dividers which can operate up to 70 GHz have been demonstrated [TKCE22]. However, since the minimum CMOS length in the used semiconductor technology is limited to 130-nm [HBB+10], it is not feasible to design a high-speed dynamic frequency divider circuit in this work. On the other hand, static frequency divider circuits can operate for a much wider frequency range and the required input voltage swing is considerably lower than with dynamic frequency divider circuits. There are basically three types of circuit topologies employed in static frequency divider circuits: injection-lock frequency dividers [Tie04, RL99], Miller (or regenerative) frequency dividers [Har89, LR03], and emitter-coupled logic (ECL) based master-slave flip-flop frequency dividers [IIY94]. Although either injection-locked or Miller frequency divider circuits can provide the higher operating frequency among static frequency divider topologies with lower power consumption, they suffer from a narrow operating frequency band-

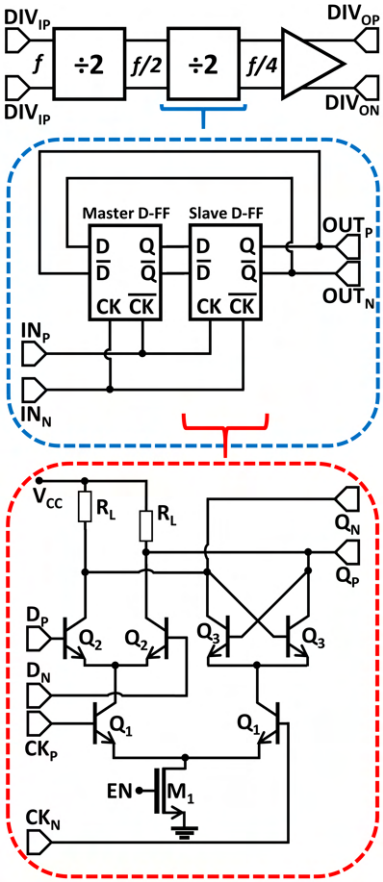


Figure 3.34: (Top) Circuit block diagram of the frequency divider chain-by-4 (middle) circuit block diagram of the frequency divider-by-2 (bottom) circuit schematic of the designed emitter-coupled logic based D-latch circuit.

width [LC08]. Therefore, they are not suitable for the purposes of this study since it is required to provide PVT robust operation over broad frequency bandwidth. Considering these points, it was decided to perform the frequency division operation by cascading two ECL-based D-latches in the master-slave configuration with a negative feedback in this study.

The block diagram of the designed frequency divider chain-by-4 consisting of two frequency divider-by-2 circuits connected in series and an ECL buffer circuit helping to impove the driving capability of the chain is shown in Figure 3.34. The circuit schematic of the one of the designed ECL based D-latch circuits is also shown in Figure 3.34. It consists of three different pairs: clock pair (Q1), data pair (Q2), and latch (or regenerative) pair (Q3). The maximum speed of the ECL based master-slave flip-flop frequency divider circuit is mainly determined by the propagation-delay in the data path [IIY94]. Therefore, the transistor size of the data and regenerative pairs should be minimized to keep the total parasitic capacitance as low as possible [IIY94]. The clock pair transistors should be able to operate two times faster than the transistors in either the data or regenerative pairs [IIY94]. However, the equivalent resistance connected to the collector nodes of these clock pair transistors are relatively very small. Therefore, the parasitics capacitances of the clock pair transistors do not introduce a significant propagation delay [IIY94]. In this study, the f_T of the SiGe HBT is about 300 GHz which already far above the VCO frequency, and therefore, the frequency divider circuits were optimized for lower power consumption. The ECL-based D-latch circuit has two different operating modes: sense mode and latch mode. If the clock signal is high, the data pair is turned on and amplifies the signal at the data input, and the output tracks the data input. Therefore, this operating mode is called sense mode. Since the clock signal is low in latch mode, latch pair is turned on. Therefore, the outputs continue to hold the data of the previous state.

While building the layout of the frequency divider-by-2 circuit, the fully difenential symmetry is provided for all pairs (clock, data, and latch). Especially in order to keep the equivalent parasitic capacitance in the data path as low as

possible, the widths of the lines connected to this path are made in the narrowest way to provide electromigration rules. The self-resonance frequency of this stage is 17 GHz, this frequency is especially set to be close to the operating frequency of the VCO, thereby relaxing the input voltage swing requirements at the input of the first frequency divider-by-2 circuit in the chain.

3.3.2 Injection-locked Voltage-controlled Oscillator

As a result of recent improvements in the optimization of monolithic inductors in semiconductor technologies, LC-oscillator topologies have become preferred over other oscillator configurations as they exhibit better phase noise performance at high frequencies. There are two types of LC-oscillator configurations highly preferred in high frequency oscillator design: cross-coupled and Colpitts. As compared and explained in [QPT+19, MMKN16, ZKF05], the Colpitts oscillator topology exhibits better phase noise performance than the cross-coupled VCO topology. The oscillation frequency of VCOs, especially those with high gain (K_{VCO}) is quite sensitive to noise coming from external sources such as supply noise and substrate noise. Therefore, a differential common-collector Colpitts VCO topology shown in Figure 3.35 was employed to reject common-mode noise such as supply noise and substrate noise. In addition, a differential Colpitts VCO provides a 3 dB improvement in phase noise performance compared to a single-ended design [Raz98].

According to [HL98], the width of the current pulses to the tank circuit should be minimized to reduce the impulse sensitivity, thus reducing the phase variation of the oscillation signal. Therefore, the bias current of the transistors Q_3 was chosen to operate in a highly nonlinear region, using the harmonic balance analysis to find the optimum bias current giving the best phase noise performance. The capacitive voltage divider (C_{B2} and C_{B2}) was implemented between the base and emitter nodes of the transistors. As explained in [HL98], the conduction-angle of the transistors, hence the effective impulse sensitivity function, depends on the capacitive division ratio. The capacitive division ratio of about four was chosen to minimize the phase noise, and this is one of the

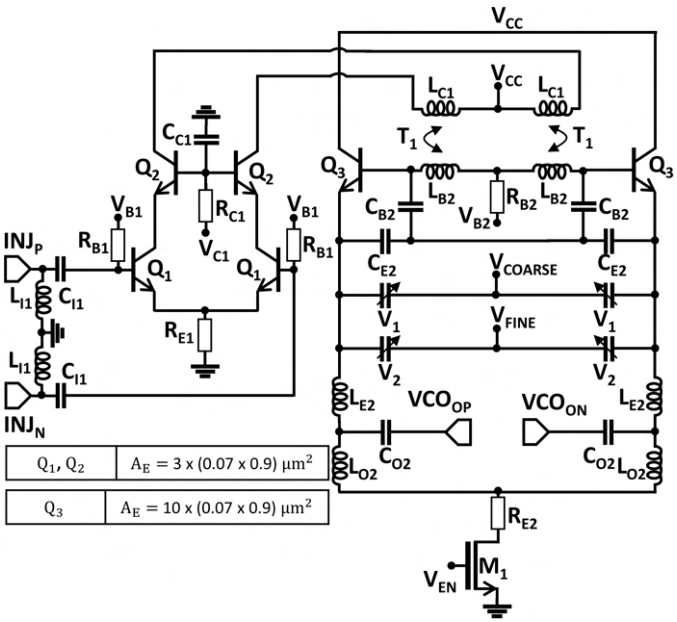


Figure 3.35: Circuit schematic of the injection-locked VCO with the injection input amplifier.

common rules of thumbs for Colpitts oscillators [Dem82]. The NMOS switch M_1 was implemented into the tail to control the enable/disable operation of the VCO. The resistor R_2 was utilized instead of an active current source to avoid the up-conversion of the flicker noise of the active devices, although the thermal noise was added. At the frequency range of interest the quality factors of the inductors and varactors play notably role on the total equivalent quality factor, which directly affects the phase noise performance of the VCO. Therefore, the width and shape of the tank inductor was designed to give maximum possible quality factor in the frequency range of interest. The size of the varactors (V_1 and V_2) was determined to provide maximum possible quality factor while meeting the frequency tuning range requirement mentioned earlier.

The injection lock signal is amplified by a fully-differential single-stage cascode amplifier, called the injection input amplifier, which is shown in Figure 3.35. The output of the injection input amplifier is magnetically coupled to the tank inductor L_{B2} over its output inductor of L_{C1}. The injection input amplifier isolates the core of the VCO from the injection-locking port of the transceiver chip, so that the oscillation frequency does not depend on the impedance of the predecessor stage of the injection input amplifier in a MIMO array. The tail resistor R_{E1} was employed to enhance the common-mode rejection ratio (CMRR) of the injection input amplifier. The base bias voltage was applied through high value resistor R_{B1}. The input impedance was matched to differential 100Ω using a high-pass matching network consisting of the shunt-inductor L_{I1} and the series-capacitor C_{I1}. The shunt inductor also provides a DC short circuit for ESD protection as the input of the injection input amplifier is directly connected to the injection-locking port of the transceiver chip. As explained in [Raz04], the oscillation frequency of an injection-lock VCO will be equal to the frequency of the applied injection-lock signal if the frequency of the injection-lock signal is close enough to the oscillation frequency and its amplitude is high enough to lock the VCO. The frequency range where the injection lock signal can lock the VCO signal is called "lock range". The minimum power level required for the injection-lock signal to be able to lock the VCO is called “sensitivity”. If the frequency of the VCO is forced to change when its frequency is locked by an injection lock signal, the output phase of the VCO will vary. The phase shift of θ between the phase of the injection-lock signal and the output signal of the oscillator in the locking-range can be approximately calculated by (2.18).

The IL-VCO has two tuning voltages of V_{COARSE} and V_{FINE}. The total size of the varactors controlled by the V_{COARSE} was set to be about six times bigger than the total size of the varactors controlled by the V_{FINE}. The frequency of the IL-VCOs in a daisy-chained MIMO array is set to be close proximately each other using the V_{COARSE}. And, the phase of the output signals of the IL-VCOs is controlled by the V_{FINE}. The injection-lock VCO draws a current of 13.5 mA from a supply voltage of 3.3V when the injection input amplifier is disabled. And, it consumes a current of about 25 mA when the injection input amplifier is enabled.

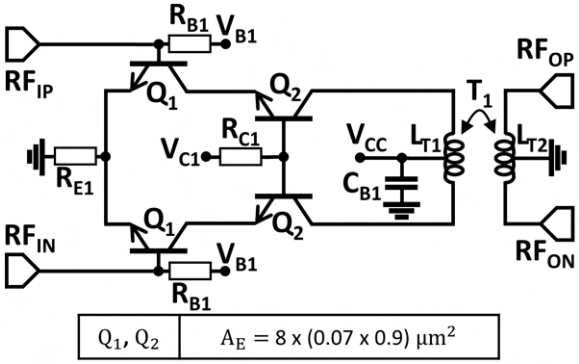


Figure 3.36: Circuit schematic of one of the buffer amplifiers of the VCO.

3.3.3 Buffer Amplifier

The buffer amplifiers, identical to each other, isolate the output of the IL-VCO from the subsequent stages, hence reducing the frequency pulling effect occurring due to the load impedance mismatch. They also stabilize the output power of the signal generation part over the frequency range of interest, as they were designed to operate in the saturated output power regime. The fully-differential single-stage cascode amplifier topology was employed since it provides high-frequency virtual grounding which enables easy implementation of on-chip inductors and transformers and reduces the parasitic effects of the supply and ground bond-wires of the transceiver chip. The circuit schematic of the buffer amplifier is depicted in Figure 3.36. The transistor size and base-emitter bias voltage were determined by considering the output power level to be able to drive the subsequent stages and the input impedance matching to the output of the injection-lock VCO. The tail resistor R_{E1} was placed to enhance the CMRR. The output of the buffer amplifier were matched to differential 100Ω load using the inductor-based transformer T_1. The designed buffer amplifier has a band-pass characteristic, so that the harmonics produced by the VCO are suppressed. The bypass capacitor C_{B1} was placed at the center tap of the inductor L_{T1} to provide common-mode AC grounding over the frequency range of interest for

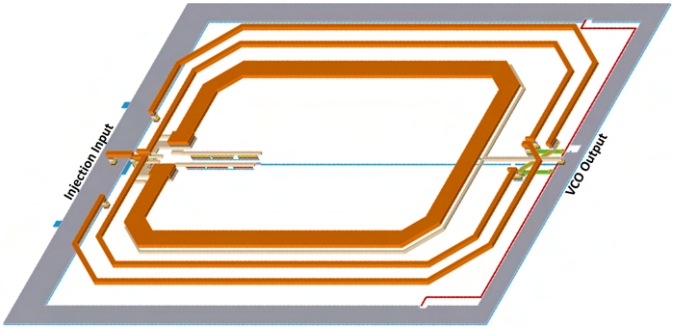


Figure 3.37: 3D layout view taken from EM simulation setup of the injection-locked VCO.

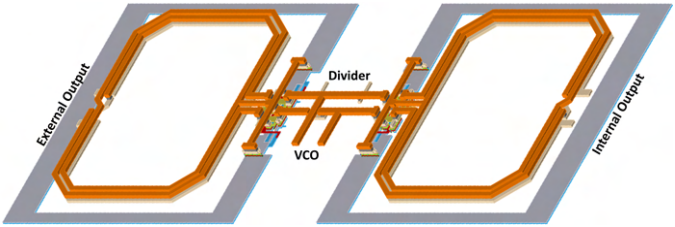
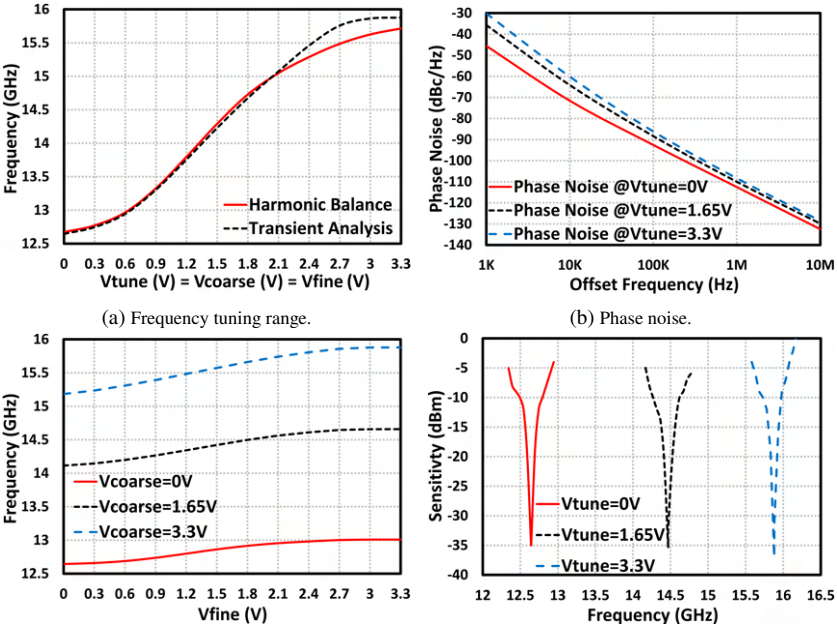


Figure 3.38: 3D layout view taken from EM simulation setup of the buffer amplifiers.

the transformer and filtering for the supply noise. The designed buffer amplifier draws a quiescent current of 10.5 mA at a supply voltage of 3.3V.

3.3.4 Simulation Results

The 3D model view of the IL-VCO, consisting of the differential common-collector Colpitts VCO and the injection input amplifier, is presented in Figure 3.37. Figure 3.38 shows the 3D model view of the buffer amplifiers with the power division network. The whole layout was simulated in ADS Momentum, and the EM-assisted circuit simulations were performed using this model. Figure 3.39a shows the harmonic balance and transient simulation results of the oscillation frequency of the designed signal generation part. There is a little dis-



(a) Frequency tuning range.

(b) Phase noise.

(c) Oscillation frequency versus V_{FINE}.

(d) Injection-locking sensitivity.

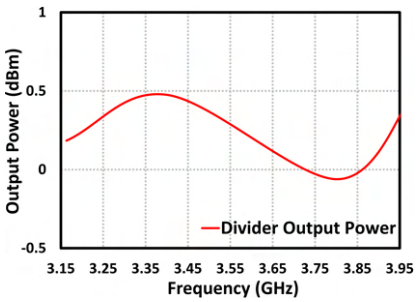
Figure 3.39: EM-assisted simulation results of the signal generation part.

crepancy between the harmonic and transient simulations for the tuning voltage values of higher than 2.1V. This discrepancy can be attributed to the convergence errors of the harmonic and transient simulation engines. The frequency tuning range is from 12.65 GHz to 15.71 GHz for a tuning voltage range of 0V-to-3.3 V according to harmonic balance simulation results. As shown in Figure 3.39b, the designed IL-VCO achieves an SSB phase noise varying between -108.3 dBc/Hz and -112.5 dBc/Hz at an offset of 1 MHz from the frequency of the carrier signal over the operating frequency range of the designed VCO. Figure 3.39c presents the frequency tuning range of the IL-VCO regarding to the tuning voltage of V_{FINE} with respect to different values of V_{COARSE}. The sensitivity of the IL-VCO with the injection lock amplifier is depicted in Figure 3.39d. The lock range is higher than 500 MHz for an injection input signal

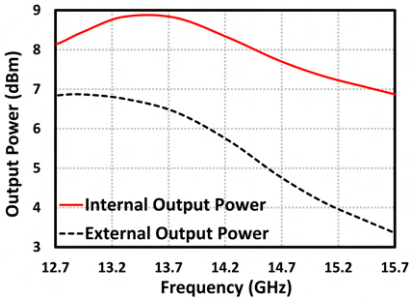
power of less than -5 dBm. Figure 3.40a presents the output power of the frequency divider chain while the all sub-blocks in the LO-signal generation part are operating. The output power of the divider chain is between -0.1 dBm and 0.5 dBm over the entire frequency range of the VCO. The simulated power values at the internal and external outputs of the LO-signal generation part is shown in Figure 3.40b. The difference between the internal and external output power results is due to the insertion loss of the bond-wires and pad-parasitics at the external port, which were taken into account during the simulations. The internal output power is higher than 7 dBm over the frequency tuning range of the designed VCO, and its peak value is about 8.8 dBm at 13.76 GHz. The external output power is approximately 6.8 dBm at the start frequency of the tuning range, which is also the maximum power value, and its minimum value is around 3.3 dBm at the last frequency point of the operating range. Figure 3.40c and Figure 3.40d present the harmonic suppression performance of the signal generation part at the internal and external outputs, respectively. The designed signal generation part achieves a harmonic rejection of more than 30 dBc over the frequency tuning range. The signal generation parts draws a DC current of 71.2 mA in total from a single supply voltage of 3.3V while the all-sub blocks are enabled.

3.4 Input Amplifier

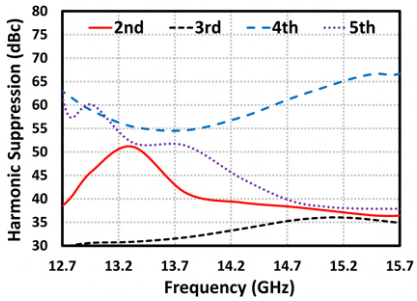
An amplifier was implemented to boost the external LO signal of the transceiver, which will be transmitted by a power distribution network with N-way depending on the number of elements in the MIMO array based on the centralized LO signal distribution network. The circuit schematic of the designed input amplifier based on the fully-differential single-stage cascode topology is presented in Figure 3.41. The inductor-based passive balun B_1 was designed and placed at the input side to perform the single-ended to differential conversion. The input of the amplifier was matched to single-ended 50Ω, using the passive balun B_1, the shunt-capacitor C_{S1}, and two series-capacitors C_{I1} also providing DC blocking for the base bias voltage of the common-emitter transistors in the cascode topology. The base bias voltage V_{B1}, which was set



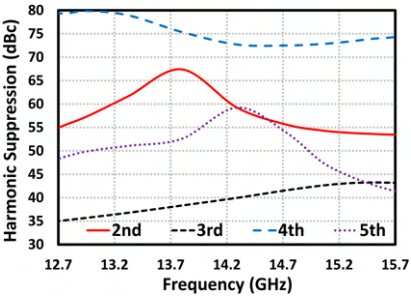
(a) Divider output power.



(b) VCO output power.



(c) Harmonic suppression levels at the internal output.



(d) Harmonic suppression levels at the external output.

Figure 3.40: EM-assisted simulation results of the signal generation part.

to be providing highest f_{max}, is applied through the high value resistors R_{B1} behaving as open-circuit for AC signals. The number of the transistors was determined by considering the output power requirements of the input amplifier. The output matching was performed using the inductor-based transformer T_1 with the shunt-capacitor C_{S2}. The bypass capacitor array C_{B1} was placed on the supply plane in order to provide common-mode AC grounding and filter the noise coming from the supply.

The 3D view of the full-layout of the designed input amplifier is presented in Figure 3.42. Its overall area is about 0.032 mm^2 (0.243 mm $\times$ 0.131 mm). The circuit simulations were performed using the EM-model of the full-layout. The amplifier draws a DC current of 10.9 mA from a single supply voltage of 3.3V.

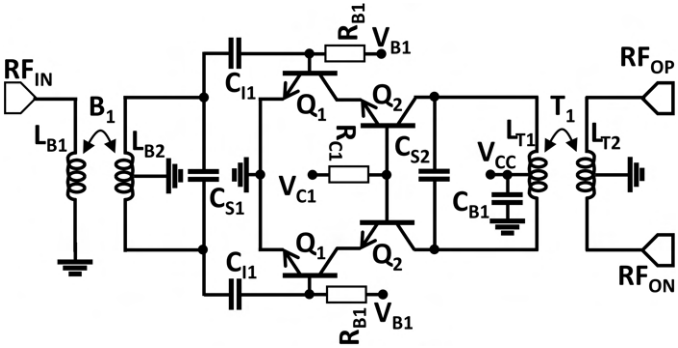


Figure 3.41: Circuit schematic of the designed input amplifier.

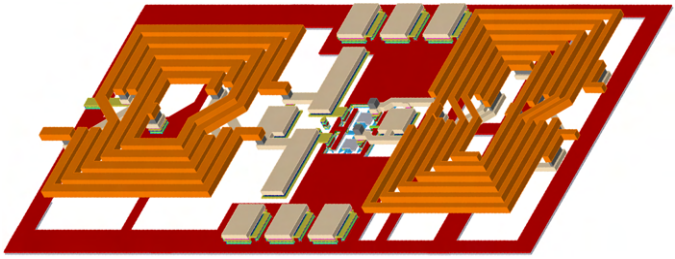
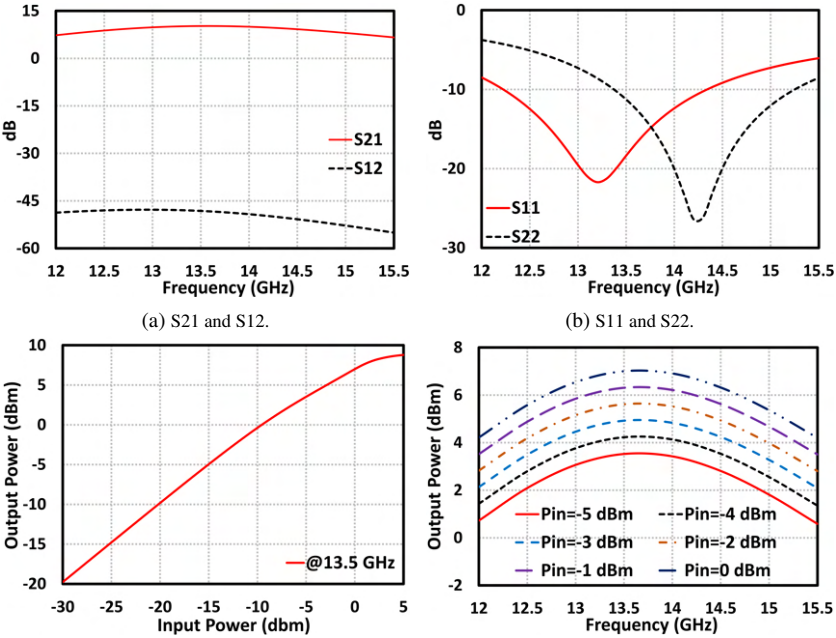


Figure 3.42: 3D layout view taken from EM simulation setup of the input amplifier

Figure 3.43a and Figure 3.43b show the simulated s-parameters results of the input amplifier. The small-signal gain of the amplifier is higher than about 8 dB over the frequency range of interest which is from 12.5 GHz to 15 GHz, and its peak value is 10.2 dB at 13.6 GHz. The input return loss is better than 7.3 dB along the frequency range of interest, and the output return loss is higher than 5 dB across the same frequency range. Figure 3.43c presents the power linearity of the designed input amplifier. The input referred 1-dB compression point is about -8 dBm. The output power versus the frequency for input power levels of higher than the 1-dB compression point is depicted in Figure 3.43d.



(a) S21 and S12.

(b) S11 and S22.

(c) Output power versus input power.

(d) Output power versus frequency.

Figure 3.43: EM-assisted simulation results of the input amplifier.

3.5 Rat-race Coupler

A rat-race coupler was implemented to provide high-isolation between the output of the transmitter channel and the input of the receiver channel while the output signal is being transmitted to the on-chip antenna and the signal received by the antenna is being transmitted to the receiver channel at the same time. The circuit schematic of the designed rat-race coupler is depicted in Figure 3.44. It was designed using differential transmission lines implemented using parallel coupled microstrip lines with 90° and 270° electrical lengths, whose the even-mode and odd-mode characteristic impedances are 70.7Ω and 200Ω, respectively. Figure 3.45 shows the 3D view of the whole layout of the designed rat-race coupler with an overall area of 0.088 mm^2 (0.22 mm × 0.4

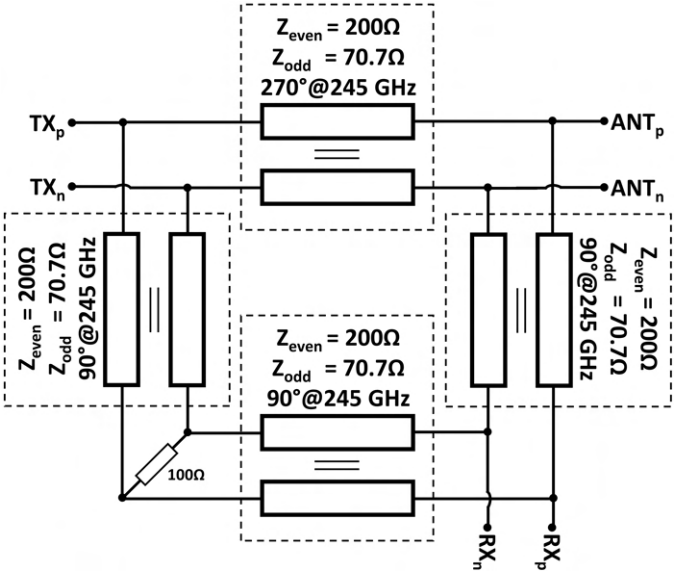


Figure 3.44: Circuit schematic of the designed rat-race coupler.

mm). Figure 3.46a and Figure 3.46b present the return loss performance of the designed rat-race coupler. The return loss is better than 19 dB for all ports over a frequency range from 220 GHz to 280 GHz. The insertion loss results are shown in Figure 3.46c. The insertion loss is better than 4 dB and 4.2 dB for the antenna-to-receiver and transmitter-to-antenna paths, respectively, over a frequency range from 220 GHz to 265 GHz. Figure 3.46d presents the isolation between the receiver and transmitter ports of the designed rat-race coupler. Its peak value is about 57 dB at 241 GHz, and it is higher than 25 dB across from 220 GHz to 265 GHz.

3.6 On-chip Antenna Loaded with Silicon Lens

Bow-tie antenna, also called butterfly antenna, is suitable for use in a wide variety of applications requiring wide frequency bandwidth, thanks to its ease

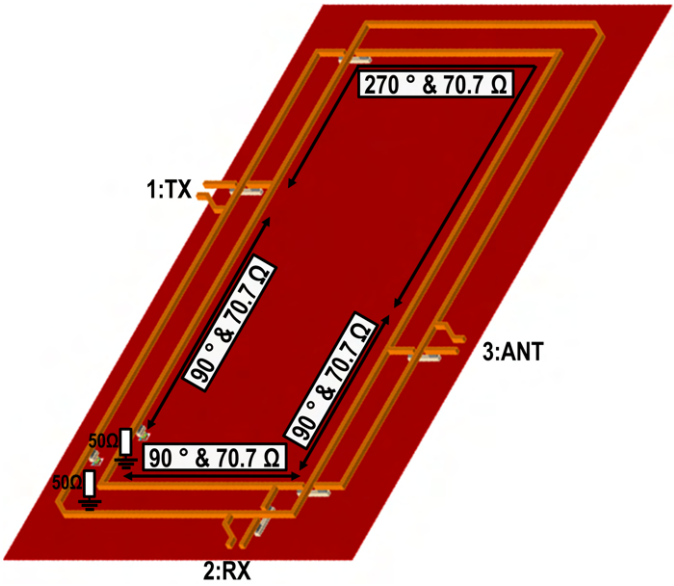
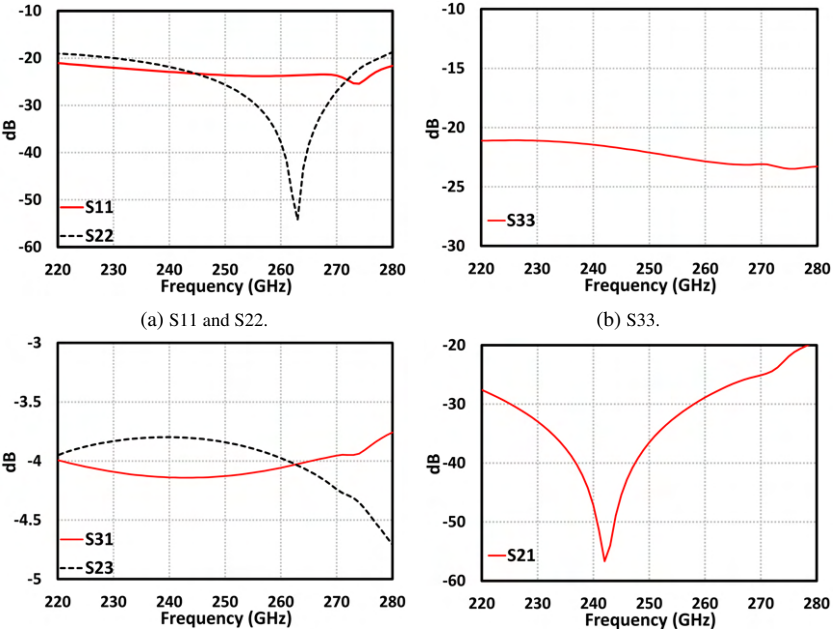


Figure 3.45: 3D layout view taken from EM simulation setup of the rat-race coupler

of fabrication and broadband input impedance matching and radiation performance [BW52]. Figure 3.47a shows a bow-tie antenna with four main design parameters: The flare angle θ_b, the arm length of the bow L_b, the gap distance between the feeding points S_b, and the minimum width of the bow W_b.

First, the design parameters were calculated using the mathematical expressions given in [RM82] and [CMP+87]. Then, parametric simulations were performed to find out the optimum values. As explained in [BGK+06] for an on-chip antenna, most of the power radiates from the back side through the high-dielectric chip substrate. Therefore, the design parameters were optimized considering the radiation efficiency and pattern on the back-side. The bow-tie structure was realized by the thickest conductor layer to minimize the electrical loss. A metal frame, consisting of all metal layers and vias, was placed to surround the bow-tie structure on three sides to meet the fabrication rules. The distance between the bow-tie structure and the metal frame was adjusted so as not to impair radiation



(a) S11 and S22.

(b) S33.

(c) S31 and S23.

(d) S21.

Figure 3.46: EM-assisted simulation results of the rat-race coupler.

performance while meeting the local fabrication rules. The designed antenna was fed with two signals of equal amplitude and opposite phase in order to keep the effect of the feed line on the radiation pattern as minimal as possible. The antenna feed line was realized using parallel coupled microstrip lines with even-mode and odd-mode characteristic impedance values of 146Ω and 50Ω, respectively.

The radiation efficiency of on-chip antennas is limited due to power loss into the substrate modes [Reb92]. A dielectric lens with the same relative permittivity as the chip substrate can be coupled to an on-chip antenna to avoid substrate modes related power loss. In addition, a matching layer can be employed to eliminate reflection losses between the dielectric lens and the air [vdVdMH99]. In this work, the designed on-chip bow-tie antenna was loaded with a hyper

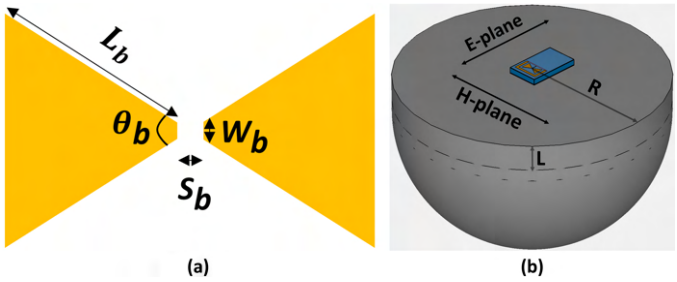
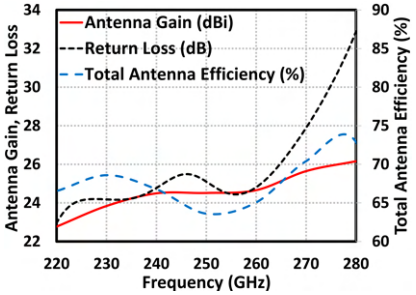


Figure 3.47: (a) A bow-tie antenna with main design parameters (b) 3D model of the designed antenna loaded with the hyper hemispherical silicon lens.

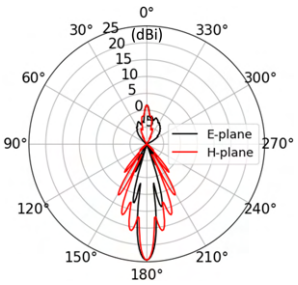
hemispherical lens made of un-doped silicon to sharpen the radiation pattern and increase the antenna gain in the broadside direction. However, the anti-reflection matching interface coating the lens could not be implemented due to manufacturing constraints. The hyper hemispherical silicon lens was attached to the backside of the chip as depicted Figure 2.7b. The mathematical expression (3.1) given in [FGR93] was used to determine the ratio of the length of the cylindrical extension L to the radius of the half sphere R, where n is the refractive index of the dielectric material of which the lens is made.

$$L = \frac{R}{n} \tag{3.1}$$

The designed antenna loaded with the hyper hemispherical silicon lens, which is shown in Figure 3.47b, was simulated by a 3D full-wave finite-difference time-domain EM solver tool. The size of the lens was determined considering the trade-off between the directivity and the beam-width. The radius of the half sphere R and the length of the cylindrical extension L were found to be 1.4-mm and 5-mm, respectively. Figure 3.48a presents the simulation results of the designed on-chip antenna loaded with the silicon lens. The return loss is better than 23 dB across from 220 GHz to 280 GHz. The simulated total antenna efficiency including the insertion loss of the feed line is between 63% and 74% from 220 GHz to 280 GHz. The designed antenna loaded with the hyper hemispherical silicon lens achieves an antenna gain of 22.8 dBi at 220 GHz



(a) Antenna gain, return loss, and total antenna efficiency.



(b) Antenna gain radiation pattern.

Figure 3.48: 3D EM simulation results of the designed bow-tie antenna loaded with the hyper hemispherical silicon lens.

and the antenna gain increases with frequency to compensate the transceiver circuit's falling output power with frequency. The simulated far-field radiation patterns at 240 GHz for the E- and H- planes are shown in Figure 3.48b. The simulated HPBW is 8.2° and 6.4°, respectively, for the E- and H- planes.

4 Characterization

The die photo of the designed transceiver chip is shown in Figure 4.1. It occupies an area of 2.72 mm^2 (2.16 mm × 1.26 mm). In addition, the transceiver test chip derived by placing a Marchand balun instead of the on-chip antenna was also manufactured, and its die photo is presented in Figure 4.2. The Marchand balun was placed for on-wafer probing and de-embedded from the measurement results using the measured insertion loss data of the back-to-back connected Marchand baluns. The designed test board used for the antenna and FMCW characterizations is demonstrated in Figure 4.3.

In this chapter, firstly, the on-wafer measurement results of the test circuits, which are the frequency multiplication-by-18 chain and the receiver channel, are presented. Then, the characterization of the signal generation part in the

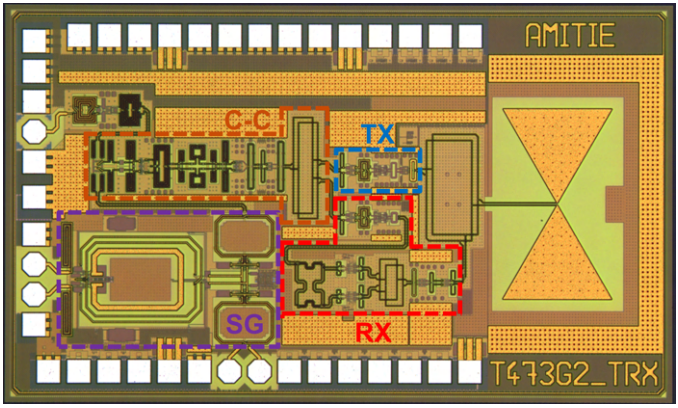


Figure 4.1: Micrograph of the designed transceiver chip (2.16 mm × 1.26 mm) (C-C: common-chain, RX: receiver, TX: transmitter, SG: signal generator).

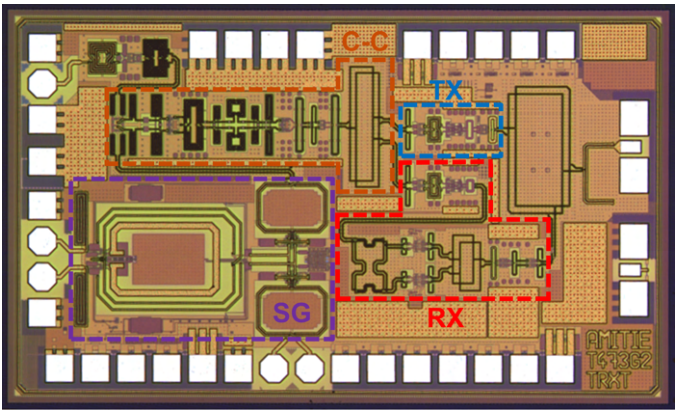


Figure 4.2: Micrograph of the transceiver test chip.

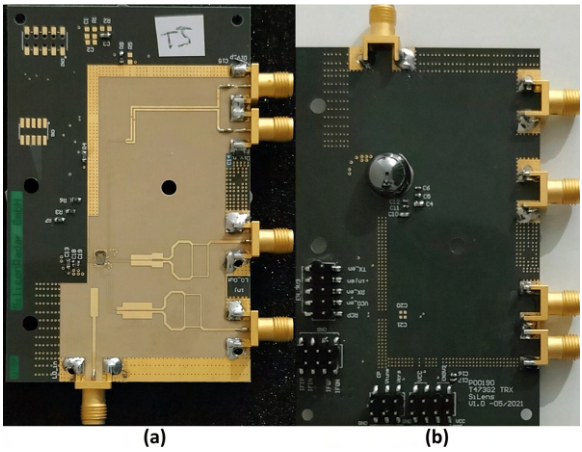


Figure 4.3: Photo of the front (a) and back (b) side of the designed test board used for the antenna characterization and the measurements requiring SMA-connection.

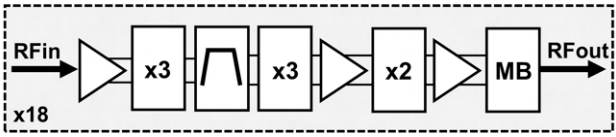


Figure 4.4: Circuit block diagram of the frequency multiplication-by-18 chain.

transceiver chip performed using the SMA ports shown in Figure 4.3 is given. Next, the on-wafer characterization results of the transceiver test chip carried out using the external VCO input and internal VCO signal are presented. After that, real-time FMCW measurements of far and near targets are demonstrated. Finally, the performance of the transceiver chip is summarized and compared with the previously reported similar studies in the literature.

4.1 Frequency Multiplication-by-18 Chain

A frequency multiplication-by-18 chain was implemented to test the circuit functionality of some sub-blocks which were used in the transceiver chip. The circuit block diagram of the implemented frequency multiplication chain is depicted in Figure 4.4. It consists of three amplifiers (12-15 GHz, 110-135 GHz, and 216-270 GHz), two frequency triplers (36-45 GHz, and 108-135 GHz), the 3rd-order Chebyshev BPF (36-45 GHz), and the modified Gilbert-cell based frequency doubler (216-270 GHz). The design, implementation and simulation results of all sub-blocks are given in Chapter 3. This section further extends my letter [TAD+22b].

The input signal is transformed to differential signal by a balun at the input of the first amplifier. The rest of the circuit is fully differential up to the Marchand-balun at the output, which was placed for high-frequency probing and de-embedded from the measurement results using the measured insertion loss data of the back-to-back connected Marchand-baluns. The die micrograph of the implemented frequency multiplication chain is shown in Figure 4.5. The chip

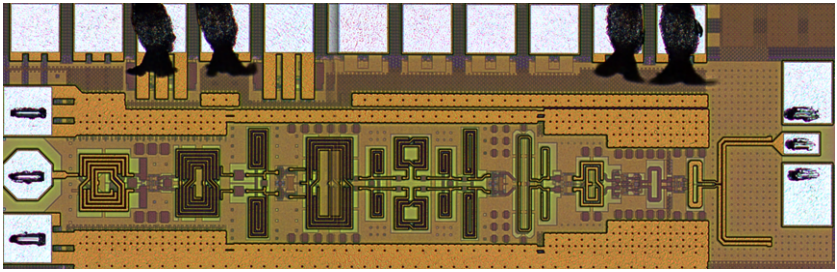


Figure 4.5: Chip micrograph of the frequency multiplication-by-18 chain.

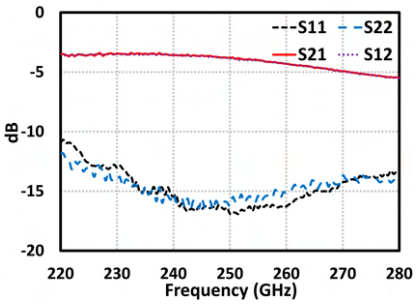
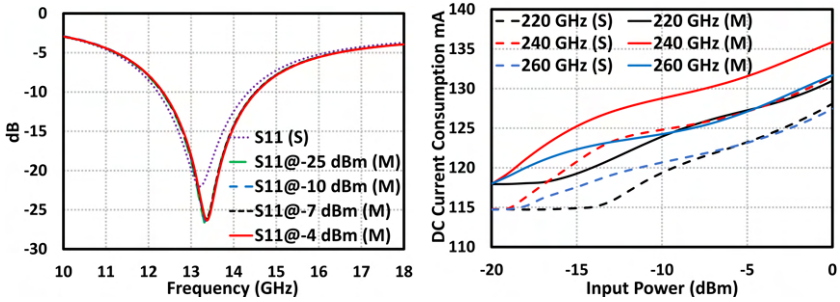


Figure 4.6: Measurement results of the back-to-back connected Marchand baluns.

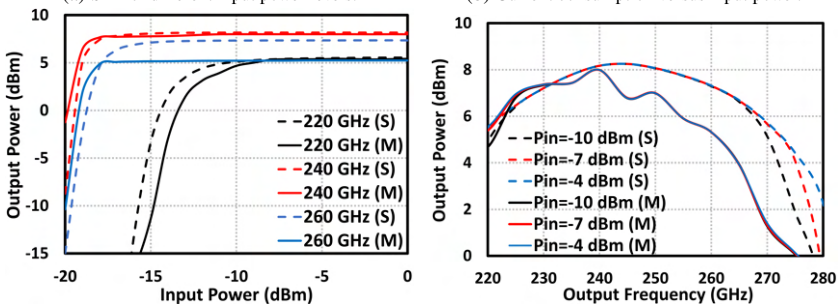
occupies an area of 0.58 mm^2 (1.35 mm $\times$ 0.43 mm) and the effective area excluding the pads and Marchand-balun is 0.28 mm^2 (1 mm $\times$ 0.28 mm). In order to perform de-embedding of the insertion loss of the Marchand-balun, a test structure, consisting of back-to-back connected Marchand-baluns, was also manufactured. The s-parameter measurement of this test structure was made by Rohde&Schwarz-ZVA24 whose frequency range was extended from 220 GHz to 325 GHz using two Rohde&Schwarz-Z325 frequency extension modules which were connected to Cascade Microtech 220-325 GHz probes with a pitch size of 50μm. The measurement setup was calibrated by Cascade Microtech 138-356 impedance standard substrate.

Figure 4.6 illustrates the measured s-parameter results of the back-to-back connected Marchand baluns. The S11 of the circuit was measured using Cas-



(a) S11 for different input power levels.

(b) Current consumption versus input power.



(c) Output power versus input power.

(d) Output power versus frequency.

Figure 4.7: Simulation (S) and measurement (M) results of the frequency multiplier-by-18 chain.

cade Microtech 67 GHz GSG probe and Keysight PNA-X N5247B VNA. The one-port SOL on-chip calibration was performed to shift the measurement reference plane to the probe tips for input power levels of -25 dBm, -10 dBm, -7 dBm, and -4 dBm. As presented in Figure 4.7a, the measured S11 is lower than approximately -8 dB across 12 to 15 GHz. The quiescent DC current consumption is 114.7 mA from a single supply voltage of 3.3V, and it consumes 130 mA for an input power of -7 dBm. Figure 4.7b shows the simulated and measured DC current consumption of the implemented frequency multiplier-by-18 chain over an input power range from -20 dBm to 0 dBm for the frequency points of 220 GHz, 240 GHz, and 260 GHz. The output power was measured by VDI Erickson PM4 power meter. The insertion loss of the output probe, which is provided by the probe manufacturer, was removed from the measure-

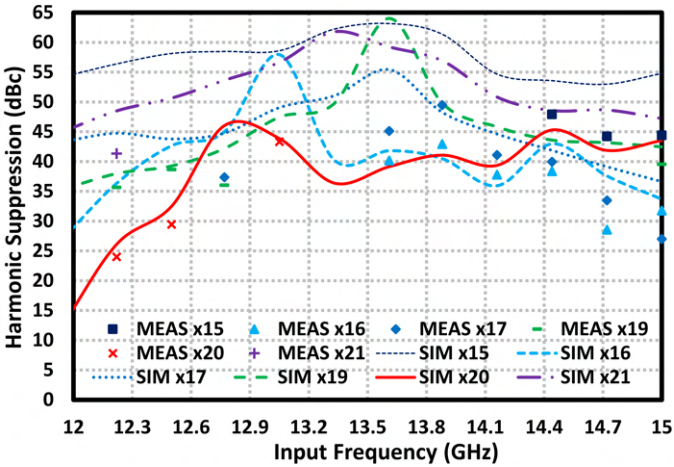


Figure 4.8: Simulated and measured harmonic suppression levels.

ment data. In addition, the measured insertion loss of the Marchand balun was de-embedded. The simulated and measured output power values versus input power are presented in Figure 4.7c for the frequency points of 220 GHz, 240 GHz, and 260 GHz. The measured output power remains almost constant for an input power of more than -7 dBm for all of the frequency points. Figure 4.7d shows the simulated and measured output power of the implemented frequency multiplication chain over a frequency range from 220 GHz to 280 GHz. The peak power value was measured to be about 8 dBm at 240 GHz, and the measured 3-dB bandwidth is 41 GHz (220-261 GHz) for an input power of -7 dBm. The measured collector (or drain) efficiency was calculated to be 1.47% at 240 GHz for an input power of -7 dBm. The in-band harmonics were measured using Agilent E4448A extended with OML-M03HWD harmonic mixer. A WR3-band attenuator was used to set the power of the 18th harmonic to be less than the compression point of the harmonic mixer, resulting in further decrease of the dynamic range which was already limited due to the high loss of the harmonic mixer. The measured and simulated in-band harmonic suppression levels are depicted in Figure 4.8. It was only possible to discern the harmonics which are over the noise floor of the setup. The measured harmonic suppression

Tabel 4.1: Comparison of the frequency multiplication-by-18 chain with the previously reported silicon-based frequency multipliers operating around 240 GHz.

Study	Tech.	f_T f_{max} (GHz)	MF[1]	Freq. (GHz)	3-dB BW[2] (GHz)	Peak P_{sat} (dBm)	Drain Efficiency	P_{DC} (mW)	Area (mm^2)
[EHB+17]	130-nm SiGe	300/500	6	230	15	-4	0.04	900	0.75
[EMK+17]	130-nm SiGe	300/500	8	236	40	0	0.4	250	1.2
[AYK+20]	130-nm SiGe	300/450	8	287	127	2.3	0.32	537	1
[BMAP20]	130-nm SiGe	250/370	8	244.5	81	-7.7	0.07	240	0.86
[SHP14]	130-nm SiGe	300/450	16	245	30	2.5	0.25	700	1.22 0.98[4]
[SRS+20]	130-nm SiGe	300/450	4	255.5	13	-8.4	0.65	22	1.02
[YCL+21]	130-nm SiGe	300/500	4	252	48	5.5	1.31[3]	270	0.29
This	130-nm SiGe	300/500	18	240	41	8	1.47	429	0.58 0.28[4]

[1]MF: Multiplication factor [2]BW: Bandwidth [3]Correction [4]Effective area excluding pads/output-balun

levels are better than 25 dBc for the input frequency range of interest which is from 12.22 GHz (220 GHz ÷ 18) to 14.5 GHz (261 GHz ÷ 18). Table 4.1 shows the comparison of the implemented frequency multiplier-by-18 chain with the silicon-based studies operating around 240 GHz. This work achieves highest output power and best efficiency with the highest multiplication factor in the literature.

4.2 Receiver Test Chip

The block diagram of the I/Q receiver test circuit, which was implemented to individually characterize the receiver channel of the transceiver consisting of the LNA, the power divider, two down-conversion mixers, and the branch-line coupler, is illustrated in Figure 4.9. Figure 4.10 shows the chip photo of the

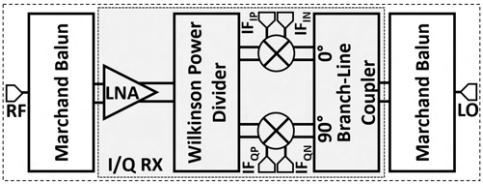


Figure 4.9: Circuit block diagram of the receiver test circuit.

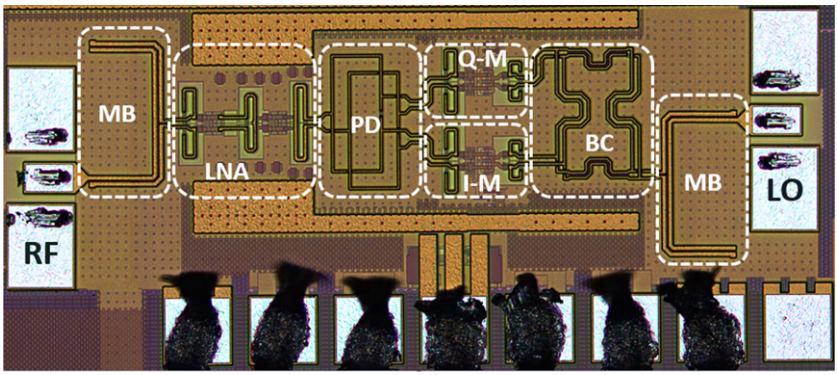


Figure 4.10: Chip micrograph of the receiver test circuit.

implemented receiver test circuit. The total area of the implemented test circuit is about 0.42 mm^2 (0.97 mm $\times$ 0.43 mm), and the effective area is about 0.14 mm^2 (0.55 mm $\times$ 0.26 mm), excluding the baluns and pads placed for single-ended probing. The insertion loss of the back-to-back connected baluns was measured as explained in Section 4.1 and de-embedded from the measurement results of the receiver channel.

The receiver consumes a DC current of 40.6 mA from a single supply voltage of 3.3V. The optimum LO power of the designed receiver channel is 3 dBm according to the simulation results. The LO input of the receiver test circuit was driven by WR3.4 SGX-M signal generator frequency extension module configurated with Rohde&Schwarz SMP22 signal generator. The output power of the frequency extension module at the LO side was characterized using VDI Ericsson PM4 power meter, and it varies from 1.8 dBm to 7.1 dBm from

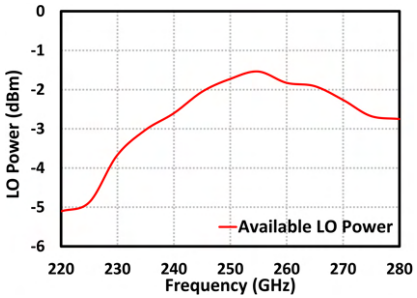
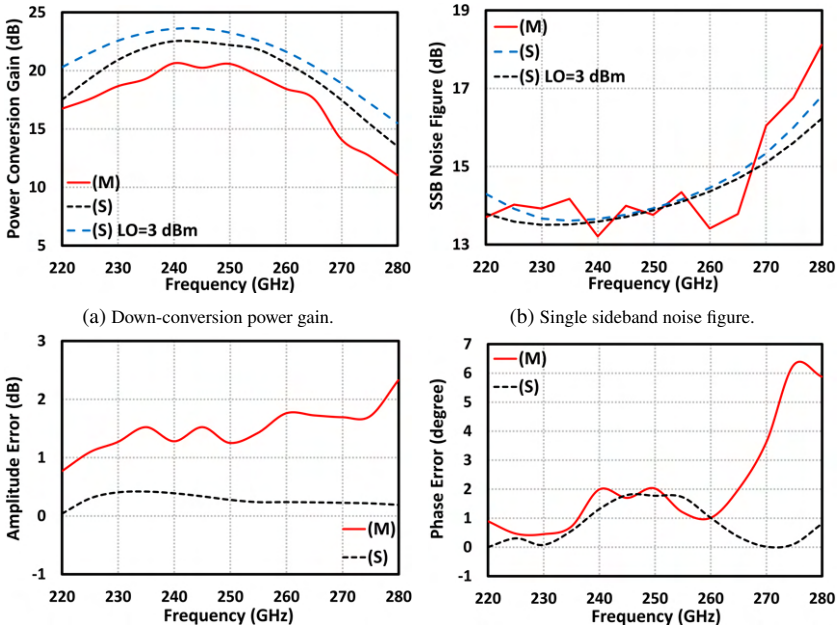


Figure 4.11: Available LO power at the input of the branch-line coupler during the characterization.

220 GHz to 280 GHz. The insertion loss data of the probe and s-bend, which is connected between the frequency signal generator module and probe, was de-embedded. The available LO power values at the input of the branch-line coupler during the characterization over the frequency range of interest, which is from 220 GHz to 280 GHz, are presented in Figure 4.11. Its maximum and minimum values are about -1.5 dBm at 255 GHz and -7.3 dBm at 215 GHz, respectively, which are far below the optimum LO power. Therefore, the down-conversion power gain and SSB noise figure simulations were re-performed for the available LO power values.

The RF input signal was applied by Keysight N5247B vector network analyzer whose frequency range was extended to the frequency range of interest. The insertion loss data of the probe, which is provided by the manufacturer, was calibrated. The frequencies of the RF and LO signals were swept simultaneously to keep the IF frequency constant at 30 MHz during the measurement. The SSB noise figure and power conversion gain were measured using the gain method [OHP12]. The differential IF outputs of the I-channel were transformed to single-ended signal by BAL-0067 balun, and then amplified by ZX60-V63+ amplifier. The output noise power density and power conversion gain were measured using Agilent E4448A PSA. The insertion loss of the balun and power gain of the external IF amplifier were de-embedded from the measurement results. The simulated and measured power conversion-gain is shown in Figure 4.12a. In addition, the simulation results with the optimum LO power of 3



(a) Down-conversion power gain.

(b) Single sideband noise figure.

(c) Amplitude error.

(d) Phase error.

Figure 4.12: Simulation (S) and measurement (M) results of the receiver test circuit.

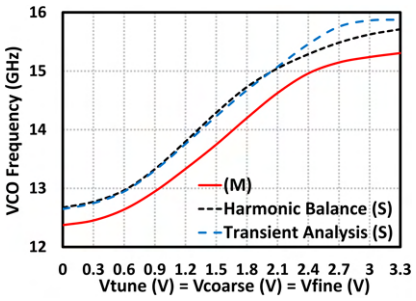
dBm were plotted for the comparison. As can be seen in Figure 4.12a, the lower LO power considerably limits the peak power conversion gain value and 3-dB bandwidth. The measured peak value of the power conversion gain is 20.6 dB at 240 GHz for an RF power of -32 dBm which is far enough below the input referred 1-dB compression point of -22 dBm at 240 GHz, and the 3-dB bandwidth is about 40 GHz, from 225 GHz to 265 GHz. Figure 4.12b presents the simulated and measured SSB noise figure results. The receiver test channel achieves an SSB noise figure of 13.2 dB at 240 GHz and better than 14.2 dB along the 3-dB RF bandwidth. Then, the IF output power of the Q-channel was characterized as mentioned above for the I-channel. Thereafter, the amplitude error was calculated by subtracting the gain of the I-channel from that of the Q-channel. Finally, the phase error between the I- and Q- channels were

Tabel 4.2: Comparison of the receiver test chip with the previously reported silicon-based receivers operating around 240 GHz.

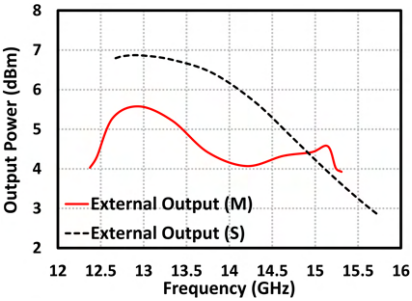
Study	Tech.	f_T f_{max} (GHz)	3-dB BW[2] (GHz)	Peak CG (dB)	NF (dB)	P_{DC} (mW)	Area (mm^2)
[TKN15]	65-nm CMOS	N/A	20	25	15 12[1]	260	2
[ADS+20]	55-nm SiGe	320/270	74	23	24.5	859 293[2]	1.84
[SGS+16]	130-nm SiGe	300/450	18	10.5	16 13[1]	866 146[2]	1.57
[EAK+17]	130-nm SiGe	300/500	55	32	13.4	575	4.5
[EMG+13]	130-nm SiGe	300/500	40	18	18[3]	458	2.3
[VGS+17]	130-nm SiGe	350/550	47	7.8	11.3 8.3[1]	916 60.8[2]	1.26
This	130-nm SiGe	300/500	40	20.6[4]	13.2 10.2[1]	134	0.42 0.14[5]

[1]Estimated DSB NF = SSB NF – 3 dB [2]Power consumption of down-conversion part [3]Simulated DSB NF [4]w/o IF amplification [5]Effective area excluding the pads/output-balun

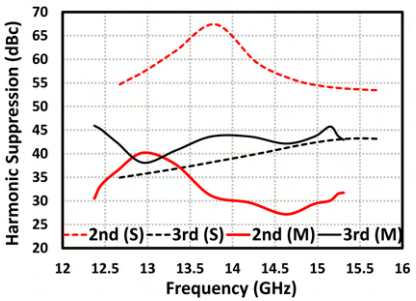
measured using DSOX3014A Oscilloscope. Thanks to the quadrature receiver architecture, the noise in the image band will be rejected in the baseband domain. Therefore, the real noise figure of the receiver will be equal to its double sideband (DSB) noise figure value which is 3 dB better than SSB noise figure for an infinite image rejection ratio. As presented in Figure 4.12c and Figure 4.12d, the measured amplitude imbalance and phase error values of the IF signals are less than 1.7 dB and 2°, respectively, over the 3-dB bandwidth. This results in an image rejection ratio of better than 20.1 dB which is causing an increase of less than 0.1 dB in DSB noise figure [Raz97]. The comparison of the implemented receiver test chip with the previously reported silicon-based receivers operating around 240 GHz is summarized in Table 4.2. This work achieves the highest power conversion gain without IF amplification among the silicon-based receivers.



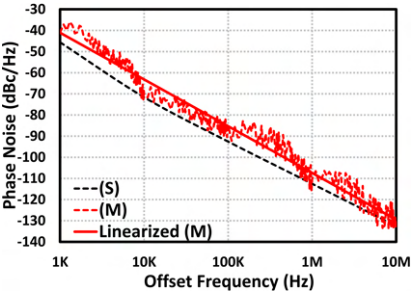
(a) Fundamental oscillation frequency.



(b) Power results of the external VCOout.



(c) Harmonic suppression levels at the external VCOout.



(d) Phase noise results at the external VCO.

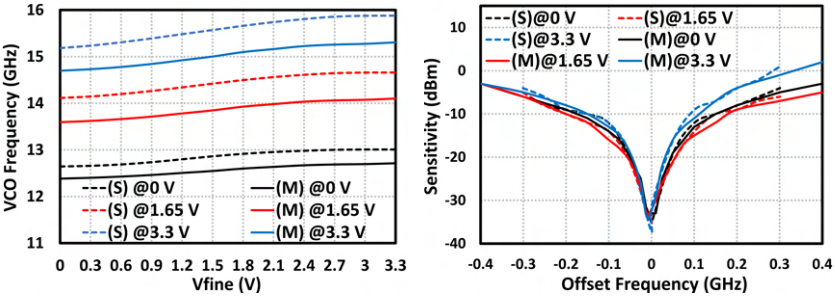
Figure 4.13: Simulation (S) and measurement (M) results of the signal generation part.

4.3 Signal Generation Part

The characterization of the signal generation part, the design of which has been discussed in Section 3.3, of the transceiver circuit was performed using the test-board presented in Figure 4.3. First, the measurements were carried out while the injection input amplifier was disabled. Then, the injection input amplifier was enabled and the performance parameters related to this case were characterized. Finally, the performance of the divider output was measured.

The signal generation part draws a DC current of 75 mA from a single 3.3 V supply while the injection input amplifier is disabled. The V_{COARSE} and V_{TINE} tuning control pins were connected together and named as the tuning

pin V_{TUNE}. The V_{TUNE} was swept from 0 V to 3.3 V in 0.3 V steps and the output frequency was measured with Keysight E4448A PSA spectrum analyzer. Figure 4.13a shows the simulated and measured output frequency results as a function of the tuning voltage V_{TUNE}. The measured frequency tuning range is from 12.373 GHz to 15.307 GHz, which agrees well with the results of the circuit simulations. The difference between the simulation and measurement results is less than approximately 400 MHz. This discrepancy can be due to the inaccurate EM modelling of the tank inductor and the process variation of the used voltage controlled capacitors since the oscillation frequency is a strong function of these two design parameters. The measured output power was measured with the same spectrum analyzer. The insertion loss of the SMA-cable connecting the VCO output of the transceiver test board to the spectrum analyzer was also measured and de-embedded from the results. Figure 4.13b presents the simulated and measured output power values versus the oscillation frequency. The measured output power varies between approximately 4 dBm and 5.6 dBm over the frequency tuning range. The circuit simulations were done using ideal models of the bond-wires and balun, resulting in disagreement with the measurement results. However, this disagreement can be ignored since the measured output power is anyhow much higher than the injection sensitivity of the VCO as will be presented later. The simulated and measured de-embedded harmonic suppression results are depicted in Figure 4.13c. The balun and impedance matching network on the test board presented in Figure 4.3 were optimized for the frequency range of 12 GHz to 16 GHz. Therefore, these structures do not provide optimum single-ended to differential transformation and differential 100Ω load for the second and third harmonic signals at the external output of the signal generation part. Consequently, the discrepancy between the simulated and measured harmonic suppression results can be attributed to the frequency limit of the passive structures on the test board. The signal generation part achieves a harmonic suppression performance of more than 27 dBc over the tuning frequency range. The measurement of the SSB phase noise was performed using the phase noise measurement mode of the same spectrum analyzer. The phase noise could only be measured in the case of that the tuning control pin was connected to the ground via a short pin header. Because, the tuning gain of the designed VCO is quite high and so that noise present in the tuning control



(a) Frequency tuning range as a function of V_{FINE}.

(b) Injection lock sensitivity.

Figure 4.14: Simulation (S) and measurement (M) results of the signal generation part.

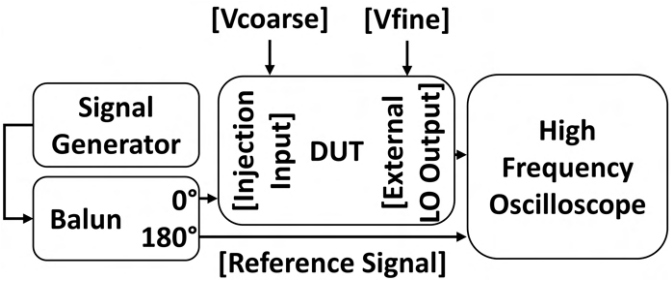
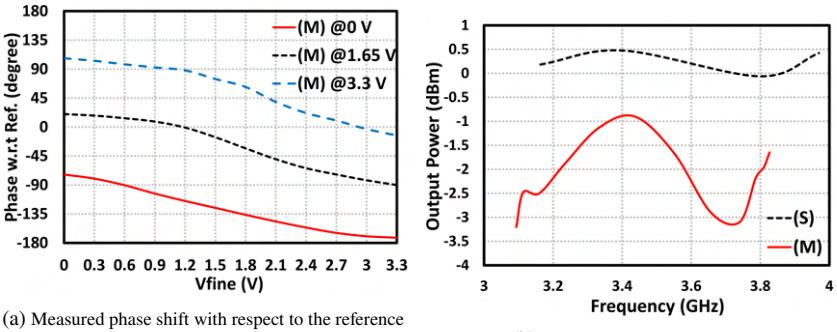


Figure 4.15: Measurement setup to measure the phase shift at the output.

signal significantly affects the oscillation frequency. Figure 4.13d shows the simulated and measured phase noise plots versus offset frequencies for a tuning voltage of 0 V. The circuit has a measured phase noise of about -109.4 dBc/Hz at an offset frequency of 1 MHz from the carrier.

The current consumption of the signal generation part is about 88 mA at a supply voltage of 3.3 V while the injection input amplifier is enabled. The V_{COARSE} and V_{FINE} tuning pins were separately controlled in order to characterize the injection-locking operation of the designed IL-VCO. Figure 4.14a presents the simulated and measured frequency tuning ranges as a function of V_{FINE} for V_{COARSE} of 0 V, 1.65 V, and 3.3 V. In order to measure the sensitivity levels of the injection input, a signal with a power of -40 dBm to 5 dBm in 1 dB steps was

applied by Rohde&Schwarz signal generator SMR40 for an offset frequency range of -400 MHz to 400 MHz from the oscillation frequency value of the VCO without injection signal. The simulated and measured injection lock sensitivity results of the designed signal generation part are shown in Figure 4.14b. The maximum injection input power requirement was found to be 2 dBm for the V_{COARSE} of 3.3V. For an injection input power of less than 2 dBm, the output frequency of the VCO is able to be locked by the injection input signal across an offset frequency range of -400 MHz to 400 MHZ. As presented in Figure 4.13b, the measured VCO output power is higher than approximately 4 dBm across the frequency range of interest, which is exceedingly enough to lock the VCO of the next transceiver circuit in a cascaded MIMO array configuration. Figure 4.15 depicts the measurement setup which is used to observe the phase change at the output of the IL-VCO. As explained in Section 2.5, the phase of the output signal of the IL-VCO is able to be shifted by changing the fine tuning voltage if the oscillation frequency of the VCO is locked to the frequency of the injection input signal. A single-tone sinusoidal signal with a power level of 3 dBm was applied to the input of Marki Microwave BAL-0067 broadband balun (300 kHz to 67 GHz) by the signal generator. One of the outputs of the balun was connected to the injection input of the transceiver test board. The other output of the balun and the external LO output of the signal generation part were connected to Keysight UXR0402A 40 GHz oscilloscope. The measured phase values of the external LO output signal with respect to the reference signal across a V_{FINE} voltage range of 0 V to 3.3 V are presented in Figure 4.16a for V_{COARSE} voltages of 0 V, 1.65 V, and 3.3 V. As can be seen, the phase can be shifted more than 90° by changing the fine tuning voltage for all states. Considering the total multiplication factor of 18, a phase shift of 90° at the fundamental frequency is more than enough to provide a full 360° phase control. The output power of the divider circuit was also characterized using the transceiver test board and the same spectrum analyzer. Figure 4.16b shows the simulated and measured divider output power of the LO signal generation part. The discrepancy between the simulated and measured output power levels can be attributed to that the circuit simulations were performed using the ideal bond-wires models.



(a) Measured phase shift with respect to the reference signal.

(b) Power of the divider output.

Figure 4.16: Simulation (S) and measurement (M) results of the signal generation part.

4.4 On-wafer Characterization of the Transceiver with External VCO

The external VCO input and transceiver in/out pads were probed with Infinity GSG 100μm 0-67 GHz and Infinity GSG 50μm 220-325 GHz probes from Cascade-Microtech, respectively. The on-chip antenna was removed from the transceiver circuit, and the implemented Marchand balun was placed instead for single-ended probing. The measured insertion loss of the Marchand balun was de-embedded from the results as described in Section 4.1. Figure 4.2 shows the photo of the transceiver test chip. As mentioned before, the transceiver circuit can be configured via the enable/disable control pins to operate in one of the following modes: transmitter, receiver, and transceiver. In this section, the transceiver test chip was characterized using the external VCO input, therefore the signal generation part was de-activated. The circuit draws a quiescent DC current of 138.1 mA, 151.6 mA, and 208 mA from a single supply of 3.3 V, respectively, for the transmitter, receiver, and transceiver operation modes.

The s-parameters of the external VCO input were measured using Cascade Microtech 67 GHz GSG probe connected to Keysight PNA-X N5247B VNA. The one-port SOL on-chip calibration was performed to shift the measurement reference plane to the probe tips for input power levels of -25 dBm, -7 dBm,

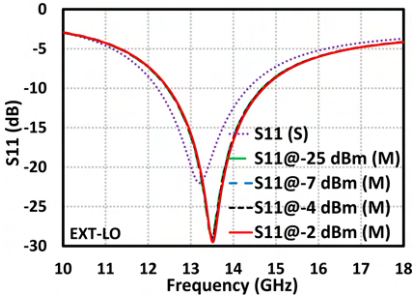
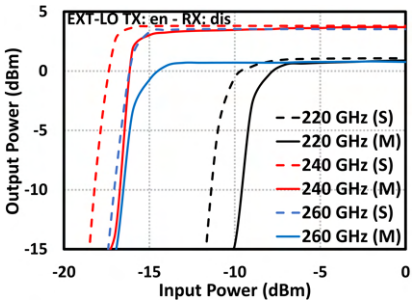


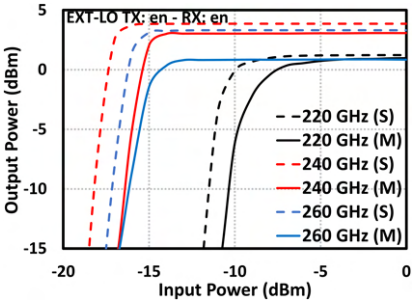
Figure 4.17: Simulated (S) and measured (M) s-parameter results of the external VCO input of the transceiver test chip.

-4 dBm, and -2 dBm. The impedance matching of the external VCO port is independent of the operating modes of the transceiver circuit, thanks to high reverse isolation from the output to the input of the common-chain. Figure 4.17 illustrates the simulated and measured s-parameter results of the external VCO input. It provides a measured return loss performance of better than 8 dB across from 12.2 GHz to 15.2 GHz for all input power levels.

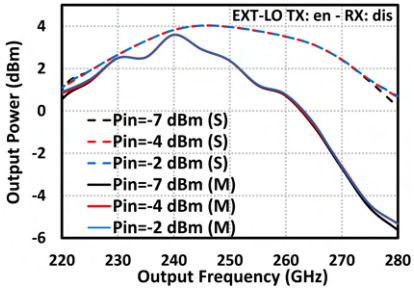
In order to measure the output power of the transceiver test chip, the external VCO input port was fed by Rohde&Schwarz SMR-40 signal generator with a single-tone sinusoidal signal from 12.22 GHz to 15.2 GHz with a step size of about 278 MHz. The power of the applied signal was varied from -20-dBm to 0-dBm in 1-dB steps. The power of the output signal at the transceiver in/out pad was measured by VDI Erickson PM4 power meter. The insertion losses of the probe and s-bend connecting the waveguide head of the probe and the power meter were calibrated. Figure 4.18a and Figure 4.18b present the simulated and measured output power versus input power at output referred operating frequency points of 220 GHz, 240 GHz, and 260 GHz for the transmitter and transceiver operation modes, respectively. For both operating modes, the circuit reaches its saturated output power for an input power of more than -4 dBm. The total DC current consumption of the transceiver test chip is approximately 159 mA and 234 mA for an input power of -4 dBm at 240 GHz for the transmitter and transceiver modes, respectively. The simulated and measured output power levels across from 220 GHz to 280 GHz are shown



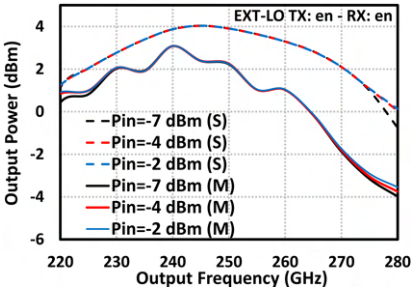
(a) Transmitter-mode: Output power versus input power.



(b) Transceiver-mode: Output power versus input power.



(c) Transmitter-mode: Output power versus frequency.



(d) Transceiver-mode: Output power versus frequency.

Figure 4.18: Simulated (S) and measured (M) output power results of the transceiver test chip using an external VCO signal.

in Figure 4.18c and Figure 4.18d respectively. In the transmitter mode, the transceiver circuit achieves a peak output power value of 3.6 dBm at 240 GHz, and its 3-dB frequency bandwidth is about 41 GHz, from 220 GHz to 261 GHz. On the other hand, its peak output power is around 3.1 dBm at 240 GHz with a 3-dB bandwidth of about 45 GHz in the transceiver mode. Compared to the measured output power of the frequency multiplication-by-18 chain, there is an average drop of about 4.2 dB in the output power of the transceiver chip. This difference fits well with the simulated insertion loss of the rat-race coupler. In addition, the difference in output power levels between the transmitter and transceiver operating modes is very limited, less than 0.5 dB,

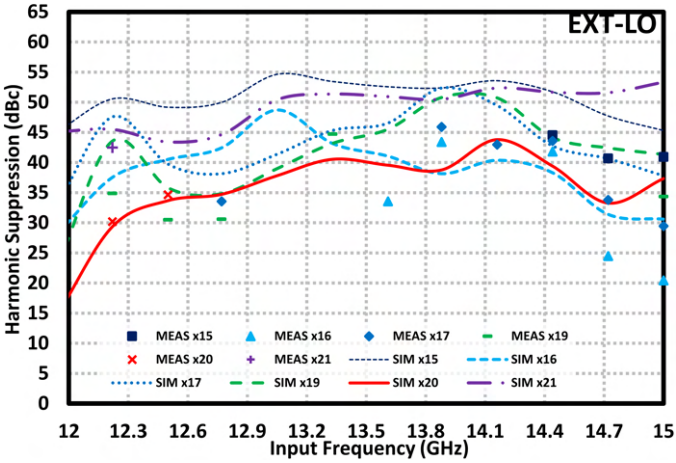
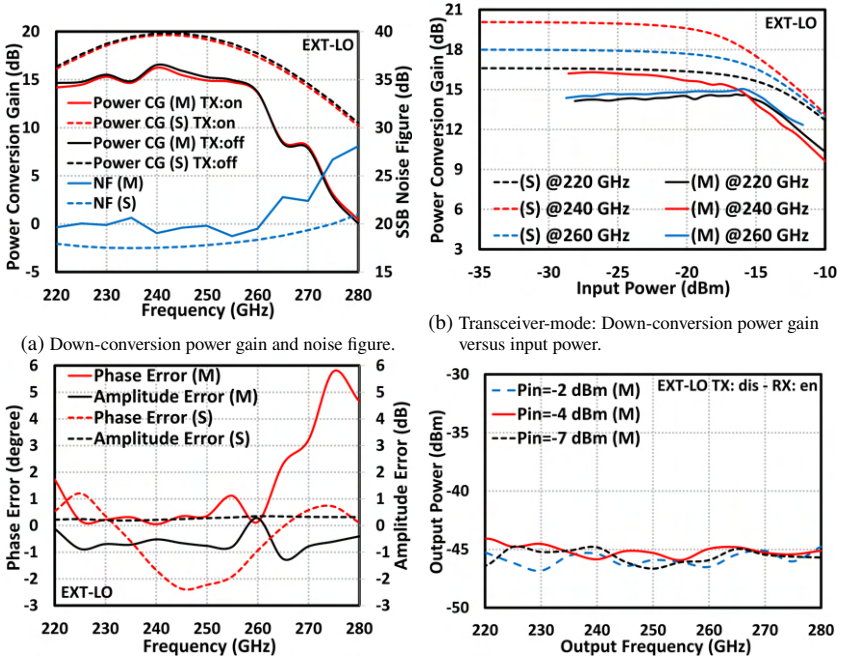


Figure 4.19: Harmonic suppression levels at the transceiver in/out pad for an external VCO signal of -4 dBm.

across the 3 dB frequency bandwidth. This indicates that the rat-race coupler provides a good level isolation between the transmitter and receiver channels as in its simulation results. Therefore, it is sufficient to characterize the in-band harmonic suppression performance at the transceiver in/out port for only one operating mode. For the transceiver mode, the power levels of the in-band harmonics were measured using Agilent E4448A spectrum analyzer whose frequency range was extended with OML-M03HWD 220-325 GHz harmonic mixer. A WR3-band attenuator was employed to set the power of the 18th harmonic, which is the desired signal, to lower than the compression point of the mixer, resulting in further decrease in the dynamic range which was already limited due to the high down-conversion loss of the used harmonic mixer. The measured and simulated in-band harmonic suppression levels are illustrated in Figure 4.19. It was only possible to measure the power values of the harmonics which are over the noise floor of the measurement setup. The transceiver test circuit achieves a measured harmonic suppression of more than 30 dBc across the frequency range of interest, which is from 12.22 GHz (220 GHz ÷ 18) to 14.5 GHz (261 GHz ÷ 18).



(a) Down-conversion power gain and noise figure.

(b) Transceiver-mode: Down-conversion power gain versus input power.

(c) Transceiver-mode: phase and amplitude error.

(d) Receiver-mode: Output power versus frequency.

Figure 4.20: Simulation (S) and Measurement (M) results of the transceiver test chip using an external VCO signal.

The receiver performance of the transceiver chip was characterized by feeding the external VCO input port with the Rohde&Schwarz SMR-40 signal generator and the transceiver in/out port with WR3.4 SGX-M signal generator frequency extension module configured with Rohde&Schwarz SMP22 signal generator. The output power of the signal generator frequency extension module versus its control voltage was measured using VDI Erickson PM4 power meter. This measurement data and the insertion losses of the probes, cables, and s-bend waveguide were de-embedded from the measurement results to calibrate the power levels at the transceiver in/out pad of the transceiver test chip. The differential IF output signals of the I-channel were converted to single-ended signal using the external BAL-0067 broadband balun manufactured by Marki

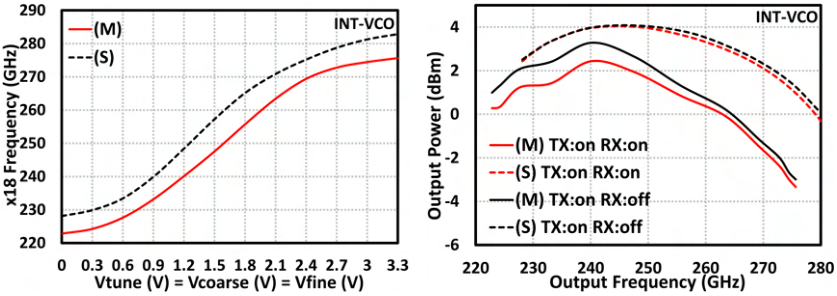
Microwave. Then, the IF output signal was amplified by ZX60-V63+ amplifier from Mini-Circuits and measured using Agilent E4448A PSA. The power of the IF output signal was measured for an input power of around -30 dBm at the transceiver in/out port since this power level is far less than the input referred 1-dB compression point of the receiver channel in the transceiver test chip as presented later. The insertion loss of the balun and power gain of the external IF amplifier were de-embedded from the IF output measurement results. The frequencies of the RF and LO signals were swept simultaneously to keep the IF frequency constant at 30 MHz during the characterization. The SSB noise figure and down-conversion power gain of the transceiver test chip were calculated by the gain method [OHP12] using the measurement results of the output power and output noise power density of the IF output signal of the I-channel. The characterization of the receiver channel of the transceiver chip was performed for an external VCO input power of -4 dBm since this power level was found to be the optimum input power during the measurements of the transmitter channel. Figure 4.20a shows the simulated and measured down-conversion power gains over a frequency range from 220 GHz to 280 GHz for the receiver and transceiver operation modes. The peak value of the down-conversion power gain was measured to be about 16.24 dB at 240 GHz, and the circuit achieves a measured 3-dB bandwidth of 41 GHz from 220 GHz to 261 GHz. The difference between the measured down-conversion power gain results of the receiver and transceiver operating modes is lower than 0.7 dB across 220 GHz to 280 GHz. This indicates that the rat-race couple provides a good level isolation between the transmitter and receiver channels as its simulation results presented before. Consequently, it was decided to measure the receiver performance metrics for only one operating configuration: transceiver mode. The simulated and measured SSB noise figure values are presented in Figure 4.20a. The circuit exhibits a measured SSB noise figure of 18.73 dB at 255 GHz, and better than 21 dB across the 3-dB bandwidth. In order to characterize the power linearity of the receiver channel in the transceiver test circuit, the input power at the transceiver in/out pad was swept from approximately -28 dBm to about -10 dBm with a step size of around 1 dB for operating frequency points of 220 GHz, 240 GHz, and 260 GHz. Figure 4.20b shows the simulated and measured power linearity of the receiver channel in the transceiver test chip. The measured input referred

1-dB compression point was found to be –16 dBm at 220 GHz, -16.5 dBm at 240 GHz, and –13.5 dBm at 260 GHz. After the characterization with the spectrum analyzer had been carried out, the IF outputs of the transceiver test chip were directly connected without any balun and amplifier to 4-port DSOX3014A oscilloscope in order to measure the amplitude and phase imbalance between the I- and Q- channels. The simulated and measured amplitude and phase error results are presented in Figure 4.20c. The receiver channel exhibits an amplitude error of less than 1-dB across 3-dB bandwidth. The measured phase imbalance is lower than 1.8° across 3-dB bandwidth from 220 GHz to 261 GHz. An amplitude imbalance of less than 1-dB and a phase error of lower than 1.8° result in an image rejection ratio of better than 24.5 dB which is causing an increase of less than 0.02 dB in DSB noise figure [Raz97].

The output power of the transceiver test chip when the transmitter channel is de-activated but the receiver channel is activated was measured to check for any leakage through the silicon substrate. Figure 4.20d illustrates the measured output power of the transceiver test chip for the receiver operating mode. The measured output power is less than the minimum detectable power level at the probe tip. It indicates that there is no significant signal leakage from the output of the frequency doubler in the receiver channel to the transceiver in/out port.

4.5 On-Wafer Characterization of the Transceiver with Internal VCO

The high-frequency characterization of the transceiver test circuit with the internal VCO signal was performed using the measurements setups and techniques described in Section 4.4, but the signal generator part was activated and the input amplifier was de-activated. The transceiver test circuit consumes a DC current of 197 mA, 213.2 mA, and 270.1 mA from a single supply voltage of 3.3 V, respectively, for the transmitter, receiver, and transceiver operation modes. The total DC current consumption increases by approximately 15.7 mA when the injection input amplifier is enabled.



(a) Output frequency.

(b) Output power.

Figure 4.21: Simulated (S) and measured (M) output frequency and power results of the transceiver test chip using the internal VCO.

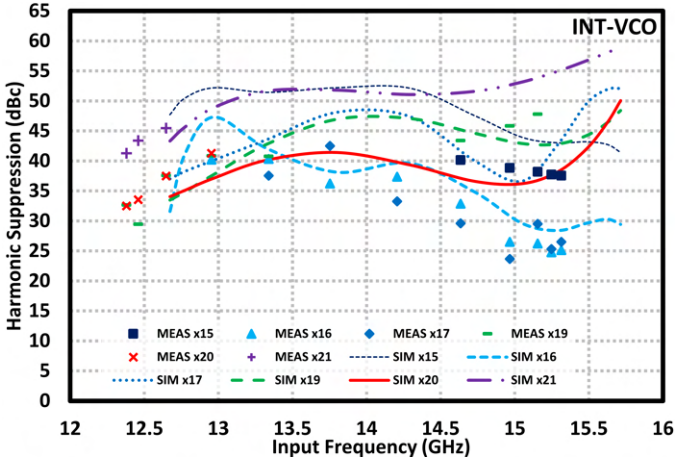
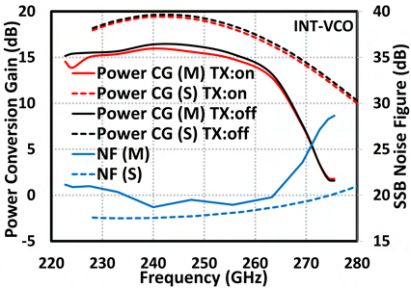


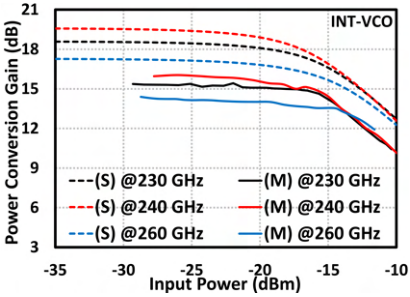
Figure 4.22: Harmonic suppression levels at the transceiver in/out pad for the internal VCO signal.

The tuning control voltage of the internal VCO was swept from 0 to 3.3 V with a step size of 0.3 V during the characterization of the transceiver test circuit with the internal VCO signal. Figure 4.21a shows the simulated and measured output frequency ranges of the transceiver test circuit versus tuning voltage. The measured operating frequency range is from 222.7 GHz to 275.6 GHz, resulting in a frequency tuning range of about 52.9 GHz. The simulated and measured output power levels at the transceiver in/out pad are presented in Figure 4.21b for the transmitter and transceiver operating modes. In the transmitter mode, the circuit achieves a peak output power of 3.3 dBm at 241 GHz, and its 3-dB bandwidth is around 43 GHz, from 220 GHz to 263 GHz. On the other hand, the transceiver test circuit has a peak output power value of 2 dBm at 241 GHz, and the 3-dB bandwidth extends from 220 GHz to 265 GHz in the transceiver mode. As also mentioned in Section 4.4, the output power difference between the transmitter and transceiver modes is very limited, indicating that the rat-race coupler provides a good level isolation between the transmitter and receiver channels as its simulation results. Consequently the in-band harmonic suppression measurements were carried out for only the transceiver operating mode. Figure 4.22 illustrates the simulation and measurement results of harmonic rejection performance at the transceiver in/out port. The measured harmonic suppression ratio is better than 23.6 dBc over the frequency tuning range of the internal VCO.

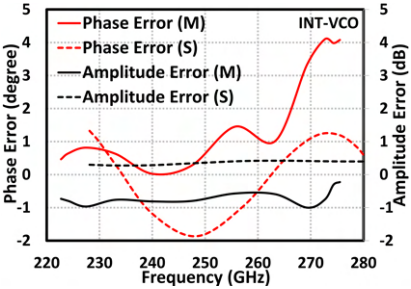
The simulated and measured down-conversion power gain results are shown in Figure 4.23a for the receiver and transceiver modes. The difference in the down-conversion power gain of the different operating modes is less than 0.5 dB across the frequency tuning range. Therefore, the remaining receiver measurements were performed for the transceiver mode only. The receiver channel in the transceiver test circuit achieves a measured peak down-conversion power gain of 16.5 dB at 240.5 GHz and has a 3-dB frequency bandwidth of about 40 GHz, from 220 GHz to 260 GHz. Figure 4.23a also presents the simulated and measured SSB noise figure versus operating frequency. The minimum value of the noise figure was measured to be 18.7 dB at 255 GHz. The measured noise figure is better than approximately 20.6 dB across the 3-dB frequency bandwidth. The simulated and measured down-conversion power gain values versus input power at operating frequency points of 230 GHz, 240 GHz, and 260



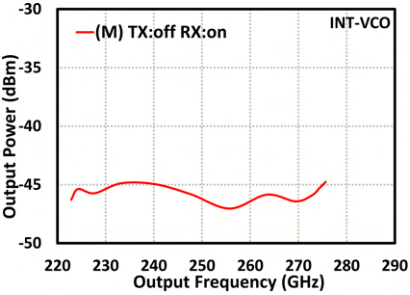
(a) Down-conversion power gain and noise figure.



(b) Transceiver-mode: down-conversion power gain versus input power.



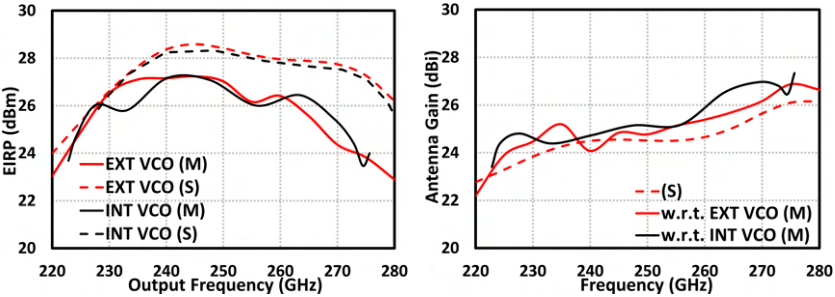
(c) Transceiver-mode: phase and amplitude error.



(d) Receiver-mode: Output power versus frequency.

Figure 4.23: Simulation (S) and Measurement (M) results of the transceiver test chip using the internal VCO signal.

GHz are shown in Figure 4.23b. The measured input referred 1-dB compression point is -15 dBm at 230 GHz, -16.4 dBm at 240 GHz, and -14 dBm at 260 GHz. Figure 4.23c presents the simulated and measured amplitude and phase error results. The circuit achieves an amplitude imbalance of lower than 1-dB and a phase error of less than approximately 4° along the frequency tuning range from 222.7 GHz to 275.6 GHz. These values ensure that the I/Q receiver channel has an image rejection ratio of higher than 23.5 dBc over the frequency tuning range [Raz97]. Finally, the output power at the transceiver in/out pad was measured while the receiver channel was enabled but the transmitter channel was disabled. The measured output power of the transceiver test chip while the transmitter channel is disabled is shown in Figure 4.23d. As also mentioned



(a) EIRP.

(b) Antenna gain.

Figure 4.24: Simulated (S) and measured (M) results of the transceiver chip with the silicon lens.

in Section 4.4, the measured output power values are lower than the minimum detectable power level at the reference plane of the measurement setup.

4.6 Characterization of the Transceiver with On-chip Antenna Coupled with Silicon Lens

The characterization of the designed transceiver loaded with the silicon lens was carried out using the test board shown in Figure 4.3. The distance between the DUT and WR-03 standard gain horn antenna was set to 40-cm. The signal received by the horn antenna was down-converted by RPG 220-325 GHz harmonic mixer with the LO signal provided by Rohde&Schwarz SMA 100B signal generator. The frequency of the signal generator was swept simultaneously with the operating frequency of the DUT to produce an IF signal of 18 MHz. The IF output of the harmonic mixer was measured using Rohde&Schwarz FSU-50 spectrum analyzer. The free-space path loss, the down-conversion of the harmonic mixer, and the antenna gain of the horn antenna were de-embedded from the measurement results.

The EIRP values of the designed transceiver coupled with the silicon lens were measured for both the external LO and internal VCO signals. As previously demonstrated in Sections 4.4 and 4.5, the difference in the output power results

between the transmitter and transceiver operating modes is negligible thanks to the high isolation rat-race coupler. Therefore, the EIRP measurement was performed only for the transceiver operation mode. Figure 4.24a presents the simulated and measured EIRP results of the transceiver coupled with the silicon lens for both the external LO and internal VCO signals. The transceiver exhibits a peak EIRP of approximately 27 dBm at around 242.5 GHz. The measured 3-dB frequency bandwidth in the bore-sight direction is about 50 GHz for the both cases, from 222.5 GHz to 272.5 GHz. The on-wafer output power measurement results of the transceiver and (4.1) were used to calculate the antenna gain of the designed on-chip bow-tie antenna loaded with the silicon lens, where G_A is the antenna gain, P_{EIRP} is the measured EIRP, and $P_{on-wafer}$ is the measured output power of the transceiver using on-wafer probes.

$$G_A = P_{EIRP} - P_{on-wafer} \tag{4.1}$$

The simulated and measured antenna gain results over frequency are plotted in Figure 4.24b. The agreement between the simulated and measured results can be considered as good enough by taking into account that the results were calculated using different measurement results of the different chips.

4.7 FMCW Characterization of the Transceiver

The FMCW functionality characterization of the designed transceiver was performed using the radar module presented in Figure 4.25. The radar module consist of the test board shown in Figure 4.3, an implemented baseband board, and the STM32 Nucleo-64 development board. The test board was plugged on top of the baseband board. The baseband board includes a fractional-N PLL (ADF4159) which has a 25-bit fixed modulus enabling the generation of highly linear FMCW chirps thanks to its high frequency resolution. A fourth-order RC loop filter with a loop bandwidth of 250-kHz was implemented on the test board by considering the trade-off between the speed of the frequency acquisition and the integrated phase noise. The IF-outputs of the transceiver are

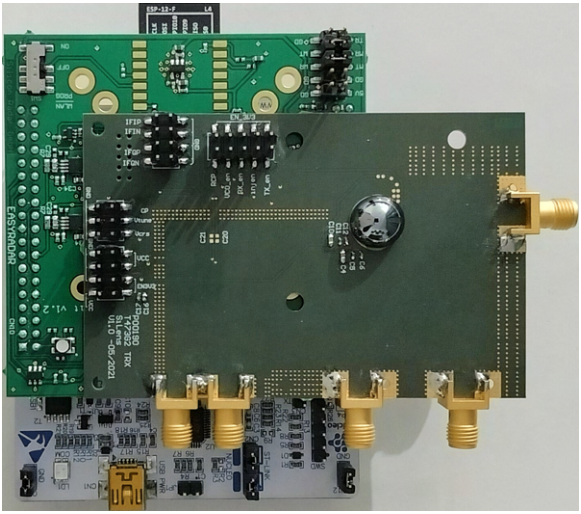


Figure 4.25: Assembled radar module.

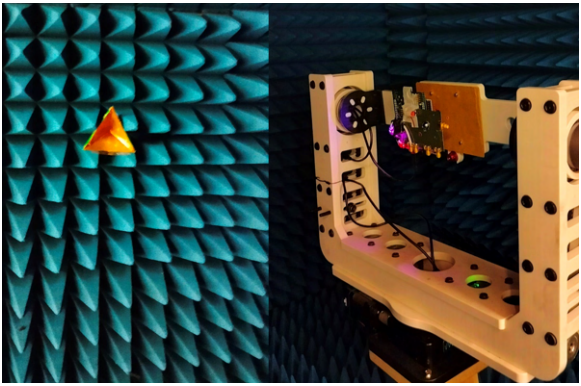


Figure 4.26: Antenna radiation pattern measurement setup.

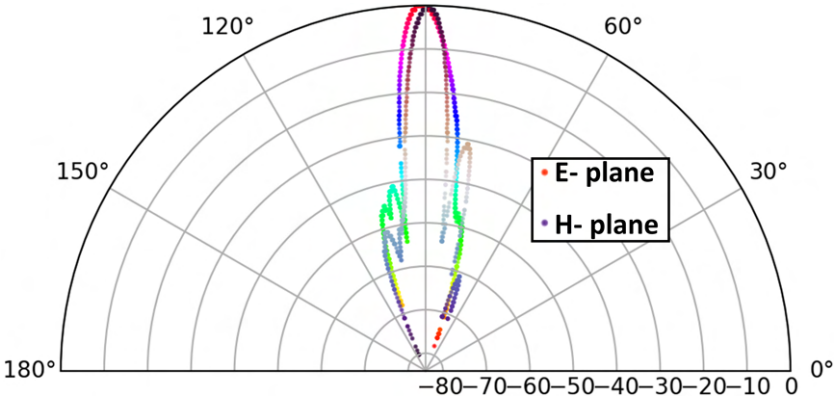
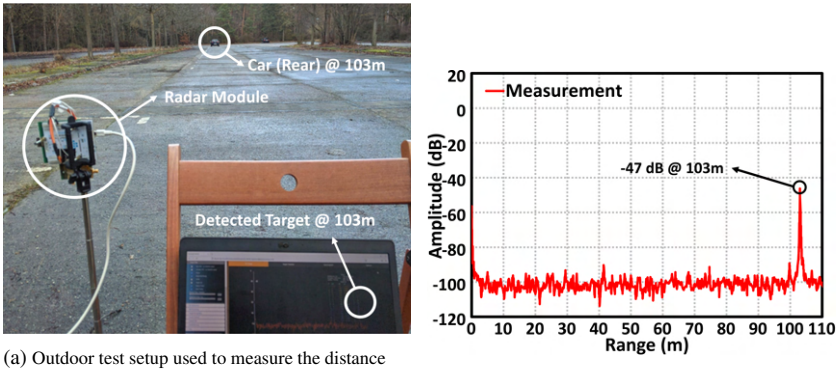


Figure 4.27: Measured antenna radiation pattern on both the E- (left) and H- (right) planes.

first amplified by an implemented baseband gain block consisting of cascaded op-amp (TL972IDGKR) based voltage gain amplifiers digitally controlled by a 4-bit gain controller. Then, an implemented analog low-pass filter is employed to filter out high frequency components and noise to anti-aliasing filtration before the digitization in order to satisfy the Nyquist sampling criterion. The implemented baseband board was plugged on top of the STM32 Nucleo-64 board including the STM32F303RE microcontroller unit (MCU). The MCU includes four 12-bit successive approximation ADCs converting the amplified and filtered IF output signals from the analog domain to the digital domain. The digitized signals are then processed for the fast Fourier transform (FFT). After the digital signal processing, the range profile of targets is visualized on a graphical user interface (GUI). The GUI allows setting the frequency modulation bandwidth, the number of chirp ramps, the length of the FFT, and the number of the FFT samples

The external PLL component can be locked in the maximum frequency range of 223 GHz to 275.4 GHz, which ideally results in a range resolution of approximately 2.9-mm. In addition, the far-field radiation pattern measurement of the DUT was performed using the radar module by setting its frequency modulation bandwidth to be 52.4 GHz so that the real two-way radiation pattern



(a) Outdoor test setup used to measure the distance of a vehicle parked 103-m away from the radar module.

(b) The measured range profile of the scene shown on the left.

Figure 4.28: Long-range FMCW test.

of the DUT was plotted for the FMCW operation. The radiation pattern of the DUT was measured in an anechoic chamber using an electronically controlled gimbal and a corner reflector. The gimbal positions the DUT to collect the measurement data for both the azimuth and elevation axes. As shown in Figure 4.26, the radar module was attached on the gimbal and the corner reflector was placed approximately 2-meters away from the DUT. Figure 4.27 illustrates the measured two-way radiation pattern for both the azimuth and elevation axes. The measured HPBW, 6-dB beamwidth for the two way radiation pattern, is 4.8-degree and 3.5-degree, respectively, for the E- and H- planes. The direction of the maximum gain is slightly tilted as can be deduced from the measured radiation pattern. The offset in the maximum gain direction is 2.4-degree and 3.7-degree, respectively, for the E- and H-planes. This was expected since it had been observed that the back surface of the rigid cardboard on which the radar module had been mounted was not uniformly flat due to the heads of the mounting screws.

Real-time FMCW range measurements of far and near targets were performed to investigate the performance of the designed transceiver. As will be presented in the performance comparison section, the designed transceiver loaded with the lens achieves the highest EIRP and the best receiver sensitivity among the

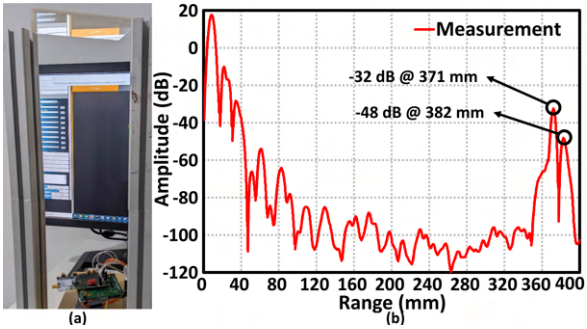


Figure 4.29: (a)Indoor test setup used to measure the thickness of a dielectric laminate (b) Measured range profile of the scene shown at left.

reported silicon-based 240 GHz radars. In order to justify this outstanding performance, the range of a vehicle parked 103-m away from the radar module was measured. Figure 4.28a shows the measurement setup used to detect the vehicle. The modulation bandwidth was set to 1.7 GHz with a center frequency of 240 GHz since the maximum sampling rate of the ADCs of the MCU is limited to 5 MS/s. The range profile of the observed scene is depicted in Figure 4.28b. The vehicle was detected with a high SNR, indicating that the maximum detectable range of the transceiver is far beyond 100-m. Then, the high range resolution capability of the designed transceiver was tested by measuring the thickness of a dielectric laminate as shown in Figure 4.29a. For this measurement, the modulation bandwidth was set to its maximum value of 52.4-GHz. Figure 4.29b presents the range profile of the observed scene of Figure 4.29a. The physical thickness of the laminate is 6-mm. However, the measured thickness is about 11-mm since the electromagnetic waves propagates at a lower speed in a material medium. Then, the relative dielectric constant of the laminate was calculated to be approximately 3.36 for the frequency range from 223 GHz to 275.4 GHz.

Tabel 4.3: Measured DC current consumption values of the designed transceiver chip.

Mode	EXT[1] LO	INT[2] VCO	INT[2] VCO + Injection-Locking
Transmitter	138.1 mA	197 mA	212.7 mA
Receiver	151.6 mA	213.2 mA	228.9 mA
Transceiver	208 mA	270.1 mA	285.9 mA

[1]EXT:External [2]INT: Internal

4.8 Performance Summary and Comparison

The chip area of the designed transceiver is 2.72 mm^2 (2.16 mm × 1.26 mm). It consist of the internal signal generation part, the input amplifier, the common-chain, the receiver, the transmitter, and the on-chip antenna loaded with the hyper hemispherical silicon lens. The transceiver chip can be configured in one of the following operating modes: transmitter, receiver, and transceiver. The measured DC current consumption values from a single supply voltage of 3.3V are summarized in Table 4.3 for all operating modes.

Table 4.4 presents the performance comparison of the designed transceiver chip with the previously reported radar front-end chips operating around 240-GHz in the literature. Although most of the reported studies are implemented in SiGe BiCMOS technologies, there are also studies demonstrating the implementations in III-V HEMT [MMW+19] and CMOS [YWC+21a] semiconductor processes. The radar front-end chip [MMW+19] implemented in the 35-nm III-V HEMT semiconductor technology exhibits the best noise figure and lowest power consumption. This performance is driven by that the f_{max} of the 35-nm III-V HEMT process is 1000 GHz, double the highest f_{max} value among other studies. The front-end chip [YWC+21a] implemented in the CMOS process achieves the highest down-conversion gain but it should be noted that it includes the IF amplification. In addition, it is based on the frequency comb technique and its measured down-conversion gain varies more than 10 dB over the operating frequency range. The radar transceiver chip presented in this dissertation achieves the highest EIRP of 27 dBm among all studies and the best noise figure of 16.2 dB among the silicon-based radar front-end chips although

Tabel 4.4: Comparison of the designed transceiver with the previously reported 240 GHz radar front-ends.

Study	**[MMW+19]**	**[TBP19]**	**[YWC+21a]**	**[JBP13]**	**[GSS+16]**	**[AFAS21]**	**[HEA+22]**	**This**
Technology	35-nm III-V HEMT	130-nm SiGe	65-nm CMOS	130-nm SiGe	130-nm SiGe	130-nm SiGe	130-nm SiGe	130-nm SiGe
f_T/f_{max} (GHz)	515/1000	250/400	-/280	240/380	300/450	250/370	300/500	300/500
Antenna	Waveguide	On-chip + PTFE Lens	On-chip + PMP Lens	On-chip + TPX Lens	On-chip + Silicon Lens	-	On-chip	On-chip + Silicon Lens
Configuration	Bistatic	Bistatic	Monostatic	Bistatic	Monostatic	Bistatic	Bistatic	Monostatic
3-dB BW[1]	40-GHz	-	-	-	27.5-GHz	30-GHz	65-GHz	41-GHz
VCO	EXT[2]	INT[3]	EXT[2]	INT[3]	EXT[2]	EXT[2]	EXT[2]	EXT[2]&INT[3]
FTR[4]	-	52-GHz	-	61-GHz	-	-	-	52.9-GHz
MF[5]	2	8	16	2	16	12	8	18
P_{peak}[6] (dBm)	8	1.8	-	-	5	10	-5.4	3.1
EIRP (dBm)	-	0.6 w/o lens	20	-1 w/o lens	-	-	-	27
RX Arch[7]	I/Q	Single	Single	Single	Single	Single	Single	I/Q
NF[8] (dB)	7	18.8	22.2	-	21.1	16	23.5[9]	15.7
RX CG (dB)	11	16.8	22	-	12.1	11	10.4[9]	16.2
Area (mm^2)	2.5	-	5	2.85	3.2	9	3.3	2.7
P_{DC} (W)	0.32	3.5	0.84	-	2	0.9	0.3	0.77[2] & 0.89[3]

[1]BW: Frequency bandwidth [2]EXT: External VCO [3]INT: Internal VCO [4]FTR: Frequency tuning range with INT VCO [5]MF: Multiplication factor [6]P_{peak}: Peak output power [7]RX Arch: Receiver Architecture [8]NF: If reported SSB NF for I/Q, then DSB NF=SSB NF - 3 dB [9]Simulation result

it is based on the monostatic configuration suffering from a significant performance drop due to the insertion loss of the coupler between the transmitter and receiver channels. Furthermore, it has one of the smallest chip area even though it has the highest multiplication factor of 18.

5 Conclusions

The design, implementation, and characterization of the ultra-high resolution radar front-end chip have been presented. It was implemented in IHP's 130-nm SiGe BiCMOS technology, SG13G2, with f_T/f_{max} of 300/500 GHz, offering high yield and very-large-scale of integration with moderate mask costs. The mainly targeted application for the developed radar front-end chip is the non-destructive inspection and characterization of materials. There are already published conceptual studies in this field of application, especially for the non-destructive characterization of GFRTs based composite materials. As stated in these studies, it is very crucial to provide high range and angular resolution for the analysis of the effects of damage on the mechanical and forming properties of GFRTs based composite materials. Therefore, in this dissertation, it has been aimed to develop a transceiver chip that operates in a broad frequency range to provide high range resolution and is suitable for building massive MIMO radar arrays to achieve high angular resolution. Furthermore, the designed transceiver chip is suitable to build massive MIMO radar arrays in the daisy-chain architecture thanks to its cascadable feature based on the ILO feedthrough synchronization technique. In this way, the drawbacks of the central LO signal distribution network in the conceptual massive MIMO radar studies can be avoided. In addition, the designed radar front-end chip has an external VCO input, making it also suitable for use in MIMO radar arrays based on the conventional central LO signal distribution architecture.

Among different signal waveforms employed in radar systems, the FMCW waveform is more suitable to build a radar with an ultra-high range resolution as it significantly alleviates the speed requirements and complexity of baseband circuitries. In an FMCW radar, the range resolution is inversely proportional

to the modulation bandwidth. Considering the technical constraints and the frequency regulation related limitations, it is more realizable to provide a wider absolute continuous frequency bandwidth by operating at a higher frequency. Therefore, the wideband frequency window around the 245 GHz ISM band was chosen for this project. In order to overcome the problems arising in the case of either using fundamental VCO or low frequency multiplication factor, a frequency multiplier circuit with a multiplication factor of 18 was employed to move the generated chirp signal into the frequency range of interest. The AoC concept was preferred for radiation considering the limits of today's packaging technologies. Since integrated antennas radiate out the significant amount of energy through the silicon substrate from the back side of the chip, a hyper hemispherical silicon lens was attached on the back-side of the chip to enhance the antenna gain. In the bistatic antenna configuration, it is not realizable to align the focal plane of the lens so that it passes through the radiation centers of both transmitting and receiving antennas. Therefore, the monostatic antenna configuration was preferred and a high-isolation rat-race coupler was placed, enabling simultaneous receiving and transmitting. A digital control circuit was employed to enable the transceiver to be configured in one of the following modes: transmitter, receiver, and transceiver.

The MIMO array concept is perfectly suited for estimating the DoA of targets at high angular resolution. In a MIMO radar array, the waveform orthogonality between transmitting elements can be achieved by utilizing a multiplexing technique to synthesize virtual antenna arrays. The TDM is the most suitable multiplexing scheme to provide waveform diversity for massive MIMO radar arrays since it does not need the high sampling rate for the digitization unlike other techniques such as FDM and CDM. The sparse non-uniformly spaced array technique can be utilized to increase the angular resolution without reducing the unambiguous FoV of a MIMO radar array. It also enables the use of larger antenna structures such as horn antennas and plastic or silicon lenses offering higher antenna gain and better SSL, since the inter-element spacing is increased. The frequency synchronization between array elements is required in TDM MIMO radar systems. On the other hand, the phase mismatch between array elements can be easily calibrated in the digital domain. Therefore, the

I/Q receiver architecture was utilized to enable the complex signal sampling required for the phase calibration techniques. Key design parameters or requirements of MIMO radar arrays, such as angular resolution, unambiguous FoV, and SSL, differ from application to application. If the centralized LO signal distribution topology is employed, the power budget calculations and the design of the LO signal distribution network must be re-performed according to the number of physical array elements and the inter-element spacing requirements for each application. On the other hand, in the daisy-chain method, the need for this bulky and costly LO signal distribution network is eliminated thanks to its scalable structure by cascading multiple array elements. The employed ILO feedthrough synchronization technique more relaxes the power requirements in the cascading operating compared to the conventional LO feedthrough method. In addition, it can be proposed that the phase-shifting capability of the ILO feedthrough technique enables the analog beamforming of the transmitter channels. In this way, a hybrid MIMO phased-array can be also built using the proposed transceiver architecture, thus it can benefit from the coherent processing gain.

The transceiver exhibits a peak EIRP of approximately 27 dBm at around 242.5 GHz. The measured 3-dB frequency bandwidth is about 50 GHz for the both external and internal VCO configurations, from 222.5 GHz to 272.5 GHz. The measured HPBW, 6-dB beam-width for the two way radiation pattern, is 4.8-degree and 3.5-degree, respectively, for the E- and H- planes. The FMCW functionality characterization of the designed transceiver was performed using the assembled radar module. The external PLL component can be locked in the maximum frequency range of 223 GHz to 275.4 GHz, which ideally results in a range resolution of approximately 2.9-mm. The designed transceiver loaded with the lens achieves the highest EIRP of 27 dBm among all studies operating around 240 GHz and the best noise figure of 16.2 dB among the silicon-based 240 GHz radar front-end chips. This outstanding performance has been proved by measuring the distance of a vehicle parked 103-m away from the radar module. In addition, the high range resolution capability has been demonstrated by a thickness measurement.

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