IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received 16 February 2024, accepted 22 March 2024, date of publication 2 April 2024, date of current version 15 April 2024.

Digital Object Identifier 10.1109/ACCESS.2024.3384296

RESEARCH ARTICLE

Wideband BPSK Transmitter Phased Array Operating at 246 GHz With ±30° Steering Range

JOACHIM HEBELER[1], (Graduate Student Member, IEEE), LUCA STEINWEG[2], (Graduate Student Member, IEEE), FRANK ELLINGER[2], (Fellow, IEEE), AND THOMAS ZWICK[1], (Fellow, IEEE)

[1]Institute of Radio Frequency Engineering and Electronics, Karlsruhe Institute of Technology, 76131 Karlsruhe, Germany
[2]Chair for Circuit Design and Network Theory, Technische Universität Dresden, 01069 Dresden, Germany

Corresponding author: Joachim Hebeler (joachim.hebeler@kit.edu)

This work was supported in part by German Research Foundation (DFG) in the Framework of the Project Adaptive Integrierte Millimeterwellen Sender (ADAMIS) under Project 394221495, and in part by the Bundesministerium für Bildung und Forschung (BmBF) within the funding for the Program Forschungslabore Mikroelektronik Deutschland (ForLab) under Grant 16ES0948.

ABSTRACT This paper presents the construction and measurement of a phased array BPSK transmitter system operating at 246 GHz with tested data rates of up to 32 Gbit s^{-1}. The system is built using custom monolithic microwave integrated circuit (MMIC) and a novel packaging solution. The construction showcases the flexibility in the chosen approach, paving a path for future systems. It is the first TX array with significant beam steering capabilities tested above a pure antenna pattern stage above 200 GHz. The system is tested for realistic usage scenarios. Bit-error-rate (BER) measurements are used to showcase real-world usability. BER over angle and BER over steering angle are measured to verify the operation of the transmitter.

INDEX TERMS BPSK, MMIC, mmWave packaging, mmWave transmitter, phased array.

I. INTRODUCTION

With the rapid expansion of internet-connected devices and available data rates, we see an ever-increasing utilization of digital technologies and services. This demand and utilization of data and data-driven applications pose a continuous demand for even higher data rate communication links, connecting the backbone of the internet and the user equipment (UE). Past advancements are largely based on higher spectral utilization by employing higher-order modulation. This is made possible by higher integration density and lower power digital electronics [1]. Higher order modulation necessitates higher linearity in the used radio-frequency (RF) systems and a more complex baseband circuitry, which is power-hungry. As we approach a limit of spectral utilization, other paths are explored. One option currently of interest is the adoption of higher operating frequencies, which allow for more bandwidth, higher data rates, and more channels to ease congestion. Currently interesting are the bands around 140 GHz [2] and 240 GHz [3], which are mainly driven by atmospheric absorption windows and solid state transistor performance. The advancements in silicon-based transistor technology enable commercially viable exploitation of the available bandwidth at these mm-wave frequencies. However, transistor technology is only one part of the equation. While higher operating frequencies open up more bandwidth, antenna sizes shrink, increasing the free space path loss (FSPL). This, together with limited transistor output power [4], limits the applicable range of such systems with some previous works reporting tested distances of less than 15 cm [5], [6] to achieve functional data links. One approach to compensate for this is high gain antennas with [7] reporting 850 m of the tested range. While an astounding result, the employed antennas with 55 dBi gain are mechanically large and unpractical for anything but stationary point-to-point links. Further, the small beam width of such antennas makes it almost impossible to aim correctly outside of static installations, rendering it useless for UE scenarios where a device is portable.

The associate editor coordinating the review of this manuscript and approving it for publication was Pavlos I. Lazaridis.

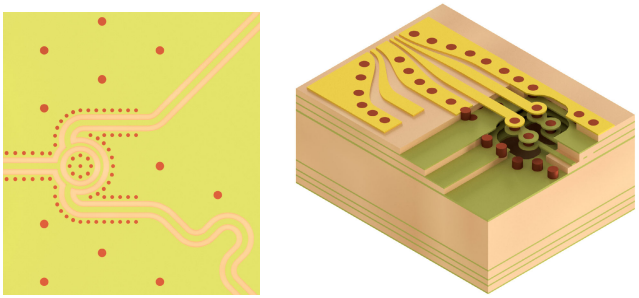
A logical next step is the combination of multiple antennas fed by multiple transmitters to achieve higher transmitted power and electronic beam steering capabilities. With this approach, high antenna gain can be combined with flexibility in beam pointing. As the antennas are small compared to typical device dimensions intended to be used by humans, even larger phased arrays are small enough to fit within UE [8]. While conceptually not novel, the terahertz domain still poses specific challenges. Aiming at large relative bandwidths within each communication channel, simple phase-shifting typologies reach their limit and must be replaced with true time delays [9]. Synchronization and delay compensation of all local oscillator (LO) and baseband (BB) signals become detrimental to achieving proper phase steering. Lastly, the integration challenge is still open. Packaging monolithic microwave integrated circuits (MMICs) and antennas at terahertz frequencies is challenging as transitions between different technologies are lossy and hard to assemble due to their size. This motivates many to use on-chip antennas [6]. Choosing this approach limits the application range the MMIC can be used in. For one, the antenna is fixed and only minor influence post production is possible and secondly, the available choices for on-chip antennas is limited due to the constraints of the back-end-of-line (BEOL) metal layers.

This paper presents a novel approach to assembling our phased array system. By employing a differential bond wire interconnect [10], we can measure our MMIC separately [11] and connect it to external antennas [12]. While the targeted data rates necessitate a true-time delay architecture, the used MMIC has an LO steering phase shifter. This deliberate choice is a trade-off between chip size, design complexity, and influence on the phased array [9].

Building upon this, we describe the assembly and measurement of a 1×2 phased array transmitter, as a proof of concept. First, we describe the setup of the transmitter and the details of routing and feeding the necessary wide bandwidth and high-frequency baseband and local oscillator (LO) signals to the MMIC. Next, the measurement setup is described, and the measurement results are discussed and compared to the state of the art. We use a bit error rate (BER) test setup to quantify the operating performance of our assembled system not only for a static link case but also for beam steering and off-boresight connection.

II. SYSTEM ASSEMBLY

The used MMIC is described in [11], and the general construction of the printed circuit board (PCB) is comparable to the design shown in [12]. Building the system on a PCB has some distinct advantages. Firstly, the integration challenge of direct-current (DC) and RF signals is reduced, as many solutions are available, especially for RF connectors. Further, it also highlights the ease of usage of the designed MMICs, as more costly systems in package solutions are avoided. However, realizing the phased array structure on the PCB, the LO signal has to be distributed to all MMICs, and the differential baseband signal has to be fed with as low of a transmission line length difference as possible. A Rat Race power splitter is constructed to implement the LO distribution. The geometry is shown in Fig. 1a. The ring has a diameter of 1.5 mm and a track width of100 µm. The grounded coplanar waveguide line coming from the connector and feeding the MMICs is 200 µm wide with a 200 µm gap. The feeding lines to the MMICs are length-matched using rounded meanders, as also visible from Fig. 1a. The MMICs have a very low necessary input LO power with only −10 dBm, simplifying the LO distribution. No additional amplifier is needed to compensate the passive power splitter. The thru measurement of rat race splitter is shown in Fig. 2. The design is centered around 64 GHz, with a lower cutoff of 40 GHz. The splitter has an insertion loss of 3.4 dB per branch, as shown in the green and purple lines. Therefore, the splitter has 0.4 dB of loss. In order to measure the splitter, feeding lines and the RF connectors are attached. The RF connectors introduce some reflections and additional loss. Thus, a simulation, including the connectors, is compared to the measurement. In the realized test sample, more reflection is present, showing higher losses around the target frequency and an asymmetry in the transmission. The asymmetry is due to the RF connectors, as the splitter and feeding lines are mirror symmetric. The feeding lines, in theory, add 3 dB more loss, and the measurement shows a loss of an average of 4 dB. Overall, the splitter operates as expected and within performance and manufacturing tolerances.



(a) Rat Race Splitter **(b) Differential Stripline Transition**

FIGURE 1. Layout of the realized rat race splitter and differential wideband transition into the PCB as a stripline.

Another challenge poses itself as the routing of the differential baseband signals. The MMICs are tested for data rates exceeding 50 Gbit s^{-1}, necessitating the careful design of the differential lines to minimize skew, offset, and band-limitation. A differential transition to stripline is necessary to achieve the targeted analog bandwidth of 50 GHz and satisfy routing demands. The principle construction is shown in Fig. 1b. The main challenges are compensating the additional capacitance by the vertical interconnect access (VIA) annular ring, reducing ground return inductance, and minimizing coupling between LO and baseband. This is achieved by adding VIA shielding around the transition and optimizing the ground profile around the

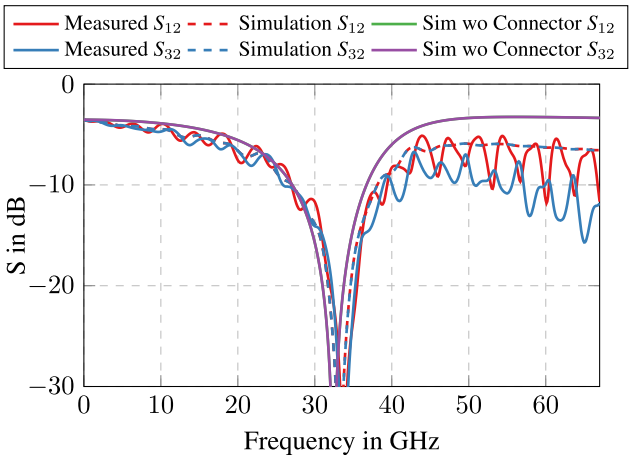


FIGURE 2. Measured and simulated S-parameters of the rat race power splitter.

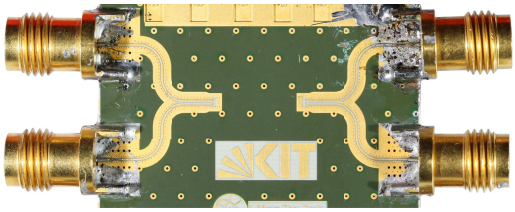


FIGURE 3. Test sample for the differential thru with the transition into the PCB.

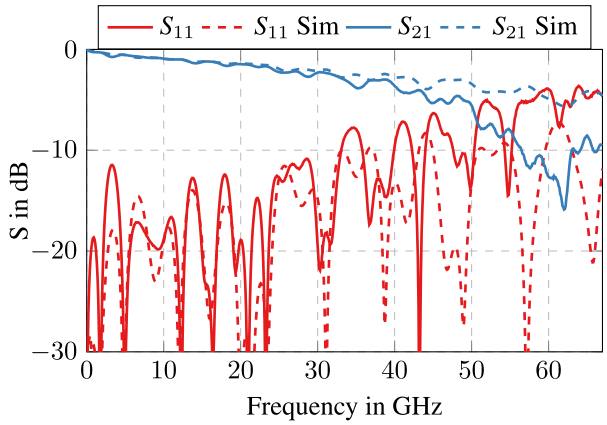


FIGURE 4. Measured and simulated S-parameters of the differential transition test structure.

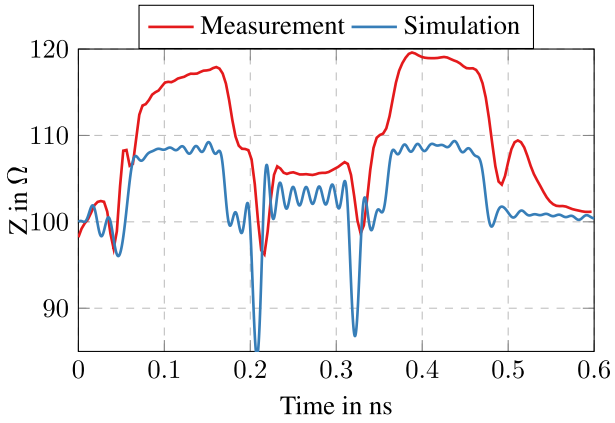


FIGURE 5. Measured and simulated time domain reflectometry plot of the differential transition.

signal VIAs. A through test structure is built to test the transition. The assembly is shown in Fig. 3. The simulated and measured response for this thru test structure with the via transition into the PCB back to back is shown in Fig. 4. The simulation shows an input return loss of less than −10 dB up to 42 GHz and an acceptably flat insertion loss. However the measurements show, that the input match exceeds −10 dB already at 32 GHz and an excessive loss after 50 GHz. Observing the impedance step response of both simulation and measurement presented in Fig. 5, a higher differential line impedance in the section connecting the RF connectors to the stripline transition is present. This worsens the input match significantly. The root cause for this is suspected to be a change in prepreg layer height. The design uses a 89 µm prepreg layer, which can, however, be significantly higher due to the solid ground plane [13]. The transition is rather decent and shows only a slight capacitive behavior, less than in the simulation.

Fig. 6 shows the realized sample for the 1×2 array system. Fig. 7 shows a closeup of the MMICs and the antennas. The wavelength in the air at the operating center frequency of 246 GHz is 1.224 mm, which would implicate an antenna spacing of 0.6112 mm for ideal grating lobe free operation. The realized construction presents an ideal case where the antennas could be placed as close as possible together. However, the realized distance between the elements is 680 µm, more than the ideal $\lambda/2$ spacing. This is due to the fundamental connection between bandwidth and antenna size [14]. The antenna is designed to cover at least 20% relative bandwidth, so it is physically larger than $\lambda/2$. This also has implications for larger array configurations, as maximum scan angle, minimum pulse length, and targeted RF bandwidth must be trade-offs against each other.

Another aspect visible from the construction in Fig. 7 is the physical size of the employed MMICs. They measure 1600 µm by 837 µm which is larger than $\lambda/2$. Shrinking the MMIC size is not viable as the main size contributors are the DC and RF pads. One can overcome some of these issues by combining multiple channels into one MMIC. However, this comes at the expense of chip cost, limited flexibility, and design effort. In the present case, some alternative antenna and routing concepts can aid in solving the routing challenge. Further investigation of these concepts is omitted in this publication to focus on the measurement aspect of wideband phased arrays.

The used antennas are shorted differential bow-tie elements manufactured in a complementary metal oxide semiconductor (CMOS) technology's BEOL process. The shorted bowtie is very inefficient on its own due to the short height between bowtie element and ground plane. A resonator is

glued on top to increase the overall efficency and antenna pattern. The resonator is a 104 µm thick glass with a thin gold layer structured into 9 square resonators of different sizes. The antenna is the same as presented in [12]. The chips are laser-diced and glued into place. The dicing process leaves a slight angle to the cutting edge, causing increased chip separation. All components are bonded together using 17 µm gold bond wire.

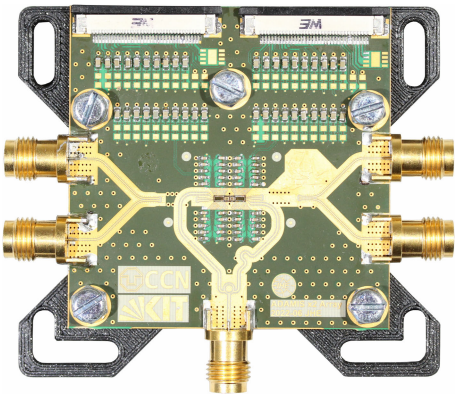


FIGURE 6. Photograph of the realized 1 × 2 array PCB.

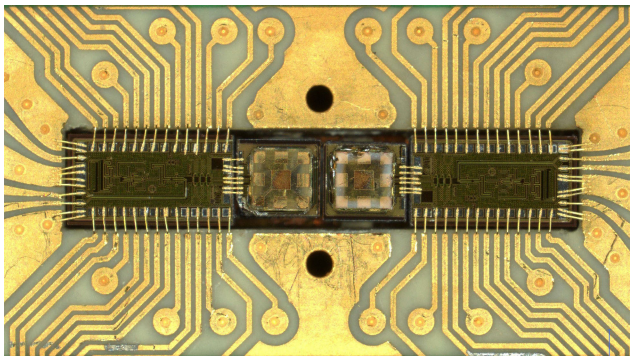


FIGURE 7. Closeup of the realized 1 × 2 array MMICs and antennas.

III. MEASUREMENT

The system is measured using a modified free space antenna measurement station as described in [12]. The measurement setup is conceptually shown in Fig. 8. The LO signal for the device under test (DUT), **D**, is generated by a *Keysight N5247B* vector network analyzer (VNA), denoted **A**. The baseband signals are generated by a *Keysight M8194A* arbitrary waveform generator (AWG). A separate AWG channel feeds the baseband input of every MMIC in the DUT; however, all channels output the same synchronized waveform. The transmitted signal is received by a *VDI MixAMC-I WR-3.4* wideband receiver, denoted **E**. The LO signal for the receiver is also generated by the *N5247B* to guarantee synchronicity between the different LO signals. To measure the RF performance, the intermediate frequency (IF) output of the receiver is connected to the *N5247B* in spectrum analyzer mode. To measure the BER, a wideband amplifier *SHF 804 TL* is used to buffer the amplitude and feed into a *Keysight UXR 1104A* real-time oscilloscope to capture the waveform. A known source in the form of a *VDI VNAX WR3.4* T/R module is used to calibrate the receiver. This yields a received power as given in equation 2. The received power depends on the transmitted power $\mathrm{EIRP_{TX}} = P_{\mathrm{TX}}(f_{\mathrm{RF}}) \cdot G_{\mathrm{TX}}(f_{\mathrm{RF}})$, the free space path loss, the receiver antenna gain $G_{\mathrm{RX}}(f_{\mathrm{RF}})$ and the transfer function of the receiver $H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}})$.

$$P_{\mathrm{RX}}(f_{\mathrm{IF}}) = P_{\mathrm{TX}}(f_{\mathrm{RF}}) \cdot G_{\mathrm{TX}}(f_{\mathrm{RF}}) \cdot \mathrm{FSPL}(f_{\mathrm{RF}}) \tag{1}$$

$$\cdot G_{\mathrm{RX}}(f_{\mathrm{RF}}) \cdot H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}}), \tag{2}$$

$$P_{\mathrm{RX}}(f_{\mathrm{IF}}) = \mathrm{EIRP_{TX}}(f_{\mathrm{RF}}) \cdot \mathrm{FSPL}(f_{\mathrm{RF}}) \tag{3}$$

$$\cdot G_{\mathrm{RX}}(f_{\mathrm{RF}}) \cdot H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}}), \tag{4}$$

$$H_{\mathrm{RX}}(f_{\mathrm{RF}}, f_{\mathrm{LO}}) = \frac{P_{\mathrm{RX}}(f_{\mathrm{IF}})}{\mathrm{EIRP_{TX}}(f_{\mathrm{RF}}) \cdot \mathrm{FPSL}(f_{\mathrm{RF}}) \cdot G_{\mathrm{RX}}(f_{\mathrm{RF}})}. \tag{5}$$

The RF signal f_{RF} is swept through the whole band, and the received power for different LO signal offsets f_{LO} is captured. As $P_{\mathrm{TX}}(f_{\mathrm{RF}})$ and $G_{\mathrm{RX}}(f_{\mathrm{RF}})$ are known, the EIRP is known. The free space path loss $\mathrm{FSPL}(f_{\mathrm{RF}})$ and the receiver antenna gain $G_{\mathrm{RX}}(f_{\mathrm{RF}})$ are then absorbed into the transfer function of the receiver that is measured. With this information, the inverse can be calculated and used to calibrate the measurements. The BER is measured by capturing 20 µs

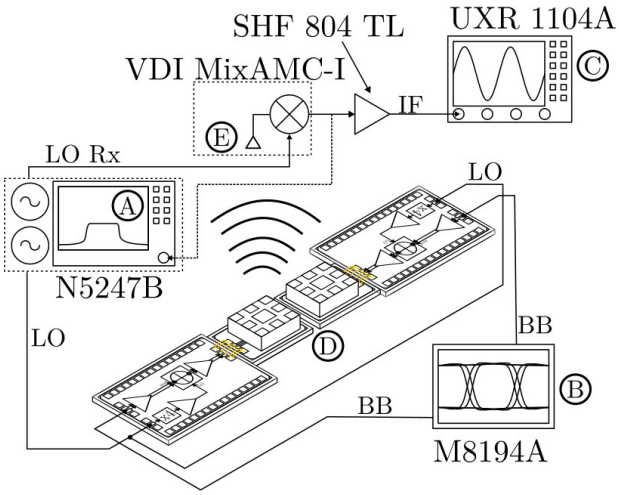


FIGURE 8. Schematic Measurement Setup.

long data bursts with the real-time oscilloscope. These data chunks are then processed on the oscilloscope, and the results are transmitted to a control computer. The demodulation signal chain is shown in Fig. 9. The IF signal from the receiver is down-converted digitally into an in-phase and quadrature (IQ) stream without phase correction. The IQ data then correlates to the transmitted sequence to recover the timing and phase over time as it sees significant drift within one decoding frame. Using this information, the IQ stream is corrected to put the signal energy into the I-data, filtered using a matched filter, and equalized. The bits are extracted

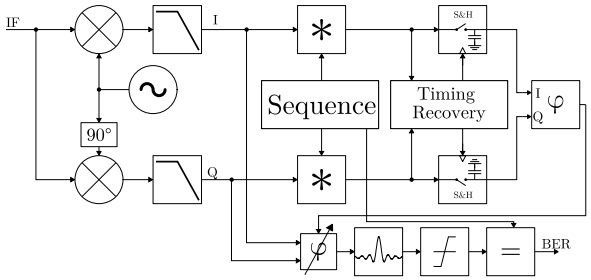


FIGURE 9. Block Diagram of the signal processing.

and compared to the transmitted sequence, calculating the bit error rate. All sources of the measurement setup are locked together with a 10 MHz reference. However, small drifts over time and mechanical movement in the receiver cause a constant phase shift. To mount the DUT, custom holders are 3D printed and mounted in the rotation center of the measurement arm. The LO and baseband signals are fed through cables from the measurement equipment outside the measurement arm's movement region. Fig. 10 shows the DUT mounted in the measurement system. The DC supplies are mounted underneath the DUT.

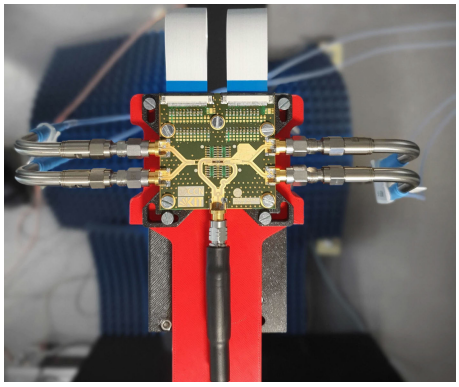


FIGURE 10. Measurement Setup of the realized system.

A. RF PERFORMANCE

First, the RF performance of the system is measured. The beam is centered to broadside radiation, and the equivalent isotropic radiated power measurement (EIRP) is captured over the frequency with the center frequency set to 246 GHz. The EIRP is shown in Fig. 11. Also shown is the frequency response of a transmitter only using a single chip as a [12]. Below 240 GHz, the array shows a higher gain and more output power as expected with an average 6 dB higher EIRP, which is in line with 3 dB of array gain and around 3 dB of power gain. However, above 246 GHz, the output power drops sharply, being 8 dB lower than the single antenna element. First, the antenna pattern is investigated to rule out issues with the chosen antenna structure. The simulation of the boresight gain of the two antennas is plotted in green dashed lines. The array has a very broad uniform gain and, thus, is not the underlying issue. Further analyzing potential connection issues with the antenna did not show significant deviation. Another aspect investigated is the two-tone response of the power amplifier (PA) in compression. The simulation results are plotted in purple dashed lines. The PA will drop the output power of the upper sideband if operated into compression. This is comparable to the observed behavior. This might result from the two systems influencing each other, causing the PAs to go into compression due to crosstalk [15].

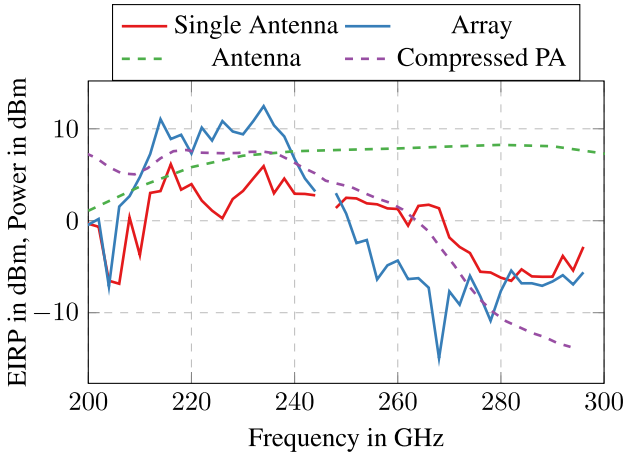


FIGURE 11. Measured frequency response at boresight with 246 GHz center frequency.

Next, the pattern of the system is measured for different phase control settings at 246 GHz. For this, the receiver is swept around the DUT, and the EIRP is captured. The results are shown in Fig. 12. The resulting beam can be controlled ±30° around the center with sidelobes appearing for larger steering angles. This is due to the non $\lambda/2$ spacing. The steering is relatively symmetric, as expected. The pattern matches the simulation results well, proving the correct operation of the antennas and the phase steering.

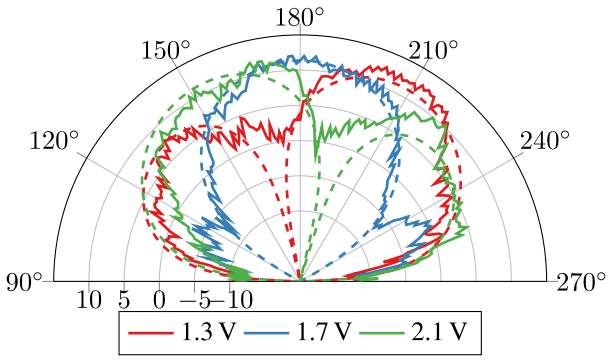


FIGURE 12. The EIRP antenna pattern in dBm for different steering values at 246 GHz. The scaled simulation in dB is shown in dashed lines.

B. BIT ERROR RATE

The bit error rate is measured to evaluate the transmission quality. The BER over data rate at boresight is measured in the first measurement and shown in Fig. 13. The BER is compared against the single chip measurement presented

in [12]. The higher signal energy of the two transmitters increases the signal to noise ratio (SNR), and the system shows lower BER up to 22 Gbit s^{-1}. Above that data, the BER for both systems converges. This is likely due to the upper-frequency band limitation already measured in Fig. 11.

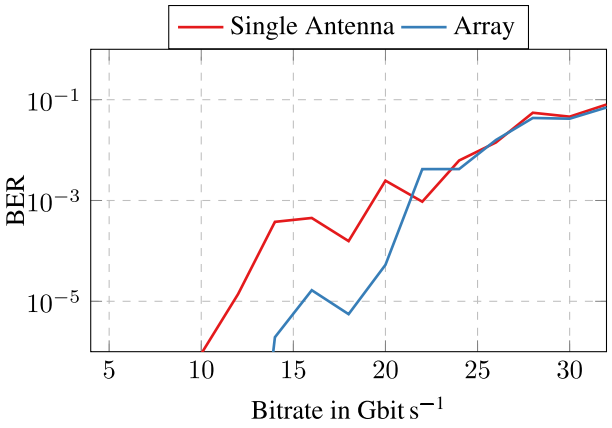


FIGURE 13. Measured BER at boresight for the array an a single antenna transmitter.

The BER is evaluated over the receiver angle sweeping the upper hemisphere. The results are shown in Fig. 14. The beam is not pointed straight up but at a 190° angle due to a calibration error in the phase control. This yields a significant drop in BER around 150°, which aligns with the measured antenna pattern. For this, the theoretical BER curve for the used antenna steering is calculated and plotted in dashed lines for comparison. While for lower bit-rates, the calculated BER matches theory, the higher data rates of 16 Gbit s^{-1} and 32 Gbit s^{-1} have a significant increase in BER at the center frequency where they should be minimal. This is assumed to be another artifact from the PA cross-talk and the induced compression artifacts [15]. We assume that the phase shift of different frequency components is different, transmitting different parts of the data signal in different directions, causing the drop in BER compared to the pure two-tone RF measurement for the RF patterns.

Lastly, the effect of beam steering on BER is measured. For this, the receiver is swept through the theoretical steering limit of 165° to 207°, which is the numerical center of the measured pattern. The numerical steering limit differs from the true array steering range due to the ripple on the pattern. The maximum value of each pattern is chosen for the lookup table, resulting in a slightly lower tested steering range. The array is steered to point at the receiver, and the BER is captured. The plot is shown in Fig. 15. Firstly, the LO phase steering seems to be working acceptably for the tested data rates. This is the first tested transmitter system using LO phase steering above 200 GHz. Comparing the BER of the 16 Gbit s^{-1} measurement shown in Fig. 14 to the measurements over steering angle, no peak in BER is visible, thus the steering improves the BER. However, the BER measures better below 180°. As the system is symmetric, antennas and MMICs are the same,

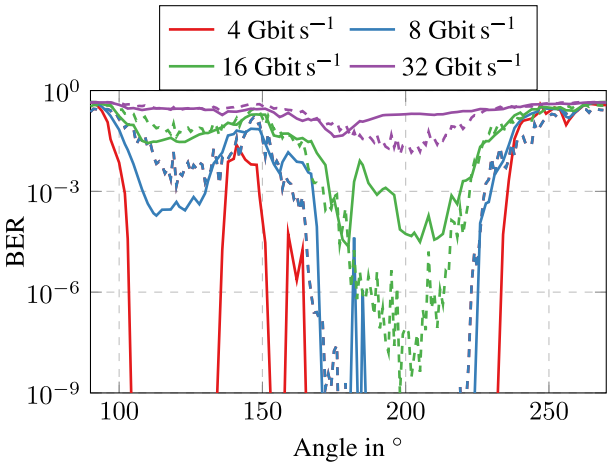


FIGURE 14. Measured BER with the beam pointed to 190° over angle. In dashed lines, the theoretical BER curves calculated from the antenna pattern are plotted.

so no such behavior should be present. Investigating the measured antenna steering pattern shown in Fig. 12, a slight difference in the pattern for 150° compared to 210° is visible. Further, from Fig. 14 an issue in the data transmission for 16 Gbit s^{-1} at 200° is known. One conclusion here is that the superposition of the two modulated signals has an angle-dependent issue.

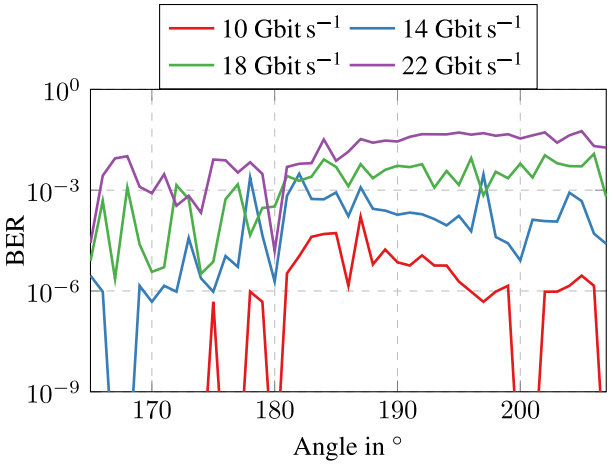


FIGURE 15. Measured BER over pattern steering angle with the beam pointed to the receiver.

Comparing the system to the state of the art presented in Tab. 1, we demonstrate the first phased array transmitter system above 200 GHz testing data rates up to 32 Gbit s^{-1}. The demonstrated steering angle and system bandwidth are competitive and, in part, exceeding the state of the art. The demonstrated packaging solutions are promising for future integration of commercial THz-transmitter systems and are, as presented here, the first of their kind. We demonstrated the broadest analysis of a phased array transmitter above 200 GHz, analyzing BER over a static link and angle, beam steering, and data rate. A similar analysis was done in [19]

TABLE 1. Comparison to the state of the art in THz phased array systems.

	This Work	[16]	[17]	[18]	[19]	[20]	[6]
Array	1x2	2x4	1x4	1x4	1x4	4x4	1x4
Technology	130 nm SiGe	45 nm CMOS	130 nm SiGe	45 nm CMOS	InP, GaAs	55 nm SiGe	130 nm SiGe
Scanning Angle	±30°	±35°	±12°	±18°	±30°	±30°	±45°
Antenna Type	Off-Chip Bowtie	On-Chip with Superstrate	SIW Cavity backed On Chip	Off-Chip Vivaldi	Reflector Antenna Array	Patch Antenna on PCB	On-Chip Patch and Lens
System Type	Tx	*Rx*	Tx	Tx/Rx	*Rx*	Tx/Rx	Tx/Rx
Power[a]	818 mW	1.16 W	1 W	750 mW	2.7 W	4.9 W	2.5 W
Center Frequency	246 GHz	140 GHz	320 GHz	256 GHz	215 GHz	150 GHz	140 GHz
Bandwidth	30 GHz	16 GHz	20 GHz	-	40 GHz	20 GHz	60 GHz
Distance	36 cm	35 cm	15 cm	3.5 cm	11.24 m	34 cm	15 cm
EIRP	12 dBm	-	10.6 dBm	−14 dBm[b]	-	26 dBm[c]	0.4 dBm[c]
Tested Data rate	32 Gbit s^{-1}	10 Gbit s^{-1}	-	26 Gbit s^{-1}	32 Gbit s^{-1}	0.104 Gbit s^{-1}	200 Gbit s^{-1}

[a]Reported DC power for Tx if applicable.
[b]From measurement plot, not reported explicitly.
[c]Calculated from P_{sat} and theoretical antenna gain.

for a phased array receiver system, although fewer data points in angle and data rate were captured and analyzed. Another apparent benefit shown in this work is the suitability of SiGe technology for phased array systems. While [19] achieves excellent RF performance, using III-V semiconductors comes at the price of very high power consumption and an excessively complicated assembly challenge combining many RF function blocks on the system level. Compared to works using CMOS such as [18], a significantly higher transmit power is achievable. Compared to works in similar technology, such as [6] and [17], a significant improvement in output power is reported here. A similar EIRP as in [17] is achieved with half the antennas and output channels. The work present in [6] is even worse with a reported P_{sat} of only −8 dBm per channel due to integration challenges in the reported design. The power supply routing is especially mentioned as an issue, which is alleviated within our work by employing DC routing on the multilayer PCB. Further, due to the complexity of the desired IQ architecture, the reported power consumption is 56% higher than a comparable 1 × 4 system realized with our proposed architecture. While undoubtedly higher spectral efficiency and, thus, the data rate can be achieved by using IQ modulation, this comes at the cost of power consumption and range.

IV. CONCLUSION

This work presents the first phased array transmitter realization built from discrete MMIC chips and antennas assembled into one package on a commercial PCB. This is the first system operating above 200 GHz built this way and shows the modularity and flexibility of the chosen approach and applicability for future commercial systems. This clearly demonstrates the feasibility of larger array implementations above 200 GHz. We demonstrate in detail the measurement of the system RF pattern and, with a significant focus, the data rate measurements over realistic usage scenarios. Utilizing the bit error rate, we investigate the influence of the system RF behavior over receiver angle and steering. To the author's knowledge, this is the first work investigating the steering behavior on wideband data transmission using LO phase steering. We are also the first to measure BER over steering angles above 200 GHz for transmitters. Our assembled system shows competitive data rates and output power over the state of the art.

REFERENCES

[1] R. Dangi, P. Lalwani, G. Choudhary, I. You, and G. Pau, "Study and investigation on 5G technology: A systematic review," *Sensors*, vol. 22, no. 1, p. 26, Dec. 2021. [Online]. Available: https://www.mdpi.com/1424-8220/22/1/26

[2] W. K. Alsaedi, H. Ahmadi, Z. Khan, and D. Grace, "Spectrum options and allocations for 6G: A regulatory and standardization review," *IEEE Open J. Commun. Soc.*, vol. 4, pp. 1787–1812, 2023.

[3] A. Pärssinen, M.-S. Alouini, M. Berg, T. Kuerner, P. Kyösti, M. E. Leinonen, M. Matinmikko-Blue, E. McCune, U. Pfeiffer, and P. Wambacq. (2021). *White Paper on RF Enabling 6G—Opportunities and Challenges From Technology to Spectrum.* [Online]. Available: https://api.semanticscholar.org/CorpusID

[4] E. Meyer et al., "The state of the art in beyond 5G distributed massive multiple-input multiple-output communication system solutions," *Open Res. Eur.*, vol. 2, no. 106, pp. 1–36, 2022.

[5] M. H. Eissa, A. Malignaggi, R. Wang, M. Elkhouly, K. Schmalz, A. C. Ulusoy, and D. Kissinger, "Wideband 240-GHz transmitter and receiver in BiCMOS technology with 25-Gbit/s data rate," *IEEE J. Solid-State Circuits*, vol. 53, no. 9, pp. 2532–2542, Sep. 2018.

[6] A. Karakuzulu, W. A. Ahmad, D. Kissinger, and A. Malignaggi, "A four-channel bidirectional D-band phased-array transceiver for 200 Gb/s 6G wireless communications in a 130-nm BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 58, no. 5, pp. 1310–1322, May 2023.

[7] I. Kallfass, F. Boes, T. Messinger, J. Antes, A. Inam, U. Lewark, A. Tessmann, and R. Henneberger, "64 Gbit/s transmission over 850 m fixed wireless link at 240 GHz carrier frequency," *J. Infr., Millim., THz Waves*, vol. 36, no. 2, pp. 221–233, Feb. 2015.

[8] Z. Hu, C. Wang, and R. Han, "A 32-unit 240-GHz heterodyne receiver array in 65-nm CMOS with array-wide phase locking," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1216–1227, May 2019.

[9] O. T. Waheed, A. Shabra, and I. A. M. Elfadel, "Impact of fractional bandwidth on the bit error rate of a beamforming system," in *Proc. IEEE 59th Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Oct. 2016, pp. 1–4.

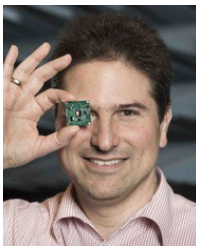
[10] J. Hebeler, L. Steinweg, and T. Zwick, "Differential bondwire interface for chip-to-chip and chip-to-antenna interconnect above 200 GHz," in *Proc. 52nd Eur. Microw. Conf. (EuMC)*, Sep. 2022, pp. 306–309.

[11] L. Steinweg, J. Hebeler, T. Meister, T. Zwick, and F. Ellinger, "8.0-pJ/bit BPSK transmitter with LO phase steering and 52-Gbps data rate operating at 246 GHz," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 7, pp. 3217–3226, Jul. 2023.
[12] J. Hebeler, L. Steinweg, T. Zwick, and F. Ellinger, "Performance evaluation of ultra wideband 246 GHz BPSK transmitters on an organic substrate with external chip and substrate antenna," *IEEE Trans. Microw. Theory Techn.*, early access, pp. 1–12, 2024.
[13] J. Hebeler, A. Bhutani, and T. Zwick, "Design and evaluation of a substrate integrated waveguide with solid side walls for H-band applications on organic substrate," in *Proc. 53rd Eur. Microw. Conf. (EuMC)*, Sep. 2023, pp. 2–5.
[14] R. C. Hansen, "Fundamental limitations in antennas," *Proc. IEEE*, vol. 69, no. 2, pp. 170–182, Feb. 1981.
[15] C. Fager, K. Hausmair, K. Buisman, K. Andersson, E. Sienkiewicz, and D. Gustafsson, "Analysis of nonlinear distortion in phased array transmitters," in *Proc. Integr. Nonlinear Microw. Millimetre-Wave Circuits Workshop (INMMiC)*, Apr. 2017, pp. 1–4.
[16] S. Li, Z. Zhang, B. Rupakula, and G. M. Rebeiz, "An eight-element 140-GHz wafer-scale IF beamforming phased-array receiver with 64-QAM operation in CMOS RFSOI," *IEEE J. Solid-State Circuits*, vol. 57, no. 2, pp. 385–399, Feb. 2022.
[17] X.-D. Deng, Y. Li, J. Li, C. Liu, W. Wu, and Y.-Z. Xiong, "A 320-GHz 1×4 fully integrated phased array transmitter using 0.13-μm SiGe BiCMOS technology," *IEEE*, vol. 5, no. 6, pp. 930–940, Nov. 2015.
[18] I. Abdo, C. da Gomez, C. Wang, K. Hatano, Q. Li, C. Liu, K. Yanagisawa, A. A. Fadila, T. Fujimura, T. Miura, K. K. Tokgoz, J. Pang, H. Hamada, H. Nosaka, A. Shirane, and K. Okada, "A bi-directional 300-GHz-band phased-array transceiver in 65-nm CMOS with outphasing transmitting mode and LO emission cancellation," *IEEE J. Solid-State Circuits*, vol. 57, no. 8, pp. 2292–2308, Aug. 2022.
[19] B. Yu, Z. Wang, O. Li, Q. Liu, H. Cai, Y. Zhou, G. Wang, B. Yan, R. Xu, and Y. Xu, "A 200-GHz four-element phased-array receiver system-in-package using HTCC technology for sub-terahertz communications," *IEEE Trans. Microw. Theory Techn.*, early access, pp. 1–15, 2023.
[20] D. del Rio, J. F. Sevillano, R. Torres, A. Irizar, P. Roux, M. M. Pirbazari, A. Mazzanti, J. Säily, A. Lamminen, J. de Cos, M. G. L. Frecassetti, M. Moretto, A. Pallotta, and V. Ermolov, "A D-band 16-element phased-array transceiver in 55-nm BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 71, no. 2, pp. 854–869, Feb. 2023.

JOACHIM HEBELER (Graduate Student Member, IEEE) was born in Homberg (Efze), in 1994. He received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Kassel, Germany, in 2016 and 2018, respectively. He is currently pursuing the Ph.D. degree with the Institute of Radio Frequency Engineering and Electronics (IHE), Karlsruhe. His research interests include mm-wave integrated circuits, especially power amplifier systems in SiGe, and packaging and antenna solutions in the sub-terahertz regime.

LUCA STEINWEG (Graduate Student Member, IEEE) was born in Bad Säckingen, Germany, in 1994. He received the Dipl.-Ing. degree in electrical engineering from Technische Universität Dresden, Germany, in 2019, and the Ph.D. degree from the Chair for Circuit Design and Network Theory, Technische Universität Dresden, in 2023. His Diploma thesis was done in co-operation with Rohde & Schwarz GmbH & Company KG, Berlin, where he investigated broadband power detectors.

FRANK ELLINGER (Fellow, IEEE) was born in Friedrichshafen, Germany, in 1972. He received the Diploma degree in electrical engineering from the University of Ulm, Ulm, Germany, in 1996, and the M.B.A. and Ph.D. degrees in electrical engineering and the Habilitation degree in high-frequency circuit design from ETH Zürich (ETHZ), Zürich, Switzerland, in 2001 and 2004, respectively. From 2001 to 2006, he was the Head of the RFIC Design Group, Electronics Laboratory, ETHZ, and the Project Leader of the IBM/ETHZ Competence Center for Advanced Silicon Electronics hosted with IBM Research, Rüschlikon, Switzerland. Since 2006, he has been a Full Professor and the Head of the Chair of Circuit Design and Network Theory, Technische Universität Dresden, Dresden, Germany. He has been a Coordinator of the projects RESOLUTION, MIMAX, DIMENSION, ADDAPT, and FLEXIBILITY funded by European Union. He coordinated the cluster project FAST with more than 90 partners (most of them from industry) and the Priority Program FFlexCom of the German Research Foundation (DFG), Germany. He has authored or coauthored more than 600 refereed scientific articles, and has authored the lecture book *Radio Frequency Integrated Circuits and Technologies* (Springer, 2008). He has been a member of the Management Board of German Excellence Cluster Cool Silicon, Germany. He was a recipient of several awards, including the IEEE Outstanding Young Engineer Award, the Vodafone Innovation Award, the Alcatel-Lucent Science Award, the ETH Medal, the Denzler Award, the Rohde & Schwarz/Agilent/GerotronEEEf-COM Innovation Award (twice), and the ETHZ Young Ph.D. Award. He was elected as a Distinguished Microwave Lecturer of the IEEE Microwave Theory and Techniques Society, from 2009 to 2011.



THOMAS ZWICK (Fellow, IEEE) received the Dipl.-Ing. (M.S.E.E.) and Dr.-Ing. (Ph.D.E.E.) degrees in electrical engineering from Universität Karlsruhe (TH), Karlsruhe, Germany, in 1994 and 1999, respectively. From 1994 to 2001, he was a Research Assistant with Institut für Hochstfrequenztechnik und Elektronik (IHE), TH. In February 2001, he joined IBM as a Research Staff Member with the IBM Thomas J. Watson Research Center, Yorktown Heights, NY, USA. From October 2004 to September 2007, he was with Siemens AG, Lindau, Germany, where he managed the RF development team for automotive radars. In October 2007, he became a Full Professor with Karlsruhe Institute of Technology, Karlsruhe. He is currently the Director of the IHE, TH. He has co-edited three books, authored or coauthored 120 journal articles, more than 400 contributions at international conferences, and 15 granted patents. His research interests include wave propagation, stochastic channel modeling, channel measurement techniques, material measurements, microwave techniques, millimeter wave antenna design, wireless communications, and radar system design.