MightyPix at the LHCb Mighty Tracker — verification of an HV-CMOS pixel chip's digital readout

Published by IOP Publishing for Sissa Medialab

Received: *November 3, 2023*
Accepted: *February 27, 2024*
Published: *April 23, 2024*

Topical Workshop on Electronics for Particle Physics
Geremeas, Sardinia, Italy
1–6 October 2023

MightyPix at the LHCb Mighty Tracker — verification of an HV-CMOS pixel chip's digital readout

S. Scherl[a,b,*] **N. Striebig**[b] **K. Hennessy**[a] **I. Perić**[b] **and E. Vilella**[a]

[a] *Department of Physics, University of Liverpool, Oliver Lodge Laboratory, Oxford Street, Liverpool L69 7ZE, United Kingdom*
[b] *Institute for Data Processing and Electronics, Karlsruhe Institute of Technology, Hermann-von-Helmholtz-Platz 1, 76344 Eggenstein-Leopoldshafen, Germany*

E-mail: s.scherl@liverpool.ac.uk

Abstract: MightyPix is a high voltage complementary metal-oxide-semiconductor (HV-CMOS) active pixel sensor, currently being developed for the Mighty Tracker, an upgrade proposed for LHCb in anticipation of the High Luminosity LHC. To ensure that MightyPix will be able to handle the particle hit rates at the Mighty Tracker, which are expected to reach 17 MHz/cm^2, simulations of the chip's digital readout mechanism were performed. Using simulated particle hits the chip's performance within the LHCb environment is characterised. For this, a behavioural model of the first prototype, MightyPix1, representing the analogue pixel matrix, together with the synthesised digital logic is used. Simulation results show the MightyPix1 readout mechanism having an efficiency over 99 % up to 20 MHz/cm^2. The bottleneck was found to be the speed at which the hits are read out. This yielded new design ideas to improve the readout for MightyPix2, leading to an efficiency of over 99 % up to 30 MHz/cm^2.

Keywords: Particle tracking detectors (Solid-state detectors); Performance of High Energy Physics Detectors; Radiation-hard detectors

*Corresponding author.

https://doi.org/10.1088/1748-0221/19/04/C04045

Contents

1 MightyPix at the Mighty Tracker

Part of the upgrade towards the High Luminosity LHC [1] at CERN is the development of a new tracker [2] for the LHCb experiment. This hybrid tracker, called Mighty Tracker, will combine scintillating fibres in the outer regions and silicon sensors in the inner regions, where the hit density and radiation damage are highest. For the silicon region, a new high voltage complementary metal-oxide-semiconductor (HV-CMOS) pixel chip [3, 4], MightyPix, is being developed, based on knowledge of previous HV-CMOS sensors, ATLASPix and MuPix [5].

The first prototype, MightyPix1, was implemented in the TSI 180 nm process and fabricated at the end of 2022. With a size of 2 cm × 0.5 cm it has the full height and one quarter width planned for the final MightyPix. The pixel matrix has 320 rows and 29 columns, with a pixel pitch of 165 µm × 55 µm. The data format is 2 × 32 bit with an output rate of 1.28 Gbit/s. The chip implements a configuration shift register interface, an I^2C interface, and the LHCb specific Timing and Fast Control (TFC) interface. There is a 40 MHz external clock and a CML and CMOS PLL for internal clock generation. The on-chip bias voltages are generated via integrated 10 bit voltage DACs.

MightyPix1 is the first monolithic silicon sensor compatible with the LHCb system. As a high voltage monolithic active pixel sensor (HV-MAPS), the sensor and readout electronics are integrated in one device, shown schematically in figure 1 *(left)*. By applying around −150 V to the substrate, a depletion region of $\mathcal{O}(10 - 100\,\mu\text{m})$ forms between the substrate and deep n-well. The readout electronics sit within shallow wells inside the deep n-well, isolating them from the high voltage. Incident particles induce electron-hole pairs in the depletion region. The charge is collected by the pixel n-well, amplified by the charge sensitive amplifier (CSA) and converted to a digital signal by the comparator. The hit information is then sent out of the pixel to the pixel's hit buffer, where the hit data is stored in Dynamic Random Access Memory (DRAM) cells.

The readout, shown in figure 1 *(right)*, is driven by a finite state machine (FSM) located in the digital part of the periphery. After the hit is stored in the hit buffer, it is read to the end of column (EoC) buffer. The time this takes depends on the hit's time over threshold (ToT) and the FSM speed. While there is one hit buffer per pixel, there is only one EoC buffer per column. If a column contains multiple

2024 JINST 19 C04045

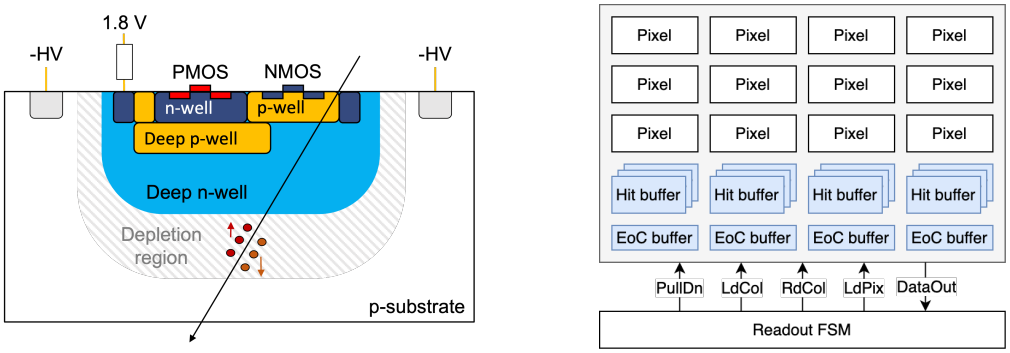

Figure 1. *Left:* working principle of HV-CMOS. *Right:* MightyPix1 readout mechanism.

hits, the one from the lowest row is read first due to the implemented priority logic. Once its hit buffer is freed up a pixel can detect a new hit. For each hit read from the EoC buffers a 2×32 bit data word, containing pixel address, time stamp, and ToT, is sent off-chip.

2 Simulation goals and method

The goal of the simulations presented here is to determine if the MightyPix1 readout mechanism is able to handle the highest particle hit rates at the Mighty Tracker, which are expected to reach $17\,\mathrm{MHz/cm^2}$. This is done by sending simulated data to a model of MightyPix1 and analysing the data detected by MightyPix1. This way the MightyPix1 readout mechanism can be characterised and its efficiency simulated. As the simulation is a quasi-perfect system, without temperature fluctuations, radiation damage, or similar negative effects, the simulation shows what the chip is theoretically capable of, with the goal of identifying potential bottlenecks in the readout mechanism.

2.1 Chip model

As the focus lies on the readout mechanism of MightyPix1, only relevant parts of the chip were implemented in the simulation. These are the pixel matrix, hit buffers, and EoC buffers, which were modelled behaviourally using SystemVerilog, and the digital part, containing the readout FSM, for which the Register Transfer Level (RTL) design was used. The modelled parts are fully parameterizable and can be adapted in chip size, number of rows and columns, number of bits used for the time stamp, and the priority logic.

As MightyPix1 has a comparator in every pixel, converting the analogue pulse from the CSA to a digital pulse, the pixel matrix is modelled as an array of digital outputs. The pixel matrix model can be fed with simulated data, which the readout mechanism then processes. The hit buffer and EoC models replicate the physical implementations on Gate Transfer Level (GTL), with the DRAM cells storing the hit information modelled behaviourally. The capacitances of the DRAM cells are modelled as triregs.[1] The data retention time was verified to be long enough to safely store the hit information for $\mathcal{O}(1\,\mathrm{s})$, which is $\mathcal{O}(10^3)$ larger than the maximum readout time (see section 2.3).

[1] Trireg is a special data type in Verilog used to model capacitances.

2024 JINST 19 C04045

2.2 Simulated data

To simulate hits seen in the MightyPix1 model, three parameters are required: the pixel coordinates, the time of hit (ToH), and the ToT. The simulation additionally requires the number of events and the hit rate. Using these inputs, hits are simulated and read into the MightyPix1 model. The hits are processed by the readout system and a data set containing all detected hits is generated. The simulated data are compared to the detected data, resulting in a detailed summary of all correctly detected and missing hits. The results are analysed to characterise the readout mechanism in detail, including the efficiency, readout time of the hits, and distribution of detected and missing hits.

A total of 40 data sets were generated, containing simulated particle hits for hit rates from 1 MHz/cm^2 to 40 MHz/cm^2, each containing 500 000 events. The events are spaced 25 ns apart, the number of hits per event being Poisson distributed. Within one event the hits occur in a time window of $O(1\,\text{ns})$, being evenly distributed within this period. An analogue simulation of the pixel was performed, using a threshold of 1000 e$^-$ and input signals of 2400 e$^-$ to 24 000 e$^-$. As reference, a minimum ionising particle (MIP) creates around 85 electron-hole pairs per µm depletion region [6]. The simulation gave ToTs between 1.3 µs and 1.8 µs. As a worst case scenario the ToT of all simulated hits was therefore fixed to 2 µs. Recent measurements of MightyPix1 [7] yielded a ToT of (1.49 ± 0.55) µs, confirming the simulation results.

2.3 Limiting factors beyond MightyPix

For MightyPix1, the data size and speed of the readout link have been fixed. These values give an upper limit to the rate that can be sent off-chip without losses, and is here referred to as readout limit. With a pixel matrix area of 0.8422 cm^2, data size of 2×32 bit per hit and readout link speed of 1.28 Gbit/s the readout limit lies at 23.75 MHz/cm^2. Up to that point the efficiency of the chip's readout mechanism could theoretically reach 100 %. Beyond that rate the efficiency will necessarily drop, as the hits arrive faster than the data words can be sent off-chip through the readout link.

At the LHC hits need to be assigned to the correct bunch crossing (BX), and are thus given a unique bunch crossing ID (BXID), which goes up to 3564, after which it is reset and starts again. As the bunches arrive with 40 MHz, the BXID is reset every 89.1 µs. If hits take longer than that to be read out, the assigned BXID will be incorrect and the hits counted as not detected. This leads to a readout time limit of 89.1 µs.

3 Results for MightyPix1

The simulated efficiency is given by the ratio of hits detected by the MightyPix1 model to the total number of simulated hits. The uncertainty is given by the Clopper-Pearson 95 % confidence interval (CI). In the figures it is visualised as blue band, but in some cases too narrow to be visible.

Figure 2 shows the simulated efficiency of the MightyPix1 readout mechanism. Hit rates up to 40 MHz/cm^2 are shown on the left. A clear drop in the efficiency is visible at 21 MHz/cm^2, which is slightly lower than the readout limit of 23.75 MHz/cm^2. The right shows a close up of the region with over 99 % efficiency. At 17 MHz/cm^2, the maximum expected hit rate at the Mighty Tracker, the simulated efficiency is 99.55 %, with a CI of 99.52 % to 99.58 %.

The sharp decrease in efficiency can be explained by looking at the time it took to read out the simulated hits at rates of 20 MHz/cm^2, 21 MHz/cm^2, and 22 MHz/cm^2, shown in figure 3, which is

2024 JINST 19 C04045

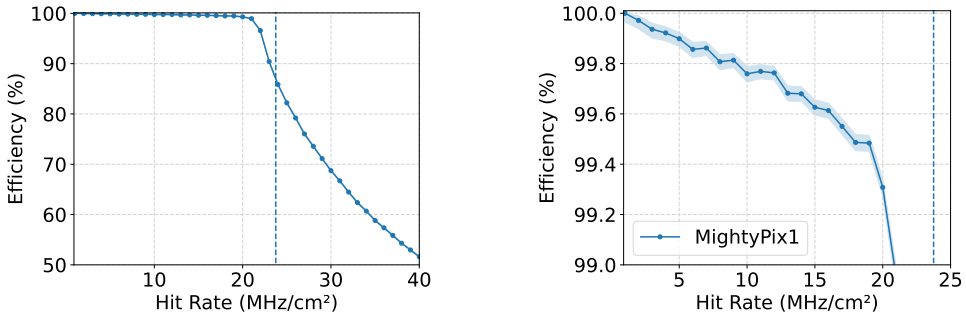

Figure 2. Simulated efficiency of the MightyPix1 readout mechanism for hit rates up 40 MHz/cm^2 *(left)* and a close up of the region with over 99 % efficiency *(right)*. The CI is shown as blue band, but too narrow to be visible for higher rates. The dashed line at 23.75 MHz/cm^2 marks the readout limit.

the region of the drop-off. As expected, the readout times increase with increasing row number. This is due to the mentioned priority logic, where hits from lower rows are read first. While the majority of hits have a readout time of 2 µs to 5 µs, there is a tail of longer readout times from hits in higher rows. At 20 MHz/cm^2 this tail extends to around 60 µs, which is not visible in the histogram, but in the scatter plot above the histogram. For 21 MHz/cm^2, this tail reaches 89.1 µs. As mentioned in 2.3, this is the readout time limit, imposed by the LHC BXID. Hits taking longer to read out will not be detected correctly. At 22 MHz/cm^2 there is already a visible cut in the readout times at this limit, showing that a significant number of hits are lost due to their long readout time. The sharp drop in efficiency is therefore due to the hits taking too long to be read out.

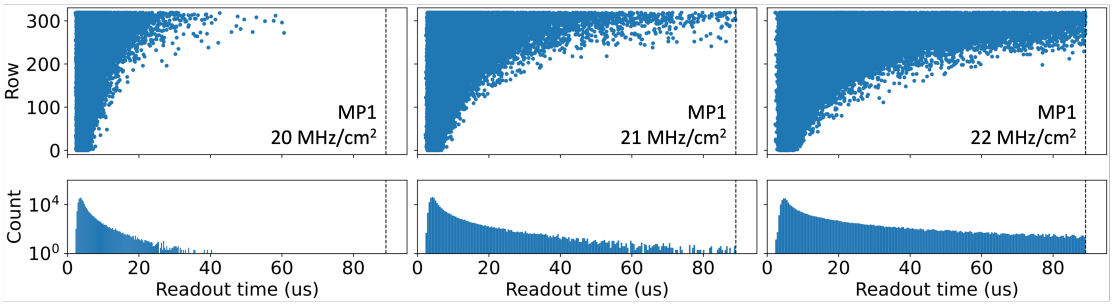

Figure 3. Readout time of simulated hits for the 320 rows of MightyPix1 for a hit rate of 20 MHz *(left)*, 21 MHz *(middle)*, and 22 MHz *(right)*. The dashed line at 89.1 µs marks the readout time limit.

4 Improvements for MightyPix2

To increase the efficiency of the next chip iteration, MightyPix2, improvements were implemented in the readout mechanism, shown in figure 4. The data size was decreased from 2 × 32 bit to 48 bit per hit, which was possible without loss of information, as the 2 × 32 bit were not fully used. This increases the readout limit to 31.66 MHz/cm^2. Additionally, the speed of the readout FSM was increased from 32 bit at 40 MHz to 48 bit at 160 MHz. A gearbox was also implemented to store up to 16 hits in a FIFO before they are sent off-chip through the 1.28 Gbit/s readout link.

2024 JINST 19 C04045

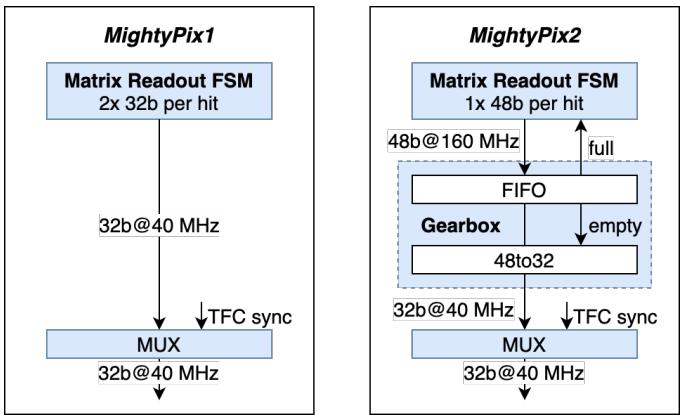

Figure 4. Readout mechanism of MightyPix1 *(left)* and improved readout mechanism for MightyPix2 *(right)*.

Figure 5 shows the efficiency of the MightyPix1 readout mechanism and the improved readout mechanism for MightyPix2. Whereas the MightyPix1 efficiency drops around 20 MHz/cm^2, the MightyPix2 efficiency stays over 99 % up to the increased readout limit of 31.66 MHz/cm^2.

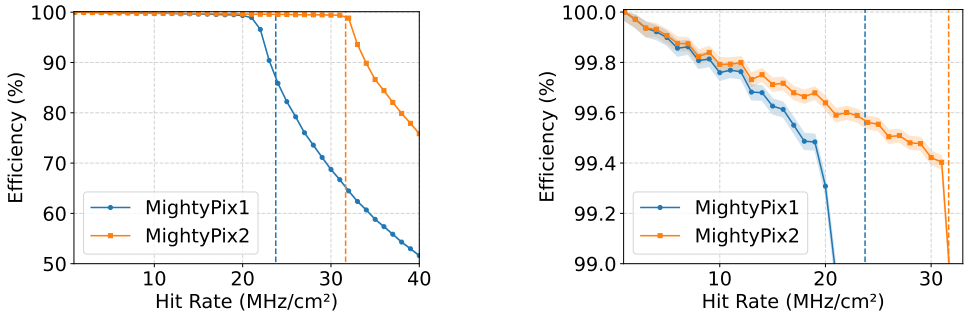

Figure 5. Simulated MightyPix2 efficiency for hit rates up to 40 MHz/cm^2 *(left)* and a close up of the region with over 99 % efficiency *(right)*. The CIs are shown as blue and orange bands, but too narrow to be visible for higher rates. The dashed lines at 23.75 MHz/cm^2 and 31.66 MHz/cm^2 mark the readout limits.

Figure 6 shows the readout times around the efficiency drop at 31.66 MHz/cm^2 for MightyPix2. At 31 MHz/cm^2 the longest readout times lie below 30 µs, hitting the readout time limit of 89.1 µs at the readout limit of 31.66 MHz/cm^2. For higher rates the hits cannot be sent off-chip fast enough, due to the readout link speed and data size, and the efficiency drops.

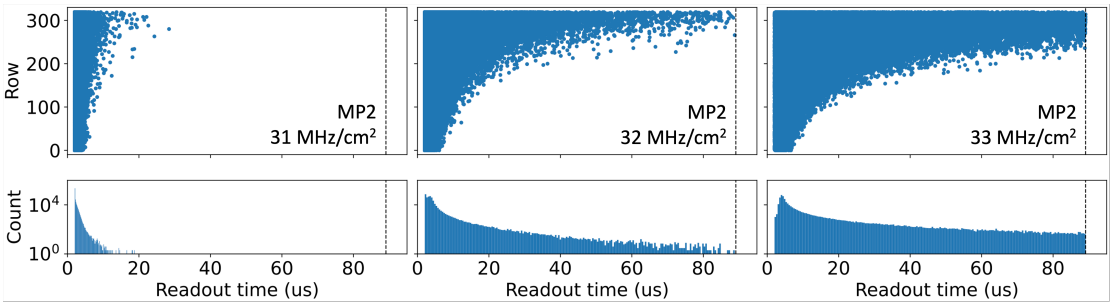

Figure 6. Readout time of simulated hits for the 320 rows of MightyPix2 for a hit rate of 31 MHz *(left)*, 32 MHz *(middle)*, and 33 MHz *(right)*. The dashed line at 89.1 µs marks the readout time limit.

2024 JINST 19 C04045

5 Conclusion

Simulations of the MightyPix1 readout mechanism show an efficiency of over 99 % for hit rates up to 20 MHz/cm^2. This indicates its capability to handle the hit rates at the new LHCb Mighty Tracker, which are expected to reach 17 MHz/cm^2. The limiting factor proved to be the speed at which the hits are read from the hit buffers. The simulation assumes a quasi-perfect environment, without temperature fluctuations, radiation damage, or similar negative effects. Factors like tilted tracks, charge sharing, or noise hits, were not included due to a lack of detailed information on their presence at the Mighty Tracker. To account for these unknowns, efforts were made to improve the readout system for MightyPix2, to increase the safety margin. This included reducing the data size by 25 %, increasing the speed of the readout FSM, and adding a gearbox containing a FIFO to store the hits before they are sent off-chip. The improved readout mechanism showed an efficiency over 99 % up to 31.66 MHz/cm^2, nearly twice the maximum expected hit rate at the Mighty Tracker.

References

[1] I. Béjar Alonso et al., *High-Luminosity Large Hadron Collider (HL-LHC): Technical design report*, CERN-2020-010, CERN, Geneva (2020).

[2] LHCb collaboration, *Framework TDR for the LHCb Upgrade II: Opportunities in flavour physics, and beyond, in the HL-LHC era*, CERN-LHCC-2021-012, CERN, Geneva (2021).

[3] I. Perić, *A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology*, *Nucl. Instrum. Meth. A* **582** (2007) 876.

[4] I. Perić et al., *High-Voltage CMOS Active Pixel Sensor*, *IEEE J. Solid State Circuits* **56** (2021) 2488.

[5] A. Schöning et al., *MuPix and ATLASPix — Architectures and Results*, *PoS* **Vertex2019** (2020) 024 [arXiv:2002.07253].

[6] M. Moll, *Radiation Damage in Silicon Particle Detectors*, Ph.D. Thesis, Universität Hamburg (1999).

[7] L. Dittmann, private communication (2023).

2024 JINST 19 C04045