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ABSTRACT

Silicon–germanium heterostructures are a promising quantum circuit platform, but crucial aspects, such as the long-term charge dynamics and cooldown-to-cooldown variations, are still widely unexplored quantitatively. In this Letter, we present the results of an extensive bias cooling study performed on gated silicon–germanium quantum dots with an Al₂O₃ dielectric. Over 80 cooldowns were performed in the course of our investigations. The performance of the devices is assessed by low-frequency charge noise measurements in the band of 200 μHz to 10 mHz. We measure the total noise power as a function of the applied voltage during cooldown in four different devices and find a minimum in noise at 0.7 V bias cooling voltage for all observed samples. We manage to decrease the total noise power median by a factor of 6 and compute a reduced tunneling current density using Schrödinger–Poisson simulations. Furthermore, we show the variation in noise from the same device in the course of eleven different cooldowns performed under the nominally same conditions.

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Electron spins in silicon–germanium represent a promising implementation of the solid state quantum computer. Single and two-qubit gates have been reported to reach gate fidelities above the error correction threshold.^{1–3} Recently, quantum error correction was performed on a three qubit device⁴ and intermediate range coupling opened new prospects regarding a scaled up quantum processor.^{3,5–7} Since quantum-dot based qubits need to be tuned and re-tuned, the long-term stability of the qubit working point has gained research interest.^{8–10} Furthermore, it has been shown that the charge noise level in SiGe devices is strongly dependent on the applied global field.¹¹ Bias cooling is a readily accessible method which only relies on equipment already present in the typical semiconductor quantum dot setup. To perform bias cooling, the same bias cooling voltage V_{BC} is applied to all gates of the sample during cooldown from room temperature to mK temperatures. This causes charges to be trapped in localized defects which interact with the global electric field, thereby changing the stability of gate-defined quantum dots. In gallium arsenide, bias cooling has been proven to reduce switching noise and, therefore, improve the sample stability¹² by filling DX centers in the dopant layer and, therefore, reducing the effective leakage rate of electrons from the

gate layers into the two-dimensional electron gas (2DEG). In silicon–germanium, no such centers are present and bias cooling has not been quantitatively investigated yet.

We present the results of a systematic bias cooling study, quantitatively investigating the noise power in the voltage range between -1 and 1 V for V_{BC} . More than 80 cooldowns were performed on four different samples. Depending on the applied gate voltage during cooldown, we reduce the total noise power in the frequency band of 200 μHz to 10 mHz by a factor of 6, in comparison to the zero volt case. We use four gated Si/SiGe devices nominally equal to the device used in Refs. 5 and 13 [see Fig. 1(a)]. It contains two single-electron transistors (SETs) operating as proximal charge detectors and nine central finger gates as well as two confinement gates.

The gatestack is fabricated upon a Si/SiGe heterostructure, which consists of a 1000 nm Si_{0.7}Ge_{0.3} graded buffer layer on an Si substrate, a 10 nm Si channel, followed by a 30 nm Si_{0.7}Ge_{0.3} spacer layer and capped by 2 nm naturally oxidized Si [see Fig. 1(b)]. The heterostructure confines electrons in the growth direction, effectively forming a 2DEG in the silicon channel, when accumulated. Ohmic contacts to the quantum well layer are realized by implantation of phosphorus

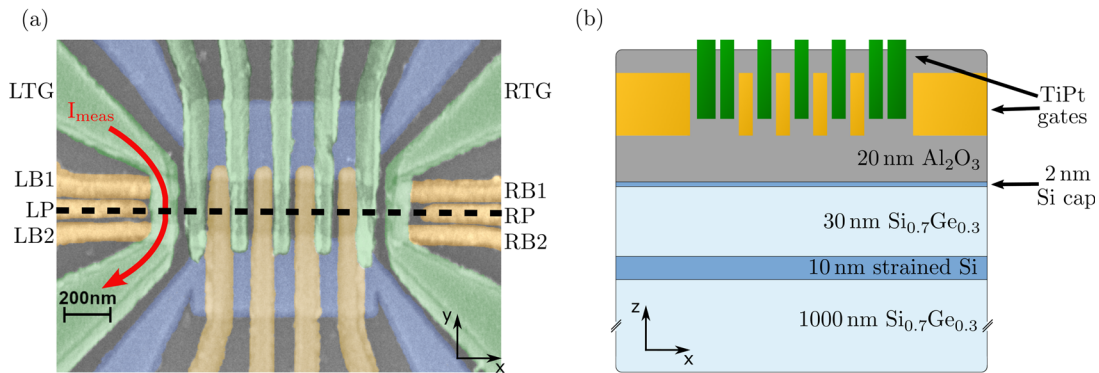


FIG. 1. (a) False colored scanning electron micrograph. Bottommost gate layer in blue, topmost layer in green. The path of the current I_{meas} used in the measurements is denoted in red. (b) Schematic cross section with layer thicknesses to scale. The 2DEG is defined in the 10 nm strained Si layer. The SiGe spacer layer is protected from oxidation by a 2 nm silicon cap layer. The dashed line in (a) represents the corresponding position of the schematic cross section in (b).

and activated by rapid thermal processing at 700 °C for 15 s. The gate stack is an overlay of three metal layers consisting of 15, 22, and 29 nm Pt on top of a 5 nm Ti adhesion layer. The metal layers are electrically insulated from the substrate and from each other by 10 nm atomic layer deposited Al_2O_3 .

To characterize the performance under different bias cooling conditions, an efficient thermal cycling mechanism is needed. A heater consisting of a constantan wire was installed in the mixing chamber of the used dilution refrigerator. The sample is heated locally to 300 K, while the 4 K stage of the fridge is kept below 10 K. This is achieved by thermally insulating the mixing chamber plate by stopping the circulation of the mixture while a high flow of liquid helium is supplied to the 4 K stage. An automated thermal cycle from 30 mK to 300 K and back to 30 mK takes 3.5 h.

We monitor the turn-on voltage V_T after reaching the base temperature. To do this, we accumulate the electron gas using all gates, effectively forming a conductive sheet underneath the gate structure. This way, we minimize the effect of singular defects on the conducting channel. We measure the conductance G in between the Ohmic contacts of the left SET. Once it reaches one third of the saturation value ($G_{\text{sat}}/3$), which was measured in a separate cooldown, the accumulation voltage is not increased further. The first apparent effect of bias cooling is that the accumulation voltage of the device shifts nearly linearly with the applied bias cooling voltage (Fig. 2). Charge carriers are trapped in between the quantum well and the metal gates. We suspect electrons getting caught at the Si- Al_2O_3 interface.^{14,15} This interface is known to form an SiO_x layer, in which silicon atoms are partially replaced by aluminum atoms.^{16,17} These form acceptor states, which trap electrons. By applying the bias cooling voltage V_{BC} during cooldown, we change the electrochemical potential of the defects, allowing thermally excited electrons to change the population of the defect states. Applying positive voltages attracts additional electrons into acceptor states, increasing the turn-on voltage. Negative biases reduce the population of the Al vacancies below its equilibrium, creating an excess of positively charged defects, decreasing the accumulation voltage. Next, we characterize the noise power for each bias voltage. To investigate the charge noise we form a single electron transistor in between barrier gates (e.g., LB1 and LB2). The gate layout of the used device is shown in Fig. 1(b). The challenge hereby is tuning the SETs

to comparable working points, although the sample provides a different electrostatic environment in each cooldown. Noise seen by SET devices depends on their working point.¹⁸ Therefore, it is essential to repeat a fixed measurement protocol. Our protocol consists of six steps summarized in Figs. 3(a) and 3(b). After accumulating the sample to the reference conductance of $G_{\text{sat}}/3$ (step 1), we define the accumulation voltage V_{ref} which is used as a starting point for the device tuning. With all gates at V_{ref} , the device is in a state where a 2DEG is accumulated in the silicon quantum well below every metal gate. In step 2, we lower the voltages of all gates except the top gates and barriers of the SETs by 500 mV to deplete the sample and confine the 2DEG only below the top gates. In step 3, the top gate voltage [and in the first iteration also the barrier voltages, not shown in the voltage chronogram in Fig. 3(b)] is increased until a third of the saturation conductance is

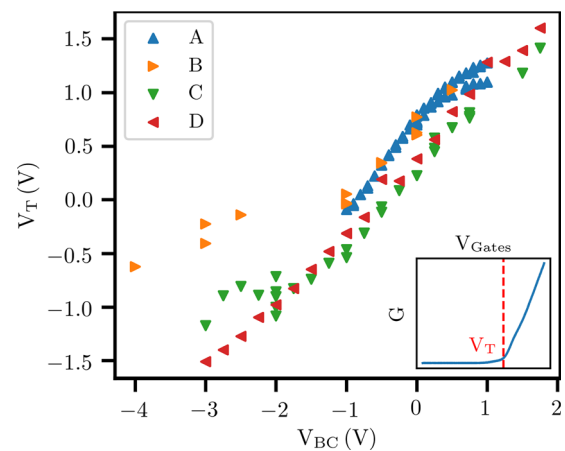


FIG. 2. Turn-on voltage of the device over applied bias voltage during cooldown for four nominally equal devices. In between -1 and 1 V all samples behave linearly showing similar slopes. Below -1 V the behavior differs. This might be due to different defect densities in the heterostructure. The inset shows an exemplary accumulation curve. The red-dashed line indicates the turn-on voltage, which is defined by the channel conductivity G crossing a value of $0.4 \mu\text{S}$.

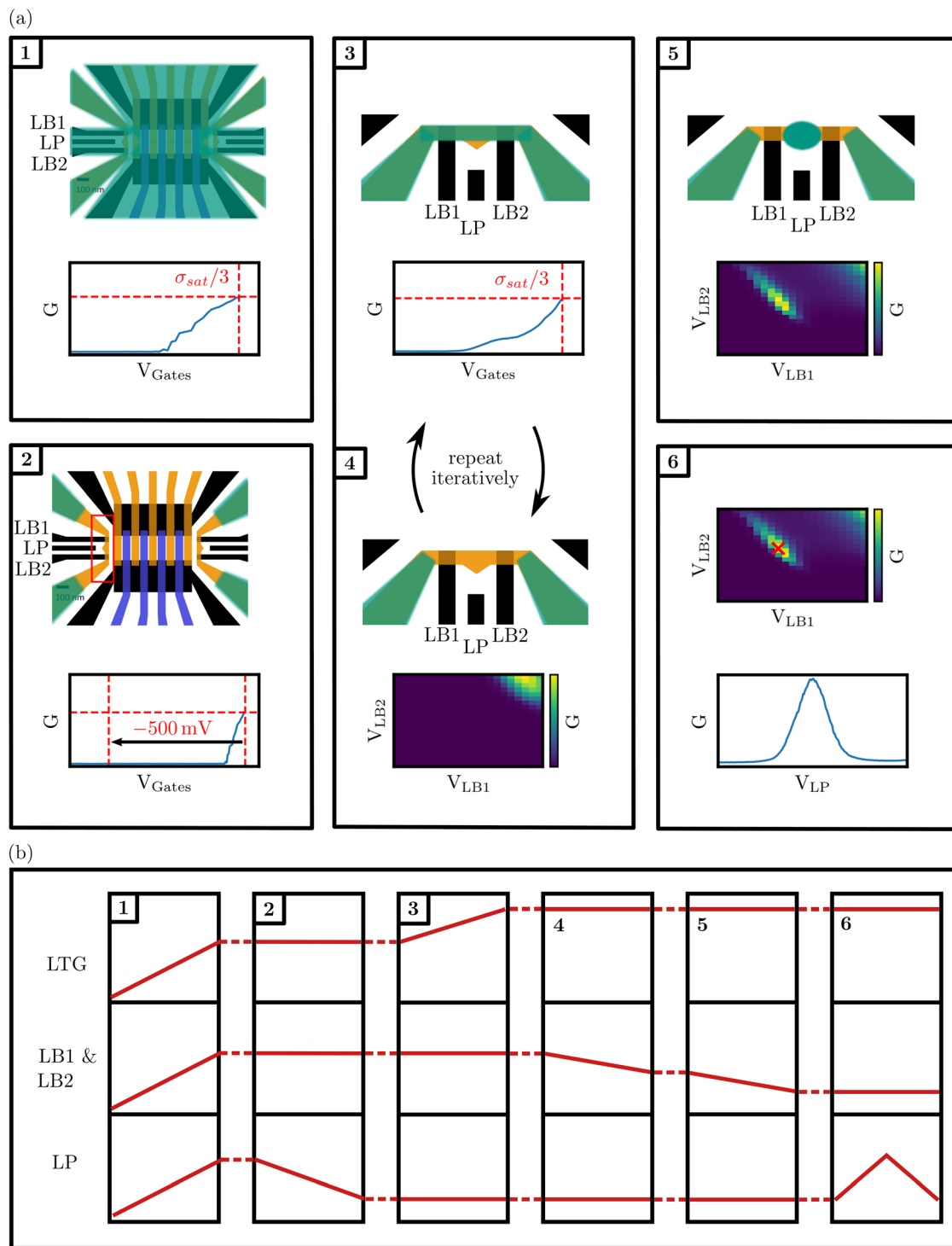


FIG. 3. (a) Tuning workflow which was performed after each cooldown. The red square in step 2 denotes where the cutout shown in steps 3 to 5 lies within sample. The sample is accumulated to the reference conductance of $G_{\text{sat}}/3$ (step 1). The voltages applied to all but the SET gates are reduced by 500 mV to confine the 2DEG (step 2). By using the SET gates, a closed conducting channel is formed (step 3). A $100 \times 100 \text{ mV}^2$ sweep is performed with both barrier gates (step 4). Steps 3 and 4 are repeated iteratively until a Coulomb oscillation is observed (step 5). The barrier gates are tuned to the first Coulomb peak (step 6) and a plunger trace is recorded. (b) Simplified chronogram of the voltages applied to the SET gates. Numbers 1–6 correspond to the tuning steps in panel (a).

reached in the measured channel. In step 4 the “cutoff” voltage of the barrier gates is determined by lowering the voltages of the barrier gates to the point where the conducting channels are fully confined and the measured current is cut off. Slightly above this cutoff voltage, we perform a $100 \times 100 \text{ mV}^2$ sweep downward with both barrier gates. We record the current through the channel to see whether Coulomb oscillations are present. If not, we now lower the barrier gates by another 100 mV and re-accumulate the conducting channel with the top gate again up to a conductance of $G_{\text{sat}}/3$. By repeating steps 3 and 4 iteratively, we find the lowest (granulated by the resolution of our voltage steps) top gate voltage that allows formation of quantum dots, which are identified by a 2D barrier sweep exhibiting the Coulomb oscillations (step 5). The barrier gates are tuned to the first Coulomb peak (step 6) and a plunger trace is recorded. If the recorded trace shows a secant-like Coulomb peak, the SET has been formed and the tuning routine came to a successful conclusion.

With the quantum dot formed, we characterize its noise in the band of 200 μHz to 10 mHz using peak tracking.⁸ The lower bound on the measured frequencies is set by the total length of our peak-tracking measurements (5 h) and the upper bound is set by the rate at which the plunger gate can be swept to record the position of the peak in gate space. The number of points recorded per plunger sweep varies depending on the expected drift of the sample. Therefore, a trace can contain 150 to 250 individual data points and be measured in 30 to 70 s depending on the number and sampling rate of the points. We continuously sweep the plunger and record the conductivity of the SET device [Fig. 4(a)]. The shown result was recorded on sample A

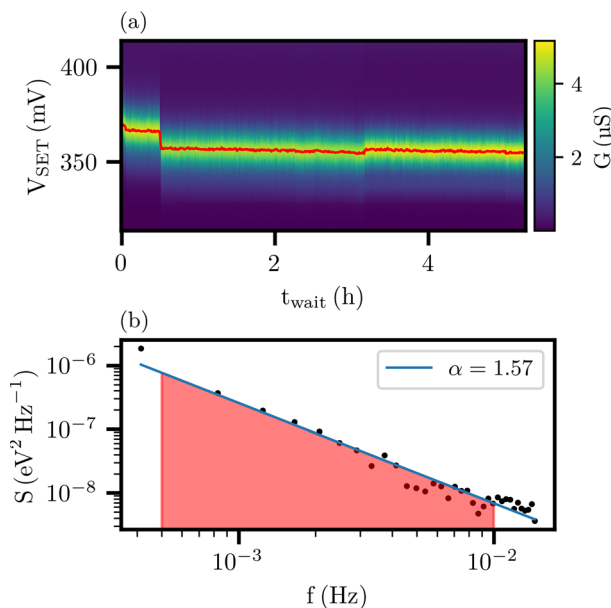


FIG. 4. (a) Peak-tracking measurement performed on sample A with a V_{BC} of 0 V. The colorplot consists of Coulomb peak traces recorded back to back. The red line indicates the position of the peak maxima. (b) Noise power spectral density, fitted with a β/f^α power spectrum. To calculate the total noise power, the spectrum is integrated over the highlighted frequency range. The conversion of V_{SET} to the chemical potential of the SET is done by a static lever arm of 0.039 eV/V.

after being cooled down with 0 V. We extract the exact peak position by fitting each individual trace with a secant function and define the position of its maximum as the peak position. The conversion of V_{SET} to eV is done by a static lever arm of 0.039 eV/V. This value is the average of multiple extracted lever arms measured (using Coulomb diamond measurements¹⁹) for different samples and bias cooling voltages spanning a range from 0.035 to 0.040 eV/V.

Next, we perform a Welch estimation of the power spectral density using the standard `signal.welch` method from the `scipy` python package. To exclude artificial frequencies arising from a drift in between the start and end points of a trace, we additionally employ a Hann-type windowing function. The estimation is always performed on the first measured peak. The result can be found in Fig. 4(b). The resulting spectrum follows a $1/f^\alpha$ -noise distribution with $\alpha = 1.57$. This lies in between $\alpha \approx 1$, suggesting the presence of many two-level fluctuators with a broad distribution of time scales,²⁰ and $\alpha \approx 2$, indicating the presence of random walk noise.²¹ Subsequently, we integrate the fitted spectra in the band of 200 μHz to 10 mHz, highlighted in purple in Fig. 4(b). Quoting the total noise power instead of, e.g., 1 mHz noise has the advantage that all frequencies in the measured band contribute to the noise value. This metric is chosen because we want to weigh both, the rarely occurring large jumps as well as the small displacements in peak position that happen in between every single datapoint.

The procedure is applied to all measured peak tracks. A selection measured on sample B is found in Figs. 5(a)–5(c). Peak tracks dominated by large jumps tend toward $\alpha \approx 2$, while peak tracks which are dominated by fluctuations around the original working point tend toward $\alpha \approx 1$. The resulting noise spectra are shown in Fig. 5(d). The noise power vs bias cooling voltage can be seen in Fig. 5(e). Four samples show a significant noise reduction at 0.7 V. Sample B shows an improvement in the integrated noise power by two orders of magnitude. Toward more positive voltages, samples B and C show an increase in noise.

We identify two types of noise on the SET peak position. A high-frequency, low-amplitude fluctuation and rarely occurring jumps with a large amplitude. These jumps occur on the timescale of hours and drastically affect the noise performance (Fig. 5). Since the individual peak-tracking measurements have a length of five hours, they may not lead to statistically significant data. To gain insight into the significance of our observations, we performed a measurement campaign consisting of 22 cooldowns of sample A. We measured eleven times the zero-bias followed by the 0.7 V bias. The results of the noise power integrated from 200 μHz to 10 mHz are shown in the Fig. 5(f). The orange line shows the median. The median value of the 0.7 V measurements is reduced by a factor of 6 in comparison to the median of the 0 V measurements. To determine the statistical significance of the measured results, we performed an unpaired t-test comparing the measured datasets for 0 and 0.7 V, which results in a probability of 0.143% that the two measured sample means arise from the same normal distribution.

Three-dimensional Poisson–Schrödinger simulations have been performed on the SET-area of the investigated devices. SiGe heterostacks are known to induce tunneling currents from the Si-channel²² into the cap. Charge redistributions, as seen in Fig. 5(a), could be caused by local metal-to-insulator transitions, triggered by tunneling into the cap.^{22,23} This interpretation is plausible, since the cap-oxide

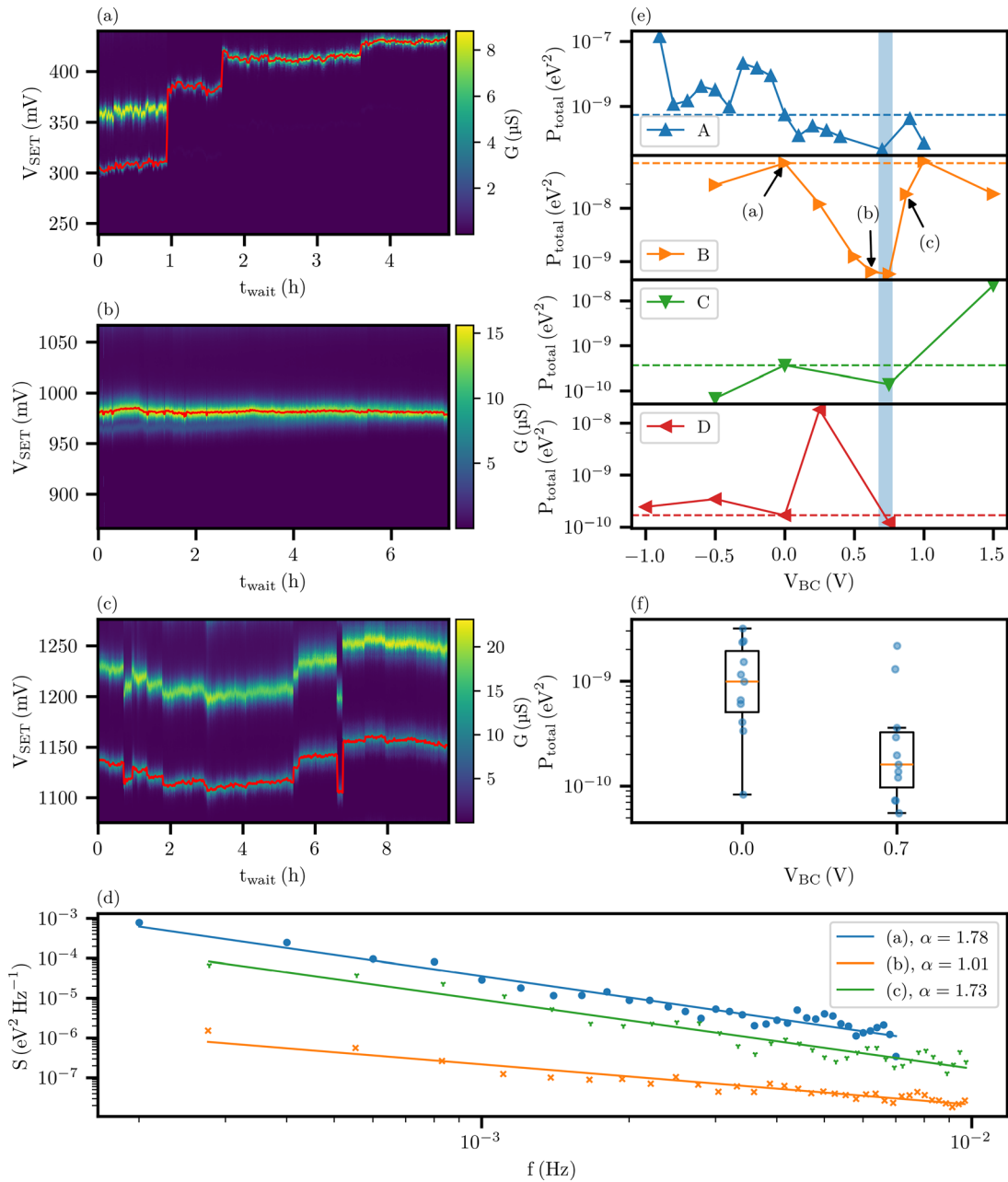


FIG. 5. (a)–(c) Peak-tracking measurements performed on sample B for 0, 0.625, and 0.825 V. (b) shows a vanishing side peak, which might indicate the presence of a parasitic dot. (d) Noise power spectral densities fitted with a β/f^α power spectrum. (e) Integrated noise power vs bias cooling voltage. While the noise increases toward negative biases for most samples, a local minimum at 0.7 V is found in each trace. The dashed line denotes the 0 V noise level. (f) Boxplot of the integrated noise power of 22 peak trackings performed in alternating 0 V/0.7 V cooldowns. The box includes the interquartile (IQR) range and the whiskers extend up to 1.5 times the IQR. The orange solid line displays the median value. The median value of 0.7 V is almost an order of magnitude lower than for 0 V.

interface itself is MOSFET-like. In MOSFET devices the length scales of localization length vs potential variation²⁴ are known to create a percolation-induced metal-to-insulator transition.²⁵ In that case, the 2DEG in the cap breaks down into charge carrier puddles containing mobile carriers. With the simulations we wish to verify that tunneling

currents into the cap exist and can, therefore, source electrons which cause the charge redistributions. Bias cooling was included in the simulation by placing interface charges in the interstitial silicon-oxide layer under the metal gates. The interface-charge density under each gate layer was calculated based on the turn-on voltage shift. We

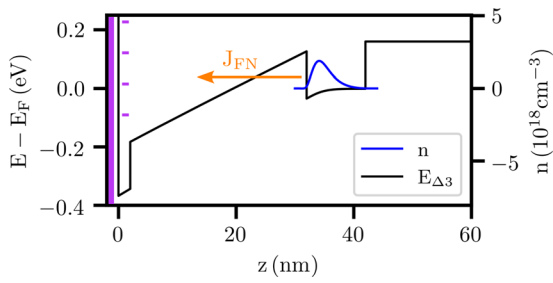


FIG. 6. Simulated band structure alignment at the working point of a sample cooled down with $V_{BC} = 0.7$ V. E_{Δ_3} is the energy of the lowest conduction band. The violet region indicates the assumed position of the interface charges. They were distributed in a 1 nm thick sheet located 1.2 nm above the Si-cap-oxide interface. The orange arrow indicates the direction of the Fowler-Nordheim tunneling current density J_{FN} . The electron density n is plotted in blue.

simulated the density needed to shift the turn-on voltage of gate layer n (with $n \in \{1, 2, 3\}$) individually. The same charge density is assumed under each gate of a specific gate layer. To reflect the device's real working point, the gate voltage configurations from individual measurements have been reproduced in simulation. The spatially large regions are treated (substrate, buffer, and spacer) in Thomas-Fermi²⁶⁻²⁸ approximation. The regions where quantum confinement plays a major role (channel and cap), however, are treated with a self-consistent Schrödinger-Poisson approach in effective mass approximation.^{29,30} In Fig. 6, the simulated band diagram in growth direction for a sample cooled down with $V_{BC} = 0.7$ V is shown. The barrier in between the silicon channel and the silicon cap layer is of triangular shape, meaning that the tunneling currents can be calculated using the Fowler-Nordheim³¹ model. With the resulting electric field and electrochemical potential, we calculate the tunneling rates from the SiGe channel into the silicon cap. The spatially varying tunneling currents are shown in Fig. 7(a) for the 0 V and (b) for the 0.7 V bias cooling case. First, it is important to note that the maximum tunneling rate for the 0.7 V case is reduced by seven orders of magnitude in comparison

to the 0 V case. Furthermore, the dot region itself does not act as a source of electrons in the 0.7 V case, meaning the number of tunneling electrons is not only reduced, but the tunneling events are mainly taking place further away from the region of interest. Generally, the bias cooled samples are operated at lower internal electric fields, as seen in Figs. 7(c) and 7(d). In the bias cooled case, the electric field difference in between the dot region and the barriers is larger. This means that a dot can be accumulated at lower accumulation gate fields, since the electric field of the barriers is more sharply defined due to the frozen-in charges, which are located at the Si-cap- Al_2O_3 interface.

We repeated the simulation for each working point in Fig. 5(f), to verify an interrelation in between tunneling events and noise. In Fig. 8, the measured noise power is plotted vs the calculated maximum tunneling current. The 0 V cases show a bunching toward high tunneling rates and high noise, whereas the 0.7 V cases show bunching toward low tunneling and low noise. One possible explanation for the correlation of high noise and high tunneling rates is that the electrons flowing from the channel into the cap cause local metal-insulator transitions in the disordered silicon cap.²² The avalanche-like charge redistributions seen in the peak-tracking measurements might be caused by a few excess electrons, locally exceeding the percolation density, triggering a large charge transfer, which is supported by the fact that the number of large charge redistributions is reduced in the 0.7 V dataset. At a high bias cooling voltage, a high number of the acceptor defects located at the Si-cap Al_2O_3 interface are charged. We propose two main mechanisms to explain the increase in noise for voltages above 0.7 V. First, the high density of negatively charged defects leads to working points with high electric fields. Additional tunneling could be a result. Furthermore, the increase in charged defects at the interface could lead to the individual defects exchanging charges, therefore, effectively raising the noise again. For bias cooling voltages exceeding 2 V, the 2DEG is accumulated without the application of an accumulation voltage. Here, the trapped charges mimic the role of a dopant. For more negative voltages the noise is increasing in the case of samples A and D, not showing a global trend.

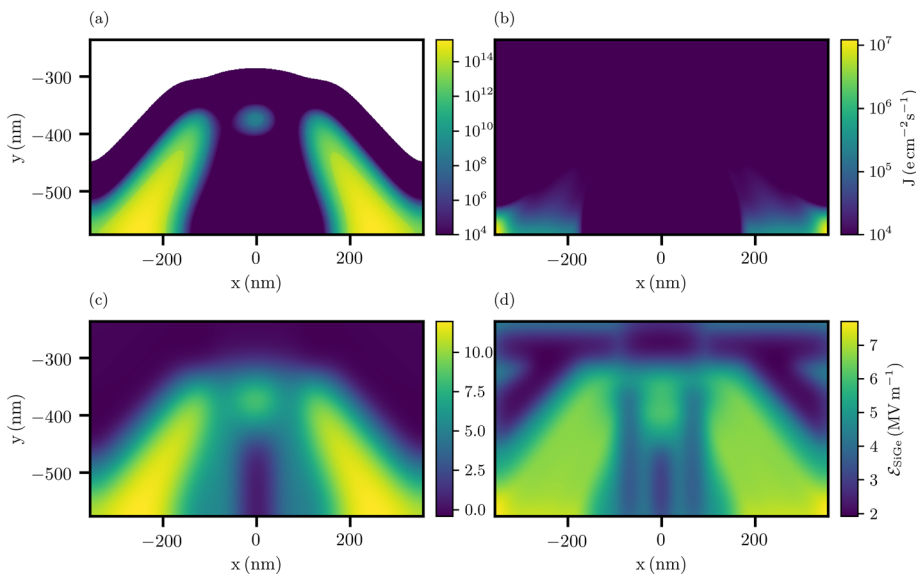


FIG. 7. (a) Simulated tunneling current from the silicon channel into the silicon cap for a sample cooled with a 0 V bias (a) and 0.7 V bias (b). Simulated electric field distribution at the channel-spacer interface of a sample cooled with a 0 V bias (c) and 0.7 V bias (d).

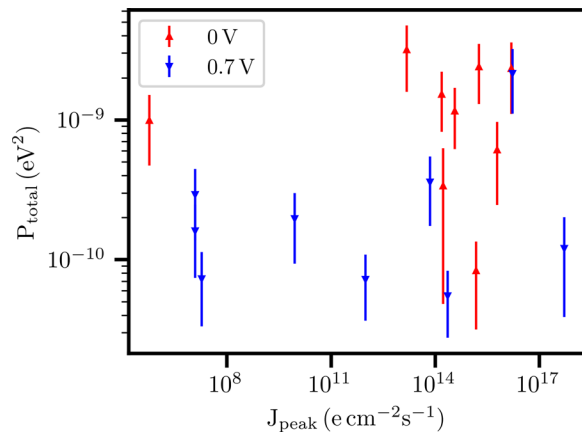


FIG. 8. Measured integrated noise density vs simulated peak tunneling current. The datapoint belonging to the 0.7 V dataset in the high-tunneling, high-noise quadrant shows an excess of telegraph noise which was only recorded once.

In conclusion, we found that bias cooling of undoped Si/Si_xGe_{1-x} heterostacks causes charges to be trapped in between the silicon channel and the metal gates. This shifts the turn-on voltages linearly with the applied cooldown bias in the range of -1 to 1 V. We investigated the low-frequency charge noise of bias cooled devices. For this we used peak-tracking measurements. To quantify the noise for each bias cooling voltage, we computed the total noise power for every peak track, which has a minimum around 0.7 V bias cooling voltage. In samples A and B, a global minimum is visible in the total noise power. Samples C and D show a local minimum around 0.7 V. In the case of sample B, we could reduce the total noise power by a factor of 120 during the 0.75 V cooldown in comparison to the 0 V cooldown, and during a 22-cooldown campaign the measured median of the total noise power was reduced by a factor of 6 for the 0.7 V cooldown in comparison to the 0 V value. Our measurements show that a significant variation of the noise level can occur as a function of cooldown bias and that this variation is not a random fluctuation from cooldown to cooldown. While a cooldown bias of 0.7 V leads to good results on all four devices considered, more statistics would be needed to tell if this value reflects a device-independent optimum, and how the optimal cooldown strategy depends on the device design. Another important implication of the significant variation between cooldowns and bias voltages is that a lot of statistics is needed to draw reliable conclusions from noise measurements. In addition, we present the results of a three-dimensional Schrödinger–Poisson simulation, based on measured working points. Here, we find that samples cooled down with a 0.7 V bias show a by seven orders of magnitude reduced tunneling current from the channel into the cap. While the direct proof remains elusive, we correlate the simulation to our noise measurement results, and find a bunching of datapoints in the high-noise, high-tunneling as well as in the low-noise, low-tunneling quadrants. As a next step, bias cooling could be extended to qubit samples, investigating the effect on coherence. Furthermore, tunneling in the cap has been proposed as one of the root causes of the quantum dot instabilities.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Julian Ferrero: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Writing – original draft (lead). **Thomas Koch:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Sonja Vogel:** Data curation (equal); Formal analysis (equal); Writing – review & editing (equal). **Daniel Schroll:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Viktor Adam:** Conceptualization (equal); Data curation (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Ran Xue:** Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Inga Seidler:** Investigation (equal); Methodology (equal); Writing – review & editing (equal). **Lars R. Schreiber:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Writing – review & editing (equal). **Hendrik Bluhm:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (equal); Investigation (equal); Methodology (equal); Project administration (equal); Writing – review & editing (equal). **Wolfgang Wernsdorfer:** Conceptualization (equal); Funding acquisition (lead); Methodology (equal); Supervision (lead); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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