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Anodization-free fabrication process for high-quality cross-type Josephson tunnel junctions based on a Nb/Al-AlO$_x$/Nb trilayer

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Abstract

Josephson tunnel junctions form the basis for various superconductor electronic devices. For this reason, enormous efforts are routinely taken to establish and later on maintain a scalable and reproducible wafer-scale manufacturing process for high-quality Josephson junctions. Here, we present an anodization-free fabrication process for Nb/Al-AlO$_x$/Nb cross-type Josephson junctions that requires only a small number of process steps and that is in general intrinsically compatible with wafer-scale fabrication. We show that the fabricated junctions are of very high quality and, compared to other junction types, exhibit not only a significantly reduced capacitance but also an almost rectangular critical current density profile. Our process hence enables the usage of low capacitance Josephson junctions for superconductor electronic devices such as ultra-low noise dc-superconducting quantum interference devices (SQUIDs), microwave SQUID multiplexers based on non-hysteretic rf-SQUIDs and RFSQ circuits.

Keywords: Josephson tunnel junctions, microfabrication process, Nb/Al–AlO$_x$/Nb trilayer, subgap leakage, thermal activation theory, unshunted dc-SQUIDs, capacitance measurements

1. Introduction

Josephson tunnel junctions are key components of any superconductor electronic device. This includes superconducting quantum bits [1], superconducting quantum interference devices (SQUIDs) [2], rapid single flux quantum (RSFQ) circuits [3, 4], Josephson voltage standards [5], single electron transistors (SETs) [6, 7], Josephson parametric amplifiers [8, 9] or superconductor-insulator-superconductor (SIS) mixers [10, 11]. Most of these devices are based on refractory Josephson tunnel junctions made of an *in-situ* deposited Nb/Al-AlO$_x$/Nb trilayer, the latter being an excellent choice regarding junction quality, tunability of the critical current density, scalability and run-to-run reproducibility of characteristic junction parameters as well as resilience to thermal cycling. A key requirement for realizing integrated circuits based on these junctions is the availability of a wafer-scale fabrication process [12–14]. For this reason, research facilities make huge efforts to

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establish and maintain a fabrication process for high-quality Nb/Al-AlO_x/Nb Josephson tunnel junctions. In some cases, these efforts are further challenged by the need for minimizing the junction capacitance C_{JJ} to allow, for example, improving the energy resolution of SQUIDs [15, 16].

The capacitance $C_{JJ} = C_{int} + C_{par}$ of a Josephson tunnel junction is composed of an intrinsic and a parasitic contribution. The intrinsic capacitance C_{int} depends on the material and the dimensions of the tunnel barrier and is determined by barrier thickness d (setting the critical current density) and the junction area A_{JJ}. It scales inversely with the tunnel barrier thickness d. At the same time, the critical current density j_c scales exponentially with the tunnel barrier thickness d. For this reason, reducing the junction area A_{JJ} and simultaneously increasing the critical current density j_c effectively lowers the intrinsic junction capacitance assuming a fixed target value of the critical current I_c. The parasitic capacitance C_{par} is due to overlaps of the superconducting wiring with the junction electrodes that are separated by the wiring insulation. It strongly depends on the fabrication technology, i.e. the type and thickness of insulation layers, the required actual overlap between wiring layers, etc.

In the past, several fabrication processes for Nb/Al-AlO_x/Nb Josephson tunnel junctions have been developed. These are based on reactive ion etching and wet-chemical anodization [17, 18], chemical-mechanical polishing [19, 20], focused ion beam etching [21] or shadow evaporation [22]. Though these processes are used with great success, they either yield junctions with high capacitance or are prone to process variations due to barrier inhomogeneities or lithographic misalignments. Moreover, wet-chemical anodization requires a galvanic connection to ground, necessitating a temporary electrical connection of electrically floating devices such as rf-SQUIDs or qubits to their environment which must be removed in later fabrication steps. This complicates the fabrication process and introduces potential steps for junction damage.

Within this context, we present a variant of a fabrication process for cross-type Josephson tunnel junctions [18, 23, 24] that does not depend on wet-chemical anodization. Our process is hence particularly suited for fabricating electrically floating superconducting quantum devices. At the same time, the junction capacitance is minimized. Moreover, our process requires only a small number of fabrication steps, has in general the potential for wafer-scale fabrication and yields junctions with very high tunnel barrier homogeneity.

2. Description of fabrication process

Our Josephson tunnel junctions are based on a Nb/Al-AlO_x/Nb trilayer that is *in-situ* sputter-deposited on a thermally oxidized Si substrate. The thickness of the lower Nb base electrode, the Al layer and the upper Nb counter electrode are 100 nm, 7 nm and 100 nm, respectively. All layers are dc magnetron sputtered from 3 inch targets in a high vacuum (HV) sputter system with a base pressure in the order of 10^{-6} Pa.

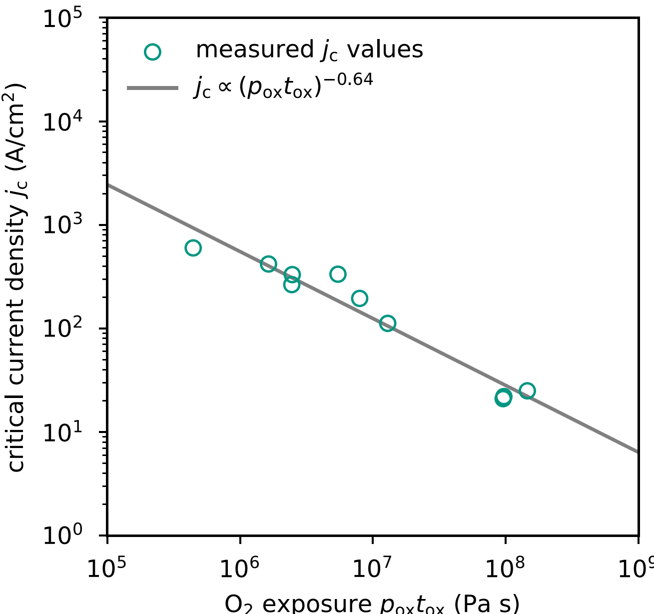

Figure 1. Measured dependence of the critical current density j_c on the oxygen exposure $p_{ox}t_{ox}$. The solid line is a fit to the measured data indicating the exponential dependence of the critical current density on the oxygen exposure.

During sputtering, the substrate is passively cooled by a thin layer of vacuum grease between substrate and sample holder. Prior to metal deposition, the substrate is pre-cleaned by an rf driven Ar plasma in the load-lock of the sputtering system. Both Nb layers are sputtered with a rate of 0.63 nm/s at a constant dc power of 300 W. The pressure of the Ar atmosphere during sputtering is 0.96 Pa to yield Nb free of mechanical stress [25]. The Al film is deposited in an Ar atmosphere with a pressure of 0.72 Pa using a dc power of 100 W resulting in a deposition rate of 0.31 nm/s. For tunnel barrier formation within the load-lock of the sputtering system, the Al layer is oxidized at room temperature in a static O_2 atmosphere with pressure p_{ox}. The critical current density j_c of the tunnel junctions depends on the total oxygen exposure $p_{ox}t_{ox}$ according to $j_c \propto (p_{ox}t_{ox})^{-0.64}$ (see figure 1). We typically vary the oxidation time t_{ox} at a fixed value of the oxidation pressure of $p_{ox} = 4$ Pa.

Figure 2 shows the individual fabrication steps for our cross-type Josephson junctions. After trilayer deposition (see figure 2(a)), a positive, high-resolution UV photoresist (AZ MIR 701 29CP supplied by Microchemicals GmbH) is spin-coated on top of the trilayer and patterned as a narrow stripe using direct laser lithography. The width of this stripe defines one of the lateral dimensions of the final Josephson junction (see below). The resulting photoresist mask is used for etching the entire trilayer stack (see figure 2(b)). Both Nb layers are etched by inductively coupled plasma reactive ion etching (ICP-RIE) using SF_6 and Ar in a mixing ratio of 2 : 1 at a constant pressure of 2 Pa as process gas. The rf power and the ICP power are 10 W and 300 W, respectively, resulting in an etch rate of 2.5 nm/s. The Al-AlO_x layer and the thermal oxide of

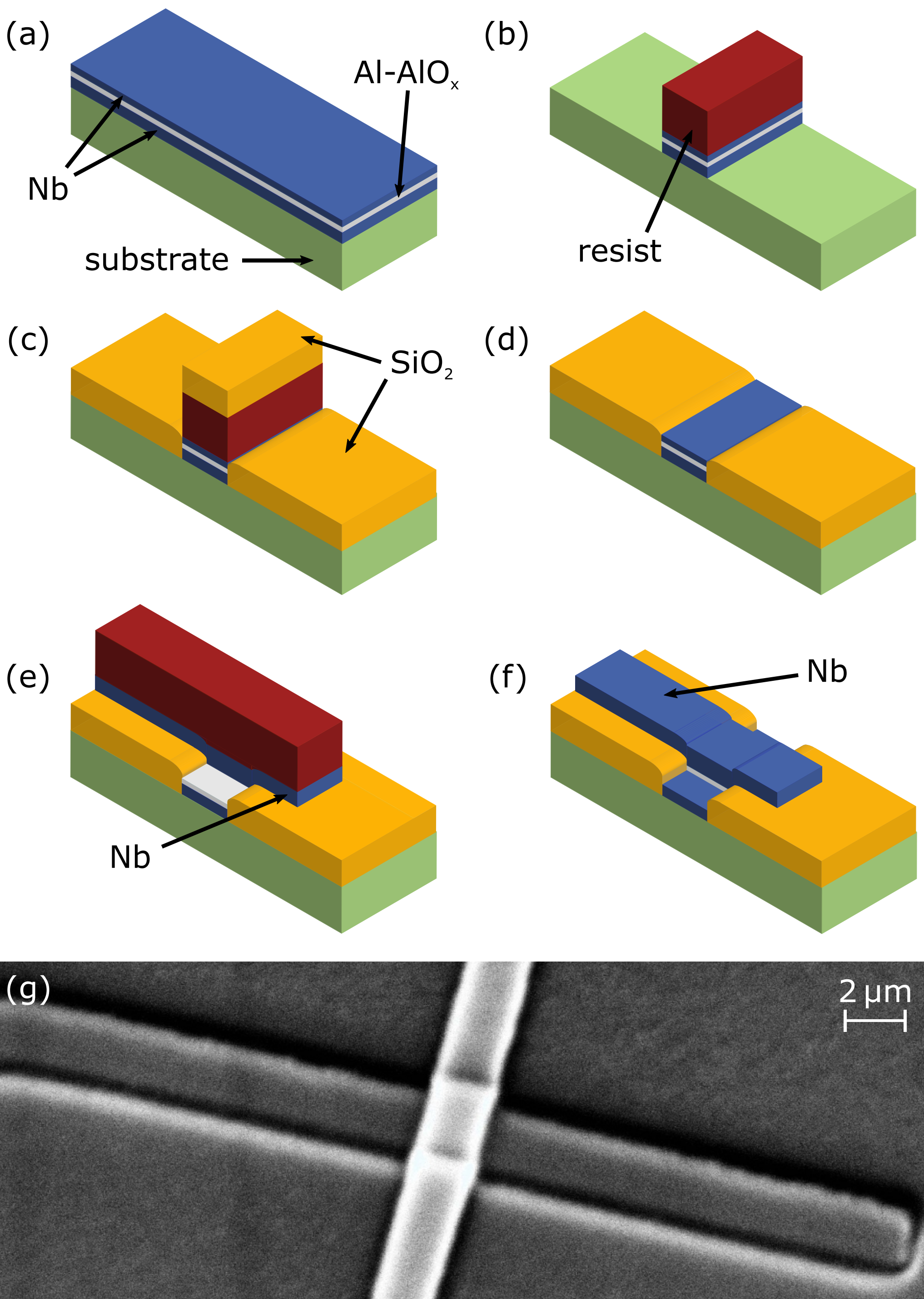

Figure 2. (a)–(f) Schematic overview of the different steps of our fabrication process for cross-type Josephson junctions. Shown are the state of the junction after (a) deposition of the Nb/Al–AlO$_x$/Nb trilayer, (b) trilayer patterning as a stripe, (c) deposition of the dielectric insulation layer for planarization, (d) removal of the photoresist mask, (e) deposition and patterning of the Nb wiring layer, and (f) removal of the residual Al and photoresist. Dimensions are not to scale. (g) Scanning electron microscope image of a finished cross-type Josephson junction.

the Si substrate, respectively, act as etch stop for the ICP-RIE processes. The Al-AlO$_x$ layer is wet-chemically etched with an etching solution consisting of phosphoric acid, nitric acid, acetic acid and water that are mixed in a ratio of 16 : 1 : 1 : 2. As will be shown in section 4, wet-chemical etching of the Al layer is key to guarantee a high junction quality when omitting wet-chemical anodization.

The next step is the deposition of a dielectric insulation layer (see figure 2(c)). The insulation is intended not only to protect the sidewalls of the patterned trilayer stripe, but also

to quasi-planarize the trilayer stack before the deposition of subsequent layers. For insulator deposition, we use the same photoresist mask as for trilayer patterning, i.e. the mask is not removed after the prior etching steps. It is important to note that the photoresist acts as a shadow mask during dc magnetron sputter deposition, resulting in trenches beside the trilayer stripe as can be seen in the scanning electron microscope (SEM) image of a finished junction in figure 2(g). We empirically found that the thickness of the insulation layer at the lowest point of these trenches is only about 50% of the nominally deposited material. For this reason, the thickness of the insulation layer must be at least twice the layer thickness of the Nb base electrode to prevent shorts between the base electrode and subsequent wiring layers. We hence deposit a 220 nm thick SiO_2 layer by rf magnetron sputtering utilizing a separate HV sputtering system, a gas mixture consisting of 60% Ar and 40% O_2 at a constant pressure of 0.7 Pa as process gas, and an rf power of 250 W. This results in an overall deposition rate of 1.3 nm/s.

After removal of the photoresist mask (see figure 2(d)), a Nb wiring layer with a thickness of 200 nm is dc magnetron sputter deposited using a HV sputter system with a base pressure below 6×10^{-6} Pa and a 2 inch Nb target. The Ar pressure and the dc power are 0.3 Pa and 70 W, respectively, resulting in a deposition rate of 0.3 nm/s. Prior to the deposition, the surface of the Nb counter electrode (upper Nb layer of the trilayer stripe) is pre-cleaned by Ar ion milling to remove native oxides and hence to ensure a superconducting contact between the counter electrode and the deposited Nb layer. This final layer is patterned by structuring a high-resolution UV photoresist (same as for trilayer patterning) as a narrow stripe that is oriented perpendicular to the embedded trilayer stripe and ICP-RIE for Nb etching. The top Nb layer of the trilayer stack is etched within the same etching cycle to define the final size of the counter electrode (see figure 2(e)). By this, we yield rectangular Josephson tunnel junctions from the overlap of the trilayer and Nb wiring stripe. Finally, the residual Al-AlO_x of the trilayer is removed by wet etching to enable later electrical contacts to the Nb base electrode (see figure 2(f)).

It is worth mentioning that the area of our cross-type Josephson junctions is only limited by the resolution of the lithographic tool and not by alignment accuracy. Due to the minimum structure size of our laser lithography tool of 1 μm, we are able to reliably fabricate cross-type junctions with a nominal area of $1\,\mu\text{m} \times 1\,\mu\text{m}$, but even sub-micrometer-sized junctions are achievable with the help of e.g. DUV steppers or electron beam lithography. Even though such small junctions require higher values of the critical current density to achieve a target value of the critical current, the total junction capacitance is reduced as the intrinsic capacitance C_{int} linearly decreases with the junction area A while the intrinsic capacitance per unit area C'_{int} only logarithmically increases with the critical current density j_c [26, 27]. In addition, the capacitance of cross-type junctions has a negligible parasitic contribution as there are no direct wiring overlaps. Besides that, only two lithographic layers are required during the entire fabrication process. The higher values of the critical current density further lower the time taken to fabricate a batch of cross-type junctions as, according to figure 1, the oxidation time for the formation of the tunnel barrier gets significantly shorter assuming a fixed oxidation pressure.

3. Experimental techniques for junction characterization

Up to now, we have successfully fabricated more than 15 batches of cross-type junctions with linear dimensions varying between 1.0 μm and 4.2 μm using our anodization-free fabrication process. The characteristic figures of merit and hence the quality of fabricated junctions as well as their uniformity across an entire wafer were determined by recording the current-voltage (IV) characteristics (see figure 3 as an example) of a sub-sample of each batch at a temperature of $T = 4.2$ K in a differential four-wire configuration. The utilized measurement set-up comprises low-pass filters at room and cryogenic temperatures to filter external rf interference signals. The dc bias current I is generated by applying a triangular voltage signal V_{gen} with a frequency of 3 Hz to the series connection of all resistors in the input circuit of the set-up. This includes the equivalent resistance $R_{\text{LPF}} = 10.4\,\text{k}\Omega$ of both rf filters as well as the voltage-dependent resistance $R(V) = V/I$ of the Josephson junction to be measured. The actual bias current through the junction hence depends on the voltage drop V across the junction and is given by

$$I = \frac{V_{\text{gen}}}{R_{\text{LPF}}}\left(1 - \frac{V}{V_{\text{gen}}}\right). \tag{1}$$

The voltage drop V is measured using a battery-powered differential amplifier. To screen the samples from disturbances induced by variations of magnetic background fields, the cryoprobe is equipped with a mu-metal and a superconducting shield made of Nb.

The quality of each Josephson junction is evaluated by means of different figures of merit, among those the critical current I_c, the normal state resistance R_N, the gap voltage V_{gap}, and the subgap resistance R_{sg}. As conventional, the subgap resistance is determined at a voltage value of $V = 2$ mV in the subgap region. From these quantities, the characteristic resistance ratio R_{sg}/R_N and the I_cR_N product are calculated. The former is a junction area independent figure of merit to quantify subgap leakage, e.g. due to defects or shorts in the tunnel barrier [28, 29]. The latter is a measure for the strength of Cooper pair tunneling that depends on the profile of the electric potential along the tunnel barrier [30].

The critical current I_c of each Josephson junction was determined by its relation $I_c = \kappa I_{\text{gap}}$ [31] to the gap current I_{gap} as the switching current I_{sw} at $T = 4.2$ K, extracted from IV-characteristics, is always significantly smaller than the true critical current. The gap current corresponds to the amplitude of the quasiparticles' tunneling current at the gap voltage. The

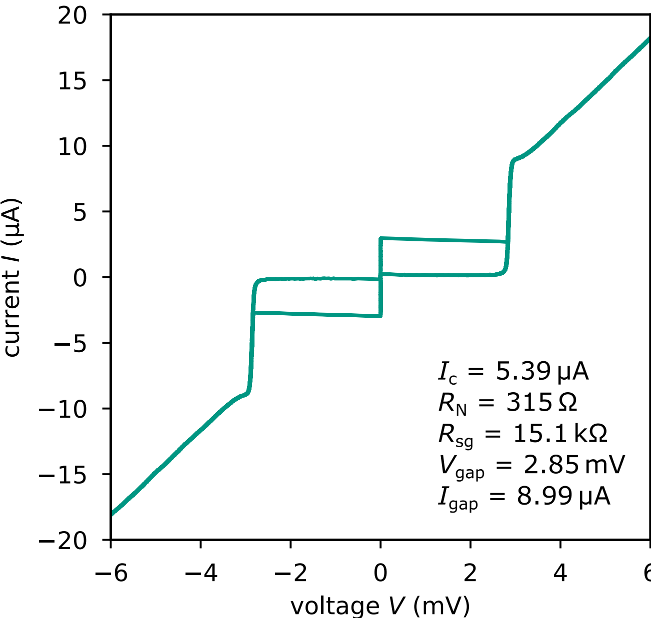

Figure 3. Current–voltage characteristic of one of our cross-type junctions with a target area of $1\,\mu m \times 1\,\mu m$ recorded at a temperature of $T = 4.2\,K$. All figures of merit except for the critical current I_c were taken directly from the characteristic. The critical current was obtained by the method described in section 3.

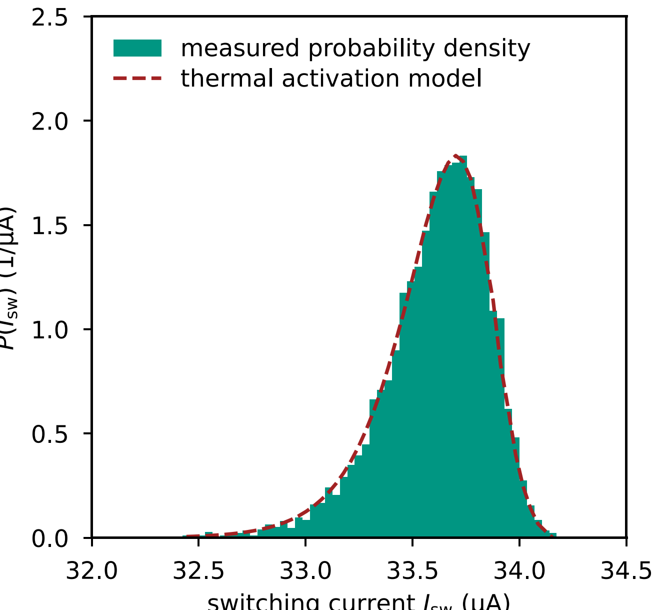

Figure 4. Switching current distribution $P(I_{sw})$ of a $3.4\,\mu m \times 3.4\,\mu m$-sized cross-type junction recorded at a temperature of $T = 4.2\,K$. For the measurement, the switching current of the junction was measured 5000 times by ramping up the bias current and recording the current values at which the junction switches from the superconducting into the normal conducting state. The solid red line represents a fit for a critical current of $I_c = 38.6\,\mu A$ according to the thermal activation model represented by equations (2) and (3).

deviation between the switching current I_{sw} and the critical current I_c is caused by thermal noise [32, 33]. The recursion formula

$$P(I_{sw}) = \tau^{-1}(I_{sw})\left(\frac{dI}{dt}\right)^{-1}\left[1 - \int_0^{I_{sw}} P(I)\,dI\right] \quad (2)$$

describes the related probability of the Josephson junction to escape from the zero-voltage state at a nominal switching current I_{sw} within the interval dI when a bias current I is injected with a sweep rate dI/dt. The temperature dependent escape rate

$$\tau^{-1} = a_{th}\frac{\omega_0}{2\pi}e^{-E_0/k_B T} \quad (3)$$

is a function of a temperature and damping dependent thermal prefactor a_{th}, the oscillation frequency $\omega_0 = \omega_p\left[1 - (I/I_c)^2\right]^{1/4}$ of the Josephson junction with $\omega_p = \sqrt{2\pi I_c/\Phi_0 C_{JJ}}$ denoting the plasma frequency and the height of the potential barrier E_0 [34]. It can be calculated from the measured switching current distribution $P(I_{sw})$ of a junction to determine its true critical current I_c by using iterative numerical methods [35]. Figure 4 shows as an example of the measured switching current distribution $P(I_{sw})$ at $T = 4.2\,K$ and a fit according to equations (2) and (3) for one of our cross-type junctions with a critical current of $I_c = 38.6\,\mu A$. The dimensionless factor $\kappa = I_c/I_{gap}$, used to calculate the critical current from the measured gap current, is independent of the junction size and constant for an entire junction batch. It was determined by measuring and evaluating the switching current distribution of some representative junctions from each batch.

In order to investigate the spatial profile of the critical current density j_c along the tunnel barrier, the dependence of the maximum supercurrent $I_{s,max}$ through the junction on an external magnetic field B_y was measured [36]. For these measurements, the mu-metal shield of our junction characterization set-up was removed and a Helmholtz coil was attached to the sample holder such that the junction was located in the center of the coil. To analyze the measured data (see, for example, figure 9 in section 4), a model of the distribution of the critical current density $j_c(z)$ was generated and the absolute value of the Fourier transform of this model was compared to the measured data.

The specific capacitance C'_{int} of our Josephson junctions was determined by observing Shapiro steps in unshunted dc-SQUIDs [37, 38]. For this, two types of symmetric, unshunted dc-SQUIDs based on cross-type junctions were designed and fabricated. Both variants differ by the junction size (see below). Figure 5 shows a micrograph and the corresponding equivalent circuit model of such a current-biased SQUID comprising $2\,\mu m \times 2\,\mu m$-sized cross-type Josephson junctions. The SQUID loop with inductance $L_s = 2(L_1 + L_2)$ is composed of two sections. The upper section with inductance $2L_1$ is patterned from the 200 nm thick Nb wiring layer. In contrast, the lower section with inductance $2L_2$ is formed by the 100 nm thick lower Nb layer of the trilayer stack. Both sections are connected via the Josephson junctions. Moreover, feedlines for injecting control currents $I_{ctr,1}$ and $I_{ctr,2}$ are connected to both loop sections at the location of the Josephson junctions. A 400 nm thick Nb ground plane, separated by an insulating SiO_2

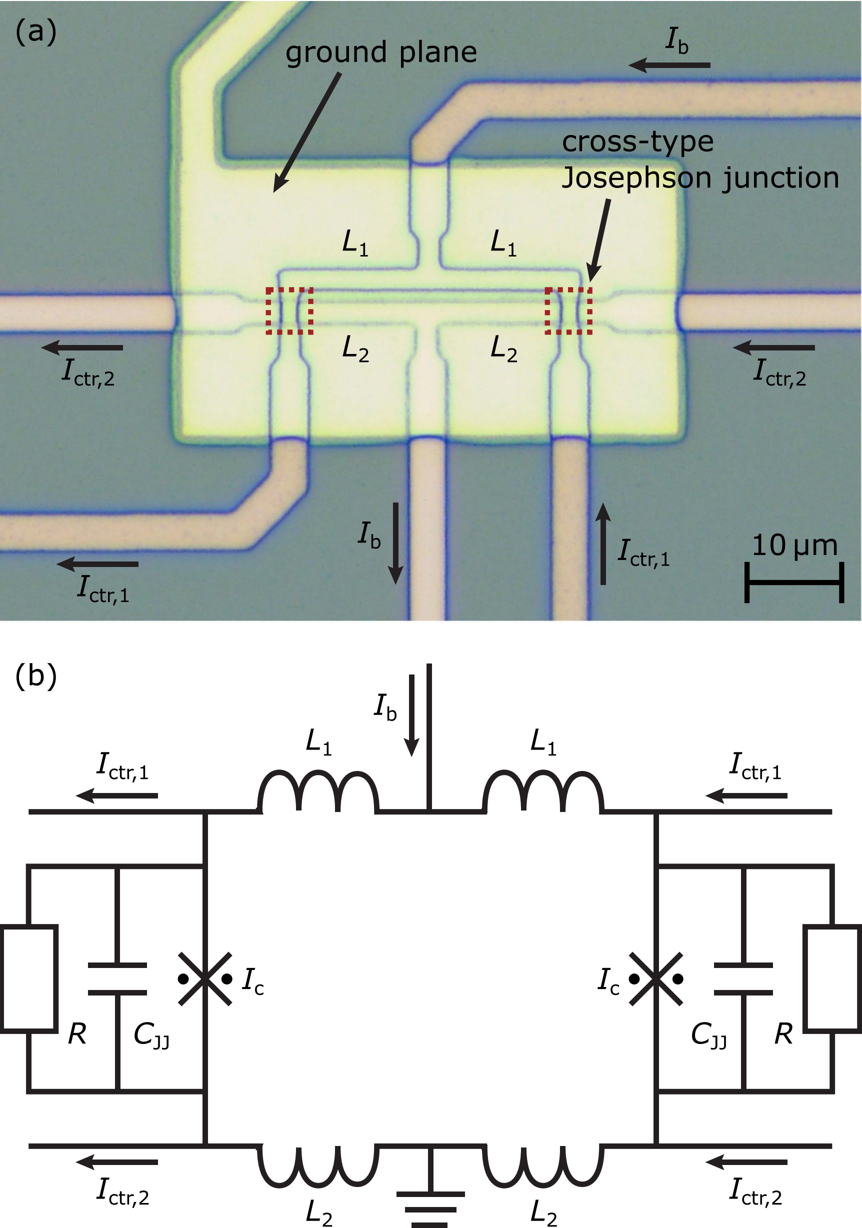

Figure 5. (a) Micrograph and (b) equivalent circuit model of a symmetric, unshunted dc-SQUID based on $2\,\mu\text{m} \times 2\,\mu\text{m}$-sized cross-type junctions (framed by dashed red boxes) biased by a current I_b. The SQUID was designed and fabricated to determine the specific capacitance of our Josephson junctions.

layer, was patterned on top of all devices to reduce cross-talk between both loop sections [39]. The resulting parasitic capacitance which is connected in parallel to the capacitance of the two Josephson junctions was estimated to be about 6 fF and corresponds to only 3 % of the smallest measured capacitance.

To observe the actual resonance steps in the *IV*-characteristic, the maximum supercurrent of a respective sample SQUID was suppressed by applying a control current through one of the feedlines. For $\Phi_s = 2L_i I_{ctr,i} = (n+1/2)\Phi_0$ with $i \in \{1,2\}$, $n \in \mathbb{Z}$ and Φ_s denoting the magnetic flux threading the SQUID loop, the maximum supercurrent is at its minimum. At the same time, the periodicity $|\Delta I_{ctr,i}| = \Phi_0/(2L_i)$ of the maximum supercurrent modulation with $\Delta I_{ctr,i}$ being the current difference between two neighboring minima was used to determine the inductance of the SQUID loop [40]. The value of L_s for our unshunted SQUIDs with $2\,\mu\text{m} \times 2\,\mu\text{m}$-sized junctions was simulated to be $L_s = 14.7\,\text{pH}$ using InductEx (numeric simulation software by SUN Magnetics (Pty) Ltd) and is in perfect agreement with the experimental value of $L_s = 14.0\,\text{pH}$ taking into account possible fabrication induced size and alignment variances. We also fabricated devices with $4\,\mu\text{m} \times 4\,\mu\text{m}$-sized cross-type junctions to determine the specific capacitance C'_{int} for junctions with critical current densities $j_c < 100\,\text{A/cm}^2$. Here, the

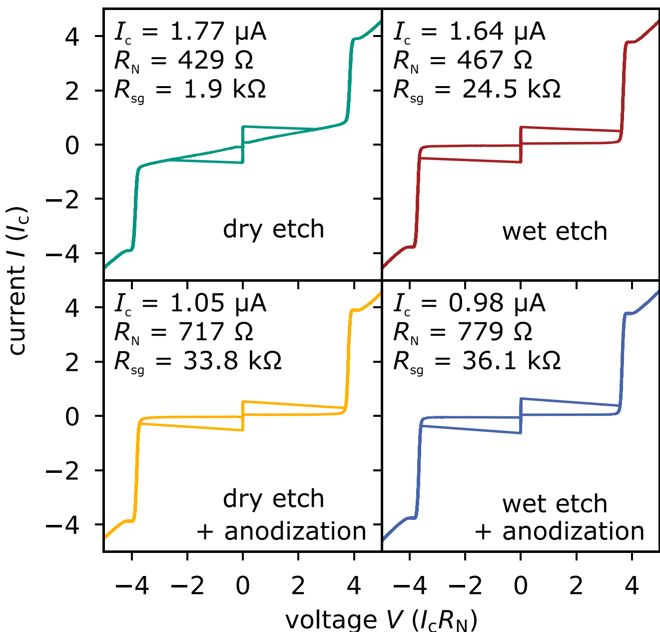

Figure 6. Normalized IV-characteristics of anodized (lower row) and non-anodized (upper row) cross-type junctions with a target area of $A_{tar} = 2.9\,\mu m \times 2.9\,\mu m$ measured at $T = 4.2$ K. The Al-AlO_x layer was etched using Ar ion milling in an ICP-RIE system (left column) or using an acidic etching solution based on nitric and phosphoric acid (right column). Note that the current drops to a value below the critical current I_c as the junction jumps into the voltage state due to the voltage dependent junction resistance that is connected in series with the bias resistors (see description of experimental set-up in section 3).

calculated loop inductance is $L_s = 9.6$ pH which is again in good agreement with the experimental value of $L_s = 10.6$ pH.

4. Results and discussion

4.1. Sidewall insulation and characteristic resistance ratio

A key factor for the reliable and reproducible fabrication of high-quality cross-type Josephson junctions based on a Nb/Al-AlO_x/Nb trilayer stack is a sufficient galvanic isolation between the base electrode of the junction and a subsequent wiring layer to its top electrode. In our process, this insulation is realized by the quasi-planarizing insulation layer with sufficient thickness to compensate for trenching effects and, even more important, the usage of wet-chemical etching during trilayer etching (see figure 2(b)). During the wet etching process for removing the Al-AlO_x layer, nitric acid oxidizes the Al surface, while phosphoric acid dissolves the native as well as the continuously formed aluminum oxide. Since niobium, similar to aluminum, oxidizes in nitric acid, but niobium oxide does not dissolve in phosphoric acid [41], an oxide layer of a few nm thickness forms on the exposed sidewalls of the patterned Nb/Al-AlO_x stripe and on the surface of the still unstructured lower Nb of the trilayer. This oxide layer serves as a passivation layer. Moreover, compared to plasma induced ion milling no etching residues from redeposited Al atoms [42] appear during wet etching. These residues potentially adhere to the sidewalls of the etched structure forming shorts across the tunnel barrier. Similarly, the passivation layer protects against the formation of shorts originating from potential redeposits during Nb base electrode etching. Overall, the passivation layer formed during wet etching takes on the same task as wet-chemical anodization, however, without the need for a galvanic contact between all patterned trilayer structures.

To prove that wet etching of the Al-AlO_x layer using our acidic etching solution in fact substitutes the anodization of the sidewalls of the patterned trilayer stack, we prepared two distinct batches of cross-type junctions. The Nb/Al-AlO_x/Nb trilayer of both batches was sputtered in the same deposition run by placing both substrates side-by-side on the sample holder in the sputter system. For one batch, the Al-AlO_x layer was wet-chemically etched, for the other batch Ar ion milling within the ICP-RIE system was used. For about one half of the Josephson junctions of each batch, the sidewalls were additionally anodized after etching the trilayer stripe.

Figure 6 shows current-voltage characteristics of representative cross-type Josephson junctions for each variant. Irrespective of the actual etching technique, the junctions with anodized sidewalls are of high quality which is indicated by very low subgap leakage. Non-anodized junctions for which the Al-AlO_x was wet-chemically etched are of the same quality and have low subgap leakage. In contrast, the IV-characteristics of non-anodized, dry etched cross-type junctions exhibit severe leakage. We attribute this to vertical shorts across the tunnel barrier caused by non-passivated Al and Nb redeposits. For the dry etched junctions, where anodization is subsequently performed, these redeposits get oxidized during anodization. We note that the critical current I_c of anodized junctions is about 40% smaller than of non-anodized junctions and attribute this to the reduced junction area due to the anodization induced thick oxide layer on the sidewalls.

The number of redeposits that potentially lead to shorts across the tunnel barrier and hence the subgap leakage are expected to increase with the junction width W. Figure 7 displays the dependence of the characteristic resistance ratio R_{sg}/R_N on the width of the quadratic Josephson junctions from the two examined batches and confirms this hypothesis. We observe an increase of spread with increasing junction size for the dry etched junctions with non-anodized sidewalls (filled circles). Note that the yield of junctions of this variant is only 48%, i.e. about every second junction has very high subgap leakage or shows an Ohmic IV-characteristic. The fact that this large spread is not observed for anodized junctions from the same batch (open diamonds) is a clear indication that the leakage originates from the sidewalls and not from the tunnel barrier itself. The significantly larger yield of about 90% for all other variants further emphasizes that.

The comparison between the non-anodized, wet-chemically etched junctions (filled triangles), the anodized junctions from the same batch (open squares) as well as the dry etched, anodized junctions (see figure 7) shows that the use of an acidic etching solution for removing the Al-AlO_x layer indeed replaces wet-chemical anodization of the sidewalls of cross-type Josephson junctions. These three variants show a significantly smaller spread of the characteristic

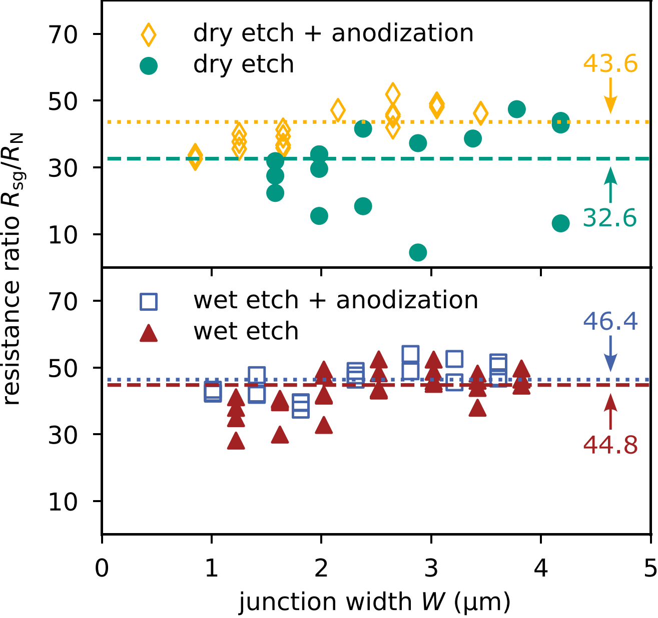

Figure 7. Resistance ratio R_{sg}/R_N versus junction width for quadratic cross-type junctions based on the same Nb/Al-AlO$_x$/Nb trilayer with anodized (open symbols) and non-anodized (filled symbols) sidewalls, whose Al-AlO$_x$ layer was dry etched (diamonds and circles) or wet etched (squares and triangles). Dotted and dashed horizontal lines mark the mean value for anodized and non-anodized junctions, respectively.

resistance ratio as compared to the one with non-anodized dry etched junctions. The ratio tends to get larger the larger the junction is. We attribute this to edge effects that are not caused by redeposits at the sidewalls. Moreover, a direct comparison of the mean characteristic resistance ratios indicates that wet etched, non-anodized junctions (filled triangles) show generally lower subgap leakage than dry etched, anodized specimens (open diamonds). This favors the usage of our fabrication process as compared to processes relying on dry etching the Al-AlO$_x$ layer and subsequent wet-chemical anodization.

4.2. Scalability and uniformity of critical current and normal state resistance

For all batches of Josephson junctions that were produced using our anodization-free fabrication process, we checked for the scalability of the critical current I_c and the normal state resistance R_N with respect to the junction area as well as for the uniformity of these parameters within a batch. Figure 8(a) and (b) show as an example the results for the batch with internal labeling KA-CJJ-3w9 with a critical current density of about $600\,\mathrm{A/cm^2}$. This batch contains a total of 16 chips with 8 junctions each, 6 of which were measured per cool-down. As expected, both, the critical current I_c and the normal state resistance R_N, scale linearly with the effective and the inverse effective junction area, respectively. We note that the effective junction area A deviates from the target value A_{tar} as the lateral junction size deviates by a length ΔW. We determine the deviation by a linear fit $R_N = \rho_N/(W_{tar}+\Delta W)^2$, ρ_N denoting the normal state resistivity, to the data in figure 8(a) and find that the size of the cross-type junctions of the batch internally labeled KA-CJJ-3w9 is on average only $0.19\,\mu$m smaller than the target value. We attribute this deviation to size variations in the photoresist masks and to a parasitic lateral material loss during both ICP-RIE and isotropic wet etching. Deviations from the linear fit only occur for the smallest junctions with a target area of $A_{tar} = 1\,\mu\mathrm{m}\times 1\,\mu\mathrm{m}$, for which a potentially location dependent variation of the junction size has the greatest effect.

Besides the scalability of the critical current and the normal state resistance, our cross-type junctions also show a high quality that is reflected, for example, by the high average values of the characteristic resistance ratio of $R_{sg}/R_N > 30$ for small junctions with $W < 2\,\mu$m and of usually $R_{sg}/R_N > 40$ for junctions with $W \geq 2\,\mu$m (compare figure 7) or the value of the gap voltage V_{gap}. For all batches, $V_{gap} > 2.8\,$mV, i.e. the gap voltage is very close to the value or the energy gap of Nb [43] and the proximity effect due to the Al layer is negligible. We find $\langle R_{sg}/R_N\rangle = 44.3$ for batch KA-CJJ-3w9 summarized in table 1 and the values for the gap voltage of all 30 junctions measured are normally distributed with a standard deviation of only $\sigma = 0.01\,$mV from the average $\langle V_{gap}\rangle = 2.84\,$mV. The I_cR_N product (see figure 8(c)) is independent of junction size and is as high as $I_cR_N = 1.7\,$mV for the example batch discussed here. This observation and the almost size independent resistance ratio (see figure 7 and table 1) indicate that the performance of Nb/Al-AlO$_x$/Nb Josephson tunnel junctions produced with our cross-type fabrication process is not affected by edge effects caused by the process but rather by the intrinsic properties of the tunnel barrier that, of course, could be further optimized.

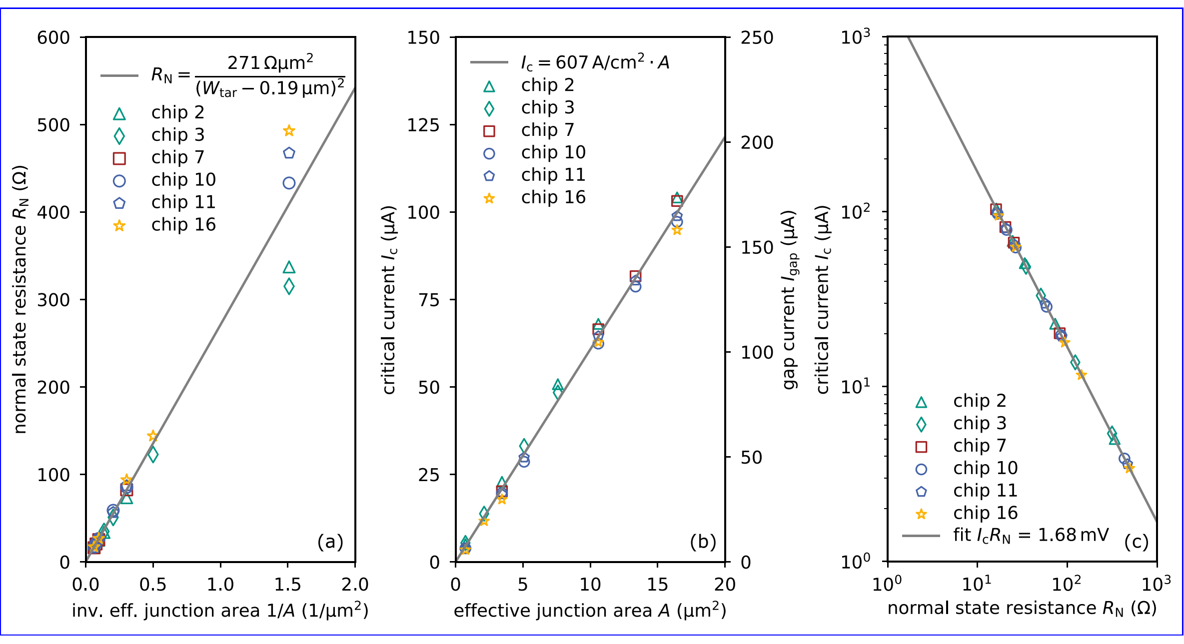

Figure 8. Dependence of (a) the normal state resistance R_N and (b) the critical current I_c on the inverse effective junction area and effective junction area $A = (W_{tar} + \Delta W)^2$, respectively, for cross-type junctions from different test chips of a single batch internally labeled KA-CJJ-3w9 produced with our anodization-free fabrication process.The solid lines indicate the result of a fit (a) $R_N = \rho_N/(W_{tar} + \Delta W)^2$ and (b) $I_c = j_c \cdot A$ of the expected linear dependencies and allow to determine the critical current of this batch to be $j_c = 607\,A/cm^2$ and a deviation of the junction size from the target value by only $\Delta W = -0.19\,\mu m$. (c) Critical current I_c versus normal resistance R_N for junctions from example batch KA-CJJ-3w9. The solid line represents the result of a fit according to I_cR_N = const. and allows to determine that the I_cR_N-product takes a value of 1.68 mV.

Table 1. Summary of the characteristic figures of merit of cross-type junctions from the batch internally labeled KA-CJJ-3w9 measured and determined at 4.2 K. Values in one row correspond to the mean values per junction size across all measured 6 test chips.

target size (μm^2)	I_{gap} (μA)	I_c (μA)	R_N (Ω)	V_{gap} (mV)	I_cR_N (mV)	R_{sg}/R_N
1 × 1	7.10	4.26	409	2.85	1.74	47.6
1.6 × 1.6	21.2	12.7	133	2.84	1.69	47.1
2 × 2	33.3	20.0	84.3	2.84	1.69	46.1
2.4 × 2.4	50.8	30.5	55.3	2.84	1.69	47.8
2.9 × 2.9	82.7	49.6	34.2	2.85	1.70	42.9
3.4 × 3.4	108.0	64.8	25.9	2.84	1.68	37.4
3.8 × 3.8	133.7	80.2	20.7	2.84	1.66	42.2
4.2 × 4.2	166.0	99.6	16.5	2.84	1.64	42.7

4.3. Profile of the critical current density

The usage of our fabrication process for cross-type Josephson junctions turns out to positively affect the critical current density profile $j_c(z)$ of the tunnel barrier. This can be seen by a comparison between the critical current density distributions shown in figures 9(b) and (d). Both profiles were generated as models to describe the measured dependencies of the maximum supercurrent $I_{s,max}(I_B)$ of a $13\,\mu m \times 13\,\mu m$ window-type and a $4.2\,\mu m \times 4.2\,\mu m$ cross-type Josephson junction on the current I_B through the Helmholtz coil of our measurement setup (see section 3). The corresponding plots are shown in figures 9(a) and (c), respectively. The batch of Nb/Al-AlO$_x$/Nb window-type junctions was fabricated separately using an anodization-free process based on the one described in [44] in which the Al-AlO$_x$ layer was etched by Ar ion milling. The modeled critical current density profile plotted in figure 9(b) is based on two assumptions: 1.) Due to small damages at the edges of the tunnel barrier during dry etching of the Nb top electrode and the Al-AlO$_x$ layer, the flanks of the j_c-profile are not upright but slightly quadratically shaped. 2.) The momentum of the Ar ions during surface cleaning of the top electrode prior to the deposition of the Nb wiring is transferred to the underlying tunnel barrier where it causes damage and thus a reduced critical current density. The area in which this effect occurs is restricted to the size of the window in the insulation layer which is $11\,\mu m \times 11\,\mu m$. The measured magnetic field dependence agrees very well with the prediction from the modeled $j_c(z)$-profile. The modeled critical current density profile of the cross-type junction shown

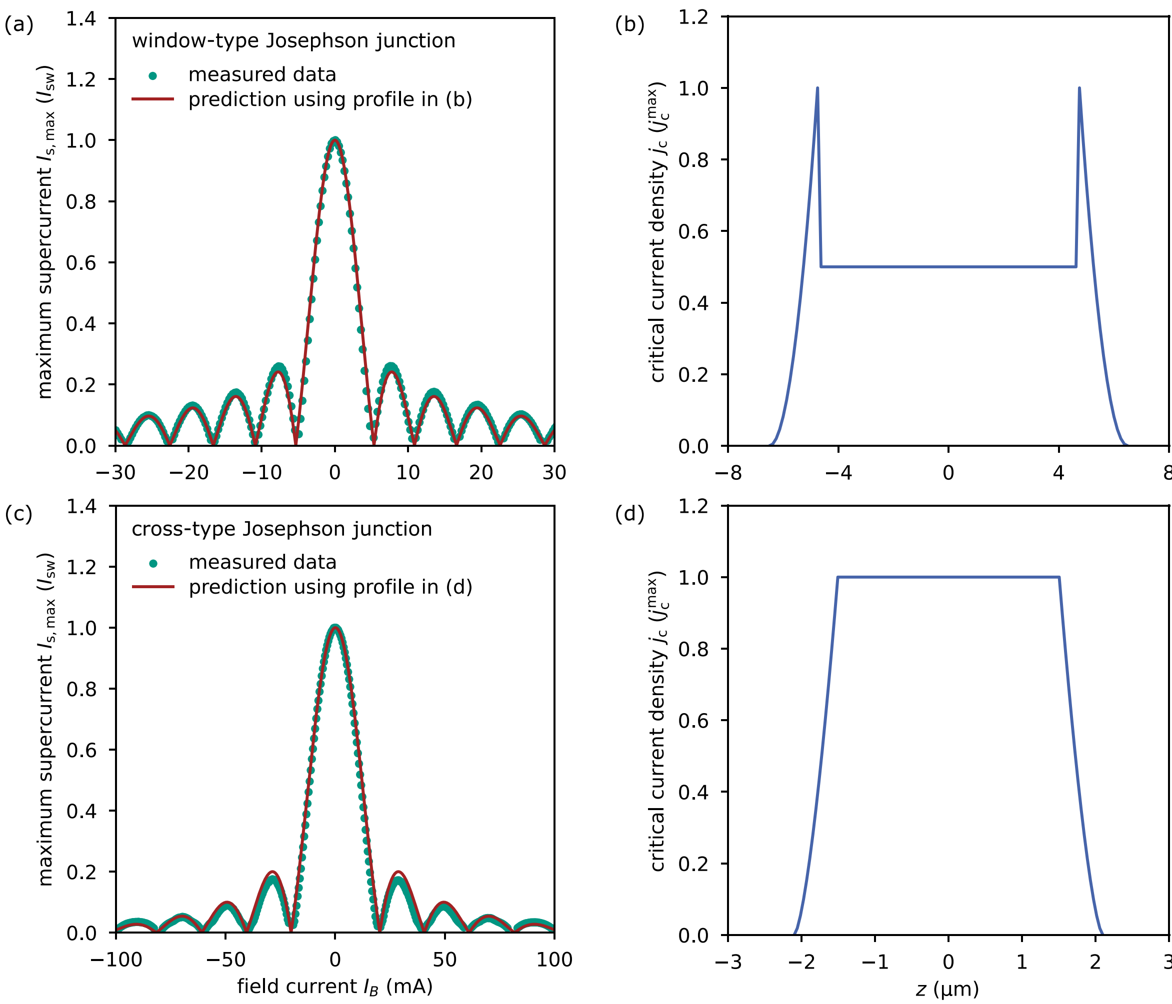

Figure 9. Magnetic field dependence of the normalized maximum supercurrent $I_{s,max}$ of (a) a $13\,\mu m \times 13\,\mu m$ window-type junction and (c) a $4.2\,\mu m \times 4.2\,\mu m$ cross-type Josephson junction. For normalization the switching current I_{sw} for zero magnetic field was used. The solid red line corresponds to the predicted magnetic field dependence assuming the corresponding critical current density profile $j_c(z)$ plotted in (b) and (d), respectively.

in figure 9(d) only assumes small damages at the edges of the tunnel barrier during dry etching of the trilayer stack. It clearly exhibits no indentation and yet describes the measured data in figure 9(c) well. Since there is no insulation window on top of the top electrode for a cross-type Josephson junction, the momentum/energy transfer of the Ar ions should be distributed evenly over the entire tunnel barrier, giving rise to a more homogeneous tunnel barrier.

4.4. Capacitance measurements

We measured the capacitance C_{JJ} of several cross-type Josephson junctions taken from batches with different critical current densities using unshunted dc-SQUIDs as described in section 3. As the parasitic capacitance C_{par} is expected to be negligible due to the missing overlap of wiring layers, the measured values should resemble the intrinsic capacitance related to the tunnel barrier. Figure 10 summarizes the result of our measurements and shows the dependence of the inverse junction capacitance per area C'_{JJ} on the critical current density j_c for each measured SQUID. We note that the specific capacitance $C'_{JJ} = C_{JJ}/A$ is derived from the measured capacitance value C_{JJ} as well as the effective junction area A that is determined from fitting the dependence of the normal state resistance on the junction area (see section 4.2). Moreover, figure 11 shows an example of a recorded Shapiro step of a current-biased SQUID with an experimentally determined loop inductance of $L_s = 14.0\,\mathrm{pH}$ and a critical current of $I_c = 9.65\,\mu A$ of the Josephson junction. The resonance voltage $V_{res} = 221\,\mu V$ for deriving the junction capacitance

$$C_{JJ} = \frac{\Phi_0^2}{2\pi^2 V_{res}^2 L_s} \tag{4}$$

was determined by fitting the expected shape of the resonance curve to the actual data [47]. The value of the damping parameter $\Gamma = I_c R / V_{res}$ required for performing this fit was extracted from its relation to the current ratio $I_{res}/2I_c$ [48]. For the resonance curve shown in figure 11, $\Gamma = 13.3$. The amplitude of the measured resonance step does not reach

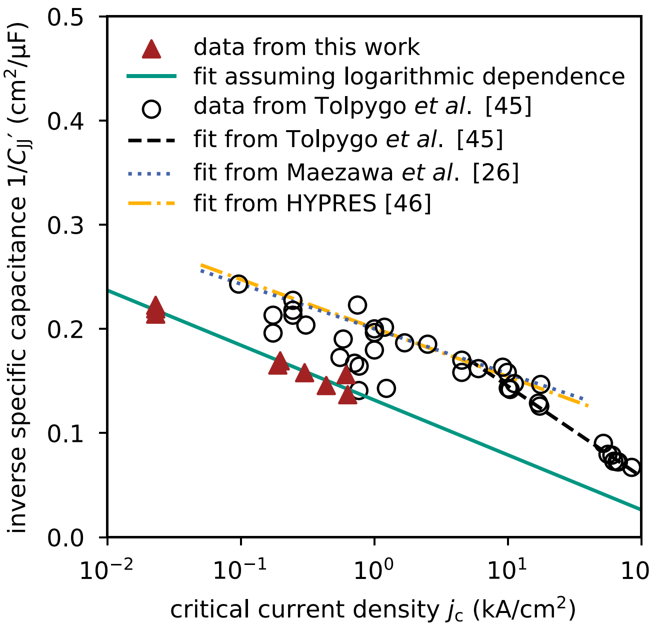

Figure 10. Inverse specific capacitance C'_{JJ} versus critical current density j_{c}. For our data, each data point represents one characterized unshunted SQUID. The solid green line with $1/C'_{\mathrm{JJ}} = 0.132\,\mathrm{cm}^2/\mu\mathrm{F} - 0.053\,\mathrm{cm}^2/\mu\mathrm{F}\,\log_{10}\left(j_{\mathrm{c}}\,\mathrm{cm}^2/\mathrm{kA}\right)$ represents the result of a fit to the data assuming a logarithmic dependence. The data points and the dashed line in black are from [45], the dotted blue line is from [26] and the dash-dotted yellow line is from [46] for comparison.

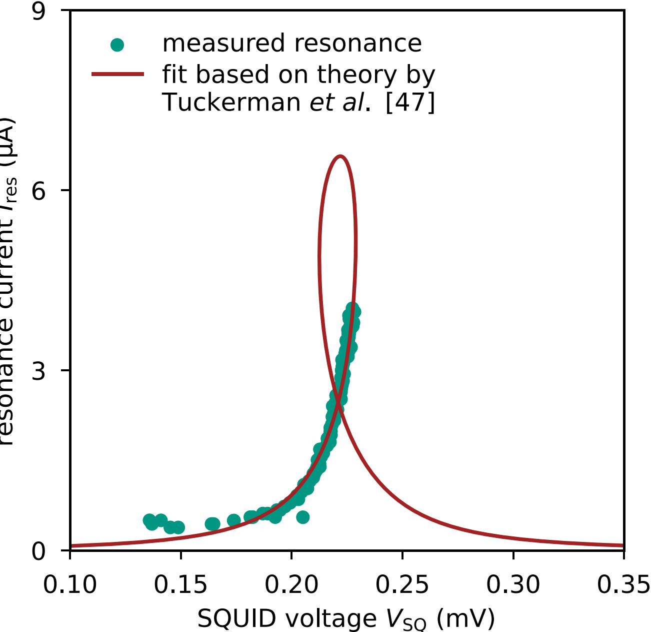

Figure 11. Expected and measured voltage-dependence of the resonance current I_{res} for an unshunted dc-SQUID with inductance $L_{\mathrm{s}} = 14.0\,\mathrm{pH}$, resonance voltage $V_{\mathrm{res}} = 221\,\mu\mathrm{V}$, damping parameter $\Gamma = 13.33$ and junction critical current $I_{\mathrm{c}} = 9.65\,\mu\mathrm{A}$. More details are given in the main text.

the theoretically expected value due to thermal suppression at $T = 4.2\,\mathrm{K}$.

The solid line in figure 10 represent a fit to the data assuming a logarithmic dependence of the specific capacitance on the critical current density [26, 27]. We find

$$\frac{1}{C'_{\mathrm{JJ}}} = 0.132\frac{\mathrm{cm}^2}{\mu\mathrm{F}} - 0.053\frac{\mathrm{cm}^2}{\mu\mathrm{F}}\log_{10}\left(\frac{j_{\mathrm{c}}}{\mathrm{kA}/\mathrm{cm}^2}\right). \quad (5)$$

For comparison, we also display the data and derived functional dependencies of the specific capacitance published in [45] and the references therein. We see that in a critical current density range between approximately $0.01\,\mathrm{kA}/\mathrm{cm}^2$ and $10\,\mathrm{kA}/\mathrm{cm}^2$ the slope of the functional dependence of our cross-type Josephson junctions is similar to those published by other research groups [26, 46]. Nevertheless, the offset is slightly higher which might be related to different crystal structures of the aluminum oxide barrier.

5. Conclusion

We have developed an anodization-free fabrication process for Nb/Al-AlO_x/Nb cross-type junctions. Our process requires only a small number of fabrication steps and can easily be adapted for wafer-scale fabrication. Fabricated junctions are of very high quality as indicated by the measured values for the subgap to normal state resistance ratio and the $I_{\mathrm{c}}R_{\mathrm{N}}$ product. Compared to other junction types manufactured under the same technical conditions, our cross-type Josephson junctions show not only a significantly reduced specific capacitance but also an almost rectangular critical current density profile. Our process hence enables the usage of low capacitance Josephson junctions for superconductor electronic devices such as ultra-low noise dc-SQUIDs, microwave SQUID multiplexers based on non-hysteretic rf-SQUIDs, and RFSQ circuits.

Data availability statement

The data that support the findings of this study are available upon reasonable request from the authors.

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