Error Storage Based Online Linearization of the Nonlinear Transfer Function of a High Power Dual Active Bridge

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***Abstract*—This paper introduces an error storage based online linearization method for the reduction of the nonlinearity inherent in the current transfer function of a Dual Active Bridge in order to increase the possible dynamics of current and voltage control. The proposed algorithm autonomously learns deviations from the ideal current transfer function based on previous operational data of the current controller. This approach enables real-time compensation through the implementation of an error storage system, resulting in an effective online compensation method. Furthermore, this method is not limited to Dual Active Bridges but can also be used for any other time invariant system with repeating operation points and nonlinear transfer characteristics. The algorithm is implemented on a Field Programmable Gate Array and experimentally verified on a 40 kW test bench. Experimental measurements affirm the practical feasibility and effectiveness of this algorithm.**

***Index Terms*—DCDC-Converter, Dual Active Bridge, Error Compensation, Linearization**

I. Introduction

In the field of power electronics, the Dual Active Bridge (DAB), originally introduced in [1], has attracted considerable interest for its adaptable and efficient power conversion capabilities. The DAB transfers power between two galvanically isolated voltage levels through a medium frequency transformer while maintaining precise adjustability of the controlled variables such as the output current. Contrary to the simplistic theoretical description of the current transfer function for Single Phase Shift (SPS) modulation [1], the current transfer function of a real DAB is generally nonlinear when the DAB is designed for a high power levels [2]–[5]. In particular, this effect is more dominant, if the leakage inductance of the AC circuit is small. This nonlinearity has several causes, including the switching dynamics of the semiconductors, parasitic capacities of the semiconductors and the influence of different control strategies and operation points. In most applications, standard PI-controllers can effectively manage the nonlinearity of the transfer function within certain limits. At stationary operation points, the actual output current eventually matches the setpoint. However, achieving the highest dynamic performance of the DAB poses a significant challenge due to the aforementioned nonlinearity. While understanding the parasitic principles that cause this nonlinear behavior is essential to systematically reduce them, this paper primarily focuses on the development and utilization of a compensation strategy to mitigate or even eliminate the adverse effects of the nonlinearity. This approach aims to improve the overall performance, controllability and operation range of the DAB. The aim is to introduce an adaptable, scalable and versatile online method to linearize the nonlinear current transfer function of a DAB with SPS modulation. However, the functionality of the presented method is neither restricted to the DAB as the used topology nor to SPS as the used modulation scheme. The paper is organized as follows. Section II highlights the main reasons for the nonlinearity of the DAB's current transfer function. In Section III, the concept and the mathematical basics of the method, called Error Storage Based Online Linearization (ESBOL), are introduced and explained in detail. In Section IV, the test bench used to generate the measured results with and without the adaptation method, shown in Section V, is presented. Finally, Section VI summarizes the most important results of the proposed method.

II. Derivation of Nonlinearity

To comprehend the reason for the nonlinearity of the current transfer function, it is necessary to analyze the equivalent circuit diagram of the DAB, taking into account the parasitic output capacitances in parallel with the MOSFETs, C_{oss}. Figure 1 shows the equivalent circuit of a DAB with only the capacitors at T1 and T2. U_{p} is the primary DC voltage,

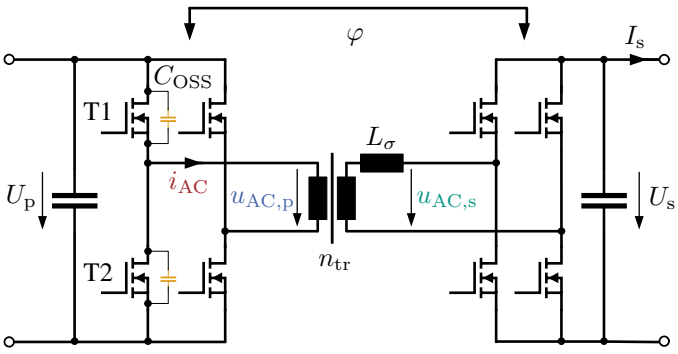


Fig. 1: Circuit diagram of a DAB with parasitic capacities C_{OSS} highlighted in orange across T1 und T2.

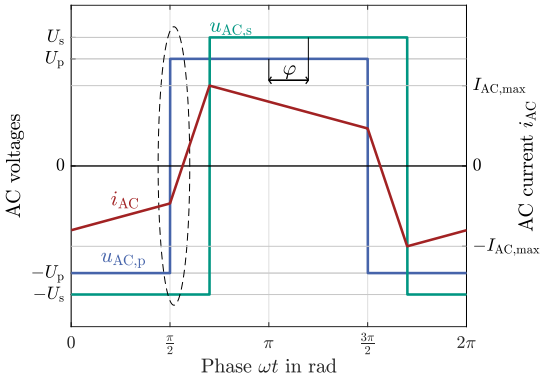
$u_{AC,p}$ is the AC voltage on the primary side of the transformer. Replacing each index 'p' with index 's' represents the corresponding values on the secondary side. The AC current through the transformer is called i_{AC}. The rectified and filtered transformer current leads to the secondary output current I_s. The leakage inductance L_σ is transformed to the secondary side. For simplicity, the transformer's winding ratio n is set to 1. The value φ is used as the phase shift between the primary and the secondary sides of the two full bridges. Dividing the basic power transfer equation of the DAB (1), shown in [1], by the secondary DC voltage U_s gives the rectified and filtered output current I_s as shown in (2). To obtain the control variable φ as a function of the required output current, (2) can be rearranged to (3).

$$P_s = U_s \cdot I_s = \frac{n_{tr} U_p U_s}{2\pi^2 f_{sw} L_\sigma} \cdot \varphi(\pi - |\varphi|) \tag{1}$$

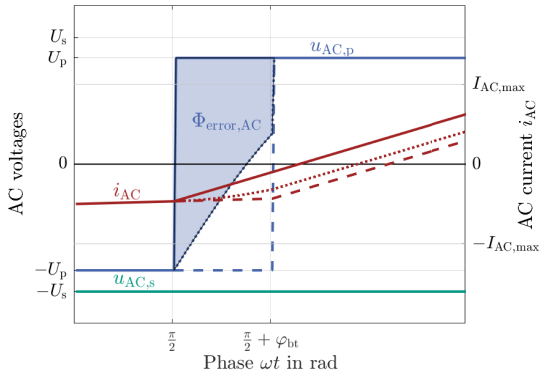
$$I_s = \frac{n_{tr} U_p}{2\pi^2 f_{sw} L_\sigma} \cdot \varphi(\pi - |\varphi|) \tag{2}$$

$$\varphi = \mathrm{sign}(I_s^*) \cdot \frac{\pi}{2} \left(1 \pm \sqrt{1 - \frac{8 f_{sw} L_\sigma |I_s^*|}{n_{tr} U_p}} \right) \tag{3}$$

Hence, the controller can calculate the necessary phase shift φ according to (3) leading to a perfectly linear transfer function. In these equations the variable f_{sw} is the switching frequency of the DAB. Figure 2a shows the general voltage and current curves of the AC circuit in a DAB operated with SPS modulation according to the theory. The blue line represents the AC voltage of the primary side $u_{AC,p}$, the green line represents the AC voltage of the secondary side $u_{AC,s}$ with an intended phase shift of φ according to (3). The resulting AC current in the transformer i_{AC} is shown in red. However, due to parasitic effects of the system the actual voltage and current curves look different. These effects are caused by the parasitic capacitances of the MOSFETs, the blocking time T_{bt} between the low and the high side MOSFETs, and the stray inductance L_σ. The non-ideal, encircled commutation process in Figure 2a is shown in more detail in Figure 2b. The solid blue line shows the ideal commutation process of the primary full bridge voltage $u_{AC,p}$. The solid red line shows the AC current i_{AC}



(a)



(b)

Fig. 2: Qualitative voltage and current waveforms of a DAB with SPS modulation. Here the DAB works in positive boost mode, i.e. $I_s > 0\,\mathrm{A}$ and $U_s > U_p$. In (a), the ideal waveforms are shown and in (b) a zoom of the non-ideal commutation process of the primary full bridge (dashed oval) is depicted. The blocking time T_{bt} can be represented as a blocking angle $\varphi_{bt} = T_{bt} \cdot f_{sw} \cdot 2\pi$.

according to an ideal commutation. In contrast, the two dashed lines show the worst case scenario of the AC voltage and the AC current, respectively. A possible real commutation process is illustrated with the dotted lines of the AC voltage and the AC current. This ultimately results in a different phase shift φ than intended because of the additional error in the voltage-time-area $\Phi_{error,AC}$. As a consequence, there is a deviation in the expected output current I_s. In particular, if the setpoints change frequently, the accuracy and therefore the dynamics of the output current will decrease, which may ultimately lead to a deviation in the output voltage.

In [2], researchers conducted an analysis of the effect of varying semiconductor blocking times T_{bt} on the nonlinearity of the current transfer function. Their results showed a correlation between increased blocking time and increased deviations between the actual and ideal transfer functions. As shown in Figure 2b, reducing the blocking time T_{bt} and thus φ_{bt} leads to a smaller possible error in the voltage-time area $\Phi_{error,AC}$. In an effort to mitigate this nonlinearity, [3] introduced a non-

linear cancellation algorithm designed to linearize the transfer function. However, this algorithm is challenging to tune and there is still an output power offset when the phase shift φ is close to zero. In [4], an alternative modulation strategy has been proposed involving the incorporation of additional zero voltage levels for each full bridge. It should be noted that this method is not universally applicable to all DABs, as it implicitly requires a relatively high leakage inductance within the transformer. Recent research [5] has demonstrated the ability of a mathematical equation to accurately describe the resonant commutation process of parasitic capacitances, stray inductance of the transformer and the resulting voltage-time error that leads to nonlinearity. However, this equation and the subsequent iteration loops required to determine optimal switching angles are currently impractical for real-time applications. In contrast, the method proposed in this paper does not require a detailed understanding of the causes behind the nonlinearity in the SPS mode. Nevertheless, understanding the parasitic effects can help optimize the overall design of the power electronic system and reduce the required resolution of the method, thus saving logic elements on the Field Programmable Gate Array (FPGA).

III. Concept

The idea of ESBOL is based on an iterative learning algorithm of a time-invariant (TI) system, where the algorithm learns iteratively from errors in the past. An overview of different iterative learning algorithms, which inspired ESBOL is given in [6]. In the first approximation, the DAB is a TI system, so the same current setpoint I_{sp} of the overlaid controller always leads to the same value of the manipulated variable of the modulator $I_{\mathrm{sp,mod}}$. As a result, the output value of the integral controller (I-controller), which is the sum of all errors at the current setpoint, can be used to update the iterative learning system to improve control performance in subsequent control cycles. This system utilizes the I-controller's integrated error to gradually correct deviations between the actual and ideal transfer functions and stores them for future operating points. Notably, this is achieved without the need for additional sensors or offline data processing.

A. Control structure

The control structure of ESBOL, shown in Figure 3, consists of two main parts: a nonlinear feedforward (FF) control of the current setpoint $I_{\mathrm{inv,tf,ip}} = f\left(I_{\mathrm{sp}}\right)$ and a standard I-controller, which is essential to maintain accuracy due to unexpected model deviations. The modulator, described in more detail in [7], generates the gate signals for the semiconductors based on the primary and secondary voltages of the DAB (U_{p} and U_{s}), and the manipulated variable $I_{\mathrm{sp,mod}}$, which combines the current setpoint $I_{\mathrm{inv,tf,ip}}$ with the output of the I-controller I_{i}. As a reference, the control structure, without the usage of the error storage system, is a direct FF control of the setpoint, i.e. $I_{\mathrm{inv,tf,ip}} = I_{\mathrm{sp}}$. The ESBOL method is implemented as a functional block (in blue) after the I-controller. Hence, the modulator's final current setpoint $I_{\mathrm{sp,mod}}$ includes two distinct components: the time-dependent I-controller value I_{i}, and the FF current $I_{\mathrm{inv,tf,ip}}$ as shown in (4).

$$I_{\mathrm{sp,mod}} = I_{\mathrm{inv,tf,ip}} + I_{\mathrm{i}} \tag{4}$$

The following subsections detail the initial setup, the update and the readout of the error storage system.

B. Setup and initialization of the error storage system

The principle of the ESBOL method is based on an adaptive error storage system, highlighted in Figure 4. It consists of a function for limiting the input value, the write/store system and the read function.

The write/store system consists of discrete breakpoints of current setpoints. The resolution of the system can be adjusted by varying the number N of error storage blocks employed. In this paper, $N = 41$ of these blocks are used as breakpoints, resulting in a resolution of the entire operating range of the DAB of $2.5\,\%$. The following equations are valid for an odd number of n. For even numbers, the equations have to be slightly modified. The value stored by each breakpoint is initialized as shown in (5). Where I_{max} is the absolute maximum value of the output current of the DAB and m is the index of the breakpoint.

$$S_n = -I_{\mathrm{max}} + \frac{n-1}{N-1} \cdot 2I_{\mathrm{max}}, \qquad n \in \{1, 2, ..., N\} \tag{5}$$

Depending on the FPGA used, it is possible to increase the number of these breakpoints. However, this choice involves a trade-off between resolution and used logic elements of the FPGA. The content of the storage blocks is initialized with the corresponding value of the ideal and linear transfer function. This means that, without further learning, the output of the error storage block is equal to the input value ($I_{\mathrm{inv,tf,ip}} = I_{\mathrm{sp}}$).

C. Update the error storage system

When the update of the system is activated ($w_{\mathrm{active}} = 1$), the current value of the I-controller I_{i} is limited to the update value I_{u} according to (6). The variable I_{tol} is a threshold value of I_{i} which leads to an update of the storage value. $I_{\mathrm{max,step}}$ is the maximum step size of the update value I_{u}. These two values are used to tune the adaption speed during the learning process and to avoid oscillations. On top of that, the current setpoint I_{sp} has to be in a $5\,\%$ range of the breakpoint distance to an existing breakpoint S_{x} to activate an update cycle. This range can be further modified and the activation of a learning cycle can be improved, to be more flexible.

$$I_{\mathrm{u}} = \begin{cases} \min\{I_{\mathrm{i}} - I_{\mathrm{tol}}, I_{\mathrm{max,step}}\}, & \text{if } I_{\mathrm{i}} \geq I_{\mathrm{tol}} \\ \max\{I_{\mathrm{i}} + I_{\mathrm{tol}}, -I_{\mathrm{max,step}}\}, & \text{if } I_{\mathrm{i}} \leq -I_{\mathrm{tol}} \\ 0\,\mathrm{A}, & otherwise \end{cases} \tag{6}$$

According to (7), the resulting value I_{u} is added to the previous value of the update step $k-1$ of the storage block $S_{n,k-1}$ at position n, which corresponds to the breakpoint of the setpoint I_{sp}. The variable n can be calculated with (8).

$$S_{n,k} = S_{n,k-1} + I_{\mathrm{u}} \tag{7}$$

$$n = \frac{I_{\mathrm{sp}}}{I_{\mathrm{max}}} \cdot \frac{N-1}{2} + \frac{N+1}{2} \tag{8}$$

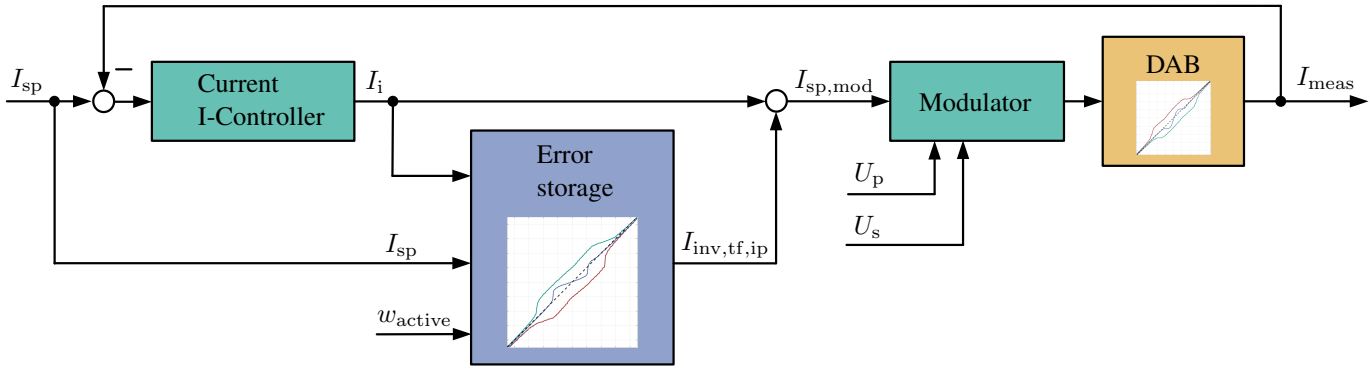


Fig. 3: Control structure of the current controller for the DAB. Without the Error storage system, a constant FF gain of 1 is implemented ($I_{\mathrm{inv,tf,ip}} = I_{\mathrm{sp}}$).

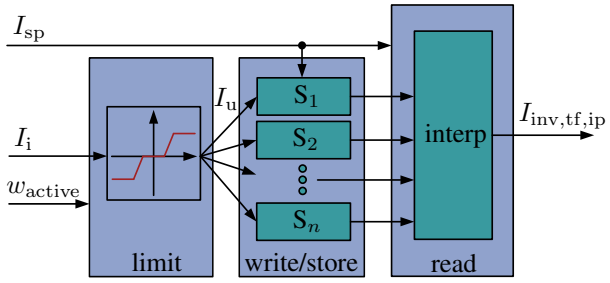


Fig. 4: Adaptive error storage system

D. Readout the error storage system

To read out the error storage system, only one input value is required: the current setpoint I_{sp}. Given that the n storage blocks S_1 to S_n are evenly and discretely distributed across the entire current operation area of the DAB, perfect alignment of the real setpoints I_{sp} with these storage blocks is unlikely. Hence, the implementation of linear interpolation between adjacent storage blocks aids in achieving higher accuracy. The choice of a linear interpolation is motivated by the general linear behavior of the DAB's ideal current transfer function. The resulting interpolated error compensation value $I_{\mathrm{inv,tf,ip}}$ is then added to the I-controller's output I_{i} to get the modified setpoint $I_{\mathrm{sp,mod}}$ for the modulator.

E. Mathematical description of ESBOL

The open loop transfer function of the combination of modulator and DAB is defined as $G_{\mathrm{DAB}}\left(I_{\mathrm{sp,mod}}\right) = \frac{I_{\mathrm{meas}}}{I_{\mathrm{sp,mod}}}$. Due to the nonlinear characteristic, it is not the identity relation, i.e., $G_{\mathrm{DAB}}\left(I_{\mathrm{sp,mod}}\right) \neq 1$, as shown in Figure 6a. However, after a full learning process, the I-controller's value is negligible, i.e. $I_{\mathrm{i}} \approx 0\,\mathrm{A}$, if the current setpoint I_{sp} is close to a breakpoint. Consequently, if the stored values of the storage system are plotted over the current setpoints I_{sp}, another transfer function can be observed as plotted in Figure 6b, which is denoted as $E_{\mathrm{S,DAB}}\left(I_{\mathrm{sp}}\right)$. It can be seen that the resulting function is almost equal to the inverse transfer function of the DAB. Therefore, even with using a rather slow I-controller, a very precise and highly dynamic control can be achieved, since (9) applies.

$$G_{\mathrm{DAB}}\left(E_{\mathrm{S,DAB}}(I_{\mathrm{sp}}) \cdot I_{\mathrm{sp}}\right) \cdot E_{\mathrm{S,DAB}}(I_{\mathrm{sp}}) \cdot I_{\mathrm{sp}} = I_{\mathrm{meas}} \approx I_{\mathrm{sp}} \tag{9}$$

F. Limitations of ESBOL

In this section the shortcomings and limitations of ESBOL are analyzed and evaluated.

1) Necessary adaption phase: In contrast to offline compensation methods such as those mentioned in Section I or [8], which start changing the behavior immediately, ESBOL is an online adaptation method and therefore only gradually improves the behavior of the DAB when it is operated at certain operating points. However, it is robust to higher or lower deviations than expected and learns accordingly.

2) Breakpoints are not reached during operation: As mentioned above, if online adaption is not possible, ESBOL will not learn and thus will not improve the dynamic behavior. However, the dynamics will not be worse than if ESBOL is not implemented since it is initialized with unity gain. Nevertheless, it is possible to change the stored value during the initialization phase according to existing knowledge of the system.

3) Varying voltage levels and modulation schemes: Each error storage system is specific to the voltage combination of primary and secondary voltages present during the learning process and to the modulation scheme used. If the voltage range of the application is large the existing error is not fully compensated. This disadvantage can be overcome by implementing multiple error storage systems in parallel and activating them according to the corresponding operating points.

4) Plateaus with no slope in transfer function: The inverse of plateaus with near-zero slope in the current transfer function cannot be accurately represented due to the limited resolution of the error storage system. This limitation results in a theoretically infinite slope. However, in practice, ESBOL still enhances the dynamics of the current controller. This improvement occurs because the operating points between two breakpoints are still improved by the FF control, and the I-controller further reduces the residual current error.

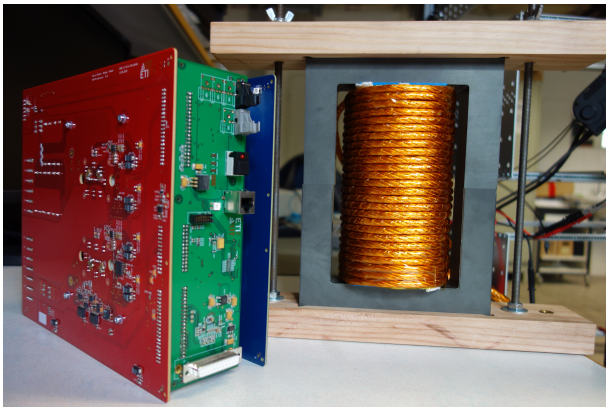


Fig. 5: Picture of one $40\,\mathrm{kW}$ DAB.

TABLE I: Parameters of the test bench

Symbol	Meaning	Value
	DAB parameter	
P_{nom}	Nominal output Power	$40\,\mathrm{kW}$
U_{p}	Primary voltage	$750\,\mathrm{V}$
U_{s}	Secondary voltage range	$720\,\mathrm{V}$-$780\,\mathrm{V}$
$I_{\mathrm{s,max}}$	Maximum output current	$50\,\mathrm{A}$
f_{sw}	Switching frequency	$50\,\mathrm{kHz}$
T_{bt}	Inverter blocking time	$200\,\mathrm{ns}$
	Transformer parameter	
n_{tr}	Winding ratio	$1:1$
$L_{\sigma,\mathrm{T}}$	Leakage inductance	$11\,\mu\mathrm{H}$
$L_{\mathrm{h,T}}$	Magnetizing inductance	$1\,\mathrm{mH}$
	ESBOL parameter	
N	Amount of breakpoints	41
I_{tol}	Minimum value of I_{i} to trigger an update	$100\,\mathrm{mA}$
$I_{\mathrm{max,step}}$	Maximum update current	$50\,\mathrm{mA}$
update rate	w_{active} is activated every ... cycle	10

IV. Test bench

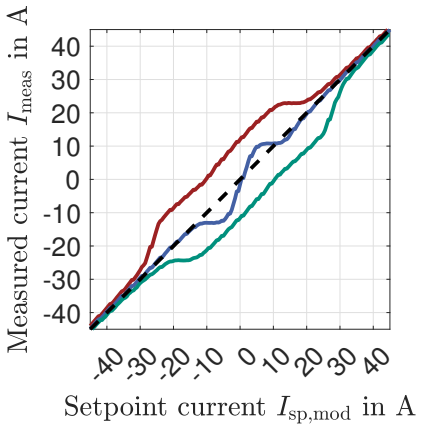
ESBOL is implemented on an Artix 7 FPGA with 35k logic elements. It is experimentally verified on a test bench with a nominal power of $P_{\mathrm{nom}} = 40\,\mathrm{kW}$. The primary voltage is set to $U_{\mathrm{prim}} = 750\,\mathrm{V}$. The error storage system is implemented with $n = 41$ breakpoints, spanning from $-50\,\mathrm{A}$ to $50\,\mathrm{A}$, resulting in a step size of $2.5\,\mathrm{A}$. The test bench consists of two identical DABs where the first one is a voltage controlled DAB which controls the voltage on the secondary side U_{s}. The second DAB is the Device Under Test (DUT) with ESBOL working in current control mode and transfers power between the primary and the secondary side. One of the DABs is shown in Figure 5. The primary voltage U_{p} is controlled by a grid connected Active Front-End (AFE), which is a three-phase two level converter, to cover the losses of the system. The overall system is controlled by a state machine running on the highly performant signal processing platform, developed in the institute explained in [9]. The parameters of the test bench are summarized in Table I.

V. Experimental results

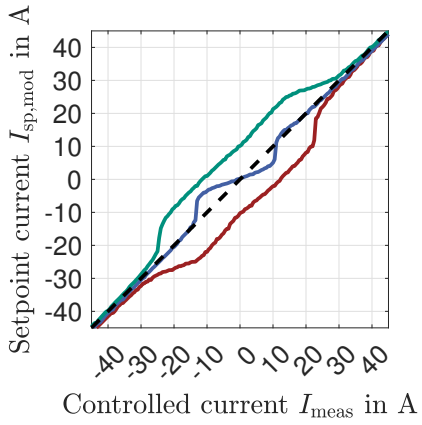
The current setpoint I_{sp} in open- and closed-loop control mode ranges from $-45\,\mathrm{A}$ to $45\,\mathrm{A}$, and it is increased in steps of $0.5\,\mathrm{A}$. In Figure 6a, the reference transfer function with open-loop control of the DAB is presented. It becomes apparent that the transfer function has small errors when the setpoint values are of high absolute magnitude. Conversely, nonlinearity in the behavior becomes evident when setpoints are lower. The commutation processes within the blocking times T_{bt} of the semiconductors have the greatest influence on these setpoints. The errors are even more obvious if the voltage of the secondary side U_{s} is not the same as the voltage of the primary U_{p}.

In order to update the error storage system, the I-controller is activated to have closed-loop control. Using the error storage system and updating the error values at the specific current setpoint leads to inverse transfer functions as shown in Figure 6b. After the training cycle, the learning active flag w_{active} and the I-controller are deactivated to establish exclusive open-loop but FF control of the system. The resulting transfer function is presented in Figure 6c. Only negligible deviations are recognizable between the ideal and the measured transfer functions. A plot of the remaining normalized errors is displayed in Figure 6d. The maximum resulting error is less than $4\,\%$ of the nominal current of $50\,\mathrm{A}$ of the DAB. Further reduction is attainable by increasing the number of breakpoints. Consequently, the results affirm the effectiveness of the proposed method. Figure 6 illustrates the transfer function and the improvement achieved by online linearization in stationary operating points. However, dynamic behavior is more critical, as even a slow I-controller will eventually lead to the correct setpoint $I_{\mathrm{sp,mod}}$ for the modulator in stationary operation points. The potential of ESBOL becomes apparent when the current setpoints I_{sp} of the DAB change continuously and with a high frequency, such as when it is used as a module in a Solid State Transformer (SST) as illustrated in [10]. The dynamic behavior is shown in Figure 7. The green curve shows the step responses of the I-controller with direct FF control of the setpoint current. The blue curve is the result of the I-controller with ESBOL.

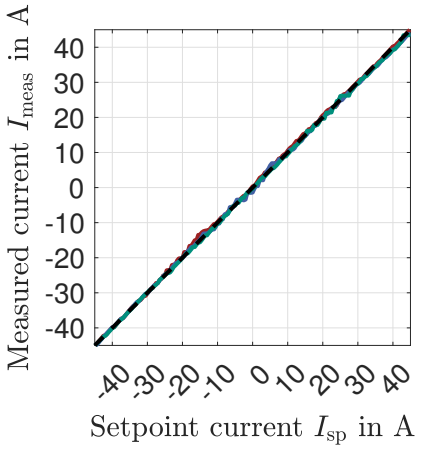
Figure 7a shows a comparison of setpoints changes from $I_{\mathrm{sp}} = -10\,\mathrm{A}$ to $I_{\mathrm{sp}} = 10\,\mathrm{A}$ at $t = 0\,\mu\mathrm{s}$ of the I-controller with static FF and the same I-controller with ESBOL. Whereas Figure 7b shows the opposite step change from $I_{\mathrm{sp}} = 10\,\mathrm{A}$ to $I_{\mathrm{sp}} = -10\,\mathrm{A}$. It is obvious, that using ESBOL leads to better dynamic behavior of the output current I_{s} with less overshoot and about half as long settling time. This is caused by better FF control and therefore less integration effort of the I-controller. The effects of the nonlinear transfer function can be seen in particular in the green curve in Figure 7b. From $t = 500\,\mu\mathrm{s}$ to $t = 1000\,\mu\mathrm{s}$ the output current does not change even though there is a deviation between the setpoint and the measured current. That is caused by the zero slope plateau of the blue transfer function in Figure 6a at about $I_{\mathrm{sp}} = -10\,\mathrm{A}$. Even though the setpoint for the modulator changes due to the integrating I-controller, the output remains the same for a while until this plateau is overcome.



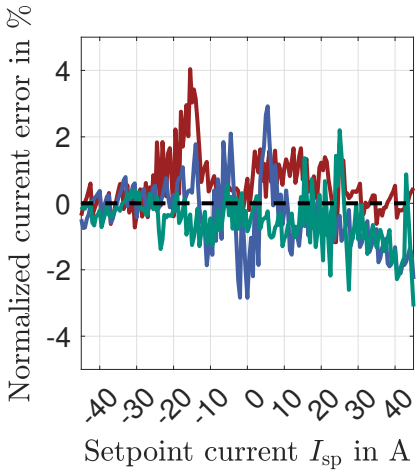
(a) Measured open-loop transfer function $I_{\mathrm{meas}} = G_{\mathrm{DAB}}\left(I_{\mathrm{sp}}\right) \cdot I_{\mathrm{sp}}$.



(b) Plot of stored values $E_{\mathrm{S,DAB}}(I_{\mathrm{sp}}) \cdot I_{\mathrm{sp}}$ after learning process.

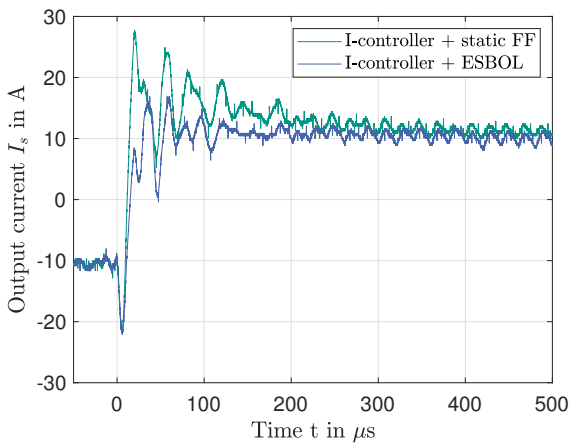


(c) Resulting open-loop transfer function with ESBOL.

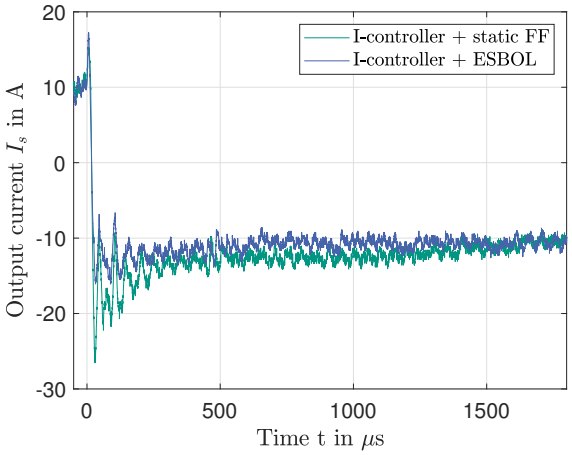


(d) Normalized error in open-loop control with ESBOL.

Fig. 6: Results of current transfer function (a) and inverse transfer function (b) of the used DAB. In each sub-figure the following legend is used. The red line ▬ indicates the results for $U_{\mathrm{s}} = 720\,\mathrm{V}$. The blue line ▬ indicates the results for $U_{\mathrm{s}} = 750\,\mathrm{V}$. The green line ▬ indicates the results for $U_{\mathrm{s}} = 780\,\mathrm{V}$. The dashed line ▬ highlights an ideal transfer function. The primary voltage is set to $U_{\mathrm{p}} = 750\,\mathrm{V}$.



(a) Setpoint change from $-10\,\mathrm{A}$ to $10\,\mathrm{A}$.



(b) Setpoint change from $10\,\mathrm{A}$ to $-10\,\mathrm{A}$.

Fig. 7: Current control dynamics of the DAB with the I-controller and static FF control (green) and with ESBOL and the I-controller (blue) ($U_{\mathrm{p}} = U_{\mathrm{s}} = 750\,\mathrm{V}$).

VI. Conclusion

This paper introduces an error storage based online linearization method, ESBOL, for addressing the nonlinear transfer function of a DAB with low leakage inductance L_σ. ESBOL even can be applied without the need for specific knowledge regarding the causes of nonlinearity and it is not restricted to DABs. It is effective over a wide voltage transfer range between the primary and secondary sides of the DAB. Due to the adaptive nature of ESBOL, the resulting current transfer function of the DAB gradually improves as the system operates in various points. This enhancement leads to greater precision and higher control dynamics in regulating the output current of the DAB. Further research can be carried out on the parallel use of multiple independent error storage systems for different voltage levels in parallel, utilizing data from the error storage system for parameter identification, and applying ESBOL to a voltage-controlled DAB.

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